# Distortion Minimization for Ultra-Low THD Class-D Power Amplifiers

Mario Mauerer and Johann W. Kolar

***Abstract*—The effects of key sources of total harmonic distortion (THD) in power output signals of digitally controlled switch-mode (Class-D) converters/amplifiers are analyzed. Extensive measurements with a 400 V amplifier prototype, based on gallium nitride (GaN) power transistors, support the investiga-tions. First, the semiconductor loss model and a comprehensive circuit simulation of the converter with its closed-loop feedback system is presented to provide insights on distortion caused by junction temperature variation of the power transistors. Half-bridge interlock time is identified as a significant source of nonlinearity and hence, three simple and effective methods to reduce its deteriorating effect on THD are presented. Another important contribution to linearity arises from the closed-loop feedback controllers, which benefit from small delays and/or, high converter switching frequencies. It is also shown how a Kalman filter, which can be used to significantly reduce converter output noise, deteriorates the THD due to its linear system model. Finally, a method to reduce harmonic distortion and other disturbances caused by a non-ideal DC supply is also demonstrated. By rigorously eliminating distortion sources and applying the presented compensation methods, amplifier output current THD values below −100 dB (0.001%) are achieved and experimentally verified in wide load current ranges.**

***Index Terms*—Dead time, feedback control, feedforward compensation, high power amplifiers, Kalman filter, total harmonic bistortion (THD), wide-bandgap semiconductors.**

## I. Introduction

PRECISION switch-mode, i.e., Class-D amplifiers are power electronic converters that provide output voltage or current waveforms with little deviation from (often arbitrarily shaped) reference input signals. Consequently, additional output signal components, such as noise or harmonic distortion, are unfavorable for different industrial, medical and research applications.

In high-energy particle accelerators, such amplifiers provide the currents for the superconducting magnets and beam forming structures. They operate with output powers exceeding 100 kVA, while achieving steady-state current accuracies below 10 ppm (with respect to the full-scale current) [1], [2]. Medical magnetic resonance imaging (MRI) applications require high-bandwidth, high-current and low-noise power converters to drive gradient coil currents, with amplitudes regularly in excess of 500 A. The coil current quality strongly influences the imaging capability [3], [4].

Nanoscale-precision positioning applications, required in integrated circuit manufacturing processes, employ different actuators such as magnetic bearings or linear motors that are supplied with currents of low noise and/or low distortion in order to prevent the generation of undesired forces and thus, disturbing movements of the positioning systems [5]. Due to continuously shrinking semiconductor feature sizes and the desire for an increased manufacturing throughput, the requirements with respect to noise, linearity and power of precision amplifiers that drive such actuators with controlled currents, are increasing equally [6], [7].

Due to stringent requirements on actuator current noise and distortion in high-precision positioning applications, linear or hybrid power amplifiers, together with analog feedback control systems, are often employed [8]–[10]. For nanoscale positioning applications, THD figures below −90 dB are desired. However, for high-power applications, e.g., high-speed positioning systems or MRI, linear or hybrid amplifiers are difficult to employ due to their restricted output power capability, limited scalability and reduced efficiency [11], [12]. These disadvantages can be overcome with switch-mode power converters. Furthermore, a digital control system, as opposed to analog controllers, is deployable on different converters with only minor modifications, which reduces development time and cost. It also significantly improves design flexibility and allows the application of advanced control system and signal processing concepts.

The considered motion systems are characterized by positioning stages with little damping and friction (e.g., due to the usage of air or magnetic bearings) and thus, the noise current easily translates to undesired forces or torques of the actuators [13]–[15]. Noise components of the output currents are of special disadvantage in mechatronic positioning applications that rely on slowly varying or static currents, e.g., in magnetic levitation bearings or vibration isolation systems [16], [17].

Distortion arises due to nonlinear transfer functions in the amplifier signal and power paths, and can manifest itself with spectral components at integer multiples of the output signal's desired fundamental frequency (i.e., harmonics). If the desired output signal contains more than one frequency component, intermodulation distortion occurs [18]. These effects require consideration in continuously moving mechatronic applications like integrated semiconductor lithography or excimer laser annealing of displays, where the actuator current should not contain harmonics, or other unwanted signal components originating from nonlinear effects in the power amplifiers,

Manuscript received May 15, 2018.

The authors are with the Power Electronic Systems Laboratory, ETH Zurich, Switzerland (e-mail: mauerer@lem.ee.ethz.ch).

Digital Object Identifier 10.24295/CPSSTPEA.2018.00032

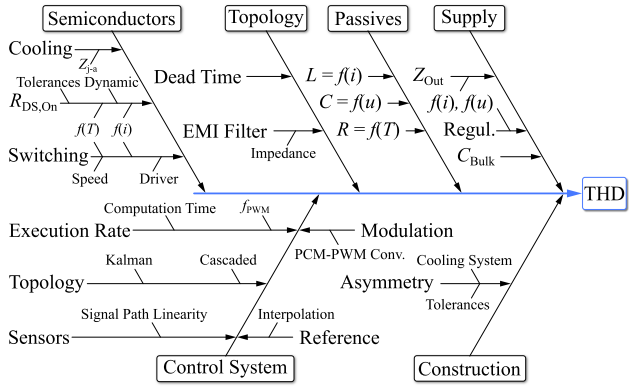


Fig. 1. Nonidealities of system components influencing the total harmonic distortion (THD) of the output quantities of digitally controlled switch-mode power amplifiers. $f(T)$ indicates a dependency of the temperature $T$. Likewise, $i$ and $u$ represent currents and voltages, respectively. PCM: Pulse-code modulation.

in order to reproduce the demanded forces (and hence, the movements) as exactly and linearly as possible [5], [7], [19].

This work investigates different sources of harmonic distortion and their significance in a digitally controlled, precision switch-mode power amplifier. Fig. 1 lists key system components and nonidealities that contribute to output distortion [7], [20]–[22]. A hardware demonstrator system is used to support the presented insights with measurements. It operates as a single-phase DC/AC inverter and can provide up to 400 V and a controlled output current of up to 25 A (peak) to a resistive-inductive load. Fundamental amplifier output current frequencies for common mechatronic applications range from several hertz up to hundreds of hertz. The results presented in this work are applicable for a wide frequency range, as outlined in the corresponding sections of this work. Four half-bridges, encompassing gallium nitride (GaN) enhancement-mode high-electron-mobility (E-HEMT) power transistors (*GaN Systems, GS66508T*), allow the implementation of two different power stage topologies, which is used in the investigation of dead time related distortion. This work does not consider sources of noise in the discussed amplifier systems, only harmonic distortion. This is possible as the underlying and systematic causes of noise and distortion are fundamentally different and rarely interacting. However, the topic of noise is covered by a second, future publication of the authors in this journal.

Several key contributions arise from this work. The recent availability of fast-switching gallium nitride power semiconductors in low-parasitic packages enables kilowatt-range power amplifiers with unprecedented output distortion figures. This is verified with detailed measurements that reveal THD values below −100 dB. To facilitate the usage of the new power devices in industrial applications, detailed loss models and converter design guidelines, with respect to low-distortion amplifiers, are presented. Furthermore, different methods have been discussed in the past that aim to mitigate distortion caused by half-bridge interlock/dead time. The flexible hardware demonstrator utilized in this work allows a direct comparison of three important distortion reduction techniques. Their specific advantages and implementation details are discussed and verified with comprehensive measurements in order to facilitate future design decisions. Furthermore, modern high-performance signal processors enable extraordinary high-frequency, high-gain feedback controllers. Control system considerations and measurements with different configurations highlight the effect and limits of this important system component. Additionally, the construction and verification of the discussed ultra-low-distortion power amplifiers requires specialized components and design approaches, and sophisticated measurement techniques, which are presented in detail. Hence, this work provides sensitivity analyses of amplifier subsystems with respect to distortion such that amplifier designers can direct their resources and attention to the critical system components.

The amplifier system, including its underlying design decisions, is introduced in Section II. After introducing the semiconductor loss model, Section III investigates to what extent the thermal variation of the power transistor junction temperatures contributes to load current THD. Next, Section IV presents the deteriorating effect of the half-bridge interlock time on load current THD and introduces three methods to effectively reduce this distortion component. Measurements demonstrate the performances. Section V illustrates and experimentally verifies how the THD performance of the closed-loop control system is increased with the converter switching frequency. In this context, the effects of a Kalman filter on load current THD are also discussed. The sensitivity of the power amplifier to its DC supply is investigated theoretically and experimentally in Section VI. All in all, amplifier load current THD figures of −100 dB are achieved in wide load current ranges with the demonstrator system. Finally, Section VII presents a brief conclusion and an outlook on amplifier systems of even lower THD.

## II. System Overview

A hardware demonstrator serves as versatile test bed for the investigation of different key influence factors on load current THD. Fig. 2 illustrates its power stage topology, driving a single-phase bridge-tied load, i.e., it is connected between two phases, each comprising two interleaved converter half-bridge legs. This allows the application of the full DC-link voltage to the load and provides a better power supply rejection than a single-ended amplifier configuration [24]. The two interleaved half-bridges in each phase enable the implementation of two operating modes. If both half-bridges conduct an (ideally) identical current, the regular interleaved topology is employed. A second mode of operation, known as dual buck converter, is achieved by introducing a circulating current to the two half-bridges in each phase, with the effect that the dead-time related distortion can be reduced, as shown in [7], [20], [25]and in Section II-B below. The EMI filters at the input and output of the converter ensure compliance with common norms and protect sensitive equipment near the load from high-frequency signal components. By changing the phase shifts between the

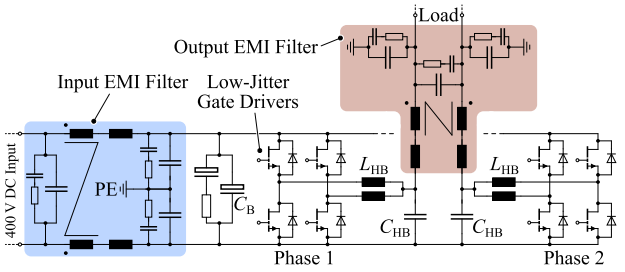


Fig. 2. Hardware demonstrator power circuit topology. Two interleaved half-bridges in two phases drive a bridge-tied load. $C_B$ = 1.8 mF, $C_{HB}$ = 12 µF, $L_{HB}$ = 700 µH. The low-jitter gate drivers are presented in [23].

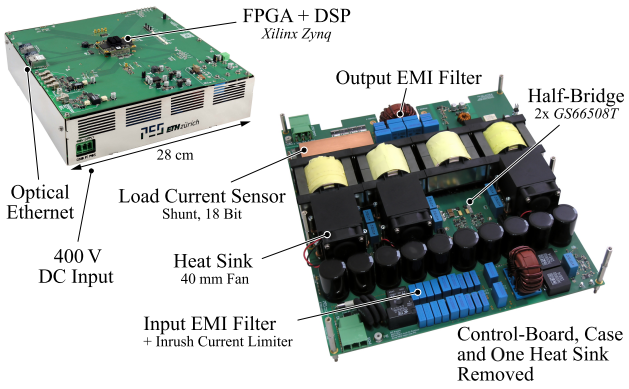


Fig. 3. Hardware demonstrator (with and without enclosure) employing four 650 V GaN (*GaN Systems GS66508T*) half-bridges, high-resolution ADCs and a high-performance digital processor and FPGA. The max. input voltage is 400 V DC. The system is capable of driving a single-phase bridge-tied load with current amplitudes up to 25 A peak.

PWM carriers of the four half-bridges, the high-frequency spectral content (both common-mode and differential-mode components) of the load voltage can be influenced [21]. The demonstrator hardware is depicted in Fig. 3.

### *A. Power Semiconductors*

As the switching behavior of the power transistors influences the amplifier's achievable THD, fast-switching state-of-the-art gallium nitride power transistors (*GaN Systems GS66508T,* 650 V, 30 A, 50 mΩ) are employed to create a power stage that can provide output signals of inherently low distortion [20]. The converter is designed for an input voltage of ≤ 400 V DC and the load current amplitude $\hat{i}_L$ can reach 25 A (e.g., peak value of a sinusoidal signal). The expected output frequencies range from DC up to ≈ 200 Hz, which is a common range in mechatronic motion systems. The converter's switching frequency extends to 200 kHz, which is facilitated by the fast switching speed of the GaN transistors and their lack of a reverse recovery effect, resulting in low hard-switched losses. As the switching transistors are cooled from the top side, no thermal printed circuit board vias are required, which would otherwise disrupt the commutation loop of the half-bridges. This enables low-inductance commutation loops and fast switching actions with little voltage overshoots and ringing [23]. Fig. 4 illustrates the circuit board crosssection of a top-cooled

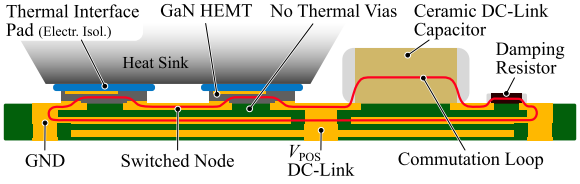


Fig. 4. Simplified circuit board cross-section illustrating the layout of a top-cooled half-bridge. The lack of thermal vias allows for a low-inductance vertical commutation loop. Only the top two copper layers are shown. Geometric proportions are altered for better visualization.

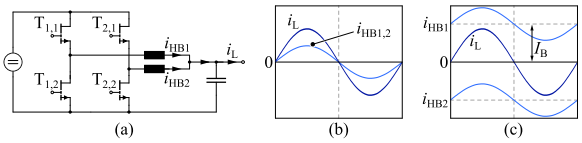


Fig. 5. (a) Interleaved power stage topology of one phase of the prototype system. (b) Regular interleaved operation, where each half-bridge conducts an identical current. (c) Dual buck operation: A circulating bias current renders the half-bridge currents unidirectional. The bias current is introduced by altering the reference currents with the feedback control system according to (1).

half-bridge, featuring one heat sink and a 40 mm fan for forced air cooling (cf. Fig. 3).

Each transistor is driven by an *LM5114* gate driver with separate turn-on/off resistors of 6.7 Ω and 3.3 Ω, respectively. The gate voltage applied to turn the transistors on is 6 V and −3.3 V to ensure reliable turn-off. The gate control signal is isolated using a low-jitter digital isolator (*Si8271*, 40 ps RMS jitter, 30 ns delay), which reduces wideband noise in the switched half-bridge output voltages [23], [26].

Short (i.e., 30 ns) half-bridge interlock/dead times are achieved with the fast-switching GaN transistors. This is the time interval $T_D$ required between the turn-off of a half-bridge transistor and the subsequent turn-on of the complementary device, during which both power transistors are turned off, in order to prevent a destructive half-bridge shoot-through or short-circuit. SiC Schottky diodes (*CREE C3D1P7060Q*) are placed in parallel to the transistors to conduct the current during the dead time interval in order to eliminate the otherwise high voltage drop of the GaN transistors in reverse conduction [27]. As shown in this work, low dead times significantly reduce amplifier output distortion and are thus highly beneficial for the discussed applications.

### *B. Power Circuit Topology*

Fig. 5(a) illustrates the interleaved half-bridge converter legs of a phase of the demonstrator system (which employs two phases in total, cf. Fig. 2). Conventionally, both half-bridge currents $i_{HB1,2}$ are ideally identical, as shown in Fig. 5(b). For this regular operating mode, it is well-established that dead time is a significant cause of distortion in the half-bridge output waveforms, as further explained in Section IV below.

The dual buck (DB) power stage topology, also named opposed current converter or balanced current amplifier, whose operating principle is described in [7], [20], [28], [29], does traditionally not require dead time and is hence not subject to

this cause of distortion. Its key characteristic is the introduction of a circulating bias current to the two interleaved half-bridges, such that each half-bridge exhibits unipolar currents:

$$i_{\mathrm{HB1,2}}(t) = i_{\mathrm{L}}(t)/_2 \pm I_{\mathrm{B}}. \quad (1)$$

The resulting current waveforms are illustrated in Fig. 5(c). This also has the effect that the half-bridge currents are dominated by the (constant) bias current and are thus less modulated by the load current. This renders the variation of the half-bridge voltage switching transitions less pronounced, which further reduces distortion.

As the half-bridge currents are unipolar, the two half-bridge transistors $T_{1,2}$ and $T_{2,1}$ could be replaced with power diodes, which would constitute the conventional dual buck topology [7]. However, this is not done in the demonstrator system in order to improve the efficiency and linearity of the topology, as analyzed in [20]. A dead time is then still required, but, due to the unipolar half-bridge currents, it does not affect the voltage-forming behavior of the half-bridges and hence, does not introduce distortion.

Starting from a conventional, interleaved half-bridge operation, the dual buck behavior is simply obtained by introducing the circulating current between the two half-bridges by means of the control system, i.e., the half-bridge current references of the two half-bridge P-controllers are adapted according to (1). It should be noted that the bias current can be modulated to reduce losses, as shown in [7]. However, this increases distortion and is thus not further considered.

As the dual buck operating mode results in higher transistor RMS currents, the resulting losses must be carefully considered to prevent additional distortion and thermal overload. Therefore, Section III-A introduces the loss model of the GaN E-HEMTs.

### *C. Feedback Control System*

To increase the amplifier's reference tracking and disturbance attenuation performance, a closed-loop feedback con-trol system is used. Its structure is illustrated in Fig. 6. It comprises three cascaded controllers. A type-III (lead-lag) controller regulates the amplifier's precision output current. It provides the load voltage references to the two proportional-integral (PI) phase voltage controllers. The innermost control loop consists of proportional (P) controllers that act on the half-bridge currents. All feedback loops are tuned, using loop shaping, to achieve open-loop phase margins of at least 50° and gain margins of ≈ 6 dB, while the gains of the open-loop transfer functions are maximized to achieve a high disturbance rejection in each loop [30], [31]. This necessitates the careful analysis of the time delays in the controlled plants, caused by the PWM and the calculation of the feedback controllers [31], [32]. These delays reduce the controller phase margins. The gain of the proportional half-bridge current controllers could be selected arbitrarily high if there was no such delay, as their plants exhibit only first-order integrative characteristics.

Fig. 7 illustrates the important time delays. At the start $t_{\mathrm{u}}$ of each PWM cycle, the necessary measurements are obtained and the error signals for the feedback controllers are formed. As all controllers are implemented with digital logic in an FPGA, they can therefore provide the newly calculated duty cycles (i.e., the inputs to the controlled system) before the start of the next PWM period, i.e., during the time $T_{\mathrm{D,Ctrl}}$. Due to the triangular carrier, the delay of the PWM is constant: $T_{\mathrm{D,PWM}} = T_{\mathrm{PWM}}/2$ [32].

Consequently, the PWM frequency of the power converter influences the achievable performance of the feedback control system, as, with reduced delays, higher open-loop gains can be achieved for the given required phase margins. Fig. 8 exemplarily shows the difference in control system performance when the controller is tuned for a PWM rate of 100 kHz and 200 kHz. The open-loop gain (which is a measure of the disturbance rejection capability [30]) is ca. 9 dB larger when the converter (and the control system) operate at 200 kHz in-stead of 100 kHz. The indicated gray area is maximized during controller tuning, using a numerical optimization method that performs the loop shaping of the individual feedback loops, with consideration of the aforementioned time delays and the required phase/gain margins.

All controllers are executed synchronously with the converter switching frequency (regular symmetric PWM sampling) [33]. However, they can also be updated twice per PWM cycle (regular asymmetric sampling), with the result-ing implications and limitations discussed in Section II. In order to reduce the quantization noise of the low-resolution PWM, digital delta-sigma noise shapers are employed. They do not affect THD, as they only act on the modulator's quantization noise [34]. As the ratio of the PWM sampling rate ($f_{\mathrm{PWM}}$) to common load current fundamental frequencies $f_{\mathrm{F}}$ is high (> 500), distortion caused by the sampling of the PWM modulator is not relevant, as it is in the order of ≈ −110 dB (THD) for the discussed system [33], [34]. However, for mechatronic applications with fundamental frequencies in excess of ≈1 kHz (e.g., magnetic bearings in high-speed motors), the modulation harmonics potentially become considerable. For such applications, the modulation method must be changed (e.g., by means of a hysteretic modulator), or the PWM frequency must be sufficiently increased [33].

Remark: Sensor noise can be reduced by utilizing a Kalman filter that provides the low-noise estimates of the voltages and currents for the feedback system, as also shown in Fig. 6 [35]. Details of the converter noise performance are not scope of this paper. Nonetheless, Section V-A presents implications of the Kalman filter on the amplifier linearity.

All important system voltages and currents are measured using high-resolution, low-noise acquisition systems as indicated in Fig. 6. All analog-to-digital converters (ADCs) feature an amplitude resolution of 16 bits and a maximum sample rate of 1 MHz (*LTC2368-16 and ADS8861*), except for the load current ADC, which is an 18-bit, 5 MHz device (*AD7960*) in order to minimize the intrinsic sensor noise of the load current measurement. All currents are measured using shunt resistors (with isolated ADCs), as this enables a superior

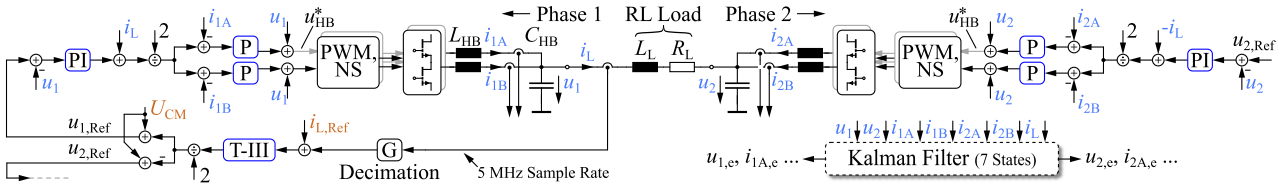


Fig. 6. Cascaded control system structure of the hardware demonstrator. The pulse-width modulators employ digital noise shapers (NS) to reduce quantization noise. The control topology comprises of three cascaded controllers with feedforward compensation. Proportional (P) current controllers are used for the four half-bridge currents, proportional-integral (PI) voltage controllers for the two phase voltages and a type-III (lead-lag) controller for the load current. $L_{HB}$ = 700 µH, gapped ferrite core. $C_{HB}$ = 12 µF, film capacitors.

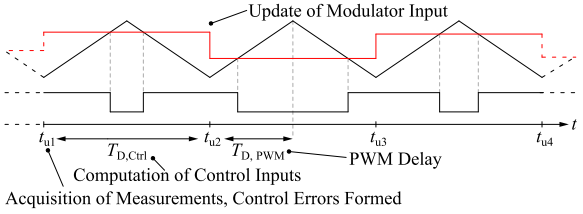


Fig. 7. Time delay model for the forward path of the P-type current controller plants. The total delay is $T_{Fwd} = T_{D,Ctrl} + T_{D,PWM} = 1.5T_{D,PWM}$. The control system performance improves with increased switching frequencies.

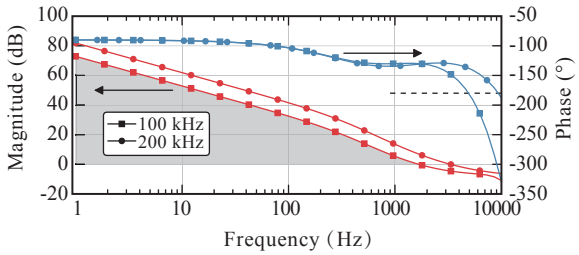


Fig. 8. Open-loop bode plot of the type-III load current controller and its plant (5 Ω + 2.5 mH load configuration) for PWM frequencies of 100 kHz and 200 kHz (which correspond to the control system execution frequencies). The gray area is maximized by controller tuning.

noise and distortion performance as compared to integrated solutions [36]. The DC-link and phase voltages (≤ 400 V) are measured using resistive dividers that are optimized for low noise and distortion [36]. The 5 MHz load current ADC employs oversampling and a 6th-order anti-aliasing Butterworth filter. This sensor is capable of measuring THD down to a level of ≈ −110 dB, which is mainly limited by the operational amplifiers in its gain stage and anti-aliasing filter (*LT1028, AD8620* and *ADA4932*) [36]. This is sufficient for the demonstrated performance, as the THD is limited by other factors, such as half-bridge dead time.

Due to the large number of high-speed and high-resolution ADCs, as well as the need to calculate complex control system tasks, such as a Kalman filter, a high-performance processing system (*Xilinx Zynq Z-7020*) is used to manage converter operation [37]. It features an FPGA as well as two 666 MHz *ARM Cortex-A9* CPUs with double-precision floating-point units. A 1 GiB DDR3 memory is connected to the processing system, which allows the recording of large amounts of internal data, such as ADC samples. A 100 Mbits$^{-1}$ optical Ethernet link (*100BASE-FX*) facilitates the transmission of such data to an external computer for further analysis and processing.

### *D. Measurement Methods and Definitions*

Common loads for the discussed precision amplifiers are often electromagnetic actuators or magnetic bearings that can be described by a series connection of a load inductor $L_L$ and a load resistor $R_L$. For linear permanent magnet motors, values for $R_L$ are in the range of 1 Ω to 10 Ω , whereas the inductance values $L_L$ range from 100 µH to 100 mH. Consequently, three different resistive-inductive loads are used for all measurements presented in this work: 2 Ω + 10 mH, 5 Ω + 2.5 mH and 10 Ω + 100 µH. The load resistors and inductors need to be highly linear as they otherwise introduce undesired distortion components which prevents an accurate evaluation of the converter THD. Consequently, for the load resistors, thick film, high-power resistors with a low thermal coefficient of resistance are used (*Vishay LPS 600*), that implement the three different load resistance values. The magnetic cores of the load inductors are made from laminated silicon steel (designed for low-frequency power grid applications) in case of the 2.5 mH and 10 mH inductors, whereas the core of the 100 µH inductor is a gapped ferrite. All inductors have a sufficient current and saturation rating of > 25 A RMS. Their respective linearities are demonstrated with measurements in Section V.

As the power amplifier is capable of supplying a current with very low distortion, a sufficiently linear and low-noise sensor is required to accurately obtain a reference current measurement. Consequently, a *LEM IT 65-S* flux-gate current transducer is used as reference current sensor to measure the amplifier load current THD [38]. Three primary winding turns are used to fully utilize the sensor's range. Its burden resistor has a value of 47 Ω and consists of ten paralleled metal film resistors to minimize power dissipation and thus, maintain lin-earity. The burden voltage is measured with a *Rohde&Schwarz UPV* audio analyzer, which is a low-noise, high-precision spectrum analyzer [39]. This setup can measure THD levels of ≈ −108 dB (dominated by odd harmonics and limited by the *LEM* current sensor), which is sufficiently accurate for the presented measurements. All measured THD and SNR figures in this work are directly obtained by this instrument.

In order to measure the amplifier output THD, a sinusoidal digital current reference $i_{L,Ref}$ (cf. Fig. 6) is used with a fundamental frequency $f_F$ of 35 Hz or 210 Hz. The amplifier then also creates a load current with the same fundamental frequency. This selection of $f_F$ ensures that its harmonics do not interfere with

the 50 Hz grid harmonics that are being coupled into the *LEM* current sensor through external stray fields, but are not present in the actual load current (as determined by experimental validations). Furthermore, these frequencies are in the range of common actuator current frequencies used in positioning applications. The THD of the load current is defined as:

$$\mathrm{THD} = 20\log_{10}\frac{\sqrt{i_2^2+i_3^2+\cdots+i_9^2}}{i_1}, \tag{2}$$

where $i_1$ is the current amplitude of the fundamental component (at frequency $f_F$) and $i_2 \ldots_9$ are the amplitudes of the first eight integer harmonics of the fundamental (at frequencies $k f_F$, with $k \in [2, 3, \ldots, 9]$).

Two different high-power DC supplies (*HP 6035A* and *Sorensen SGI 600-17*) are used for the measurements, whereas their selection does not affect the measured THD figures (but the achievable load currents, due to their output limits), as verified by measuring the amplifier's output THD with both DC supplies in certain measurements.

## III. Distortion Due to Power Transistor Junction Temperature Variation

Commonly used switching transistors in power electronic converters exhibit a nonlinear behavior of the on-state resistance $R_{DS,on}$ as a function of the junction temperature [27], [40]. Naturally, the total transistor losses and hence, $T_j$ and $R_{DS,on}$, are a function of the converter operating point (i.e., its output current and/or voltage), which causes a modulation of the main conduction path resistances and hence, harmonic distortion. Even as modern wide-bandgap semiconductors show a less pronounced temperature-dependent $R_{DS,on}$ than their silicon counterparts [27], this nonlinear effect has to be considered for highly linear amplifiers, which necessitates a detailed power transistor loss model.

### *A. Transistor Loss Model*

The majority of power stage losses are generated by the hard-switching GaN transistors. Consequently, to prevent thermal overload and to optimize the utilized transistors with respect to the active die area, their losses and thermal model is presented.

The evaluation of the transistor switching losses is aggravated by the fact that they depend significantly on the gate drive configuration, and sufficient data is rarely found in data sheets. Loss measurements of the utilized GaN power transistors for soft- and hard-switching transitions are provided in [41], which are used here to derive the transistor losses occurring during a complete PWM cycle as a function of the half-bridge current and the DC-link voltage. The loss model is extended by incorporating additional parasitic capacitances, which cause increased hard-switching losses (e.g., due to the PCB routing or the half-bridge inductors). Dynamic behavior of the transistor on-state conduction resistance $R_{DS;on}$ is not observed and is thus not modeled [42]. The resulting loss energies for each half-bridge transistor during one PWM cycle (i.e., two switching transitions) are illustrated in Fig. 9 for a DC-link voltage of 400 V and under the assumption of a constant half-bridge current during the PWM cycle. Measurements of the overall converter losses corroborate the accuracy of this transistor loss model. The polynomial fit for the high-side transistor switching losses are listed in TABLE I.

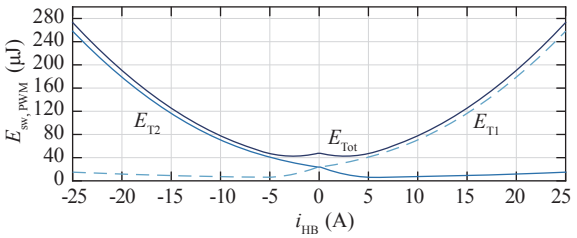


Fig. 9. Measured transistor switching loss energies for a half-bridge consisting of a high-side ($T_1$) and low-side ($T_2$) transistor (*GaN Systems GS66508T*) [41]. These energies are dissipated once per PWM cycle. Positive half-bridge currents $i_{HB}$ flow out of the half-bridge (hard switching of $T_1$) and negative currents flow into the half-bridge switch-node (soft/partially soft switching of $T_1$). $u_{DC} = 400$ V. Gate driver: *LM5114*. Turn-on/off resistors: 6.7 Ω /3.3 Ω. Turn-on/off voltages: 6 V/ 3.3 V. Numeric fitting data provided in TABLE I.

TABLE I
Polynomial Fitting Coefficients for the Switching Energy $E_{T_1}$ Dissipated During One PWM Cycle (See Fig. 9). Unit: µJ.

$$E_{T1} = c_0 + c_1 i_{HB} + c_2 i_{HB}^2 + c_3 i_{HB}^3 + \cdots + c_6 i_{HB}^6$$

| Range of $i_{HB}$ | $c_0$ | $c_1$ | $c_2$ | $c_3$ |
|---|---|---|---|---|
| 0 A to 25 A | 24.17 | 1.943 | 0.2544 | 0.001716 |
| −25 A to 0 A | 25.43 | 8.29 | 1.303 | 0.09475 |
| | $c_4$ | $c_5$ | $c_6$ | |
| 0 A to 25 A | 0 | 0 | 0 | |
| −25 A to 0 A | 0.003415 | 5.322e-5 | 1.985e-7 | |

To accurately model the transistor conduction losses, with consideration of the temperature-dependent $R_{DS,on}$, a computer simulation is employed. This allows to track the variation of the junction temperature $T_j$ during converter operation with fundamental output frequencies $f_F$ of several tens of hertz, which are common in mechatronic positioning applications. Note that a simple thermal model, consisting only of thermal resistances, is insufficient to correctly model the behavior of $T_j$ during a fundamental period, as the converter is not operated with a constant load current and hence, the thermal capacitances greatly influence the dynamics of $T_j$. Fig. 10 illustrates the thermal simulation model employed for each transistor. Once per PWM cycle, the individual conduction and switching losses ($P_C$, $P_{Sw}$) are evaluated and applied to the equivalent thermal model, which consists of two capacitances and resistances that implement the important thermal dynamics. The capacitance $C_j$ and resistance $R_{jc}$ model the thermal behavior of the transistor chip. Their values are often provided by manufacturers or can be extracted from the transient thermal impedance curve often found in power transistor data sheets. $C_{HS}$ and $R_{ca}$ represent the heat sink and the thermal resistance from transistor case to

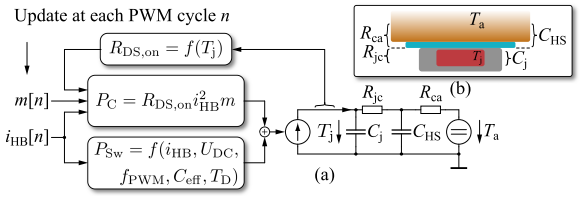


Fig. 10. (a) Thermal model used to simulate the thermal cycling of $R_{DS,on}$ during amplifier operation, including transistor conduction and switching losses. (b) The model uses the thermal junction-case resistance $R_{jc}$, the thermal junction capacitance $C_j$, the thermal resistance of the heat transfer pad and the heat sink to ambient, $R_{ca}$, and the thermal capacitance of the heat pad and heat sink, $C_{HS}$. The modulation index $m$ is the relative on-time of the high-side half-bridge transistor during one PWM cycle.

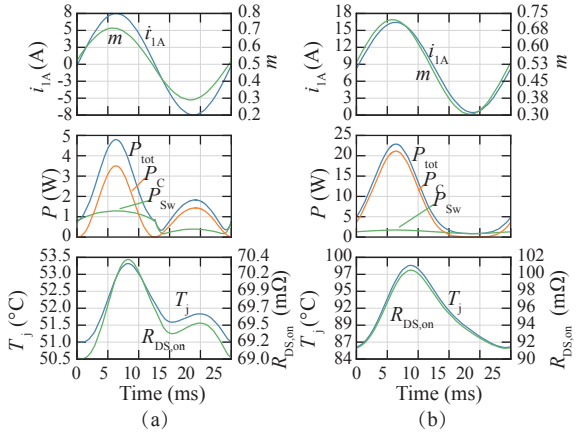


Fig. 11. Simulation results of the thermal behavior of a high-side half-bridge transistor during one fundamental load current period. (a) Regular interleaved mode. (b) Dual buck current control. $m$: half-bridge modulation index (relative turn-on time of the high-side transistor during a PWM period). Middle plots: transistor losses, $P_{tot} = P_C + P_{Sw}$. $\hat{i}_L = 16$ A, $f_F = 40$ Hz, $I_B = 8$ A, $f_{PWM} = 100$ kHz, $u_{DC} = 200$ V, $L_L = 2.5$ mH, $R_L = 5\,\Omega$, $T_a = 40$ °C, $R_{jc} = 0.5$ K W$^{-1}$, $C_j = 2.4$ mF, $R_{ca} = 5.5$ K W$^{-1}$, $C_{HS} = 10$ mF.

ambient. Values are given in Fig. 11. It is assumed that the heat sink fins and base plate are fixed at the ambient temperature $T_a$. This is justified as the heat sink has a comparably large thermal capacitance due to its mass and hence, its temperature variation is negligible. However, the thermal capacitance $C_{HS}$ models the capacitance of the less massive heat spreader, which connects the transistor case thermally to the base plate of the heat sink. The values of this capacitance/resistance are found using a thermal 3D FEM simulation that incorporates the utilized geometries and required material properties.

The temperature dependence of the $R_{DS,on}$ is usually provided by manufacturer data sheets, which facilitates the evaluation of the transistor conduction losses [27], [40]. Note that, as this model incorporates the important nonlinearities, it is capable of predicting thermal runaway, which can be caused by high transistor losses and the fact that the currents are impressed by the feedback control system. The disadvantage of this approach is that the thermal system requires time to reach its steady-state value, which prolongs simulations. This can be alleviated by initializing the thermal model to the expected temperatures.

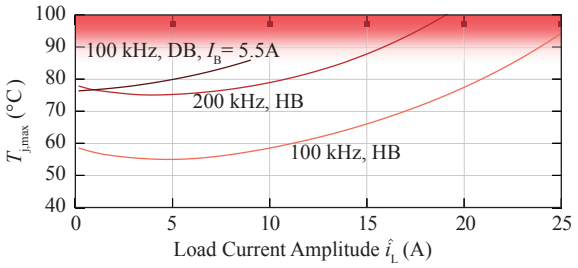


Fig. 12. Calculated peak junction temperatures during converter operation with PWM frequencies of 100 kHz and 200 kHz for the regular interleaved half-bridge (HB) and dual buck (DB) configurations (with a constant bias current of $I_B$ = 5.5 A). This is valid for all considered load configurations and for fundamental load current frequencies below ≈ 40 Hz.

### *B. Amplifier Operating Range*

Using the presented thermal model, incorporated into a complete converter circuit model and also including the cascaded feedback control system, the transistor thermal behavior can be investigated [43]. Fig. 11 exemplarily illustrates simulation waveforms. The load current $i_L$ is sinusoidal with an ampli- tude $\hat{i}_L$ of 16 A and a frequency of 40 Hz. In Fig. 11(a), the converter is operated with the regular, interleaved power stage topology. It can be seen that the junction temperature varies by ≈ 2.3 K. On the other hand, if the converter is operated with the dual buck mode (cf. Fig. 11(b)), which results in higher half-bridge currents as indicated, a variation of $T_j$ of ≈ 12 K ensues, which consequently also leads to a higher variation of the $R_{DS,on}$.

This simulation approach can be used to investigate the converter's highest allowable load current amplitude for a given operating configuration. The load current limit is set such that the peak junction temperature of the power transistors does not exceed ≈ 90 °C, in order to prevent thermal runaway and to provide some safety margin. The operating point illustrated in Fig. 11(b) exceeds this boundary, as the peak junction temperature reaches 98 °C. The allowable load current limits for different operating modes used in this work are illustrated in Fig. 12. Note that the transistor losses are practically independent of the chosen load resistor/inductor values, as they mainly depend on the switched current and not on the half-bridge duty cycles. The same applies for the fundamental frequency $f_F$ of the sinusoidal load current, as the reactive power (due to the half-bridge filter capacitors) is negligible at the considered frequencies. It is evident that the dual buck approach, due to its circulating bias current and thus, the increased transistor losses, can provide less load current before the junction temperatures reach critical values, which is an inherent limitation of this operating mode [7].

The achieved overall peak power conversion efficiencies of the demonstrator system are illustrated in TBALE II. They are obtained using a power analyzer to measure the active power at the converter input and the load ($P_L$). Note that the auxiliary power required for control and cooling fans is not included. Depending on the fan speed, the converter requires ≈ 10 W to 30 W of auxiliary power. The shown conversion efficiencies demonstrate the advantage of switch-mode power converters as compared to hybrid or linear solutions. Furthermore, the

TABLE II
MEASURED PEAK POWER CONVERSION EFFICIENCIES OF THE DEMONSTRATOR SYSTEM FOR DIFFERENT LOAD CONFIGURATIONS

| $u_{DC}$ | $f_{PWM}$ | $R_L + L_L$ | $\hat{i}_L$ | $P_L$ | $\eta$ |
|---|---|---|---|---|---|
| Regular Interleaved Topology: | | | | | |
| 400 V | 100 kHz | 10 Ω + 100µH | 18.5 A[a] | 1.7 kW | 96.5 % |
| | | 5 Ω + 2.5 mH | 24.0 A | 1.4 kW | 94.4 % |
| | | 2 Ω + 10 mH | 24.0 A | 576 W | 88.0 % |
| 400 V | 200 kHz | 10 Ω + 100 µH | 16 A | 1.3 kW | 94.7 % |
| | | 5 Ω + 2.5 mH | 16 A | 640 W | 90.4 % |
| | | 2 Ω + 10 mH | 16 A | 256 W | 80.3 % |
| Dual Buck Topology ($I_B$ = 5.5 A): | | | | | |
| 400 V | 100 kHz | 10 Ω + 100 µH | 8 A | 320 W | 85.4 % |

[a] Limited by load resistor dissipation capability.

achieved output powers exceed typical values of precision amplifiers currently employed in industry. The loss model also reveals that with an ohmic load of 14 Ω, a DC-link voltage of 400 V and a PWM frequency of 100 kHz, a load power of 4 kW is thermally feasible (sinusoidal load current with $\hat{i}_L$ = 24 A).

As the power transistor losses limit the load current, the next section shows the possibility of optimally extending the achievable output current range by paralleling power transistors.

### C. Extending the Load Current Range

It is illustrated how the load current range can be extended by changing the power transistor's active area (e.g., by placing two power transistors in parallel). This reduces the current of each transistor and hence, its losses and junction temperature, as shown above.

As the losses $P_T$ of a single *GS66508T* transistor are known in detail (cf. Fig. 9), the losses of $n$ parallel transistors, operating with a total half-bridge current $i_{HB}$, can be derived with:

$$P_{T,\,Tot} = nP_T\left(i_{HB}/n\right) \ . \tag{3}$$

This assumes that each transistor has its individual gate driver and cooling system, such that for each transistor, the same losses as presented in the previous section occur. Note that $n$ does not necessarily have to be integer, as long as the gate driver and cooling system is also scaled accordingly.

The resulting total transistor losses are illustrated in Fig. 13 for different $n$ and load current amplitudes $\hat{i}_L$, and a DC-link voltage of 400 V with a PWM frequency of 200 kHz. Note that these are the averaged transistor losses over one load current fundamental period. From this analysis, it can be seen that a single *GS66508T* transistor is the optimal selection for the operation with $\hat{i}_L \approx 20$ A at the indicated DC-link voltage and switching frequency. This extension of load current capability can similarly be achieved by introducing more interleaved half-bridges instead of paralleled transistors [44].

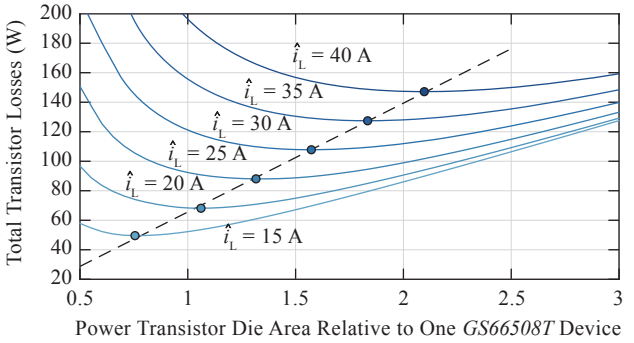


Fig. 13. Transistor losses (conduction and switching) of the demonstrator system, averaged over a fundamental period of the load current, for different load current amplitudes $\hat{i}_L$. The active transistor area is scaled relative to the active area of a single *GaN Systems GS66508T* transistor. $f_{PWM}$ = 200 kHz, $u_{DC}$ = 400 V. Regular interleaved power stage topology.

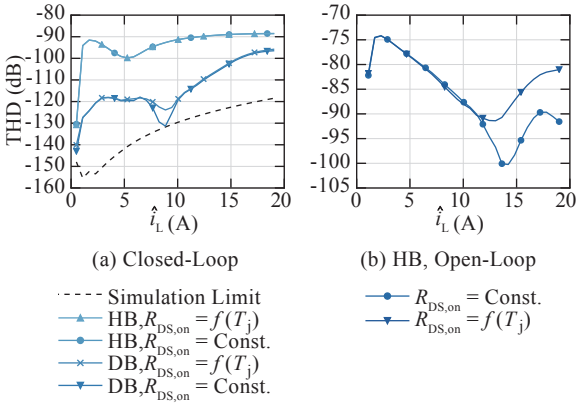


Fig. 14. Simulated THD of regular interleaved (HB) and dual buck (DB) topologies, incorporating thermal $R_{DS,on}$ cycling. (a) Closed-loop feedback control, $T_D$ = 40 ns. (b) Open-loop operation, $T_D$ = 10 ns. The simulation limit is the best achievable THD with an ideal amplifier model, only restricted by the simulation time step.

### D. Distortion Analysis

The presented transistor losses and thermal simulation model is used, in conjunction with a circuit simulation of the power amplifier demonstrator that also includes its closed-loop feedback control system, to assess the load current THD, with consideration of the junction temperature variation of each power transistor [43]. This approach allows the direct manipulation of thermal system properties, such that their influences on THD can be methodically investigated. A similar investigation regarding open-loop amplifiers has been performed in [20].

Fig. 14(a) visualizes simulation result with the load current THD of the two considered power stage topologies: Regular interleaved (HB) and dual buck (DB), for different load currents with closed-loop converter operation. Note that the power semiconductor switching action is assumed ideal in order to reduce the model complexity. Consequently, the indicated THD values are not directly comparable to measurements. However, they do reflect the influence of the $R_{DS,on}$-variation on THD.

It shows that the fluctuation of the junction temperature and the resulting change in $R_{DS,on}$ has only a negligible effect on

the distortion of the closed-loop converter system, even at high load currents and with the dual buck topology, which causes a significantly larger variation in $R_{DS,on}$, as shown in Section III-B. The thermal influence on THD manifest only when the closed-loop control system is not utilized, as Fig. 14(b) illustrates. However, in order to visualize the miniscule effects on THD during open-loop operation at all, the dead time is reduced to 10 ns in the simulation.

It can be concluded that the thermal dependency of the $R_{DS,on}$ does not significantly contribute to the output THD of a wide-bandgap, switch-mode power amplifier, even during open-loop operation, as other nonlinearities, most notably dead time, are source of more prominent distortion components.

## IV. Distortion Due to Dead Time

It is well-known that half-bridge interlock/dead time is a significant source of distortion in Class-D power amplifiers or DC/AC inverters [21], [22]. Consequently, this section demonstrates the amplifier's THD sensitivity to dead time and presents three methods that can be employed to significantly reduce dead time related distortion.

Fig. 15 briefly illustrates the nonlinear mechanism in half-bridges with dead time. The shape and time instants of the switched half-bridge output voltage transitions in $u_{SN}$ depend on the instantaneous magnitude and polarity of the half-bridge current $i_{HB}$, which is proportional to the load current and consequently, due to this load current dependent switch-node voltage behavior, indicated with the colored areas, harmonic distortion is introduced.

In the illustrated example, the first switching action undergoes a hard-switched transition whereas the second one is either fully soft or achieves partial soft-switching, which depends on the instantaneous value of $i_{HB}$, the power tran-sistor parasitic capacitances, the DC-link voltage (due to the nonlinear transistor capacitances), as well as other parasitic circuit capacitances, e.g., the load capacitance [45].

Using the demonstrator system, the effect of dead time on the amplifier output current distortion is experimentally investigated. Fig. 16 illustrates the THD for different dead times as a function of the load current amplitude of the 10 Ω + 100 µH load. As expected, dead time only affects odd harmonics, as the half-bridge output waveform error is a function of the current polarity, which renders it half-wave symmetrical. The amplitudes of the even harmonics are constant and independent of dead time, as the logarithmic fit matches well. The odd-order harmonics, which dominate the THD, depend significantly on dead time, which corroborates the expected high sensitivity to this cause of distortion. In the following, three methods are presented that ameliorate the distortion caused by dead time.

### A. Dead Time Minimization

The first approach to increase the amplifier linearity is to simply reduce dead time as much as possible. As Fig. 16 illustrates, 30 ns of dead time result in a THD of ≈ −100 dB

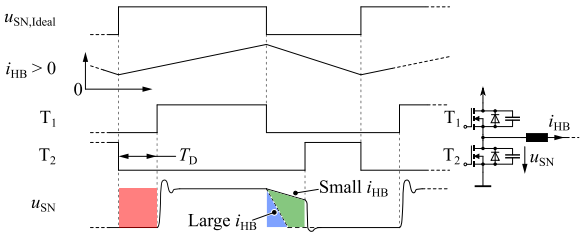


Fig. 15. Time-domain waveforms illustrating the cause of dead time related distortion in a half-bridge configuration. Depending on the magnitude and polarity of the half-bridge current $i_{HB}$, the switch-node voltage $u_{SN}$ deviates from the ideal shape, as indicated with the colored areas. Note that the low-frequency waveform of $i_{HB}$ is not visible during one PWM cycle as illustrated here, where the behavior during a time interval with $i_{HB} > 0$ is exemplarily chosen.

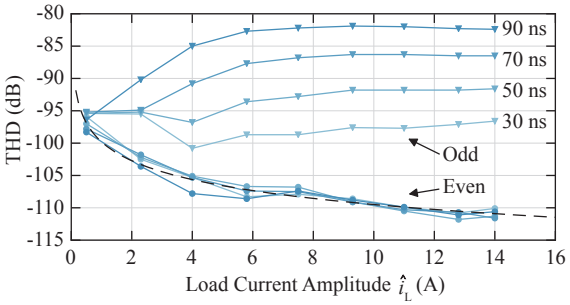


Fig. 16. Measured THD for different dead times as indicated. Load: 10 Ω + 100 µH. Odd harmonics: 3, 5, 7, 9. Even harmonics: 2, 4, 6, 8. The THD considering the even harmonics follows a logarithmic fit (dashed). $f_F$ = 35 Hz, $u_{DC}$ = 400 V, $f_{PWM}$ = 200 kHz.

over a wide load current range. Such low dead times are facilitated by the fast half-bridge switching transitions, which take less than 6 ns at a DC-link voltage of 400 V [23]. As the high-side half-bridge power transistor requires an isolated gate control signal, the propagation delay difference (skew) of the two half-bridge gate control signal paths (and the variation of this timing difference, e.g., due to temperature), which is mostly dominated by the digital signal isolators, imposes a practical lower limit to dead time, as it must be guaranteed that a minimum dead time is always ensured to prevent half-bridge shoot-through. With current digital signal isolators and gate drivers, the lower dead time limit is ≈ 30 ns to 60 ns [46]. Another option to further reduce dead time is given by special gate drivers that couple the two gate voltages and make sure that always only one transistor is conducting, while minimizing dead time at the same time [47]. However, this approach increases circuit complexity and affects the gate loop parasitic inductance, which, due to the fast switch-node transitions of the half-bridges and the low GaN HEMT gate threshold voltages, could lead to parasitic transistor turn-on [23]. Other approaches supervise the conduction state of a transistor and communicate it to the complementary gate driver that can then control the switching state accordingly [48], [49]. This method also requires more circuit elements and a fast communication channel to the isolated gate driver, which also has to be robust against fast common-mode transients.

Therefore, in the following, the second method to reduce

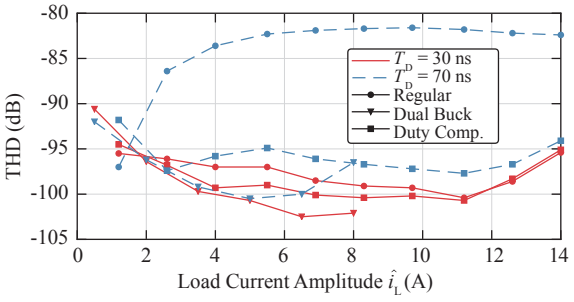


Fig. 17. Measured THD improvement using the dual buck topology and the duty cycle compensation method to reduce dead time related distortion. Load: 10 Ω +100 µH. $u_{DC}$ = 400 V, $f_{PWM}$ = 100 kHz, $f_F$ = 35 Hz. $I_B$ = 5.5 A for the dual buck topology.

dead time related distortion, based on a different power stage topology (the dual buck), as well as its effect on THD, is presented.

### *B. Dual Buck Topology*

As the demonstrator system supports the dual buck topology (see Section II-B), its effect on the load current THD can be investigated. Fig. 17 illustrates the results. By introducing the bias current ($I_B$ = 5.5 A), the THD can be significantly lowered, especially when the dead time is long. With shorter dead times, the linearizing effect of the dual buck topology is less pronounced, as the related distortion is already reduced. Unfavorably, the allowable load current amplitude is severely limited when operating the dual buck topology, which is due to the increased losses in the half-bridge transistors caused by the required bias current (see Section III-B). The inherently high losses of the dual buck topology could be lowered by dynamically adapting $I_B$ during converter operation to the momentarily occurring load current amplitudes, while still maintaining an acceptable distortion performance.

However, to circumvent the significantly higher losses and reduced load current capabilities of the dual buck, a feedforward compensation scheme is presented in the following.

### *C. Duty Cycle Compensation*

Different methods to reduce dead time induced distortion by means of a feedback or feedforward system have been presented [33], [50]–[54]. However, in the presented amplifier system, an advanced dead time compensation method can be employed, due to the availability of all half-bridge current and voltage measurements, and a high-performance digital processor. Its key feature is the continuous calculation of the faulty voltage-time areas introduced by dead time (cf. the colored areas in Fig. 15). The duty cycle of each half-bridge is then corrected such that the desired voltage-time area is applied to the half-bridge inductor, hereby reducing distortion caused by the dead time intervals. To further enhance the performance, the half-bridge current ripple is also calculated and considered. Fig. 18 illustrates the algorithm.

To model the half-bridge switching behavior, especially with

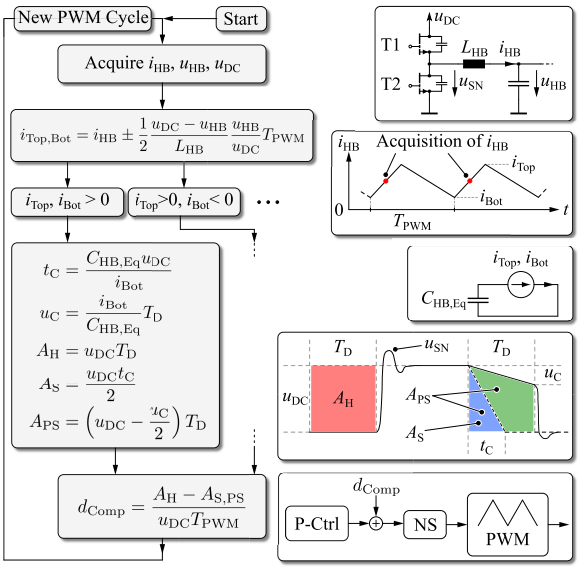


Fig. 18. Dead time compensation algorithm. The voltage-time area deviations caused by dead time are calculated and the reference duty cycle, provided by the half-bridge P-current controller, is corrected with $d_{Comp}$. Note that the algorithm is shown for $i_{Top,Bot} > 0$. For the other cases, the method works accordingly. The algorithm is not necessarily executed every PWM cycle as the calculation can take more than one cycle. NS: Noise shaper, for high-resolution PWM generation, see [34].

respect to the soft- and/or partially soft-switched transitions, resulting in the voltage-time areas $A_S$ and $A_{PS}$, the algorithm assumes a (linear) equivalent half-bridge capacitance $C_{HB,Eq}$, comprising the parasitic power transistor capacitances $C_{oss}$, as well as the parasitic capacitances in the PCB layout and the half-bridge inductor. During the switching transition, it is assumed that $C_{HB,Eq}$ is charged/discharged by a constant current, which, due to the large energy storage provided by $L_{HB}$ compared to the energies stored in $C_{HB,Eq}$, is valid for a wide current range [45]. Consequently, the soft-switched transition times of the switch-node voltage $u_{SN}$ are easily calculated as shown in Fig. 18. The value of $C_{HB,Eq}$ can be tuned during converter operation such that the THD is minimized. Due to the nonlinearity of the power transistor parasitic capacitances, the value for $C_{HB,Eq}$ depends on the DC-link voltage. In the demonstrator system, this value ranges from ≈ 300 pF to 400 pF (200 V to 400 V).

The algorithm is executed regularly and synchronously with the converter switching frequency, at a rate of 50 kHz, which is limited by the capability of the digital signal processor. Its effects on the load current THD are also shown in Fig. 17. If the system operates with $T_D$ = 70 ns, the benefits of the presented method are clearly visible, and it reaches THD levels close to what the dual buck topology can achieve, with the added benefit that the allowable load current is not limited, as the converter losses are not affected by the compensation method.

However, the dual buck topology still achieves a slightly better performance, which is mainly attributable to the fact that a linear equivalent capacitance is used to model the switching behavior, whereas the shape of the half-bridge voltage transitions is determined by the highly nonlinear power transistor ca-

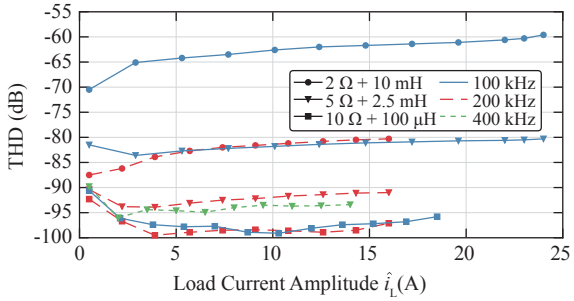


Fig. 19. Measured THD of three different loads for control system execution frequencies of 100 kHz, 200 kHz and 400 kHz. $f_F$ : 35 Hz. $u_{DC}$ = 400 V. PWM frequencies are 100 kHz and 200 kHz, whereas the 400 kHz control system rate is achieved by updating the reference twice per PWM period. Load currents are limited by the power transistor losses and/or the load resistor dissipation capabilities.

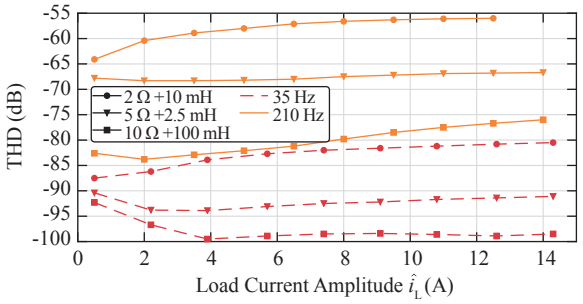


Fig. 20. THD measurements at an increased fundamental load current frequency $f_F$ = 210 Hz. The 35 Hz measurements are the results with the 200 kHz execution rate, as presented in Fig. 19.

pacitances. Additionally, the assumption of a constant current during the half-bridge transition to charge/discharge the capacitances also breaks down at small current amplitudes [45]. Furthermore, the actual dead time can also be slightly different from what the algorithm assumes, due to propagation delay skews between different gate signal paths (see Section IV-A). The algorithm could also be implemented based on a static lookup table, which would obviate the real-time calculation of the correction factors during converter operation.

## V. Control System Performance

The feedback control system is a key system component that affects the amplifier linearity considerably, as it suppresses undesired disturbances caused by nonlinear elements such as half-bridge dead time or saturating inductors [30], [31]. The structure of the demonstrator feedback system is described in Section II-C. As outlined, the power converter switching frequency, which is identical to the execution rate of the digital control system, directly affects the disturbance rejection performance of the feedback controllers. This is demonstrated in the following with measurements.

Fig. 19 illustrates measured load current THD figures for the three considered configurations, and different PWM frequencies. As expected, the THD is significantly reduced at higher controller execution rates. This especially applies to the load configurations that utilize the 2.5 mH or 10 mH iron core inductors (cf. Section II), as they are more nonlinear (i.e., they show a more current-dependent inductance variation) than the 100 µH gapped ferrite core inductor. The inductor nonlinearity manifests itself as a disturbance to the control system, which is rejected more effectively with higher control gains, and consequently, higher PWM and controller execution frequencies.

In order to double the control system execution rate, asymmetric regular sampling, where the modulator reference is updated twice per PWM cycle, can also be employed [33]. Note that this reduces the effectiveness of the digital noise shaper significantly and is hence not a preferred operating mode [34]. Nonetheless, Fig. 19 also illustrates the controller performance with asymmetric regular sampling, which results in a control system execution frequency of 400 kHz. However, THD is not significantly improved anymore. This is due to the digital implementation of the controllers in the FPGA fabric as logic circuits based on fixed-point arithmetic to enable high execution rates. Specifically, the type-III load current controller is modeled using an IIR filter which implements this controller's transfer function. As the clock frequency of the FPGA design is set to 200 MHz (again, to achieve short computation times), it prevents the usage of com-plex (i.e., wide bit-widths) multipliers and adders in order to achieve timing closure. Consequently, for high-gain controller implementations, internal signals can saturate and/or overflow, which subsequently renders the controllers unstable. Due to the implementation as an IIR filter, it is also difficult to implement stabilizing structures, such as anti-windup elements, which can further decrease the stability. Consequently, the controller gain has to be reduced in order to render it stable and hence, the control performance cannot increase arbitrarily.

A reduction in control performance is also observed at higher load current fundamental frequencies, as Fig. 20 reveals for $f_F$ = 210 Hz, which is compared to the 35 Hz, 200 kHz measurements from Fig. 19. The deterioration of the THD figures is due to the reduction of open-loop gain at higher frequencies, as illustrated in Fig. 8. This must be considered for amplifier systems that operate with elevated fundamental output frequencies. If necessary, the gains of the feedback controllers must be increased, e.g., by reducing the delay of the pulse-width modulator or the feedback sensors.

The measurements reveal a high sensitivity of the load current distortion to the control system's open-loop gain, which, due to digital implementation limits, cannot be arbitrarily increased. The necessity for linear loads, which otherwise introduce additional undesired distortion, is also demonstrated.

### *A. Kalman Filter*

As introduced in Section II, a Kalman estimator can be used to reduce noise in the acquired signals. This reduces the load current noise significantly due to the inherently high sensor noise sensitivity of closed-loop feedback control systems [31]. Details of the implementation and noise measurements are not scope of this paper. However, in the following, it is shown how

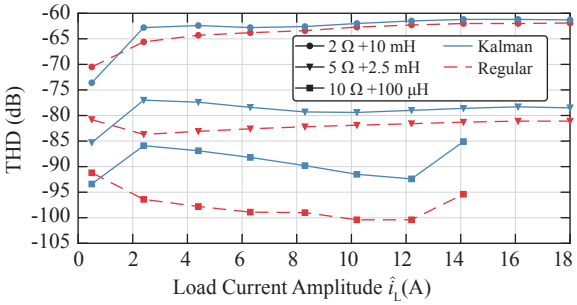


Fig. 21. Measured effect of the Kalman filter on THD. The trade-off between noise filtering and deterioration of THD is a tuning parameter of the Kalman filter. The sudden increase of THD at high load currents with the 10 Ω load is due to the DC supply output current limit. $u_{DC}$ = 400 V, $f_{PWM}$ = 100 kHz, $f_F$ = 35 Hz.

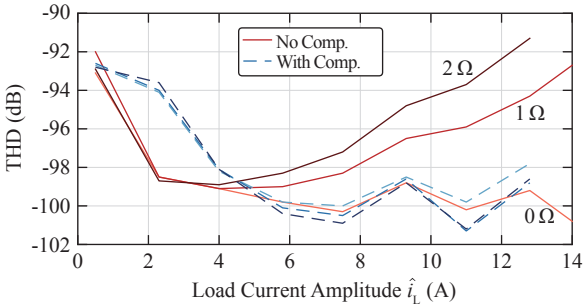


Fig. 22. Measured influence of an (ohmic) series impedance of the DC supply on the THD. Measuring the varying DC-link voltage and compensating the half-bridge duty cycles accordingly improves the THD. $u_{DC}$ = 200 V, $f_{PWM}$ = 200 kHz, $f_F$ = 35 Hz. Load: 10 Ω + 100 µH.

the converter linearity is affected.

The employed Kalman filter utilizes a linear system model of the converter and the load, in order to estimate the true values of its voltages and currents (i.e., without the measurement noise) [35]. The Kalman filter provides a tuning parameter (the Kalman gain) that weights its predictions, which are based on its linear model, against the measurements, in order to produce a new estimate of the system states. If the filter prediction is weighted more, sensor noise is effectively attenuated, since less emphasis is put on the measurements to create the new estimates. On the other hand, by weighting the measurements more than the output from the linear model, the estimates become more noisy. As a linear system model is used to create the filter predictions, nonlinearities, such as current-dependent inductances or thermal coefficients of load resistors, cannot be modeled and hence, the filter predictions do not contain corresponding harmonic distortion components. Consequently, if the Kalman gain is tuned with emphasis on the predictions, harmonics, like noise, are attenuated in the filter estimates, as the linear model allows for neither. This has the adverse effect that the actual harmonics present in the output current are then not supplied to the feedback controllers and thus, the load current THD deteriorates. The Kalman gain can be tuned to influence this trade-off between reduction in load current noise and allowable deterioration of THD [35].

Measurements shown in Fig. 21 illustrate this effect. With the Kalman filter enabled, the THD degrades, while at the same time, the load current noise is significantly reduced (not shown). Due to the high-performance processing system, the Kalman filter can be executed at a rate of 100 kHz, which is thus used as $f_{PWM}$ in this measurement.

The THD could potentially be improved by employing a Kalman system model that incorporates the nonlinearities of the physical system (e.g., current-dependent inductances). However, this requires an accurate model of the nonlinearities and potentially increases the computation time, with the result of decreasing the achievable controller execution rate, which affects THD adversely as shown earlier in this section.

## VI. DC Supply Impedance and Compensation

The supply voltage is a potential source of undesired signal components in the power converter output, as it directly affects the switched half-bridge voltages during the turn-on intervals of the high-side transistors. Open-loop Class-D amplifiers in principle have an insufficient power supply rejection and/or limited applicability for precision applications [21], [22]. If the power converter drives a bridge-tied load, as it is the case with the demonstrator system, where the load is connected between two converter phases (see Fig. 6), the load voltage, for the steady-state case and averaged over a switching period, is given as

$$u_L = u_1 - u_2 = u_{DC}\,(d_1 - d_2)\,, \tag{4}$$

whereas $d_{1,2}$ are the half-bridge duty cycles of the two phases (assuming regular interleaved operation). Thus, as $u_L$ is a function of $u_{DC}$, and $d_1 \neq d_2$ due to the bridge-tied load, the sensitivity to variations in the DC supply is high. Although this sensitivity is significantly reduced by the feedback controllers, if the DC-link voltage variation correlates to the converter output current, harmonic distortion can be introduced. This is, e.g., the case with a single-phase AC load that is characterized by a fluctuating instantaneous power and hence, an accordingly varying amplifier input current. The DC power supply, which usually has a given output series impedance $Z_s \neq 0$ and a limited disturbance rejection, cannot maintain its voltage output and hence, the DC-link voltage varies correspondingly. This variation is usually less than several volts and is finally attenuated by the closed-loop control system, but has to be considered for low-distortion power converters.

In the demonstrator system, the required half-bridge duty cycle $d$ is normally calculated from the P-current controller output, which is the requested half-bridge voltage $u^*_{HB}$ (cf. Fig. 6), by assuming a constant DC-link voltage value: $d = u^*_{HB}/u_{DC,Const}$. However, since the system is capable of measuring $u_{DC}$ during operation, the variation in $u_{DC}$ can be taken into account: $d = u^*_{HB}/u_{DC,\,Meas}(t)$. Such supply feedforward methods are also applied in audio amplifiers [55], at the disadvantage of requiring an additional voltage sensor.

The sensitivity of the load current THD to the DC supply series output resistance is investigated with the measurements shown in Fig. 22, both with and without the mentioned duty

cycle compensation. It is evident that a DC supply series impedance deteriorates the load current THD, especially at high current amplitudes, and despite the usage of closed-loop feedback control. However, when utilizing the feedforward compensation method, the THD is not affected by the varying supply voltage. The feedforward compensation approach is also effective at attenuating other undesired signal components from the DC-link voltage, which are potentially originating from the supply. Note that in Fig. 22, at low currents, the THD seems deteriorated by the usage of the feedforward compensation method. This is an artifact, as the measurement of $u_{DC}$ introduces noise to the duty cycle (through the noise of the DC-link voltage and its measurement), which consequently increases the load current noise. This masks some harmonics with noise and renders the THD measurement inaccurate at low load currents. A low-pass filter could reject some noise from the DC supply voltage measurement and reduce this effect. Nonetheless, a disadvantage of this compensation method is revealed, as it potentially increases the load current noise (whose analysis is the scope of future work).

## VII. Conclusion

Important system parameters of high-power switch-mode amplifiers that significantly influence their linearity and hence, total harmonic distortion (THD), are presented, analyzed and directly compared in order to identify critical design aspects. The findings are relevant for precision switch-mode power converters used to provide ultra-low-noise and low-distortion output voltages or currents, which are often required in different nanoscale positioning applications in the semiconductor manufacturing industry.

A 400 V amplifier prototype based on gallium nitride (GaN) power transistors and a cascaded feedback control system that uses low-distortion sensors, is utilized for investigations. Several methods and approaches are demonstrated. Load current THD values of less than −100 dB, or 0.001%, are achieved.

A detailed loss model of the converter system is used to determine the achievable load current amplitudes of the demonstrator system, which are limited by the power dissipation of the GaN transistors. In conjunction with a circuit simulation, it is revealed that the thermal modulation of the power transistor on-state resistances does not significantly contribute to distortion of the amplifier load current.

Dead time, which is inherently required in many switch-mode conversion systems, significantly increases load current distortion as it introduces a modulated voltage error at the switched half-bridge outputs. The detrimental effect of dead time on THD is demonstrated with detailed measurements. Three methods to reduce the influence of dead time on load current THD are exhibited. The first method aims at simply reducing the dead time, which is facilitated by the use of fast-switching GaN power transistors. A dead time of 30 ns is finally achieved and bounded only by propagation delay skews and tolerances in gate drivers and signal isolators. Another option to reduce such distortion is given by the interleaved dual buck power stage topology, which, by using a circulating bias current between two half-bridges, leads to unidirectional half-bridge currents. THD values of −102.5 dB are achieved, at the disadvantage of significantly increased losses and thus, a reduced load current range of the amplifier. Consequently, the third method employs a software algorithm which computes the dead time related error during converter operation and adjusts the half-bridge duty cycles accordingly. This method does not suffer from increased losses and shows a similarly high performance than the dual buck topology.

The importance of the feedback control system is also demonstrated. By increasing the power converter switching frequency, time delay in the control system plants can be reduced and consequently, the achievable open-loop gains of the feedback controllers can be increased, which effectively attenuates distortion components in the converter output signal. This also corroborates the need for low-loss GaN transistors that are capable of operating at elevated switching frequencies, despite high voltage/power levels (200 kHz at 400 V in the demonstrator system). A Kalman filter, which is effective at reducing sensor noise, can also be deployed. However, due to its linear system model, it attenuates distortion components in its estimates and hence, the THD of the controlled current deteriorates. Nonetheless, the Kalman filter provides a method to influence this behavior.

Finally, a method of rejecting disturbance and variation of the DC-link voltage is presented, as there is no ideal DC supply that could provide an ideally stable output voltage for the amplifier. The consequences of different DC supply impedances on the load current THD, and the effectiveness of the compensation method, are exhibited.

### *A. Outlook*

As the amplifier's key system components have been optimized to reduce distortion, the residual converter nonlinearity is mainly caused by external sources such as the DC supply or passive components like nonlinear filter or load inductors, or load resistors. In order to further improve the converter THD, several methods are considered.

First, the control system open-loop gains could be increased by using higher PWM frequencies, as shown in Section V. This, however, raises switching losses and reduces the available load current range of the amplifier (see Section III-B). Furthermore, the digital implementation of high-gain controllers requires great care and capable digital hardware in order to prevent numerical saturation or overflow effects. Approaches based on model predictive control are considered to be computationally too exhaustive, even with modern embedded processors [56].

Another option to increase the converter linearity would be the usage of a highly stable, low-impedance DC supply in order to provide a constant DC-link voltage for the main amplifier. Its control system could also be integrated with the amplifier to make use of feedforward compensation to further improves the supply's tracking performance.

Last, the THD could potentially be further reduced by adding distinct, low-power, high-frequency switch-mode con-version stages that could operate with high open-loop gains and thus

correct the residual errors of the load current/voltage.These auxiliary converter(s) could be, e.g., connected in series or parallel to the load, the DC-link, or the half-bridge filter capacitors [57]–[59]. However, this essentially creates a hybrid switch-mode converter system with an increased system com-plexity and development cost, which obviates the advantages of a single-stage power converter.

As mentioned in Section II, the low-distortion sensor system for the load current has an intrinsic THD limit of $\approx -110$ dB, which is primarily caused by the operational amplifiers of its analog front-end. This restriction could be overcome by reducing the filter complexity by, e.g., increasing the ADC sampling rate [36].

In conclusion, this paper demonstrates and measures important influence factors that affect distortion in ultra-high precision switch-mode power converters. Various effective countermeasures, which enable unprecedented distortion levels at high output powers, are presented. This permits the usage of switch-mode power amplifiers in domains previously occupied by inefficient, relatively complex and power-limited linear or hybrid systems.

## References


[1] F. Bordry and A. Dupaquier, "High current, low voltage power converters for IHC. Present development directions," in *Proc. of the Joint Accelerator Conferences, CERN*, Sept. 1996.

[2] F. Bouvet, "Design of the DC and AC magnet power supplies for the soleil synchrotron radiation source," in *Proc. of the European Conference on Power Electronics and Applications,* Sept. 2007, pp. 1–10.

[3] J. A. Sabaté, R. R. Wang, F. Tao, and S. Chi, "Magnetic resonance imaging power: high-performance MVA gradient drivers," *IEEE J. Emerg. Sel. Topics Power Electron.,* vol. 4, no. 1, pp. 280–292, Mar. 2016.

[4] M. L. A. Caris, "Exploring the power DCA: An asymmetric multilevel approach for high-precision power amplification," Ph.D. dissertation, *University of Eindhoven,* 2016, ISBN: 978-90-386-4181-2.

[5] R. Munnig Schmidt, G. Schitter, and J. van Eijk, *The Design of High Performance Mechatronics,* Delft University Press, 2011, ISBN: 978-1-60750-825-0.

[6] E. A. Lomonova, "Advanced actuation systems – State of the art: fundamental and applied research," in *Proc. of the International Conference on Electrical Machines and Systems*, Oct. 2010, pp. 13–24.

[7] J. M. Schellekens, "A class of robust switched-mode power amplifiers with highly linear transfer characteristics," Ph.D. dissertation, *University of Eindhoven*, 2014, ISBN: 978-94-6259-400-5, DOI: 10.6100/IR783105.

[8] P. Sriyotha, K. Nakamoto, M. Sugai, and K. Yamazaki, "Development of 5-axis linear motor driven super-precision machine," *International Academy For Production Engineering (CIRP)*, vol. 55, no. 1, pp. 381– 384, 2006.

[9] J. Otsuka and S. Hayama, "Special issue on precision and ultraprecision positioning," *International Journal of Automation Technology*, vol. 3, no. 3, pp. 223, 2009.

[10] G. Gong, "Hybrid amplifiers for AC power source applications," Ph.D. dissertation, *ETH Zurich, no. 18173*, 2009.

[11] K. Sato, "High-precision and high-speed positioning of 100 g linear synchronous motor," *Journal of the International Societies for Precision Engineering and Nanotechnology*, vol. 39, pp. 31–37, 2015.

[12] S. J. Settels, J. van Duivenbode, J. L. Duarte, and E. A. Lomonova, "Flying capacitor resonant pole inverter applying five voltage levels," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Oct. 2017, pp. 2121–2128.

[13] J. M. M. Rovers, J. W. Jansen, and E. A. Lomonova, "Multiphysical analysis of moving-magnet planar motor topologies," *IEEE Trans. Magn.*, vol. 49, no. 12, pp. 5730–5741, Dec. 2013.

[14] T. Tuma, W. Haeberle, H. Rothuizen, J. Lygeros, A. Pantazi, and A. Sebastian, "A high-speed electromagnetically-actuated scanner for dual-stage nanopositioning," in *Proc. of the 6th IFAC Symposium on Mechatronic Systems*, vol. 46, no. 5, 2013, pp. 125–130.

[15] T. Riel, R. Saathof, A. Katalenic, S. Ito, and G. Schitter, "Noise analysis and efficiency improvement of a pulse-width modulated permanent magnet synchronous motor by dynamic error budgeting," *Mechatronics, a Journal of the International Federation of Automatic Control (IFAC)*, 2017.

[16] M. Thier, R. Saathof, A. Sinn, R. Hainisch, and G. Schitter, "Six degree of freedom vibration isolation platform for in-line nano-metrology," in *Proc. of the 7th IFAC Symposium on Mechatronic Systems*, vol. 49, no. 21, 2016, pp. 149–156.

[17] F. Matichard, B. Lantz, K. Mason *et al*., "Advanced LIGO two-stage twelve-axis vibration isolation and positioning platform. part 1: Design and production overview," *Journal of the International Societies for Precision Engineering and Nanotechnology*, vol. 40, pp. 273–286, 2015.

[18] W. Kester, *The Data Conversion Handbook*. Elsevier, 2005, ISBN: 0-7506-7841-0.

[19] K. Sugioka, M. Meunier, and A. Pique, *Laser Precision Microfabrication*. Springer, 2010, ISBN: 978-3-6421-0522-7.

[20] M. Mauerer, A. Tüysüz, and J. W. Kolar, "Distortion analysis of low-THD/high-bandwidth GaN/SiC class-D amplifier power stages," in *Proc. of the Energy Conversion Congress and Exposition (ECCE USA)*, Sept. 2015, pp. 2563–2571.

[21] K. Nielsen, "Audio power amplifier techniques with energy efficient power conversion," Ph.D. dissertation, *University of Denmark*, 1998.

[22] F. Koeslag, "A detailed analysis of the imperfections of pulsewidth modulated waveforms on the output stage of a class d audio amplifier," Ph.D. dissertation, *University of Stellenbosch*, 2008.

[23] M. Mauerer, A. Tüysüz, and J. W. Kolar, "Low-jitter GaN E-HEMT gate driver with high common-mode voltage transient immunity," *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9043–9051, Nov. 2017.

[24] M. Berkhout and L. Dooper, "Class-D audio amplifiers in mobile applications," *IEEE Trans. Circuits Syst. I*, vol. 57, no. 5, pp. 992–1002, May 2010.

[25] J. M. Schellekens, H. Huisman, J. L. Duarte, M. A. M. Hendrix, and E. A. Lomonova, "An analysis of the highly linear transfer characteristics of dual-buck converters," *IEEE Trans. Ind. Electron.*, vol. 65, no. 6, pp. 4681–4690, June 2018.

[26] M. Mauerer, A. Tüysüz and J. W. Kolar, "Low-noise isolated digital shunt for precision class-d power amplifiers," *IEEE Trans. Power Electron.*, vol. 33, no. 3, pp. 1907–1910, Mar. 2018.

[27] A. Lidow, J. Strydom, M. de Rooij, and D. Reusch, *GaN Transistors for Efficient Power Conversion*, 2nd ed. Wiley, June 2014, ISBN: 978-1-118-84476-2.

[28] R. D. McLaughlin, G. Stanley, and J. Wordinger, "Audio amplifier efficiency and balanced current design – A new paradigm," in *Proc. of the 103rd Audio Engineering Society Convention*, Sept. 1997.

[29] G. R. Stanley and K. M. Bradshaw, "Precision DC-to-AC power conversion by optimization of the output current waveform – The half bridge revisited," *IEEE Trans. Power Electron.*, vol. 14, no. 2, pp. 372–380, Mar. 1999.

[30] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Springer, 2001, ISBN: 978-0-7923-7270-7.

[31] G. F. Franklin, J. D. Powell, and A. Emami-Naeini, *Feedback Control of Dynamic Systems*, 7th ed. Pearson, 2015, ISBN: 978-0-13-349659-8.

[32] L. Corradini, D. Maksimović, P. Mattavelli, and R. Zane, *Digital Control of High-Frequency Switched-Mode Power Converters*. Wiley, 2015, ISBN: 978-1-118-93510-1.

[33] D. G. Holmes and T. A. Lipo, *Pulse Width Modulation for Power Converters: Principles and Practice*. IEEE Press, 2003, ISBN: 978-0-471-20814-3.

[34] M. Mauerer, A. Tüysüz, and J. W. Kolar, "Gate signal jitter elimination and noise shaping modulation for high-SNR class-d power amplifiers,"

in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016.
[35] M. S. Grewal and A. P. Andrews, *Kalman Filtering*, 4th ed. IEEE Press, 2015, ISBN: 978-1-118-85121-0.
[36] M. Mauerer, A. Tüysüz, and J. W. Kolar, "Voltage/current measurement performance and power supply rejection in all-digital class-d power amplifiers," in *Proc. of the Annual Industrial Electronics Society Conference (IECON)*, Oct. 2016, pp. 666–673.
[37] Xilinx Co., "Zynq-7000 All Programmable SoC," June 2017, Product Specification, no. DS190, rev. 1.11.
[38] LEM Co., "Current Transducer IT 65-S ULTRASTAB," Apr. 2015, Datasheet, no. 88.K7.27.000.0, rev. 1.
[39] Rohde&Schwarz Co., "UPV Audio Analyzer," Oct. 2015, Manual and Specifications.
[40] G. Wang, J. Mookken, J. Rice, and M. Schupbach, "Dynamic and static behavior of packaged silicon carbide MOSFETs in paralleled applications," in *Proc. of the IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2014, pp. 1478–1483.
[41] E. A. Jones, F. Wang, D. Costinett, Z. Zhang, B. Guo, B. Liu, and R. Ren, "Characterization of an enhancement-mode 650-V GaN HFET," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, Sept. 2015, pp. 400–407.
[42] M. Guacci, D. Bortis, and J. W. Kolar, "On-state voltage measurement of fast switching power semiconductors," *CPSS Trans. Power Electron. Appl.*, vol. 3, no. 2, pp. 163–176, June 2018.
[43] GeckoCIRCUITS, Power Electronic Circuit Simulation Software, 2018, Gecko-Simulations Co., [Online]. Available: http://www.gecko-simulations.com.
[44] J. Ertl, "Schaltverstärker mit hoher ausgangsspannungsqualität, konzepte – eigenschaften – anwendungen (in German)," Ph.D. dissertation, *Technische Universität Wien*, 2003.
[45] M. Kasper, R. M. Burkart, G. Deboy, and J. W. Kolar, "ZVS of power MOSFETs revisited," *IEEE Trans. Power Electron.,* vol. 31, no. 12, pp. 8063–8067, Dec. 2016.
[46] Silicon Labs Co., "Si827x Digital Signal Isolator," Dec. 2017, Datasheet, rev. 0.6.
[47] A. Zajc, F. Zajc, I. Zajc Zdesar, and F. Zajc, "NZID (near zero interlock delay) driving principle," in *Proc. of the International Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management (PCIM)*, May 2014, pp. 1–9.
[48] S. K. Biswas, B. Basak, and K. S. Rajashekara, "Gate drive methods for IGBTs in bridge configurations," in *Proc. of the Annual IEEE Industry Applications Society Meeting (IAS)*, vol. 2, Oct. 1994, pp. 1310–1316.
[49] Y. Lobsiger and J. W. Kolar, "Closed-loop d*i*/d*t* & d*v*/d*t* control and dead time minimization of IGBTs in bridge leg configuration," in *Proc. of the Workshop on Control and Modeling for Power Electronics (COMPEL),* June 2013, pp. 1–7.
[50] Y. Murai, T. Watanabe, and H. Iwasaki, "Waveform distortion and correction circuit for PWM inverters with switching lag-times," *IEEE Trans. Ind. Appl.*, vol. 23, no. 5, pp. 881–886, Sept. 1987.
[51] A. R. Munoz and T. A. Lipo, "On-line dead-time compensation technique for open-loop PWM-VSI drives," *IEEE Trans.Power Electron.*, vol. 14, no. 4, pp. 683–689, July 1999.
[52] T. Sukegawa, K. Kamiyama, K. Mizuno, T. Matsui, and T. Okuyama, "Fully digital, vector-controlled PWM VSI-Fed AC drives with an inverter dead-time compensation strategy," *IEEE Trans. Ind. Appl.*, vol. 27, no. 3, pp. 552–559, May 1991.
[53] D. Leggate and R. J. Kerkman, "Pulse-based dead-time compen-sator for PWM voltage inverters," *IEEE Trans. Ind. Electron.*, vol. 44, no. 2, pp. 191–197, Apr. 1997.
[54] G. Grandi, J. Loncarski, and R. Seebacher, "Effects of current ripple on dead-time distortion in three-phase voltage source inverters," in *Proc. of the IEEE International Energy Conference and Exhibition (EN-ERGYCON)*, Sept. 2012, pp. 207–212.
[55] J. Andersen, D. Chieng, S. Harris, J. Klaas, M. Kost, and S. Taylor, "All digital high resolution class D amplifier designs using power supply feed-forward and signal feedback," in *Proc. of the 31st International AES Conference on New Directions in High Resolution Audio*, no. 24, June 2007.
[56] T. Geyer, *Model Predictive Control of High Power Converters and Industrial Drives.* Wiley, 2017, ISBN: 978-1-119-01090-6.
[57] R. B. Dai, J. L. Duarte, E. A. Lomonova, and N. J. H. Slaats, "Basic crossover correction cells for high precision power amplifiers," in *Proc. of the European Conference on Power Electronics and Applications (EPE ECCE Europe)*, Sept. 2017.
[58] G. B. Yundt, "Series- or parallel-connected composite amplifiers," in *Proc. of the Annual IEEE Power Electronics Specialists Conference (PESC)*, June 1984, pp. 121–128.
[59] H. Ertl, J. W. Kolar, and F. C. Zach, "Basic considerations and topologies of switched-Mode assisted linear power amplifiers," in *Proc. of the Applied Power Electronics Conference and Exposition (APEC)*, vol. 1, Mar. 1996, pp. 207–213.

**Mario Mauerer** received his M.Sc. degree in electrical engineering from ETH Zurich in 2014. During his subsequent Ph.D. studies, whose corresponding degree he obtained in 2018 from the Power Electronic Systems Laboratory, ETH Zurich, he investigated ultra-high precision and high-power wide-bandgap switch-mode power amplifier systems. He is currently working as a postdoctoral scientist at the Power Electronic Systems Laboratory with research topics regarding three-phase rectifiers, precision amplifiers and magnetically levitated actuators.

**Johann W. Kolar** received his M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria, in 1997 and 1999, respectively. Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drives. He has proposed numerous novel PWM converter topologies, and modulation and control concepts and has supervised over 70 Ph.D. students. He has published over 650 scientific papers in international journals and conference proceedings, 4 book chapters, and has filed more than 160 patents. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors. Dr. Kolar has received 27 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award and two ETH Zurich Golden Owl Awards for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the steering committees of several leading international conferences in the field and has served from 2001 through 2013 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.