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Motor Power Pulsation Buffer for Single-to Three-Phase Current-Source-Converter Drives

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***Abstract*—Single-phase-input variable-speed drives (VSDs) for three-phase motors typically employ bulky dc-link capacitors for buffering the inherent power pulsation at twice the mains frequency. Alternatively, the power pulsation can be accommodated in the drivetrain's moment of inertia, a concept known as motor power pulsation buffer (MPPB). This paper briefly describes how a state-of-the-art control implementation for single-to-three-phase voltage-source converters (VSCs) with MPPB functionality can be adapted to monolithic-bidirectional-GaN-transistor-based current-source converters (CSCs) which provide motor-friendly sinusoidal output voltages and feature the same transistor count.**

***Keywords*—Motor power pulsation buffer, variable speed drive, current-source inverter.**

I. Introduction

Variable-speed drives (VSDs) generally improve the system-level efficiency in high-volume industry applications of three-phase motors, including pumps, blowers, and compressors. If only a single-phase mains is available, like in rural environments or aboard trains, single-to-three-phase VSDs are required, which have been subject of extensive research, e.g., [1]–[6]. The power drawn from a single-phase grid inherently shows a twice-mains-frequency pulsation between zero and twice the average power, whereas the power output to a three-phase motor is constant. Therefore, the instantaneous power difference must be buffered, typically using a relatively large electrolytic dc-link capacitor between a mains-side single-phase power-factor-correction (PFC) rectifier and the three-phase motor inverter. However, targeting, e.g., compact systems for motor-integrated drives or high-temperature environments, electrolytic capacitors should be avoided [6].

The motor's (the drivetrain's) rotating mass with its moment of inertia is a *mechanical* energy storage (like a flywheel) that advantageously could be utilized as a power pulsation buffer by allowing a (minor) variation of the motor speed around a reference value (applications like pumps or compressors are insensitive to such minor speed fluctuations). Thus, there is no need for an electric energy storage and the dc-link capacitor can be made very small, i.e., designed for high-frequency (HF) ripple filtering only. Such motor power pulsation buffer (MPPB) concepts have been proposed earlier, e.g., in [7] with only a diode rectifier on the mains side and hence limited motor voltages if PFC functionality should be achieved, or in [8] using a single-to-three-phase matrix converter. Recently, [6] has comprehensively analyzed the MPPB concept for a motor-integrated two-stage VSD consisting of a single-phase PFC rectifier, a small dc-link capacitor, and a three-phase inverter, i.e., for a voltage-source converter (VSC) system.

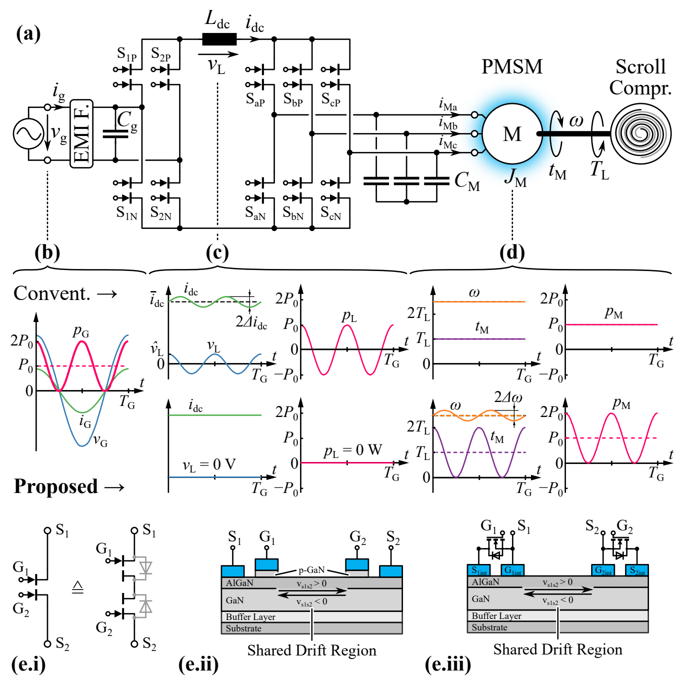

Fig. 1. Single-to-three-phase current-source-converter (CSC) motor drive. **(a)** Power circuit and conceptual key waveforms for the conventional operating mode (top row) and the proposed motor power pulsation buffer (bottom row), i.e., **(b)** grid voltage, current and power; **(c)** dc-link current and power processed by the dc-link inductor; **(d)** motor speed, torque, and power. **(e.i)** Monolithic bidirectional GaN transistor and its functional equivalent circuit; realizations as **(e.ii)** normally-off gate-injection transistor (GIT) [14], [17] and **(e.iii)** cascode configuration of a normally-on GaN transistor with low-voltage silicon MOSFETs (or GaN HEMTs) [15], [18], [19].

In this brief paper, we translate the control concept from [6] to a single-to-three-phase current-source-converter (CSC) drive as shown in **Fig. 1a-d**. Over the past decades, the interest in CSCs has steadily increased [9]–[13], first because wide-bandgap (WBG) devices allow high switching frequencies and hence small dc-link inductors, and more recently due to the availability of *monolithic* bidirectional GaN transistors [13]–[16]. These provide bipolar voltage blocking with a single drift region and thus only a slightly larger chip area compared to a standard transistor with unipolar blocking capability, see **Fig. 1e**.

Advantageously, a CSC features continuous motor voltages, which prevent HF motor losses, bearing currents, radiated EMI issues, and reflections on long motor cables and thus increased

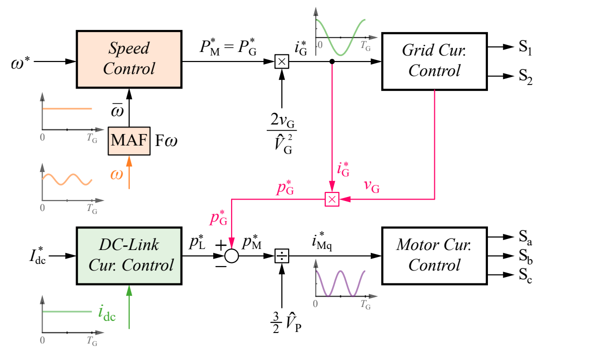

Fig. 2. High-level control diagram implementing the MPPB functionality for the CSC drive from **Fig. 1a**.

motor isolation stress [20]; with MBDSs, the transistor count does further not increase compared to the VSC topology from [6]. On the other hand, the dc-link inductor's low energy density (compared to electrolytic capacitors) would not allow buffering of the single-phase power pulsation (even though shown conceptually in the top row of **Fig. 1b-d** for illustrative purposes) with practically feasible dc-link inductors, i.e., an MPPB concept (see bottom row in **Fig. 1b-d**) is mandatory.

II. Motor Power Pulsation Buffer Control

Fig. 2 shows a high-level control diagram that implements the MPPB concept for the topology from **Fig 1a**; note the close relationship to the version for the VSC system from [6]. Here, we focus on the key aspects, which are further illustrated by the simulation results shown in **Fig. 3**. As the MPPB concept results in a variation of the motor speed ω around its average value $\bar{\omega}$, the speed controller must only act on that average value, which can be obtained using a moving average filter (MAF). From the average speed, the average power reference P_{M}^{*} and hence the grid current reference i_{G}^{*} follow. The grid-side single-phase current-source rectifier pulse-width-modulates the constant dc-link current i_{dc} such that, after (EMI) filtering, a sinusoidal grid current i_{G} in phase with the grid voltage results (PFC operation). Buffering the power pulsation in the motor implies that the dc-link current should be free of any low-frequency variation, i.e., $I_{\mathrm{dc}}^{*} = const.$, and it must be selected at least as high as the maximum amplitudes of the grid and motor currents. Together with the instantaneous grid input power p_{G}^{*}, a time-varying motor power reference p_{M}^{*} and hence an also time-varying q-current reference i_{Mq}^{*} result, which translates to motor phase current references i_{Ma}^{*}, i_{Mb}^{*}, i_{Mc}^{*} with an envelope at twice the mains frequency. Note that thus the generated torque varies between zero and twice the load torque T_{L}. Accordingly, the motor speed shows a variation which can be estimated as

$$\Delta\omega \approx \frac{P_0}{2\pi \cdot 2 f_{\mathrm{G}}} \cdot \frac{1}{\bar{\omega} J_{\mathrm{M}}} \tag{1}$$

($\approx 13\,\mathrm{rad/s}$ for the case considered in **Fig. 3**; see caption for symbol definitions). Note that an unrealistically large dc-link inductance of $L_{\mathrm{dc}} = P_0/(4\pi f_{\mathrm{G}} I_{\mathrm{dc}} \Delta i_{\mathrm{dc}}) \approx 700\,\mathrm{mH}$ would be needed if the mains power pulsation was to be buffered there, whereas $L_{\mathrm{dc}} = 1\,\mathrm{mH}$ easily suffices with the described MPPB approach. Note further that MPPB operation increases the motor winding losses by about 50% due to higher rms currents [6]. Advantageously, in contrast to VSC systems, the conduction losses of the CSC's transistors do only increase if the motor voltage is low ($V_{\mathrm{M}} < 2/3 \cdot V_{\mathrm{G}}$, both phase-to-neutral rms) and hence the motor-side peak currents define the required dc-link current level.

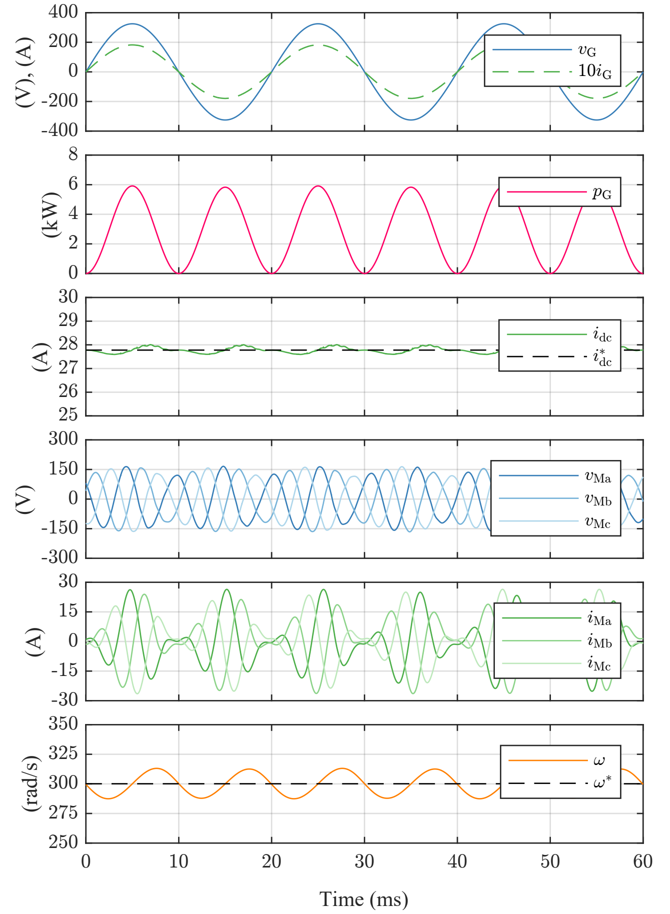

Fig. 3. Circuit simulation (PLECS) results at the nominal operating point of the topology from **Fig. 1a** (nominal power $P_0 = 2.5\,\mathrm{kW}$, grid voltage $V_{\mathrm{G}} = 230\,\mathrm{V}$ rms, grid frequency $f_{\mathrm{G}} = 50\,\mathrm{Hz}$, dc-link inductance $L_{\mathrm{dc}} = 1\,\mathrm{mH}$, motor-side filter capacitors $C_{\mathrm{M}} = 10\,\mu\mathrm{F}$) including the mechanical model of a PMSM (mechanical speed $\omega_{\mathrm{M}} = 300\,\mathrm{rad/s}$, pole pair count $p = 4$, permanent magnet flux $\Psi = 0.1\,\mathrm{Vs}$, d-/q-axis inductances $L_{\mathrm{d}} = L_{\mathrm{q}} = 2\,\mathrm{mH}$, stator resistance $R_{\mathrm{s}} = 1\,\Omega$, moment of inertia (motor and load) $J_{\mathrm{M}} = 0.001\,\mathrm{kg\,m^2}$, load with quadratic speed-torque characteristic and nominal torque $T_{\mathrm{L,N}} = 8.3\,\mathrm{Nm}$).

III. Conclusion

The inherent twice-mains-frequency input power pulsation of single-to-three-phase VSDs can be buffered utilizing the drivetrain's moment of inertia. Here, we translate the motor power pulsation buffer (MPPB) concept known for an electrolytic-capacitor-less voltage-source converter (VSC) [6] to a current-source converter (CSC) that inherently features sinusoidal motor voltages; novel monolithic bidirectional GaN transistors facilitate the realization of such CSCs with the same transistor count and similar total chip area as for VSCs. Future research should address a comparative evaluation of the CSC against the VSC concept regarding losses, size, cost, and possibly a full life-cycle analysis (LCA) [21].

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