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***Abstract*— Three-phase phase-modular isolated PFC rectifiers are an interesting alternative to phase-integrated three-phase rectifiers as matrix-type phase modules allow a single-stage isolated energy conversion between the three-phase mains and a dc bus. Therefore this paper presents a phase-modular isolated matrix-type rectifier which can be connected to the mains either in star (Y) or delta (Δ) configuration, enabling a wide input voltage range. Additionally this allows to select the voltage and current stresses of the phase module switches according to the used semiconductor technology, for example 650 V Si or GaN devices could be used in rectifiers powered from the 400 V rms or 480 V rms mains. A detailed analysis of the operating principles and switching behavior of the converter is presented, showing that zero voltage switching can be achieved in the phase modules. Additionally a third harmonic current injection concept is proposed which allows an up to 15 % higher output voltage in Δ-mode. The concepts are validated with measurements taken on a 7.5 kW, 400 V dc output voltage prototype converter achieving 97.2 % efficiency and a total harmonic distortion of < 2 % at rated power.**

***Index Terms*—indirect matrix-type, phase-modular rectifier, active third harmonic current injection, three-phase buck-type PFC converter, rectifier systems**

I. INTRODUCTION

Today power distribution systems for sensitive equipment, which requires an uninterruptible power supply (UPS), are typically realized with backup batteries. Depending on the application the batteries are either directly connected to a dc distribution bus or are part of a dedicated ac-ac UPS. Systems with a power level of more than $\approx$ 3 kW are typically supplied from the three-phase ac mains through a controlled rectifier which charges the backup batteries during normal operation. In order to comply with regulations the rectifier circuits have to achieve near sinusoidal input currents which are in-phase with the mains voltages, i.e. a power factor close to unity is required at the mains interface [1, 2]. Hence these systems are usually called power factor correction (PFC) rectifiers.

As the dc bus voltage is typically a function of the battery's state of charge the rectifier's output current and voltage have to be controlled and an adaption of the output voltage is required. Furthermore, galvanic isolation between the ac mains and the dc bus is required in certain applications, for example for safety reasons or due to different grounding schemes on ac and dc side. This can, for example, be achieved by cascading a standard three-phase boost-type PFC rectifier, like the VIENNA rectifier or a six-switch boost rectifier, and a subsequent isolated dc-dc converter. As an alternative, three-phase isolated matrix-type PFC rectifiers have been proposed, which allow a single-stage energy conversion between the three-phase ac mains and a dc bus. Both direct and indirect matrix-type PFC rectifiers, as well as systems based on an integrated active filter, have been analyzed in the literature [3–10].

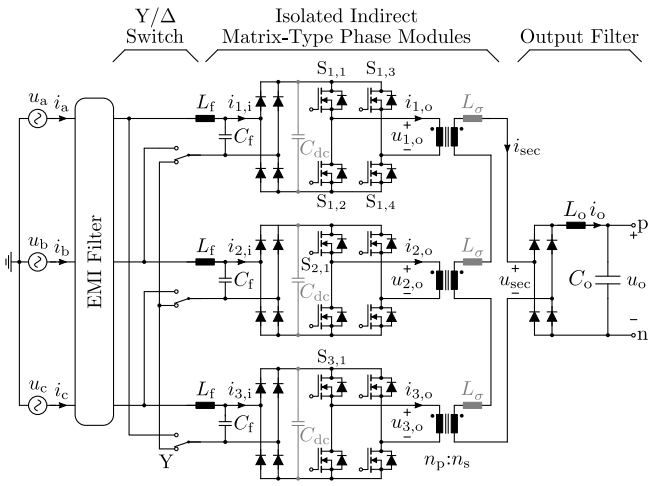

Fig. 1. Schematic of the Three-Phase Phase-Modular Isolated Indirect Matrix-Type Y/Δ rectifier (IMY/D rectifier) as proposed in [22].

All topologies mentioned above can be classified as phase-integrated topologies where a network of switches and diodes is used to apply the different line-to-line mains voltages to a single high-frequency isolation transformer. As an alternative, phase-modular topologies have been proposed for both, two-stage [11–14] and matrix-type systems where three separate phase modules are connected in star or delta at the mains input. In matrix-type systems the switches and diodes [15], and potentially also the transformer and output rectifier as well, are separated into three individual single-phase matrix-type rectifier modules. If individual phase module transformers are used, their ac output voltages can be connected in series [16, 17] or a three-phase configuration together with a three-phase diode rectifier can be used [18]. Alternatively, the secondary side voltages of the phase module transformers can be rectified individually and then

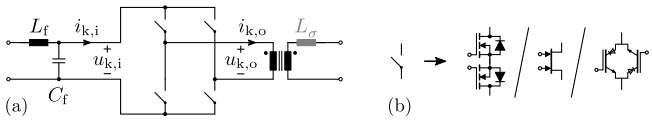

Fig. 2. Schematic of a direct matrix-type phase module using an H-bridge of bidirectional switches to directly apply $u_{\mathrm{k,i}}$ to the isolation transformer ($u_{\mathrm{k,o}}$) with alternating polarity. The bidirectional switches can be implemented, for example, by a series connection of two MOSFETs, a monolithic bidirectional GIT [24, 25] or a parallel connection of two reverse-blocking IGBTs.

connected either in series [19] or in parallel [20]. If the output rectifier is replaced by switches no dedicated dc output inductor is required and a quad active bridge converter results which allows bidirectional power flow [21].

In this paper the phase-modular indirect matrix-type PFC rectifier system (IMY/D rectifier), introduced in [22, 23] and shown in Fig. 1, is analyzed in detail. Each phase module consists of an input filter capacitor C_f and potentially an input filter inductor L_f, a full-wave diode rectifier, a full-bridge of switches and an isolation transformer. The secondary side windings of the phase module transformers are connected in series, yielding the voltage u_sec which is rectified by a full-wave diode bridge and low-pass filtered by the output filter L_o and C_o.

The phase modules shown in Fig. 1 are derived from an indirect matrix converter which means that the mains input voltage is first rectified by a full-bridge of diodes and then applied to the transformer by an H-bridge of MOSFETs or IGBTs. An additional capacitor $C_\mathrm{dc} \ll C_\mathrm{f}$ is required to provide a valid conduction path during the commutation of the active switches $\mathrm{S}_{\mathrm{k},1..4}$. Alternatively direct matrix-type phase modules (cf. Fig. 2), which consist of a single H-bridge of bidirectional switches could be used. These switches can, for example, be implemented by an antiseries connection of two MOSFETs, a monolithic bidirectional switch or an antiparallel connection of two reverse-blocking IGBTs.

It can be seen in Fig. 1 that the IMY/D rectifier is a buck-type system as the last stage of the ac input filter are capacitors (C_f) which impress a voltage and as an output inductor (L_o) is connected to the switch network on the dc side. As three individual transformers are used the phase modules can be connected to the mains either in star (Y) or delta (Δ) configuration which allows a wide input voltage range. Note that the individual phase-modules and the isolation transformers have to process a power pulsating with twice the mains frequency due to the single-phase nature of the individual phase modules. However, as matrix-type phase-modules are used, no low frequency energy storage elements are required. Due to the series connection of the transformers' secondary side windings the powers delivered by the three phase-modules add up and the power pulsations with twice the mains frequency cancel as in other three-phase PFC rectifiers. This implies that the output filter does not require any mains frequency energy storage elements either.

The basic modulation and control principles of the IMY/D rectifier are described in Section II. Based on these considerations a modified modulation scheme is proposed in Section III which allows zero voltage switching (ZVS) of all phase module inverter switches. Additionally third harmonic current injection in Δ-mode is analyzed in Section IV, showing that it allows an up to 15 % higher output voltage. Details of the implemented prototype and measurement results are discussed in Section V.

TABLE I
ELECTRICAL SPECIFICATIONS OF EXAMPLE IMY/D RECTIFIER

Nominal Mains Voltage (Line to Neutral)	$U_1 = 230\,\mathrm{Vrms}$
Mains Frequency	$\omega_1 = 2\,\pi\,50\,\mathrm{Hz}$
Nominal Output Voltage	$U_\mathrm{o} = 400\,\mathrm{V}$ dc
Nominal Output Power	$P = 7.5\,\mathrm{kW}$
Switching Frequency	$f_\mathrm{s} = 72\,\mathrm{kHz}$

II. BASIC PRINCIPLE OF OPERATION

The phase modularity of the IMY/Δ rectifier shown in Fig. 1 can be used to derive a modulation strategy achieving sinusoidal input currents which are in phase with the mains voltages

$$\begin{aligned} u_\mathrm{a} &= \hat{U}\,\cos(\omega t) \\ u_\mathrm{b} &= \hat{U}\,\cos(\omega t - 2\pi/3) \\ u_\mathrm{c} &= \hat{U}\,\cos(\omega t + 2\pi/3) \end{aligned} \tag{1}$$

resulting in a power factor close to unity. In the following derivation a Y-connection of the phase modules is assumed.

A. Modulation

As described above, the IMY/D rectifier consists of three individual phase modules which apply the corresponding rectified ac input voltage to its transformer's primary winding. As the secondary side windings of the transformers are connected in series the secondary side current i_sec flows through all three secondary side windings, if the output diode bridge is not free wheeling, i.e. if at least one phase module provides an output voltage $u_{\mathrm{k,o}}$ ($\mathrm{k} \in \{1,2,3\}$) not equal to zero. Neglecting the magnetizing current of the transformers, this implies that the current $i'_\mathrm{o} = i_\mathrm{o}\,n_s/n_p$ transformed to the primary side flows through all phase modules' full bridges. Note that the inverter switches $\mathrm{S}_{\mathrm{k},1..4}$ in the phase modules have to be operated with 50 % duty cycle and phase shift modulation in order to provide a conduction path for i_sec at all times.

Therefore, when a phase-module k is applying its line voltage to its transformer, the current i'_o is drawn from the phase-module's ac input. Assuming a constant dc output current I_o the local average $\langle i_{\mathrm{k,i}} \rangle_{T_s}$ of the phase-module's input current $i_{\mathrm{k,i}}$ over one switching frequency period $T_\mathrm{s} = 1/f_\mathrm{s}$ can be expressed as

$$\langle i_{\mathrm{k,i}} \rangle_{T_\mathrm{s}} = d_\mathrm{k}\,I'_\mathrm{o} = d_\mathrm{k}\,\frac{n_s}{n_p}\,I_\mathrm{o} \quad \forall\,\mathrm{k} \in \{1,2,3\}\ . \tag{2}$$

If sinusoidal duty cycles,

$$\begin{aligned} d_1 &= m\,|\cos(\omega t)|\,, \\ d_2 &= m\,|\cos(\omega t - 2\pi/3)|\,, \\ d_3 &= m\,|\cos(\omega t + 2\pi/3)|\,, \end{aligned} \tag{3}$$

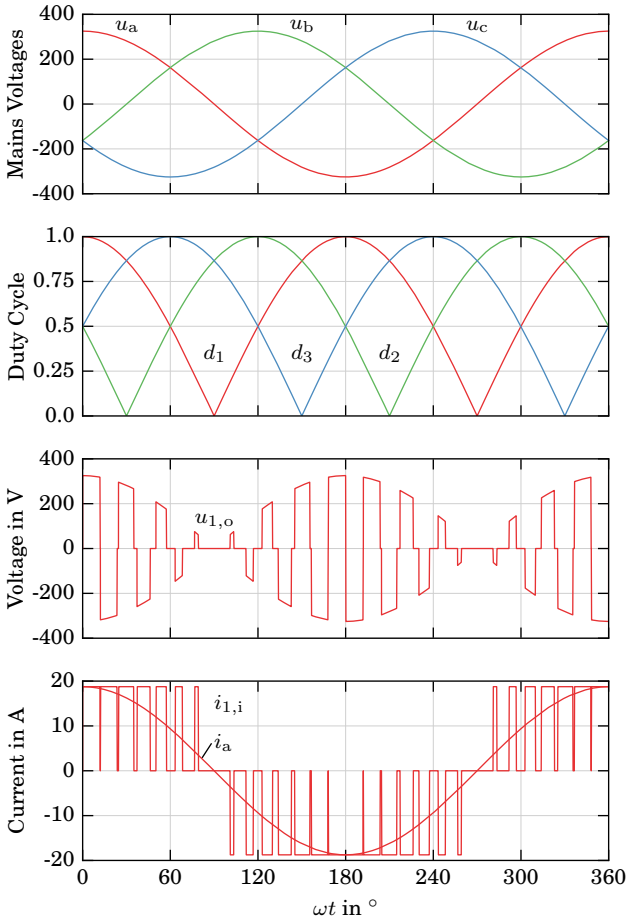

Fig. 3. Visualization for low switching frequency of the basic modulation scheme in Y-configuration at maximum modulation index $m = 1$: each phase module produces a square-shaped high-frequency transformer voltage $u_{k,o}$ k $\in \{1,2,3\}$ with a duty cycle d_k proportional to its corresponding line voltage $u_{a,b,c}$. Neglecting C_{dc}, a phase module input current $i_{k,i}$ proportional to the duty cycle d_k results. After low-pass filtering the ac input current i_a is obtained.

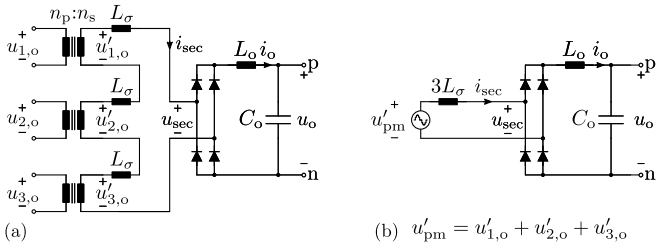

Fig. 4. (a) Circuit diagram of the IMY/Δ rectifier's output stage and (b) its equivalent circuit which shows the buck-type structure of the rectifier.

in-phase with the ac input line voltages of the phase-modules are used, sinusoidal input currents result after low-pass filtering of the switching frequency components, as shown in Fig. 3. Note that m is the converter's modulation index and describes the current transfer ratio

$$m = \frac{\hat{I}}{I'_o} = \frac{\hat{I}}{I_o}\,\frac{n_p}{n_s} \quad m \in [0,1]\,, \tag{4}$$

where $\hat{I}$ is the amplitude of the ac input line currents.

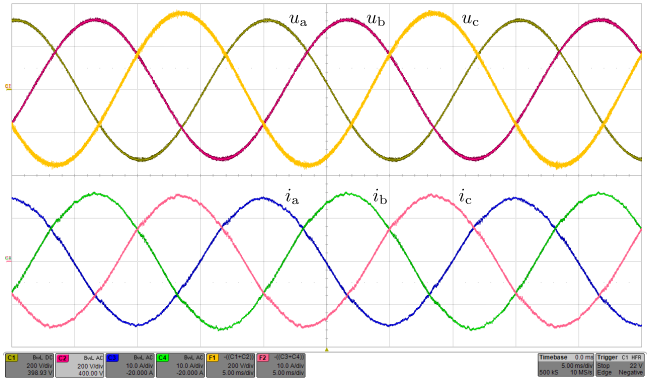

Fig. 5. Measurement results: mains voltages u_a, u_b, u_c (200 V/div, 5 ms/div) and line input currents i_a, i_b, i_c (10 A/div) in Δ-mode at nominal operating conditions specified in Table I. Note that the quantities of phases a and b were measured directly while those of phase c are recreated numerically as $u_c = -u_a - u_b$ and $i_c = -i_a - i_b$

Due to the series connection of the phase module transformer's secondary side windings (cf. Fig. 4a) the voltage u_{sec} which is applied to the dc side full-bridge diode rectifier can be approximated as,

$$u_{sec} \approx \frac{n_s}{n_p}\left(u_{1,o} + u_{2,o} + u_{3,o}\right)\,, \tag{5}$$

assuming that the transformers' leakage inductances L_σ can be neglected. As the duty cycles and line voltages vary throughout the mains period, the output voltage pulses of the individual phase modules have different amplitude and width, however, after rectification and low-pass filtering (L_o, C_o) a dc output voltage u_o results which can be calculated as

$$u_o = \langle |u_{sec}| \rangle_{T_s} \approx \frac{3}{2}\,\hat{U}\,\frac{n_s}{n_p}\,m = U_{o,max,Y}\,m\,. \tag{6}$$

This shows that the IMY/D rectifier is a buck-type rectifier topology which implies that a dc output voltage u_o between zero and an upper limit $U_{o,max}$ can be generated. A measurement of the mains voltages and the resulting input currents taken at a prototype converter built according to the specifications in Table I is shown in Fig. 5.

B. Control Scheme

A control scheme based on (6) and the equivalent circuit shown in Fig. 4 is shown in Fig. 6 and has been explained in [22] and [26]; accordingly only a brief description follows.

1) DC Output: The dc output is regulated by two cascaded control loops: an outer voltage controller G_u compares the dc output voltage u_o with its reference u_o^* to determine the output current reference i_o^*. This signal is compared to the measured inductor current i_o by the current controller G_i. By adding the measured output voltage u_o to its output the desired average rectified secondary side voltage $\langle |u_{sec}| \rangle^*_{T_s}$ is derived. Dividing by $U_{o,max}$, which is a function of the mains voltage amplitude $\hat{U}$, yields the modulation index m. According to (3) m is multiplied with sinusoidal shaping signals derived from the measured ac mains voltages as $u_{a,b,c}/\hat{U} \in [-1;1]$. After adding a zero-sequence modulation

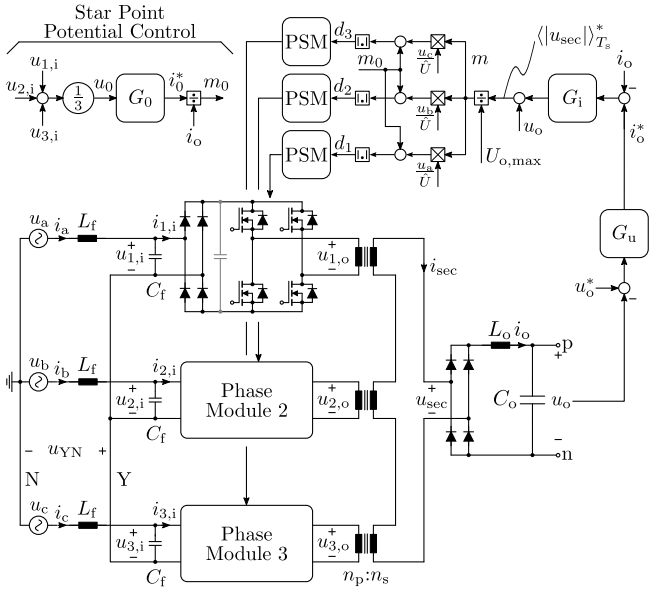

Fig. 6. Control block diagram of the IMY/D rectifier: An outer voltage controller G_u derives the reference i_o^* for the inner current controller G_i which uses the modulation index m to control i_o [26]. If a Y-configuration is used the potential of node Y (i.e. it voltage w.r.t to the ac mains neutral N, u_{YN}) is controlled by G_0 using a zero sequence input current reference i_0^* which yields a zero sequence modulation index m_0. Three individual phase shift modulators (PSM) are used, each operating the two half bridges of one phase module with 50 % duty cycle.

signal m_0 the absolute value yields the duty cycle signals $d_{1,2,3}$ used by the phase shift modulators of the three phase modules.

2) Star Point Potential: In a Y-configuration, as shown in Fig. 6, the potential of the star point Y can float with respect to the mains neutral N due to unbalances in the phase module input currents $i_{\mathrm{k,i}}$. Assuming that the mains' zero sequence sequence voltage can be neglected the voltage u_{YN} between nodes Y and N can be estimated as the zero sequence component of the measured phase module input capacitor voltages

$$u_{\mathrm{YN}} \approx u_0 = \frac{1}{3}\left(u_{1,\mathrm{i}} + u_{2,\mathrm{i}} + u_{3,\mathrm{i}}\right) \quad . \tag{7}$$

A controller G_0 is used to derive the zero sequence current i_0^* necessary to keep u_0 close to zero. Dividing this reference by the output current i_{o} yields the zero sequence modulation signal m_0 which is added to all three phase module modulation signals as described above. Note that G_0 can be omitted ($m_0 = 0$) if the phase modules are connected in Δ-configuration.

Measurement results taken at the prototype IMY/D rectifier in Y-configuration are shown in Fig. 7. The star point potential controller is turned off during the first 25 ms and u_{YN} significantly deviates from 0 causing distortions in the input and output currents. Once the controller is enabled $u_{\mathrm{YN}} \approx 0\,\mathrm{V}$ is achieved. Note that a significant switching frequency ripple of u_{YN} can be seen due to the discontinuous phase module input currents $i_{\mathrm{k,i}}$ (cf. Fig. 3) and the comparatively small value of the filter capacitors C_{f}. As these are connected to the ac mains their capacitance cannot be

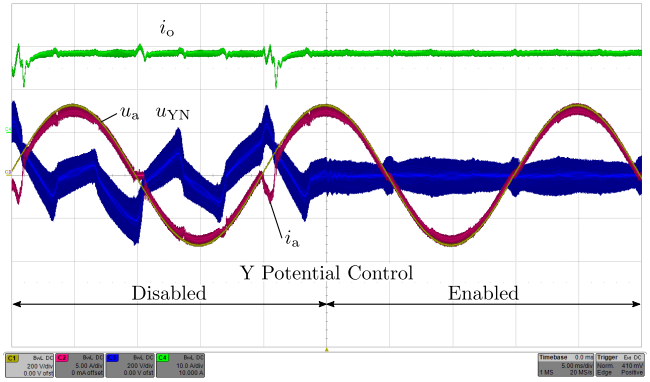

Fig. 7. Measurement results showing the mains voltage u_{a} (200 V/div), the corresponding ac input current i_a (5 A/div), the voltage u_{YN} (200 V/div) between the filter capacitor star point Y and the mains neutral N and the output current i_{o} (10 A/div). During the first 25 ms the star point potential controller is disabled which results in distortions of i_{a} and i_{o}. Once the controller is enabled a sinusoidal input current and a constant output current are achieved.

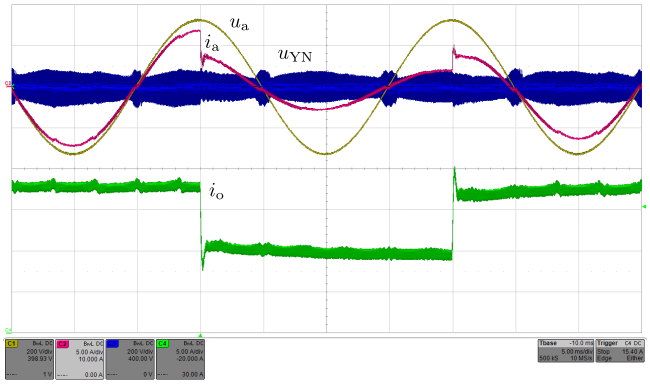

Fig. 8. Measurement results for step changes of the current controller reference signal i_{o}^* from 18 A to 9 A and back. Shown are the output current i_{o} (10 A/div), the mains voltage u_{a} (200 V/div), the corresponding ac input current i_a (5 A/div) and the star point voltage u_{YN} (200 V/div).

increased arbitrarily because of reactive power demand and power factor limitations, which is also the case in other buck-type rectifiers [27, 28]. Additional measurement results for a step change in the current reference signal i_{o}^* from 18 A to 9 A and back are shown in Fig. 8. It can be seen that the potential of the star point Y stays close to zero even during a fast transient of i_{o}.

III. Advanced Modulation for Improved Efficiency

The modulation principle described in Section II requires that all phase modules create rectangular output voltage pulses $u_{\mathrm{k,o}}$ with duty cycles d_{k} proportional to the absolute value of their corresponding ac input voltage. Note that no particular alignment of these switching frequency voltages is required for the derivation given above.

A. Symmetric Modulation

If symmetric phase shift modulation as described in [26] is used for all three phase modules, the output voltage pulses of

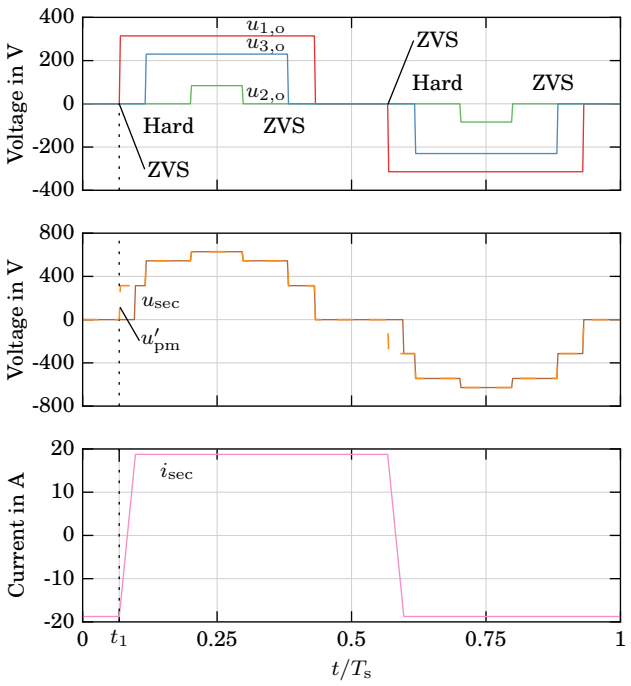

Fig. 9. Drawing ($n_s/n_p = 1$) of the three phase module output voltages $u_{k,o}$ and the resulting voltage u_{sec} which is applied to the dc side full bridge rectifier for symmetric modulation, where the switching frequency pulses in $u_{k,o}$ are center aligned. The phase module with the highest voltage ($u_{1,o}$) achieves zero voltage switching (ZVS) while the remaining two phase modules typically exhibit a hard turn on.

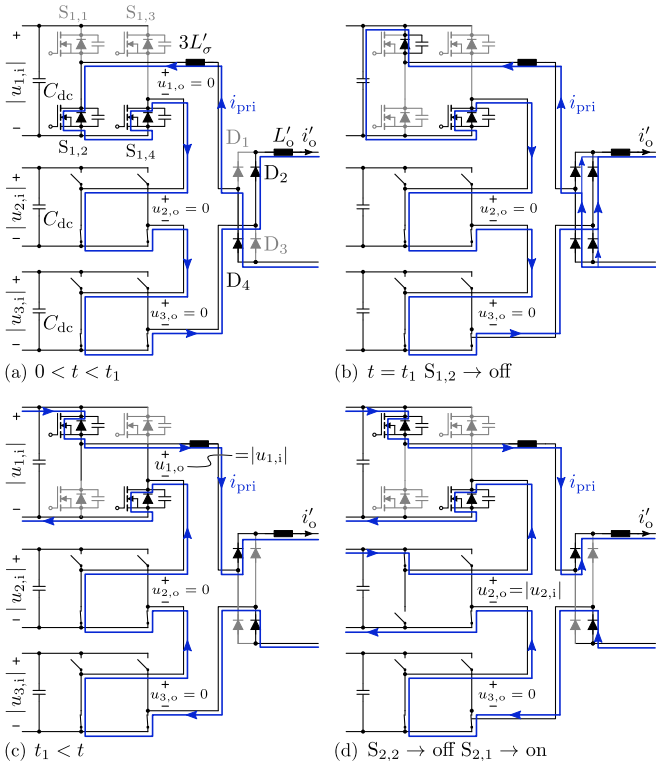

Fig. 10. Commutation of the phase modules (isolation transformers omitted for clarity) from freewheeling to active state in symmetric modulation: (a) Freewheeling at the beginning of a pulse period where $S_{k,2}$ and $S_{k,4}$ of each phase module are on. (b) $S_{1,2}$ is turned off at $t = t_1$ which start a ZVS transition in phase module 1 and forces all four output rectifier diodes to conduct. (c) Once the transformer current has reversed D_2 and D_4 turn off. (d) Phase module 2 exhibits hard switching between $S_{2,2}$ and $S_{2,1}$.

the phase modules are centered as shown in Fig. 9, forming a symmetric staircase voltage:

$$u'_{pm} = u'_{1,o} + u'_{2,o} + u'_{3,o} = \frac{n_s}{n_p}\left(u_{1,o} + u_{2,o} + u_{3,o}\right) \ . \quad (8)$$

Note that due to the phase-shift modulation of the phase modules the dc output current i_o freewheels through the phase module switches, transformer leakage inductances L_σ and the output rectifier diodes when u'_{pm} is zero, similar to a conventional phase-shift full-bridge dc-dc converter, as shown in Fig. 9 and Fig. 10 (a).

Furthermore, as the duty cycle of each phase module is proportional to the corresponding ac line voltage, the phase module connected to the highest absolute line voltage is the first one within the switching frequency cycle to switch from a freewheeling to an active state (phase a at t_1 in Fig. 9). Provided that sufficient energy is stored in the three leakage inductances L_σ, this allows zero voltage switching (ZVS) of the corresponding transistor in the phase module (module 1 in Fig. 10 (b)).

However, this first transition from freewheeling to an active state impresses a voltage on L_σ which leads to a reversal of the transformer currents i_{pri} and i_{sec} and commutates the output rectifier diodes (cf. Fig. 9 and Fig. 10 (c)). Therefore the switches in the remaining two phase modules exhibit hard switching as shown in Fig. 10 (d).

B. Asymmetric Modulation

In order to reduce the switching losses of the phase module switches the voltage pulses created by the phase modules can be aligned at the switching transition from freewheeling to active state resulting in an asymmetric, falling staircase voltage u'_{pm} as shown in Fig. 11. In this case the hard switching transitions occurring in symmetric modulation can be avoided as the half bridges in all three phase modules commutate simultaneously. Hence ZVS is achieved in all phase modules provided that sufficient energy is stored in the transformers' leakage inductances L_σ.

Detailed measurements for asymmetric modulation of a converter in Δ-configuration, taken at two different mains voltage phase angles ($\omega t \approx 0$ and $\omega t \approx 60°$) are plotted in Fig. 12. Shown are the phase module output voltage $u_{1,o}$ and the primary ($i_{1,o}$) and secondary side (i_{sec}) transformer currents. The scaling of primary and secondary side current is selected such that the turns ratio is taken into account, the difference between the currents is due to the magnetizing current of the transformer. It can be seen that in all four freewheeling ($u_{1,o} = 0$) to active voltage generation ($u_{1,o} = \pm|u_{1,i}|$) transitions, marked with dashed lines, the phase module output voltage $u_{1,o}$ has reached its final value before the primary side current $i_{1,o}$ has reversed its sign which implies that ZVS is achieved. Once $i_{1,o}$ and

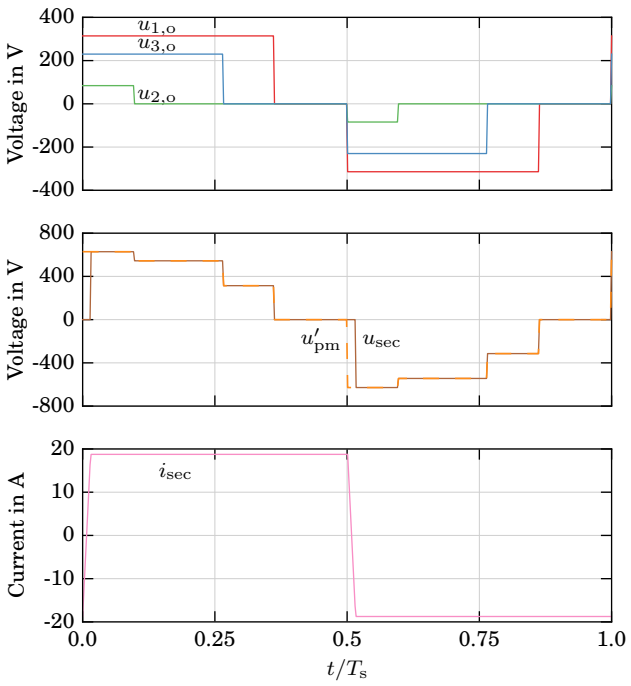

Fig. 11. Phase module output voltages $u_{a,b,c}$, secondary side voltage u_{sec} and secondary side current i_{sec} for the same operating conditions as in Fig. 9 and asymmetric modulation. By aligning the rising edges of the three voltage pulses generated by the individual phase modules ZVS can be achieved in all switching transitions, including those from freewheeling to active state at $t \approx 0$ and $t \approx 0.5T_s$.

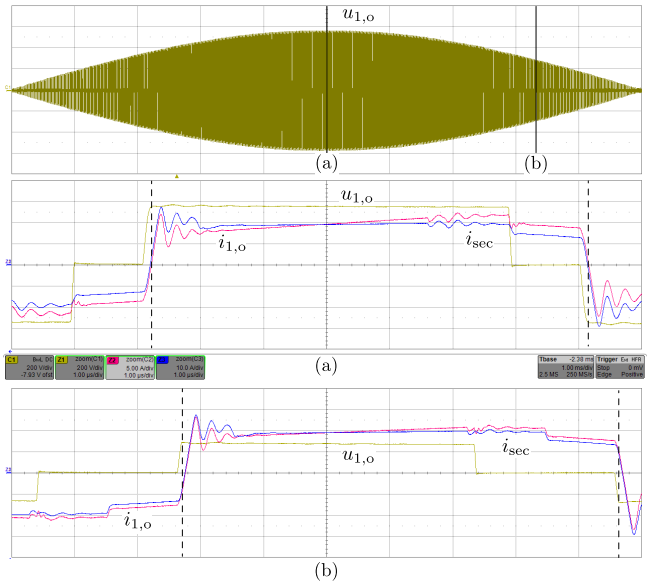

Fig. 12. Measurement results: The top plot shows the output voltage $u_{1,o}$ (200 V/div) of phase module 1 over one half cycle of the mains period (1 ms/div). In (a) a zoom (1 µs/div) at the peak of the corresponding ac voltage ($\omega t \approx 0$) is shown with $u_{1,o}$, the output current of the phase module $i_{1,o}$ (5 A/div), the secondary side transformer current i_{sec} (10 A/div). (b) shows the corresponding plot at $\omega t \approx 60°$. It can be seen that once $u_{1,o}$ has reached its final value in an freewheeling to active state transition the sign of $i_{1,o}$ has not yet changed which implies that ZVS is achieved. The corresponding instants are marked with dashed lines.

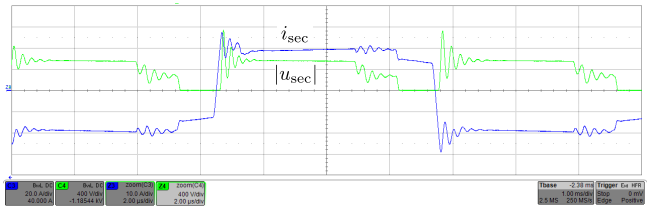

Fig. 13. Measurement results: secondary side current i_{sec} (10 A/div) and diode rectifier output voltage $|u_{sec}|$ (400 V/div) during one pulse period (2 µs/div) at $\omega t \approx 0$ and nominal operation in Δ-mode. It can be seen that the switching actions of the phase modules cause oscillations of the tank formed by L_σ and parasitic capacitances of the rectifier diodes which can also be seen in the phase module output current in Fig. 12. This leads to a peak blocking voltage of ≈ 1.1 kV on the rectifier diodes for the transition from freewheeling to active voltage generation.

i_{sec} have changed sign an oscillation occurs between the leakage inductances L_σ and the parasitic capacitances of the output rectifier diodes. This can also be seen in Fig. 13 where measurement results of i_{sec} and of the rectifier output voltage $|u_{sec}|$ are shown. In the freewheeling to active voltage generation transition a peak reverse voltage of 1.1 kV results for the rectifier diodes.

While a certain L_σ is required in order to achieve ZVS in the phase modules for a given load current a higher L_σ will change the resonance frequency and potentially lead to higher overvoltage peaks at the output rectifier diodes. If this overvoltage exceeds the diodes' rating snubber circuits are typically used which lead to an increased system complexity, higher cost and/or additional losses. Note that no snubber circuits are used in the prototype as the resulting peak voltage of 1.1 kV (cf. Fig. 13) is within the diodes' rating.

ZVS Limit: The energy required in L_σ for complete ZVS can be derived from the amount of charge necessary to charge and discharge the parasitic capacitances of the three simultaneously commutating half bridges like in phase-shift full-bridge dc-dc converters [29]. As the phase modules generally have different rectified input voltages different charges are required for each phase module:

$$\begin{aligned} Q_1(\omega t) &= Q_{oss}(|u_{1,i}(\omega t)|) \ , \\ Q_2(\omega t) &= Q_{oss}(|u_{2,i}(\omega t)|) \ , \\ Q_3(\omega t) &= Q_{oss}(|u_{3,i}(\omega t)|) \ , \end{aligned} \tag{9}$$

where $Q_{oss}(u)$ is the output capacitance charge of a single switch. This is shown in Fig. 14 where $|u_{1,i}| > |u_{3,i}| > |u_{2,i}|$ and negligible transformer magnetizing currents are assumed. Immediately after the simultaneous turn-off of switches $S_{k,4}$ the primary side transformer current i_{pri} splits between the parasitic capacitances of $S_{k,3}$ and $S_{k,4}$, cf. Fig. 14 (a). Once i_{pri} has transferred a charge equal to $2Q_2$ the body diode of $S_{2,3}$ starts to conduct as phase module 2 has the lowest absolute input voltage, cf. Fig. 14 (b). The commutation finishes when $C_{1,4}$ in phase module 1 is fully charged and $C_{1,3}$ is fully discharged, which requires $2Q_1$ to be transferred by i_{pri}. Total charges, which are transferred through the individual components during a ZVS transition, are shown in Fig. 14 (c). Assuming $C_{dc} \gg C_{oss}$ the phase module input voltages $|u_{k,i}|$ do not change significantly due

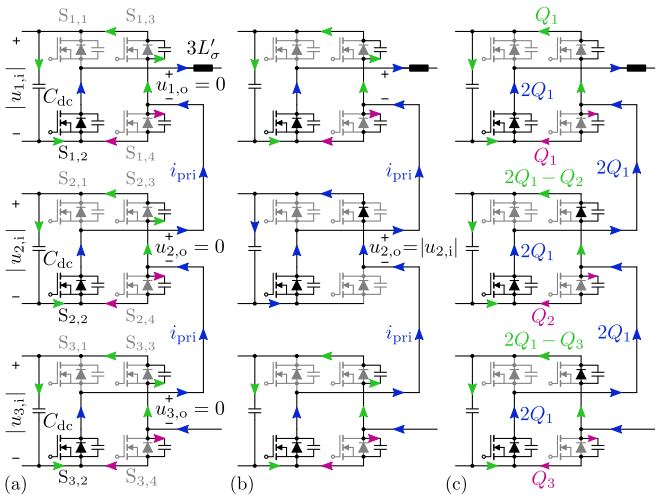

Fig. 14. Simultaneous free-wheeling to active state transition of the three phase modules in asymmetric modulation with $|u_{1,i}| > |u_{3,i}| > |u_{2,i}|$: (a) Current conduction paths immediately after the turn-off of switches $S_{k,4}$. In each phase module the transformer current i_{pri} splits between switches $S_{k,3}$ and $S_{k,4}$. (b) The switching state change of the phase module with the lowest rectified ac input voltage (module 2) is completed (capacitance of $S_{2,4}$ is charged, capacitance of $S_{2,3}$ is discharged) and i_{pri} continues through $S_{2,3}$'s body diode. (c) Charge Transfer in connection with the switching state change of all phase modules from freewheeling to voltage generation.

to the additional charge and the energy E_z transferred from L_σ into the capacitors C_{dc} follows from Fig. 14 (c) as

$$E_z = \underbrace{|u_{1,i}|\,Q_1}_{\text{Ph. Mod. 1}} + \underbrace{|u_{2,i}|\,(2\,Q_1 - Q_2)}_{\text{Phase Module 2}} + \underbrace{|u_{3,i}|\,(2\,Q_1 - Q_3)}_{\text{Phase Module 3}} \quad . \tag{10}$$

In order to achieve ZVS the energy stored in the leakage inductances L_σ before the turn-off of $S_{k,4}$ has to fulfill

$$E_{L_\sigma} = \frac{1}{2}\,3\,L_\sigma\,i_{sec}^2 \geq E_z \quad . \tag{11}$$

Note that in a real converter system the value of i_{sec} at the turn-off of $S_{k,4}$ depends on several factors and parasitic effects such as:

- dc load current,
- output current i_o ripple,
- transformer magnetizing currents,
- parasitic capacitances (e.g. transformer windings and PCB),
- conduction losses during free wheeling and
- mains voltage amplitude, unbalance and distortion.

A precise calculation at which dc output current incomplete ZVS will occur would require a comprehensive analysis of these system parameters and is out of the scope of this paper.

IV. Delta Configuration

The modulation scheme described in Section II-A assumes a Y-configuration of the phase modules, resulting in a maximum ac mains current amplitude $\hat{I}_{max,Y}$ and a maximum input power of $P_{max,Y}$

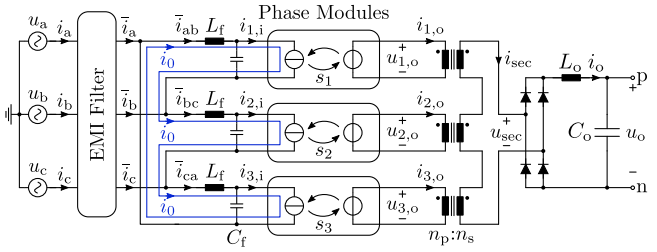

Fig. 15. Schematic of the rectifier in Δ-configuration where the phase modules are replaced by controlled current and voltage sources. In Δ-configuration a zero-sequence current i_0 can be used to operate the converter in overmodulation ($m \leq 2/\sqrt{3}$) which increases the maximum dc output voltage by ≈ 15 %.

$$\hat{I}_{max,Y} = I_o\,\frac{n_s}{n_p} \quad , \tag{12}$$

$$P_{max,Y} = \frac{3}{2}\,\hat{U}\,\hat{I} = \frac{3}{2}\,\hat{U}\,\frac{n_s}{n_p}\,I_o \quad . \tag{13}$$

Neglecting any losses in the converter the maximum output voltage in Y-mode follows:

$$U_{o,max,Y} = \frac{3}{2}\,\hat{U}\,\frac{n_s}{n_p} \quad . \tag{14}$$

The same modulation scheme can also be applied in Δ-configuration in which case the input and output voltages of the phase modules and therefore the voltage stress of the semiconductors increase by a factor $\sqrt{3}$ compared to Y-mode. If the same output voltage has to be created the transformer turns ratio can be adapted accordingly which reduces the currents in the phase modules' inverter switches by a factor $1/\sqrt{3}$.

A. 3rd Harmonic Current Injection

It can be seen in Fig. 15 that the ac inputs of the three phase modules form a closed loop in Δ-mode, which allows a zero sequence current

$$i_0 = \frac{1}{3}\,(\bar{i}_{ab} + \bar{i}_{bc} + \bar{i}_{ca}) \approx \frac{1}{3}\,\langle i_{1,i} + i_{2,i} + i_{3,i}\rangle_{T_s} \tag{15}$$

to circulate through the phase modules without appearing in the rectifier's mains input currents $i_{a,b,c}$ [30]. Note that i_0 can be controlled using the zero sequence modulation index m_0 (cf. Fig. 6) as no converter internal star point Y exists in Δ-configuration and hence no star point potential controller is required. As i_0 circulates between the phase modules but not through the mains voltage sources it does not impact the active power exchange with the mains. However the input rectifiers of the phase modules require that their input currents $i_{k,i}$ have the same sign as the corresponding phase module input voltages $u_{k,i}$, which implies $i_0 = 0$ at every zero crossing of a line-to-line mains voltage. Using 3rd harmonic current injection (3rd HCI), for example as

$$m_0 = \frac{m}{6}\,\sin(3\,\omega t) \quad , \tag{16}$$

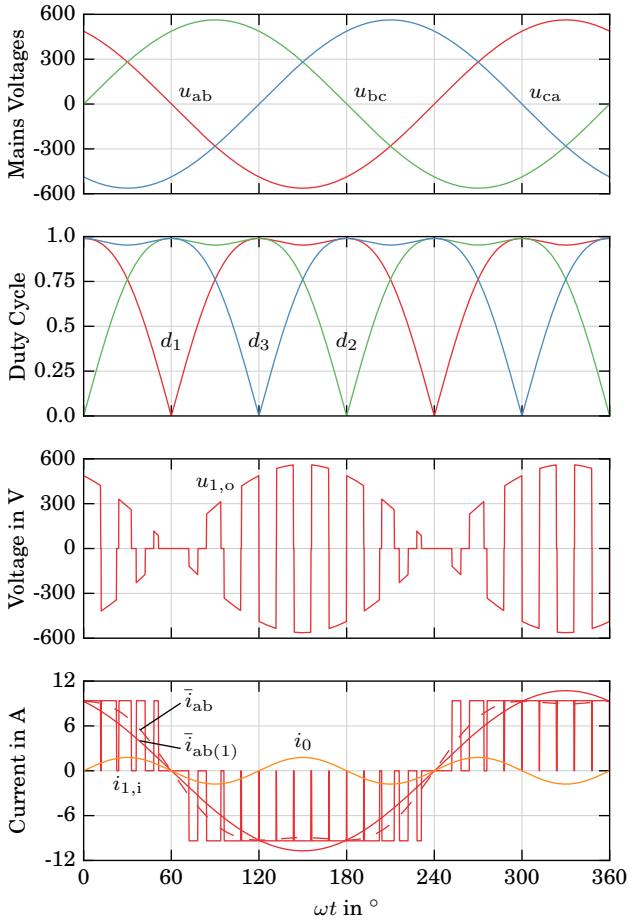

Fig. 16. Drawing of the modulation scheme using 3rd harmonic injection with reduced f_s at maximum modulation index $m = 2/\sqrt{3}$: within each pulse interval each phase module produces a square-shaped high-frequency transformer voltage $u_{k,o}$ k $\in \{1,2,3\}$ with a duty cycle d_k. Neglecting C_{dc}, the discontinuous phase module input current $i_{k,i}$ results and after low pass filtering by C_f and L_f input currents $\bar{i}_{ab}$, $\bar{i}_{bc}$ and $\bar{i}_{ca}$ proportional to d_k results. It can be seen that the mains frequency fundamental $\bar{i}_{ab(1)}$ of $\bar{i}_{ab}$ exceeds the peak value of $i_{1,i}$.

a modulation index m up to $2/\sqrt{3} \approx 1.15$ can be selected with all phase module duty cycles $d_{1,2,3} \leq 1$ [31]. A drawing of the resulting waveforms is shown in Fig. 16, showing the phase module input current $i_{1,i}$ and its low-pass filtered version $\bar{i}_{ab}$ with a fundamental $\bar{i}_{ab(1)}$ which is a factor $2/\sqrt{3}$ higher than the transformed output current $I'_o = n_s/n_p\ I_o$. The maximum mains input current, power and hence output voltage using 3rd HCI can therefore be calculated as:

$$\hat{I}_{max,\Delta} = I_o \frac{n_s}{n_p} \frac{2}{\sqrt{3}} \sqrt{3}\,, \tag{17}$$

$$P_{max,\Delta} = \frac{\sqrt{3}}{2} \sqrt{3}\,\hat{U}\,\hat{I}_{max,\Delta} = 3\,\hat{U}\,I_o \frac{n_s}{n_p}\,, \tag{18}$$

$$U_{o,max,\Delta} = 3\,\hat{U} \frac{n_s}{n_p}\,. \tag{19}$$

This increase in output voltage range typically allows a reduced turns ratio n_s/n_p which in turn reduces the current stresses (cf. Appendix A) and hence the conduction losses of the phase module switches. Measurement results with 3rd HCI are shown in Fig. 17. It can be seen that a sinusoidal mains input current i_a results even though the individual phase module input currents $\bar{i}_{ab}$ and $\bar{i}_{bc}$ contain a third harmonic.

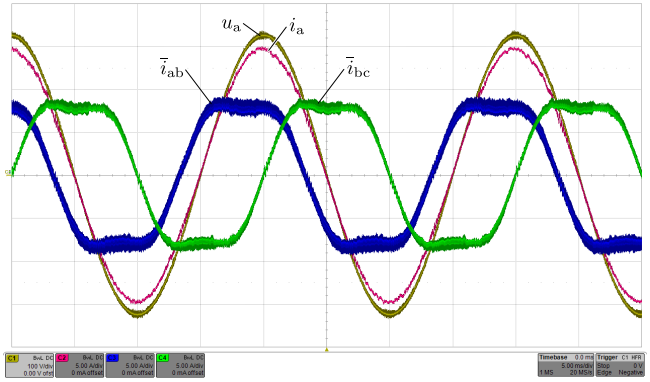

Fig. 17. Measurement results (5 ms/div) obtained from a prototype converter in Δ-configuration using 3rd HCI operated with $m \approx 1$. The low-pass filtered phase module input currents i_{ab} and i_{bc} (5 A/div) are non-sinusoidal due to the 3rd harmonic current, while the converter's mains input current i_a (5 A/div) is free of low-frequency distortions and in phase with the corresponding voltage u_a (100 V/div).

TABLE II
INPUT CURRENT SPACE VECTORS IN Δ-MODE FOR SECTORS 1 & 2

$(s_1\ s_2\ s_3)$	$\bar{i}_a/I'_o$	$\bar{i}_b/I'_o$	$\bar{i}_c/I'_o$	i_0/I'_o	$\vec{i}_i/I'_o$
(000)	0	0	0	0	0
(100)	1	−1	0	1/3	$1 - j/\sqrt{3}$
(010)	0	1	−1	1/3	$j\,2/\sqrt{3}$
(001)	−1	0	1	−1/3	$1 + j/\sqrt{3}$
(110)	−1	0	1	2/3	$1 + j/\sqrt{3}$
(101)	2	−1	−1	0	2
(011)	1	1	−2	0	$1 + j\sqrt{3}$
(111)	2	0	−2	0	$2 + j\,2/\sqrt{3}$

B. Δ Mode Modulation Boundaries

In order to analyze the IMD rectifiers modulation boundary and reactive power generation capabilities its input current space vector diagram is derived in the following. As the indirect matrix-type phase modules use an input diode rectifier, the input current $i_{k,i}$ $k \in \{1,2,3\}$ of each phase module can only have the same sign as the corresponding phase module input voltage $u_{k,i}$ which is defined by the ac mains voltage. Furthermore, whenever the phase module's inverter switches apply a non-zero voltage $u_{k,o}$ to its transformer the transformer's primary current $i_{k,o} \approx I'_o$ is drawn from the phase module input. This can be described as

$$i_{k,i} = \text{sign}(u_{k,i})\, I'_o\, s_k \quad s_k \in \{0,1\}\,,\ k \in \{1,2,3\}\,, \tag{20}$$

where s_k is one if phase module k is in an active state, i.e. applying voltage to its transformer ($u_{k,o} \neq 0$), and zero if it is in free wheeling state ($u_{k,o} = 0$).

This allows to calculate the IMD rectifier's input current space vectors $\vec{i}_i$ using

$$\vec{i}_i = \frac{2}{3}\left(\bar{i}_a + \bar{i}_b\, e^{j2\pi/3} + \bar{i}_c\, e^{-j2\pi/3}\right)\,. \tag{21}$$

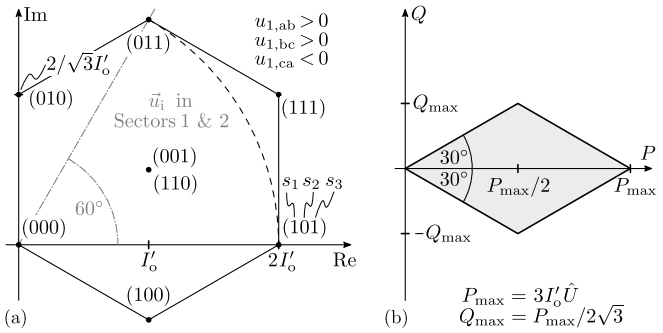

Fig. 18. (a) Space vector diagram of the rectifier's input current $\vec{i}_i$ for a mains voltage in sectors 1 or 2, i.e. $u_{1,ab} > 0$, $u_{1,bc} > 0$, $u_{1,ca} < 0$, assuming a constant dc output current $I'_o = I_o\, n_s/n_p$, and a Δ-connection of the phase modules. It can be seen from geometric identities that the maximal input current space vector amplitude in this case is given by $|\vec{i}_i| = 2\, I'_o$. The resulting active and reactive power generation limits of the rectifier are shown in (b).

TABLE III
SELECTED COMPONENTS

Input Rectifier	1200 V, 45 A Si Rectifier, DSP45-12A
Inverter	1200 V, 60 A, 25 mΩ SiC MOSFET, C2M0025120D
Output Rectifier	1200 V, 54 A SiC Schottky Rectifier, C4D40120D
Transformer	Stack of 2 E55 N96 cores, $n_p : n_s = 14 : 7$
	1260 Strands / 2205 Strands, 71 µm litz wire
	$L_\sigma = 1.25$ µH, $L_m = 200$ µH w.r.t. secondary side
Output Inductor	2 x 200 µH, 2 stacked E55 N87 cores each
	14 turns 2 mm solid copper wire
PM Filter	$L_f = 16$ µH, C058206, 11 turns, 2 in series
(Stage 1)	$C_f = 1.65$ µF, 2 x 3.3 µF 300 V_{rms} X2 in series
	$C_{dc} = 0.4$ µF, 4 x 100 nF 1000 V MLCC parallel
EMI Filter	$L_{cm} \approx 800$ µH W422-05, 3 x 10 turns, 2 mm wire
(Stage 2)	$C_{cm} = 4.7$ nF 300 V_{rms} X2 in Y connection
	$L_{dm} = 70$ µH C058083A2, 30 turns, 2 mm wire
	$C_{dm} = 470$ nF 300 V_{rms} X2 in Y connection
	$L_{damp} = 9$ µH C058059A2, 15 turns, 2 mm wire
	$R_{damp} = 1\,\Omega$

The results for an ac mains voltage vector $\vec{u}_i$ in sectors 1 or 2 ($u_{ab} > 0$, $u_{bc} > 0$, $u_{ca} < 0$) are listed in Table II and shown in Fig. 18 (a). It can be seen from the current space vector diagram that an input current vector $\vec{i}_i$ with an amplitude up to $2\, n_s/n_p\, I_o$ can be created which is in accordance with (17). Furthermore $\vec{i}_i$ can lead or lag the mains voltage $\vec{u}_i$ which implies that the IMD rectifier can be used to create reactive power at the ac input. The input current can be phase shifted up to $\pm 30°$ with respect to the mains voltage, but only for a modulation index $m < 1/\sqrt{3}$. For a higher modulation index the resulting phase shift angle, and therefore the reactive power which can be generated, reduces as shown in Fig. 18 (b). For the maximum modulation index $m = 2/\sqrt{3} \approx 1.15$ no reactive power can be generated. Note that the IMD Rectifier's input current space vector diagram is analog to the VIENNA Rectifier's input voltage space vector diagram which implies that both rectifiers have corresponding limitations on overmodulation and reactive power generation [32].

V. PROTOTYPE RECTIFIER DETAILS

All measurement results presented in this paper were taken on a 7.5 kW prototype rectifier built according to the specification given in Table I, the main components used in the prototype are listed in Table III. Pictures of the implemented prototype rectifier are shown in Fig. 19 and a brief description of the main design trade-offs follows.

A. System Design

The first decision in the design of an IMY/D rectifier is whether it should be operated in Y- or Δ-configuration or both. As given in Appendix A the voltage stress of the phase module semiconductors is higher in Δ-configuration by a factor of $\sqrt{3}$. For example, in Y-configuration semiconductors with a blocking voltage rating of 650 V, such as Si MOSFETs or GaN HEMTs can used in a rectifier operating from a 400 V rms to 480 V rms mains as the blocking voltage of the phase modules' semiconductor devices is defined by the mains' line-to-neutral voltage. In Δ-configuration the maximum blocking voltages increases by a factor of $\sqrt{3}$ and 1.2 kV devices such as SiC MOSFETs or Si IGBTs have to be used, but the maximum output voltage of the phase modules increases accordingly. If the same dc output voltage has to be created a higher turns ratio $n_p : n_s$ can be used which reduces the current stresses on the phase modules' semiconductors, as can be seen from the formulas given in Appendix A. For rectifiers which have to operate with a wide range of mains voltages, for example 150 V-460 V line-to-line voltage, both modes can be utilized, where the system is operated in Y-configuration for a low input voltage and in Δ-configuration for a high one.

As the IMY/D rectifier is a buck-type system its maximum output voltage is limited by the mains voltage and hence the transformer turns ratio $n_p : n_s$ has to be selected based on the lowest ac input voltage and the highest dc output voltage at which the rectifier has to be operated using either equation (14) or (19) according to the selected operating mode. Note that selecting a larger $n_p : n_s$ results in a lower maximum output voltage and hence a less margin for losses, mains undervoltages, etc., while at the same time reducing the conduction losses in the phase module switches. The implemented prototype uses 1.2 kV SiC MOSFETs due to their low conduction and switching losses and because they allow operation in both Y- and Δ-configuration from a 400 V rms mains. The converter is designed for Δ-configuration with a transformer turns ratio of $n_p : n_s = 2$ which results in a 22 % output voltage margin for ac input undervoltages, losses, unbalances etc.

As shown in Fig. 20 the rectifier's EMI filter stages can either be implemented as individual single-phase filters per phase module (stage 1 in Fig. 20) or as phase-integrated filter stages at the three-phase mains input (stage 2). While single-phase filter stages allow a higher degree of modularity and potentially higher flexibility in wide input voltage range designs which are operated in either Y- or Δ-configuration, integrated three-phase filters are expected to be beneficial in terms of component volume, losses and/or cost as they require only a single common mode choke per stage compared to one per phase module in phase-modular filters. However,

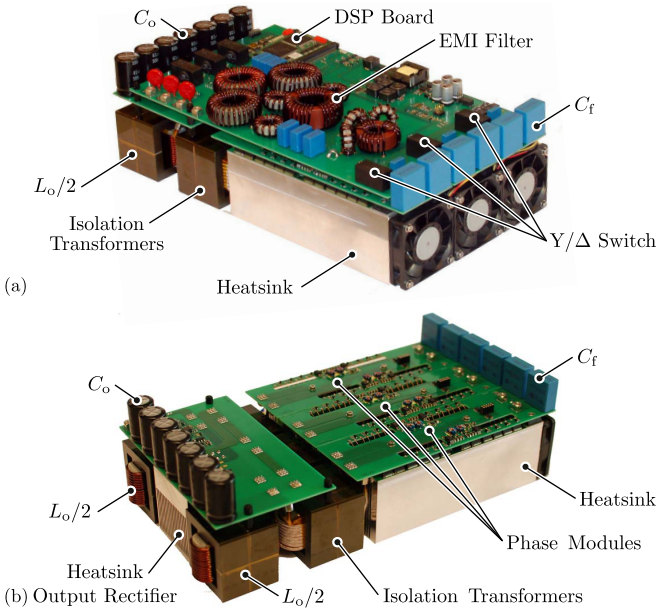

Fig. 19. Realized 7.5 kW IMY/D rectifier prototype. (a) fully assembled and (b) with the top PCB removed in order to show the phase modules and the output rectifier board.

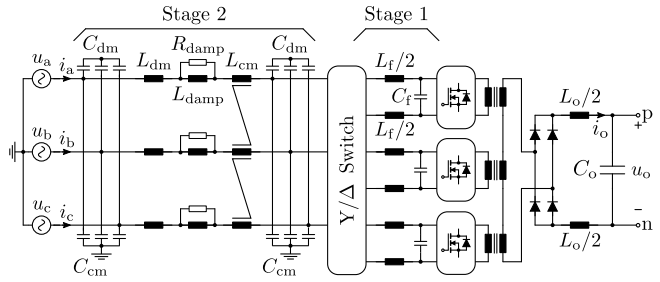

Fig. 20. Schematic of the EMI input filter implemented in the IMY/D rectifier prototype. Note that either separate single-phase filter stages for each phase module (as in stage 1 shown here), or phase-integrated three-phase filter stages (as in stage 2) can be used.

a detailed analysis of these EMI filter topologies is out of the scope of this paper.

B. Performance

The measured efficiency for asymmetric and symmetric modulation and with and without 3rd HCI is plotted in Fig. 21. As expected from the considerations above the efficiency is higher for asymmetric modulation as all phase modules achieve ZVS. At rated output power the efficiency increases from 96.9 % with symmetric modulation (without 3rd HCI) to 97.2 % with asymmetric modulation which corresponds to a reduction of the losses by 22 W. Towards light load the efficiency curves converge as even with asymmetric modulation ZVS cannot be achieved because the load current does not store sufficient energy in the leakage inductances L_σ to fully recharge all parasitic capacitors resulting in incomplete ZVS.

As the same transformer was used for operation with and without 3rd HCI basically the same efficiency results for both cases. However, without 3rd HCI the prototype has to be

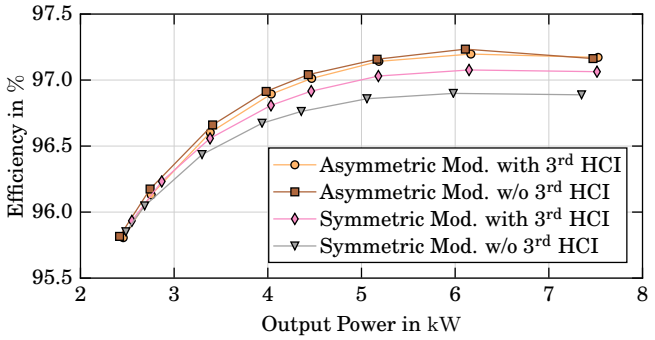

Fig. 21. Measured converter efficiencies in Δ-configuration as a function of output power for asymmetric (ZVS) and symmetric (hard switching) modulation and with and without 3rd HCI at nominal input and output voltages. The measurements were taken using a *Yokogawa WT3000* power analyzer.

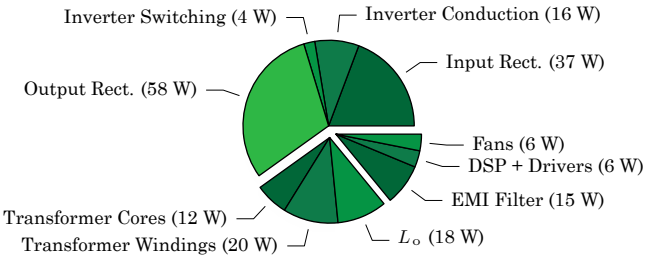

Fig. 22. Calculated component losses for nominal operation of the prototype converter in Δ-configuration with 3rd HCI and asymmetric modulation.

operated very close to the modulation limit $m \approx 1$ which would not be feasible in an application. In order to obtain the same output voltage margin as with 3rd HCI the turns ratio $n_p : n_s$ has to be reduced to $\sqrt{3}/2 \approx 87\,\%$. While this does not change the winding losses in the transformers it increases the current in the inverter switches $S_{k,1..4}$ by 15 %, leading to ≈ 33 % higher conduction losses. Note that for symmetric modulation the efficiency increases with 3rd HCI due to the changed shape of the duty cycle signal.

In Fig. 22 the calculated component losses for nominal operation in Δ-configuration with 3rd HCI are shown. About 30 % of the total losses occur in the SiC Schottky diodes of the output rectifier, while the input rectifiers and inverters account for another ≈ 30 %. The remaining losses are due the passive components, DSP, gate drivers, fans, etc. With outer dimension of 35.5 cm x 18 cm x 10.5 cm a total volume of 7.28 dm^3 and power density of 1.03 kW dm^{-3} results for the prototype rectifier. However, ≈ 60 % of this volume is occupied by heatsinks which were reused from a previous prototype based on Si MOSFET devices in an oring-configuration with considerably higher losses than the SiC MOSFETs used in this paper [26]. It is estimated that a power density of ≈ 1.4 kW dm^{-3}, or more, could be achieved with an optimized custom heatsink.

The measured total harmonic distortion values of the ac input currents are plotted in Fig. 23. It can be seen that the prototype achieves ≤ 2 % of THD for half load and higher.

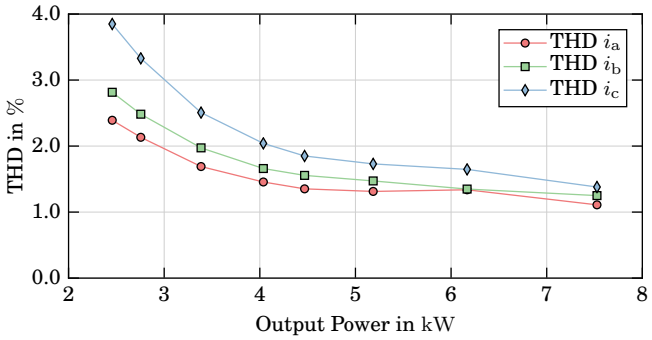

Fig. 23. Measurement results: Total harmonic distortion of the IMD rectifier's input currents as a function of dc output power for operation in Δ-configuration with purely sinusoidal mains voltages. The measurements were taken using a *Yokogawa WT3000* power analyzer.

VI. Conclusion

This paper analyzes the three-phase phase-modular isolated indirect matrix-type Y/Δ PFC rectifier (IMY/D rectifier) which consists of three individual isolated phase modules that can be connected in a star (Y) or delta (Δ) configuration. Using both configurations allows a wide input voltage range and/or to adapt the voltage and current stresses of the semiconductors to the available device technologies.

Basic and advanced modulation schemes for operation in Y- or Δ-configuration are described which enable operation with zero voltage switching of the phase modules' inverter switches, resulting in a $10\,\%$ reduction of the overall losses in a $7.5\,\mathrm{kW}$ SiC MOSFET based prototype rectifier. The modulation limits for Y- and Δ-mode are described and a thrid harmonic current injection principle (3^{rd} HCI) is proposed which allows up to $\approx 15\,\%$ higher dc output voltage and/or reduced conduction losses of the inverter switches. The prototype system achieves an efficiency of $97.2\,\%$ at full load using the proposed ZVS modulation and 3^{rd} HCI with an mains input current total harmonic distortion of less than $2\,\%$.

Acknowledgment

The authors would like to thank Ms. Shannon Long for her help in the design, assembling and commissioning of the hardware prototype.

Appendix
Semiconductor Stresses

In this appendix the voltage and current stresses of the IMY/D converters semiconductors are summarized in Table IV and Table V.

The maximum reverse voltage applied to the input rectifier diodes and inverter switches of the phase modules depends only on the ac input voltage's amplitude $\hat{U}$. In Δ-configuration the voltage applied to a single phase module, and therefore the voltage stress of the devices, increases by a factor of $\sqrt{3}$. Similarly the voltage applied to the output side diode rectifier depends on the input voltage and the transformer turns ratio. However, oscillations between the parasitic capacitances of the diodes and the transformers' stray inductances will create a transient overvoltage, as can be seen in Fig. 13.

TABLE IV
Semiconductor Voltage Stresses

	Y-Mode	Δ-Mode
Input Rectifier	$U_{\max} = \hat{U}$	$U_{\max} = \hat{U}\sqrt{3}$
Inverter	$U_{\max} = \hat{U}$	$U_{\max} = \hat{U}\sqrt{3}$
Output Rectifier	$U_{\max} = \hat{U}\frac{n_\mathrm{s}}{n_\mathrm{p}}2$	$U_{\max} = \hat{U}\frac{n_\mathrm{s}}{n_\mathrm{p}}2\sqrt{3}$

TABLE V
Semiconductor Current Stresses

	$m_0 = 0$	$m_0 = \frac{m}{6}\sin(3\omega t)$
Input Rectifier	$I_{\mathrm{rms}} = I_\mathrm{o}\frac{n_\mathrm{s}}{n_\mathrm{p}}\sqrt{\frac{m}{\pi}}$ $I_{\mathrm{avg}} = I_\mathrm{o}\frac{n_\mathrm{s}}{n_\mathrm{p}}\frac{m}{\pi}$	$I_{\mathrm{rms}} = I_\mathrm{o}\frac{n_\mathrm{s}}{n_\mathrm{p}}\sqrt{\frac{m}{\pi}\frac{19}{18}}$ $I_{\mathrm{avg}} = I_\mathrm{o}\frac{n_\mathrm{s}}{n_\mathrm{p}}\frac{m}{\pi}\frac{19}{18}$
Inverter	$I_{\mathrm{rms}} = I_\mathrm{o}\frac{n_\mathrm{s}}{n_\mathrm{p}}\frac{1}{\sqrt{2}}$ $I_{\mathrm{avg}} = I_\mathrm{o}\frac{n_\mathrm{s}}{n_\mathrm{p}}\frac{1}{2}$	
Output Rectifier	$I_{\mathrm{rms}} = I_\mathrm{o}\frac{1}{\sqrt{2}}$ $I_{\mathrm{avg}} = I_\mathrm{o}\frac{1}{2}$	

Note that the current stresses of all semiconductors are equal for Y and Δ mode as only the phase modules' input voltages change between the modes. However, if the same output and input voltages are considered in both cases a lower transformer turns ratio $n_\mathrm{s}/n_\mathrm{p}$ can be used in Δ-configuration compared to Y-configuration which reduces the current stresses of the input rectifier diodes and inverter switches.

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