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Novel Modulation Concept of the SWISS Rectifier Preventing Input Current Distortions at Sector Boundaries

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***Abstract*—This paper describes a new modulation concept for the uni- and bidirectional SWISS rectifier which mitigates input current distortions at the gird voltage sector boundaries. An analytical model is derived and compared to simulations, showing that these distortions are increasing the input current THD significantly. Furthermore, an algorithm is presented which allows the calculation of a temporary pulse width modulation for the SWISS Rectifier's active 3rd harmonic current injection network which mitigates the distortions. Simulations show that the AC input currents' THD can be reduced from 4.2 % to 0.8 % on a prototype system. The concept is verified by measurement results taken on a bidirectional 7.5 kW SWISS Rectifier prototype.**

I. Introduction

The increasing power consumption of data centers and telecommunication equipment has led to a demand for more efficient power supply systems. As data center equipment is an intrinsic DC load, DC distribution systems are expected to provide significant gains in efficiency as rectifier stages of the power supply modules can be omitted. Furthermore, a direct battery buffering of the DC bus voltage allows to omit a dedicated UPS system, which increases efficiency further, improves reliability and reduces capital cost and floor space [1][2]. Accordingly, standards for 380 V DC distribution systems have been created recently [3]. Additionally, similar benefits are expected from DC distribution systems e.g. in office builds and industry [4].

As the DC bus voltage of 380 V is lower than the full-wave rectified voltage of the 400 V AC grid, two-stage systems are normally used. These consist of a power factor correction stage (PFC) connected in series with a DC-DC converter. This is typically also the case for fast chargers of Electric Vehicle batteries which are powered from the three-phase mains [6][7]. In these applications buck-type PFC converters, like the SWISS Rectifier, are an advantageous alternative, allowing a single-stage conversion between the three-phase mains and a DC bus with lower voltage.

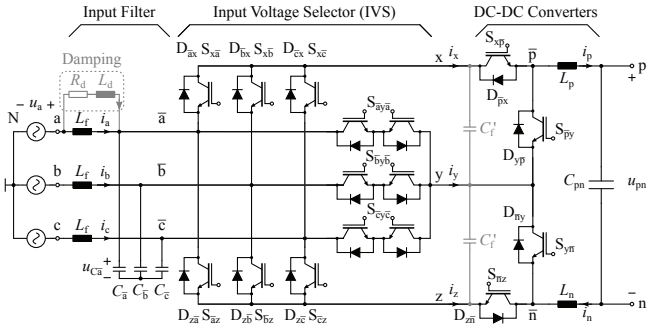

Fig. 1. Schematic of the bidirectional SWISS Rectifier with AC side EMI filter capacitors as introduced in [5]. The input filter damping structures (L_d, R_d) are not shown for phases b and c for clarity.

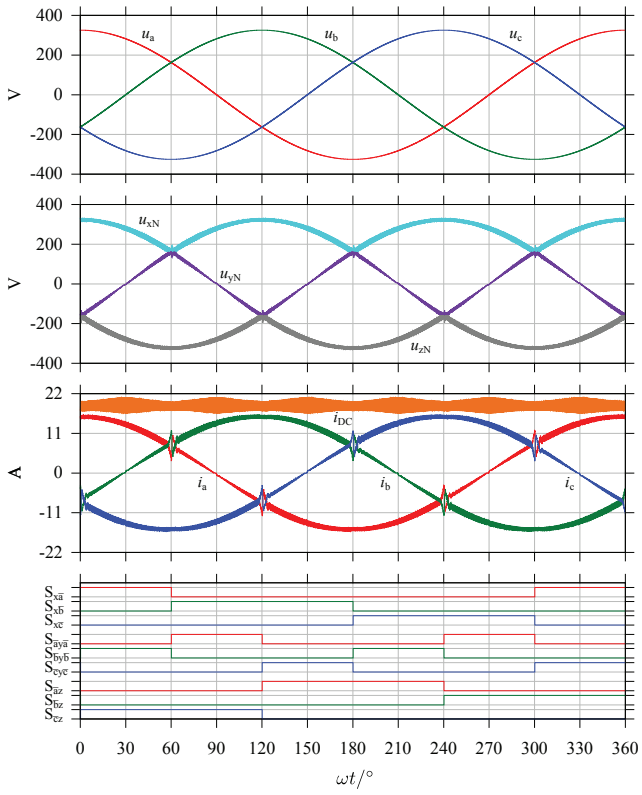

Fig. 2. Simulation results for the SWISS Rectifier specified in **Table I**, in AC-to-DC operation at nominal power. u_xN, u_yN and u_zN are the DC side voltages of the IVS with reference to the AC grid's neutral N. The distortions of the AC input currents $i_\mathrm{a,b,c}$ at intersections of the phase voltages $u_\mathrm{a,b,c}$ are visible. A low frequency (< 10 kHz) input current THD of 4.2 % results.

The schematic of the conventional bidirectional SWISS Rectifier, as introduced in [5] and [8], is shown in **Fig. 1**. It consists of an AC side input filter, an Input Voltage Selector (IVS), two DC-DC converters ($\mathrm{S_{x\bar{p}}}$, $\mathrm{S_{\bar{p}y}}$, L_p and $\mathrm{S_{y\bar{n}}}$, $\mathrm{S_{z\bar{n}}}$, L_n) and a DC output capacitor C_pn. Additional capacitors C'_f are used to shorten the commutation paths of the two DC-DC converters. The IVS consists of a three-phase full-wave diode bridge with anti-parallel switches and a third harmonic injection network. Its switches are controlled such that the input phase with highest potential is connected to node x, the one with lowest potential to node z and the remaining phase to node y. Therefore, the injection network's switches $\mathrm{S_{\bar{a}y\bar{a}}}$, $\mathrm{S_{\bar{b}y\bar{b}}}$ and $\mathrm{S_{\bar{c}y\bar{c}}}$ operate with twice the mains frequency, while the

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TABLE I
SPECIFICATIONS OF SIMULATED SWISS RECTIFIER

AC Input Voltage (Line to Neutral)	$U_1 = 230\,\mathrm{V_{rms}}$
AC Input Frequency	$f = 50\,\mathrm{Hz}$
Switching Frequency	$f_\mathrm{s} = 36\,\mathrm{kHz}$
Nominal DC Voltage	$U_\mathrm{pn} = 400\,\mathrm{V}$
DC Link Capacitance	$C_\mathrm{pn} = 470\,\mu\mathrm{F}$
DC Link Inductance	$L_\mathrm{p,n} = 250\,\mu\mathrm{H}$
DC Output Power	$P = 7.5\,\mathrm{kW}$
AC Filter Capacitance	$C_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}} = 4.4\,\mu\mathrm{F}$
DC Filter Capacitance	$C_{\mathrm{x,y,z}} = 4.4\,\mu\mathrm{F}$
AC Filter Inductance	$L_\mathrm{f} = 120\,\mu\mathrm{H}$
AC Filter Damping	$L_\mathrm{d} = 120\,\mu\mathrm{H}$
AC Filter Damping	$R_\mathrm{d} = 6.8\,\Omega$

rectifier switches $\mathrm{S_{x\bar{a}}}$, $\mathrm{S_{x\bar{b}}}$, $\mathrm{S_{x\bar{c}}}$, $\mathrm{S_{\bar{a}z}}$, $\mathrm{S_{\bar{b}z}}$ and $\mathrm{S_{\bar{c}z}}$ are operated with mains frequency. This can be seen in **Fig. 2** where the grid voltages and the IVS output voltages u_xN, u_yN and u_zN are shown.

As described in [5] the two DC-DC converters of the SWISS Rectifier can ideally be controlled in such a way that sinusoidal AC side input currents i_a, i_b and i_c result. **Fig. 2** shows simulation results for the bidirectional 7.5 kW SWISS Rectifier specified in **Table I**. While the rectifier's input currents are sinusoidal and in phase with the grid voltages, it can be seen that they are distorted at the intersections of the AC mains phase voltages u_a, u_b and u_c.

These distortions are caused by the switching frequency voltage ripple across the input filter capacitors $C_{\bar{\mathrm{a}},\bar{\mathrm{b}},\bar{\mathrm{c}}}$ [9]. This can be seen in **Fig. 3** which shows detailed simulation results for the intersection interval of the phase voltages u_a and u_b. Additionally the voltages $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ across the respective input filter capacitors and their local averages $\langle u_{\mathrm{C}\bar{\mathrm{a}}}\rangle_{T_\mathrm{s}}$, $\langle u_{\mathrm{C}\bar{\mathrm{b}}}\rangle_{T_\mathrm{s}}$ over one switching period T_s are shown. Neglecting the voltage drop due to the fundamental of the phase current i_a across L_f, the local average $\langle u_{\mathrm{C}\bar{\mathrm{a}}}\rangle_{T_\mathrm{s}}$ equals the corresponding phase voltage u_a before the current distortion starts. The same holds for $\langle u_{\mathrm{C}\bar{\mathrm{b}}}\rangle_{T_\mathrm{s}}$ and u_b. As the voltages u_a and u_b approach each other, the instantaneous voltages $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ would have to intersect for this to hold true. However, this is not the case as shown in **Fig. 3**, because the diodes $\mathrm{D_{\bar{a}x}}$ and $\mathrm{D_{\bar{b}x}}$ are starting to conduct once $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}} = u_{\mathrm{C}\bar{\mathrm{a}}} - u_{\mathrm{C}\bar{\mathrm{b}}}$ reaches zero (cf. **Fig. 4**). Therefore the local averages $\langle u_{\mathrm{C}\bar{\mathrm{a}}}\rangle_{T_\mathrm{s}}$ and $\langle u_{\mathrm{C}\bar{\mathrm{b}}}\rangle_{T_\mathrm{s}}$ no longer matches the corresponding phase voltages u_a and u_b. This impresses a voltage on the input filter inductors L_f, which leads to a distortion of the input currents i_a and i_b, as shown in **Fig. 3**.

Therefore, in the following a modified circuit topology which reduces the conduction losses in the IVS and decouples the switching operation of the DC-DC converters and the IVS is proposed. For this circuit, an analysis of the current distortion's impact on the converter's THD is given in **Chapter III**. Subsequently, a novel modulation concept, which mitigates the current distortions by temporary pulse width modulation of the IVS switches is introduced in **Chapter IV**. In **Chapter V** measurement results, taken on a 7.5 kW prototype SWISS Rectifier, are presented which verify the theoretical considerations.

II. DC Side Filter Capacitors

As written above, an implementation of the SWISS Rectifier typically requires additional filter capacitors C_f' in order to shorten the commutation paths of the two DC-DC converters

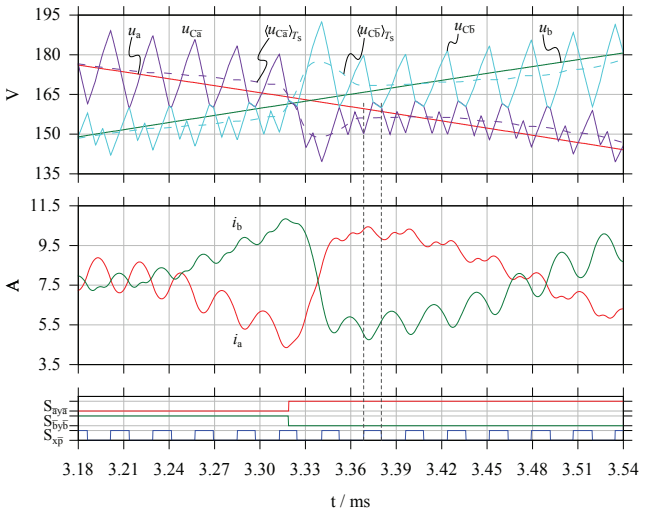

Fig. 3. Detailed simulation results for the first intersection at $\omega t = 30°$ showing the intersecting grid phase voltages u_a and u_b and the corresponding filter capacitor voltages $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$. $\langle u_{\mathrm{C}\bar{\mathrm{a}}}\rangle_{T_\mathrm{s}}$ is the average of $u_{\mathrm{C}\bar{\mathrm{a}}}$ over one switching frequency period T_s. It can be seen that no intersection of $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ occurs because of $\mathrm{D_{\bar{a}x}}$ and $\mathrm{D_{\bar{b}x}}$ (cf. **Fig. 4**).

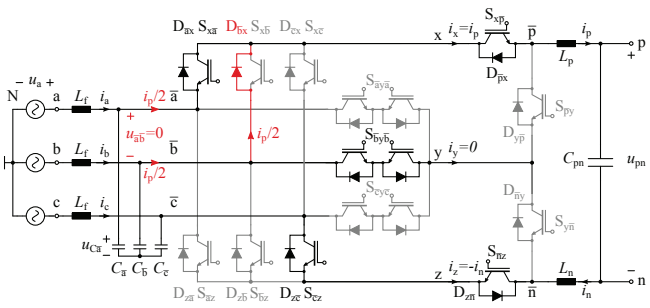

Fig. 4. Schematic of the SWISS Rectifier with $\mathrm{S_{x\bar{p}}}$ turned on, showing the additional conduction path caused by the diode $\mathrm{D_{\bar{b}x}}$ when the voltage $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}}$, i.e. the difference of the voltages of the filter capacitors $C_{\bar{\mathrm{a}}}$ and $C_{\bar{\mathrm{b}}}$ reaches zero. This implies $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}} \geq 0$ which means that $u_{\mathrm{C}\bar{\mathrm{a}}}$ and $u_{\mathrm{C}\bar{\mathrm{b}}}$ cannot intersect (cf. **Fig. 3**).

as shown in **Fig. 1**. Therefore, nodes x, y and z form a kind of split DC link which provides the input voltages u_xy and u_yz for the DC-DC converters. However, as the switches of the IVS are operated at mains frequency only, the voltages u_xN, u_yN and u_zN, are piecewise sinusoidal and hence form a three-phase system (cf. **Fig. 2**). This allows to move the input filter capacitors to the DC side of the IVS as shown in **Fig. 5**.

Throughout this paper a star connection of the filter capacitors (C_x, C_y and C_z) is assumed. However, a line-to-line (delta) connection could be used as well. Note that a total of three capacitors of equal capacitance is required in order to load the AC grid symmetrically, even for a delta connection as the voltages at nodes x, y and z are piecewise sinusoidal and form a three phase system within every 60° mains sector.

Placing the input filter capacitors on the DC side of the IVS has several advantages: It shortens the commutation paths of the DC-DC converters which means that no additional capacitors C_f' are required. Furthermore, the currents i_x, i_y and i_z flowing through the IVS are continuous in the case of DC side filter capacitors, as opposed to the original SWISS Rectifier where i_x, i_y and i_z are discontinuous due to the DC-DC converters. This leads to a reduction of conduction losses

in the IVS switches. Additionally, the DC side capacitors are decoupling the switching operations of the IVS and the DC-DC converters. In the original bidirectional SWISS Rectifier, special commutation sequences are required in the IVS in order not to interrupt the currents i_p and i_n in the output inductors [8]. This is not the case with DC side input filter capacitors, as C_x, C_y and C_z provide a conduction path for the IVS and the DC-DC converter currents at all valid switching states.

This implies that the SWISS Rectifier with DC side filter capacitors can, to some extent, be considered as a system consisting of two individual converters: an IVS stage which performs an AC-to-DC voltage conversion and a DC-DC converter stage which ensures sinusoidal input currents and provides DC output voltage control. Therefore, the IVS and the DC-DC converters can be designed, optimized and operated almost independently of each other. For example, several individual DC-DC converter modules could be fed from a single, larger IVS which provides the xyz (DC) link. In this case, the IVS and the DC-DC converters could even be spatially separated, for example accommodated in different cabinets.

III. Input Current Distortions

As described **Chapter I** the conventional SWISS Rectifier exhibits AC input current distortions at the intersections of the grid's phase voltages. This is due to the switching frequency voltage ripple at the input filter capacitors which causes additional diodes in the IVS to conduct as shown in **Fig. 4**. Note that the problem persists, even if the input filter capacitors are moved to the DC side of the IVS. In this case the voltage ripple across C_x, C_y and C_z causes diodes of turned-off DC-DC converter switches to conduct as shown in **Fig. 6**. This results in the same grid current distortions as with AC side filter capacitors, as can be seen from the simulation results shown in **Fig. 7**. An analysis of these current distortions and their impact on the AC currents' THD follows.

In order to derive an analytical model of the current distortions the switching frequency ripple components of the currents in L_f and $L_\mathrm{p,n}$ are neglected and $i_\mathrm{p} = i_\mathrm{n} = I_\mathrm{DC}$ is assumed. The grid voltages and currents are considered to be purely sinusoidal. Due to the phase symmetry it is sufficient to consider only the first intersection of u_a and u_b, i.e. $\omega t \approx \pi/3$.

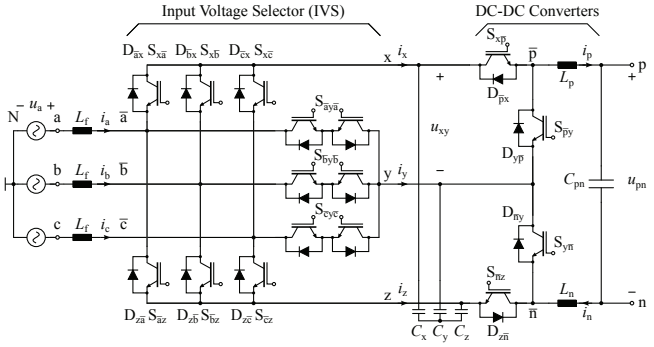

Fig. 5. Schematic of the bidirectional SWISS Rectifier with input filter capacitors placed at the DC side of the IVS. A star connection of filter capacitor is shown here, however a line-to-line (delta) connection could be used as well. The same input filter damping structure as in the original SWISS Rectifier with AC side input filter capacitors can be used.

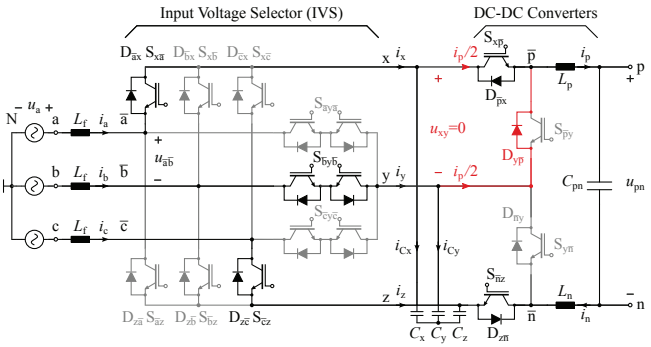

Fig. 6. Schematic of the SWISS Rectifier with $\mathrm{S}_{\mathrm{x\bar{p}}}$ turned on, showing the additional conduction path caused by the diode $\mathrm{D}_{\mathrm{y\bar{p}}}$ when the voltage u_xy across the filter capacitors C_x and C_y reaches zero. This implies that $u_\mathrm{xy} \geq 0$ (cf. **Fig. 7**).

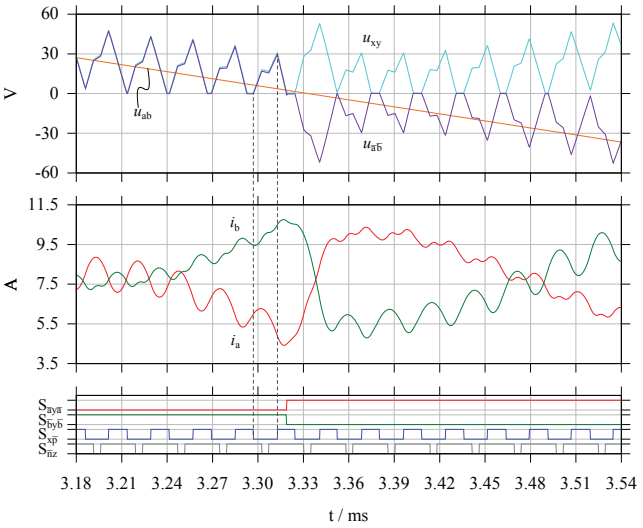

Fig. 7. Detailed simulation results for the first sector boundary (at $\omega t \approx 30°$) with input filter capacitors on the DC side of the IVS (C_x, C_y and C_z, cf. **Fig. 6**). It can be seen that u_xy cannot become negative because of $\mathrm{D}_{\mathrm{y\bar{p}}}$. This implies that the average over one switching period of the voltage $u_{\bar{a}\bar{b}}$ at the input of the IVS differs significantly from the corresponding grid voltage u_ab. Accordingly a distortion of the input currents i_a and i_b occurs.

The filter capacitors are assumed to have equal capacitance, i.e. $C_\mathrm{x} = C_\mathrm{y} = C_\mathrm{z} = C_\mathrm{f}$.

As explained above, the switching frequency ripple across the input filter capacitors is the root cause of the current distortions. Therefore, an analytical expression for its peak-to-peak value $\hat{u}_\mathrm{xy}$ is required. It can be seen from **Fig. 7** that u_xy assumes the peak value at the switching transitions of $\mathrm{S}_{\mathrm{x\bar{p}}}$. It can therefore be calculated as:

$$\begin{aligned}\hat{u}_\mathrm{xy} &= \frac{1}{C_\mathrm{f}} \int_0^{(1-d_\mathrm{p})/f_\mathrm{s}} i_\mathrm{Cx} - i_\mathrm{Cy}\, d\tau \\ &= \frac{1}{f_\mathrm{s}\, C_\mathrm{f}} \left[(i_\mathrm{x} - i_\mathrm{y})\,(1 - d_\mathrm{p}) + I_\mathrm{DC}\,(d_\mathrm{n} - d_\mathrm{p}) \right] , \end{aligned} \quad (1)$$

where d_p is the duty cycle of $\mathrm{S}_{\mathrm{x\bar{p}}}$ and d_n is the duty cycle of $\mathrm{S}_{\mathrm{\bar{n}z}}$. Assuming that the SWISS Rectifier is operated such that the AC gird currents are in phase with the gird voltages and that the current distortion is short compared to the grid

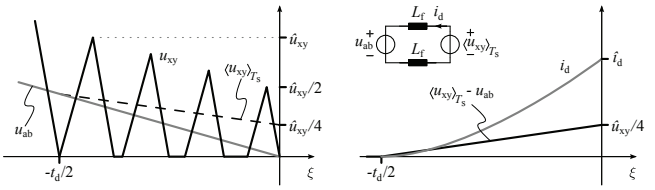

Fig. 8. Drawing (not to scale) of the assumptions made to derive (10). At the beginning of the distortion ($\xi = -t_\mathrm{d}/2$) the local average $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}$ of u_xy equals the grid voltage u_ab. The difference of $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}$ and u_ab increases linearly until $\xi = 0$ where it reaches a peak value of $\hat{u}_\mathrm{xy}/4$. This voltage, $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}} - u_\mathrm{ab}$, drives the distortion current i_d in the filter inductors of the corresponding phases.

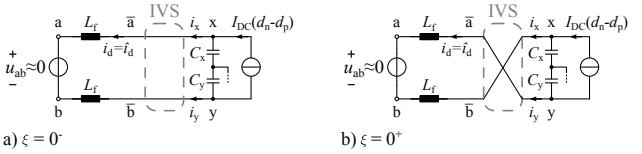

Fig. 9. Simplified schematics of the two phases with intersecting voltages: **a)** before the IVS changes polarity at $\xi = 0$ and **b)** immediately afterwards. The distortion current i_d flowing in the filter inductors L_f leads to a rapid change of u_xy after the IVS' switching as i_x and i_y change polarity.

voltage period the following simplifications hold:

$$d_\mathrm{p} = M\cos(\omega\, t) \approx \frac{M}{2} \qquad \omega t \approx \frac{\pi}{3} \tag{2}$$

$$d_\mathrm{n} = M\cos(\omega\, t - \frac{\pi}{3}) \approx M\ . \tag{3}$$

Note that M is the modulation index of the SWISS Rectifier. Neglecting any voltage drops across the switches, diodes and filter inductors, the steady state voltage transfer ratio between AC and DC side is defined as

$$U_\mathrm{pn} \approx U_{\bar{\mathrm{p}}\bar{\mathrm{n}}} = \frac{3}{2}\, M\, \hat{U}_1 \qquad M = \frac{2\, U_\mathrm{pn}}{3\, \hat{U}_1}\ , \tag{4}$$

where $\hat{U}_1$ is the amplitude of the AC grid's phase voltage [10]. By neglecting the grid frequency component of the filter capacitor current $i_\mathrm{Cx,y,z}$ further simplifications can be found:

$$i_\mathrm{x} = I_\mathrm{DC}\, d_\mathrm{p} \approx I_\mathrm{DC}\frac{M}{2} \tag{5}$$

$$i_\mathrm{z} = -I_\mathrm{DC}\, d_\mathrm{n} \approx -I_\mathrm{DC}\, M \tag{6}$$

$$i_\mathrm{y} = -(i_\mathrm{x} + i_\mathrm{z}) \tag{7}$$

By combining (1) to (7) $\hat{u}_\mathrm{xy}$ can approximated as

$$\hat{u}_\mathrm{xy} = \frac{I_\mathrm{DC}\, M}{2\, C_\mathrm{f}\, f_\mathrm{s}}\ . \tag{8}$$

When the line-to-line voltage u_ab becomes smaller than half the voltage ripple $\hat{u}_\mathrm{xy}$ calculated in (1) or (8), the current distortion starts. Hence, the time span $t_\mathrm{d}/2$ from the beginning

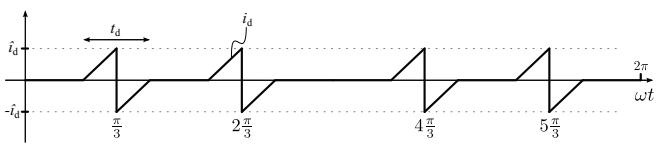

Fig. 10. Simplified distortion current within one mains period assumed for the rms-value calculation used to derive (11).

of the distortion until the zero crossing of the line-to-line voltage u_ab can be derived:

$$u_\mathrm{ab}\left(\frac{\pi}{3} - \frac{\omega\, t_\mathrm{d}}{2}\right) = \sqrt{6}\, U_1 \sin\left(\frac{\omega\, t_\mathrm{d}}{2}\right) \le \frac{\hat{u}_\mathrm{xy}}{2}\ ,$$

$$\frac{t_\mathrm{d}}{2} = \frac{1}{\omega}\arcsin\left(\frac{I_\mathrm{DC}\, M}{4\sqrt{6}\, U_1\, C_\mathrm{f}\, f_\mathrm{s}}\right) \approx \frac{1}{\omega}\frac{I_\mathrm{DC}\, M}{4\sqrt{6}\, U_1\, C_\mathrm{f}\, f_\mathrm{s}}\ . \tag{9}$$

At the beginning of the current distortion $\langle u_\mathrm{xy}\rangle_{T_\mathrm{s}}$ (the average of u_xy over one switching period T_s) is equal to the gird voltage u_ab. As can be seen from **Fig. 7**, in the center of the distortion (at $u_\mathrm{ab} = 0$), the ripple of u_xy is approximately half the value compared to the point in time where the current distortion starts. This is shown in **Fig. 8** and it enables an estimation of the distortion current's amplitude $\hat{i}_\mathrm{d}$:

$$\hat{i}_\mathrm{d} = \frac{1}{2\, L_\mathrm{f}}\int_{-t_\mathrm{d}/2}^{0} u_\mathrm{xy}\left(\frac{\pi}{3} + \frac{\xi\,\omega}{2}\right) - u_\mathrm{ab}\left(\frac{\pi}{3} + \frac{\xi\,\omega}{2}\right) d\xi\ ,$$

$$\approx \frac{1}{2\, L_\mathrm{f}}\int_{-t_\mathrm{d}/2}^{0} \frac{\hat{u}_\mathrm{xy}}{4}\left(1 + \frac{\xi}{t_\mathrm{d}/2}\right) d\xi = \frac{\hat{u}_\mathrm{xy}\, t_\mathrm{d}}{32\, L_\mathrm{f}}\ . \tag{10}$$

So far only the first half of the distortion, until u_ab reaches zero (at $\xi = 0$) was considered. Once u_ab changes its sign, the IVS commutates in order to reverse the polarity of $u_{\bar{\mathrm{a}}\bar{\mathrm{b}}}$. This is shown in the simplified schematics in **Fig. 9**. Note, that the polarity reversal of the IVS changes the sign of the IVS' DC side currents i_x and i_y. This leads to a considerably higher peak value of u_xy during the first switching period after the polarity reversal. Therefore a higher voltage is applied to the filter inductors L_f in this cycle which leads to a fast polarity reversal of the distortion current i_d. This can also be seen in the simulation results shown in **Fig. 7**. The current distortion is therefore approximately symmetric in time around the zero crossing of the line-to-line voltage u_ab (at $\omega t = \pi/3$).

For further analysis the converter's grid currents $i_\mathrm{a,b,c}$ are approximated as sum of a fundamental component $i_\mathrm{a,b,c(1)}$ which is in phase with the grid voltages and a distortion i_d. Each phase is distorted four times per gird voltage period. By modeling each distortion as one triangular wave with a period of t_d and amplitude $\hat{i}_\mathrm{d}$ (cf. **Fig. 10**), the rms value I_d of $i_\mathrm{da,b,c}$ can be calculated as

$$I_\mathrm{d} = \frac{\hat{i}_\mathrm{d}}{\sqrt{3}}\sqrt{4\, t_\mathrm{d}\, f}\ . \tag{11}$$

In order to generalize (11) for any SWISS Rectifier, the following normalization is applied:

$$C_\mathrm{f} = \frac{Q_\mathrm{f}}{3\, U_1^2\, \omega} \quad Q_\mathrm{f} = P\tan(\phi_1)\ , \tag{12}$$

$$L_\mathrm{f} = L_\mathrm{f,p.u.}\frac{R_1}{\omega} = L_\mathrm{f,p.u.}\frac{3\, U_1^2}{\omega\, P} \quad R_1 = \frac{3\, U_1^2}{P}\ , \tag{13}$$

$$I_\mathrm{DC}\, M = \hat{I}_\mathrm{a,b,c(1)} = \frac{2\, P}{3\, \hat{U}_1}\ . \tag{14}$$

Note that ϕ_1 represents the phase shift of the input current's fundamental which results from the reactive power consumption of the input filter capacitors. The reactive power created by the filter inductors is neglected as it is typically much smaller than the Q_f.

By combining (11) with (8)-(10) and applying the normalizations (12)-(14) the normalized RMS value of the current

TABLE II
COMPARISON BETWEEN CALCULATION AND SIMULATION

	Calculated	Simulated	Error
$\hat{u}_{xy}$	48.6 V	43.4 V	12 %
t_d	275 µs	279 µs	−1.4 %
$\hat{i}_d$	3.48 A	3.34 A	4.2 %
$I_d/I_{a,b,c(1)}$ (THD)	4.31 %	4.23 %	1.9 %

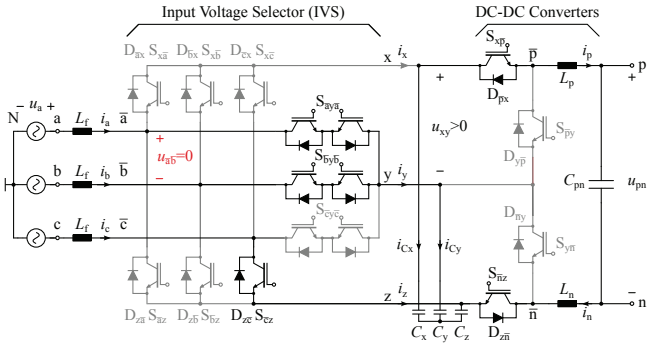

Fig. 11. SWISS Rectifier with DC side input filter capacitors and AC-to-DC power transfer during the first intersection of u_a and u_b. By turning $S_{x\bar{a}}$ off and turning on $S_{\bar{a}y\bar{a}}$ the IVS' output voltage $u_{\bar{a}\bar{b}}$ is forced to zero.

distortions can be expressed as a function of general system parameters:

$$\frac{I_d}{I_{a,b,c(1)}} = \frac{\pi^2}{16 \cdot 3^{5/4}} \frac{1}{L_{f,p.u.}} \left(\frac{f}{f_s} \frac{1}{\tan(\phi_1)} \right)^{5/2}, \qquad (15)$$

where $I_{a,b,c(1)}$ is the RMS value of the AC side input currents' fundamental component at nominal power. This allows an estimation of the current distortions' impact on the rectifier's input current THD. It can be seen that increasing the switching frequency or the input filter capacitors (increasing ϕ_1) reduces the magnitude of the current distortions with a power of 2.5, while it is inversely proportional to the input filter inductance.

Table II shows the numerical results for the equations derived above and compares the values to results obtained from a simulation of the system specified in **Table I**. The calculated values are typically within 10 % of the simulation results. Furthermore, it can be seen that the low frequency THD[1] of the rectifier's input currents is 4.2 %. A modulation technique eliminating the current distortions is presented in the following.

IV. MITIGATING DISTORTIONS BY PWM OF THE IVS

As described in the previous chapter, the AC input current distortions can have a significant contribution to the THD of a SWISS Rectifier. For the system specified in **Table I** current distortions with a normalized RMS value of 4.2 % result. However, the distortions can be prevented by properly modulating the switches in the IVS as will be shown in the following.

The root cause of the current distortions is the switching frequency voltage ripple across the input filter capacitors and the fact that the voltages u_{xy} and u_{yz} cannot be negative (cf. **Fig. 7**). However, if the input filter capacitors are placed on the DC side of the IVS, the IVS can be used to temporarily disconnect the filter capacitors $C_{x,y,z}$ from the filter inductors L_f by simultaneously turning on two of the three injection

[1]Spectral components up to 10 kHz, i.e. up to the 200th harmonic of the grid frequency, are considered.

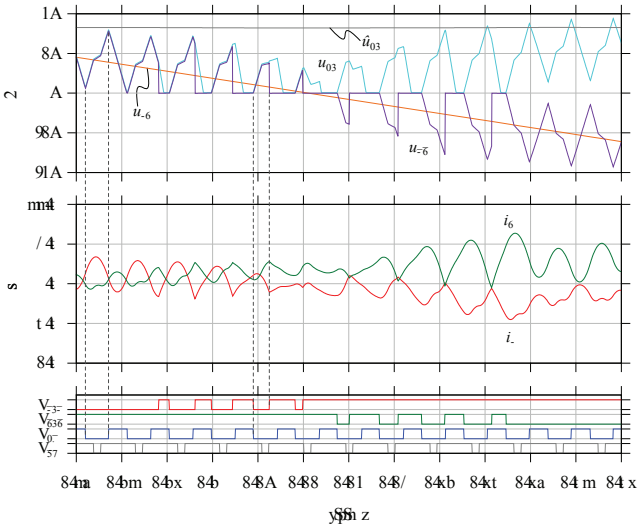

Fig. 12. Simulation results, showing pulse width modulated injection switches $S_{\bar{a}y\bar{a}}$ and $S_{\bar{b}y\bar{b}}$ during the first intersection of u_a and u_b which reduces the current distortions. Furthermore, the calculated peak-to-peak ripple of u_{xy} is shown as $\hat{u}_{xy}$.

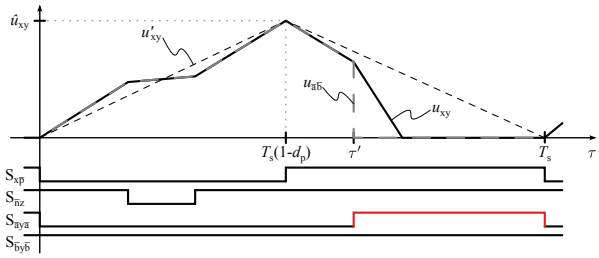

Fig. 13. Time behavior of the filter capacitor voltage ripple u_{xy} within one switching period T_s for DC-to-AC power transfer. The signal u'_{xy} is used as approximation for u_{xy} in order to simplify the algebraic calculations.

switches, e.g. $S_{\bar{a}y\bar{a}}$ and $S_{\bar{b}y\bar{b}}$. This short-circuits the corresponding input nodes $\bar{a}$ and $\bar{b}$ and results in $u_{\bar{a}\bar{b}} = 0$, as shown in **Fig. 11**. Therefore, it is possible to mitigate the current distortions by toggling the second injection switch such that the average over one switching period of $u_{\bar{a}\bar{b}}$ equals the gird voltage u_{ab}.

A. AC-to-DC Power Transfer

The following considerations focus on AC-to-DC power transfer and the intersection of u_a and u_b at $\omega t \approx \pi/3$, however, they can be generalized for the other five intersections and DC-to-AC power transfer. It can be seen from **Fig. 12** that u_{xy} increases while $S_{x\bar{p}}$ is not conducting, which implies that u_{xy} is minimal when $S_{x\bar{p}}$ is turned off. Therefore, the turn-off of $S_{x\bar{p}}$ is selected as origin for the auxiliary time axis τ.

Fig. 13 shows a diagram of the filter capacitor voltage u_{xy} during the first half of the first intersection ($\omega t \leq \pi/3$, $u_a > u_b$). The additional injection switch $S_{\bar{a}y\bar{a}}$ is turned on at time τ' and is turned off together with $S_{x\bar{p}}$ in order to allow u_{xy} to charge. In order to simplify the analytical calculations u'_{xy} is used as an approximation for u_{xy}:

$$u'_{xy}(\tau) = \begin{cases} \hat{u}_{xy} \frac{\tau}{(1-d_p)\,T_s} & \text{if } \tau \leq (1-d_p)\,T_s \\ \hat{u}_{xy} \frac{1}{d_p} \left(1 - \frac{\tau}{T_s}\right) & \text{if } \tau > (1-d_p)\,T_s \end{cases}, \qquad (16)$$

$$u_{\bar{a}\bar{b}}(\tau) = \begin{cases} u_{xy}(\tau) \approx u'_{xy}(\tau) & \text{if } \tau \leq \tau' \\ 0 & \text{if } \tau > \tau' \end{cases}. \qquad (17)$$

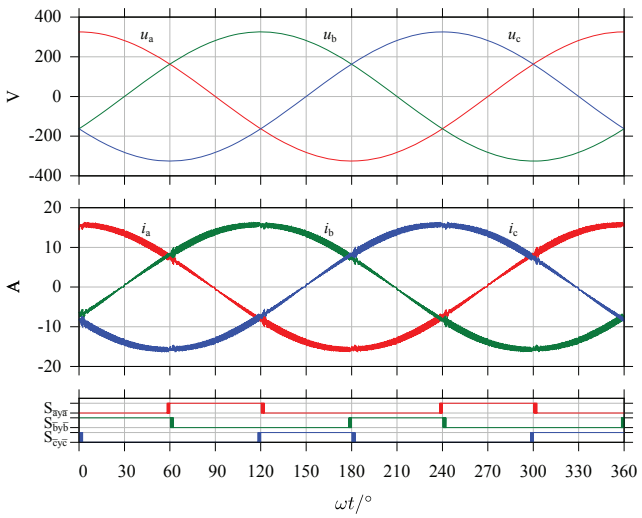

Fig. 14. Simulation results for the SWISS Rectifier specified in **Table I** using the proposed modulation technique for the IVS switches. Compared with the results in **Fig. 2**, the current distortions are significantly reduced, the low frequency ($< 10\,\mathrm{kHz}$) THD of $i_{a,b,c}$ reduces from $4.2\,\%$ to $0.8\,\%$.

Note that either equation (1) or (8) can be used to estimate the peak value $\hat{u}_{xy}$. The average $\langle u_{\bar{a}\bar{b}}(\tau)\rangle_{T_s}$ over one switching frequency period T_s of the IVS output voltage $u_{\bar{a}\bar{b}}$ can be found by integration:

$$\langle u_{\bar{a}\bar{b}}(\tau')\rangle_{T_s} = \frac{1}{T_s}\int_0^{\tau'} u_{xy}(\tau)\,d\tau \approx \frac{1}{T_s}\int_0^{\tau'} u'_{xy}(\tau)\,d\tau\ . \tag{18}$$

In order to prevent the current distortions τ' has to be selected such that $\langle u_{\bar{a}\bar{b}}(\tau')\rangle_{T_s}$ equals the corresponding AC grid voltage u_{ab} which is used as reference value u_{ref}:

$$u_{ref} = u_a - u_b = u_{ab} \tag{19}$$

By solving (18) an algebraic expression for τ' can be found:

$$u_{ref} = \langle u_{\bar{a}\bar{b}}(\tau')\rangle_{T_s} \quad \Rightarrow$$
$$\tau' = T_s \begin{cases} \sqrt{2\,\frac{u_{ref}}{\hat{u}_{xy}}\,(1-d_p)} & \text{if } u_{ref} \le \hat{u}_{xy}\,\frac{1-d_p}{2} \\ 1-\sqrt{d_p - 2\,d_p\,\frac{u_{ref}}{\hat{u}_{xy}}} & \text{if } u_{ref} > \hat{u}_{xy}\,\frac{1-d_p}{2}\ . \end{cases} \tag{20}$$

This implies that the current distortions can be mitigated by measuring the grid voltages and evaluating equations (1), (19) and (20) every switching frequency cycle. The additional injection switch $S_{\bar{a}y\bar{a}}$ is then turned on at time τ' after the turn-off of $S_{x\bar{p}}$.

All considerations and calculations given above hold only for the first half of the first current distortion, i.e. for $\omega t < \pi/3$. In the second half ($\omega t > \pi/3$) the grid voltage u_{ab} becomes negative which implies that the output voltage of the IVS has to be negative as well, while the filter capacitor voltage u_{xy} remains positive. This is achieved by modulating $S_{\bar{b}y\bar{b}}$ instead of $S_{\bar{a}y\bar{a}}$, as can be seen in **Fig. 12**. By replacing the grid voltages u_a and u_b and the injection switches with the corresponding values, this can be generalized for the other two positive grid voltage intersections ($\omega t \approx 180°, 300°$). Furthermore, the concept can be expanded to the negative side DC-DC converter ($S_{\bar{n}z}$, d_n, u_{yz}) to mitigate the current distortions at the intersections of negative grid phase voltages

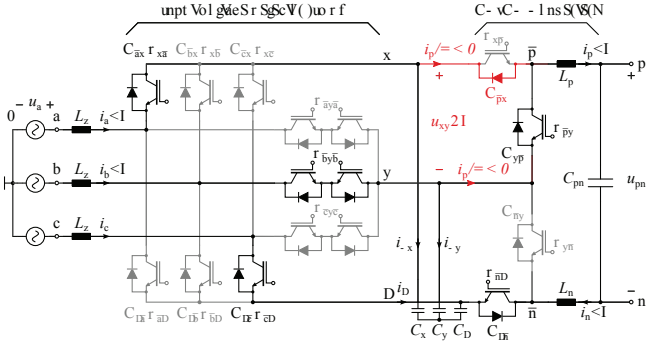

Fig. 15. Schematic of the SWISS Rectifier with DC-to-AC power transfer ($i_p < 0$, $i_n < 0$) during the first intersection of u_a and u_b. When the filter capacitor voltage u_{xy} reaches zero the diode $D_{\bar{p}x}$ is forward biased and starts to conduct, thus preventing u_{xy} from reversing polarity. Therefore, similar input current distortions as for AC-to-DC power transfer result (cf. **Fig. 6**).

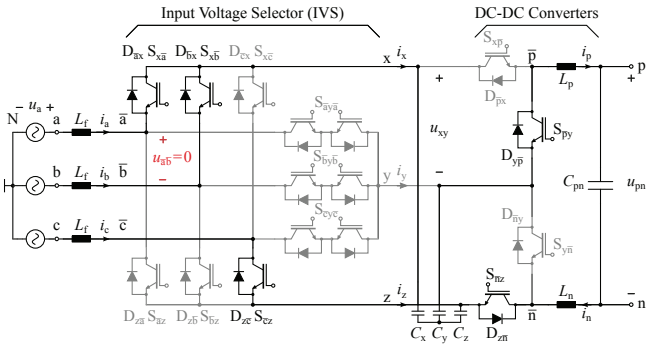

Fig. 16. SWISS Rectifier with DC-to-AC power transfer ($i_p < 0$, $i_n < 0$) during the first intersection of u_a and u_b. Two Rectifier switches ($S_{x\bar{a}}$, $S_{x\bar{b}}$) are turned on simultaneously ($S_{\bar{b}y\bar{b}}$ is turned off) in order to achieve $u_{\bar{a}\bar{b}} = 0$.

($\omega t \approx 0°, 120°, 240°$). The resulting formulas are summarized in **Table III**. Simulation results for AC-to-DC operation of the SWISS Rectifier with the compensation enabled for all intersections are shown in **Fig. 14**.

B. DC-to-AC Power Transfer

The previous descriptions focus on AC-to-DC power transfer, however, the current distortions exist for DC-to-AC power transfer as well. A similar mitigation strategy can be used as will be shown in the following.

As depicted in **Fig. 15** the diode $D_{\bar{p}x}$ starts to conduct for DC-to-AC power transfer once the filter capacitor voltage u_{xy} reaches zero. Therefore, the local average of u_{xy} starts to deviate from the grid voltage u_{ab} once the ripple is larger than $2\,u_{ab}$ as explained above for AC-to-DC power transfer. Thus similar grid current distortions result.

In order to temporarily disconnect the grid filter inductors L_f from the filter capacitors $C_{x,y,z}$ two rectifier switches, e.g. $S_{x\bar{a}}$, $S_{x\bar{b}}$ are turned on simultaneously as shown in **Fig. 16**. Simulation results of a SWISS Rectifier using this modulation technique are shown in **Fig. 17**. Note that, unlike for AC-to-DC power transfer, it is not possible to modulate the injection switches $S_{\bar{i}y\bar{i}}$ ($\bar{i} = \bar{a}, \bar{b}, \bar{c}$) because u_{xy} has to be discharged to zero once the additional switch is turned on at τ'. It can be shown that this is the case only when the rectifier switches $S_{x\bar{a},\bar{b},\bar{c}}$, $S_{\bar{a},\bar{b},\bar{c}z}$ are modulated.

The equations required to implement the mitigation algorithm for DC-to-AC power transfer are summarized in the right column of **Table III**. Note that the switching transition

TABLE III
EQUATIONS REQUIRED TO IMPLEMENT THE DISTORTION MITIGATION ALGORITHM

AC-to-DC Power Transfer	**DC-to-AC Power Transfer**
Modulation: $S_{\bar{a}y\bar{a}}$, $S_{\bar{b}y\bar{b}}$, $S_{\bar{c}y\bar{c}}$	Modulation: $S_{x\bar{a}}$, $S_{x\bar{b}}$, $S_{x\bar{c}}$
Positive Voltage Intersections	
Origin of τ': $S_{x\bar{p}}$ $1 \rightarrow 0$	Origin of τ': $S_{x\bar{p}}$ $0 \rightarrow 1$
$\tau' = T_s \begin{cases} \sqrt{2\,\frac{u_{ref}}{\hat{u}_{xy}}\,(1-d_p)} & \text{if } u_{ref} \le \hat{u}_{xy}\,\frac{1-d_p}{2} \\ 1-\sqrt{d_p\left(1-2\,\frac{u_{ref}}{\hat{u}_{xy}}\right)} & \text{if } u_{ref} > \hat{u}_{xy}\,\frac{1-d_p}{2} \end{cases}$	$\tau' = T_s \begin{cases} \sqrt{2\,\frac{u_{ref}}{\hat{u}_{xy}}\,d_p} & \text{if } u_{ref} \le \hat{u}_{xy}\,\frac{d_p}{2} \\ 1-\sqrt{(1-d_p)\left(1-2\,\frac{u_{ref}}{\hat{u}_{xy}}\right)} & \text{if } u_{ref} > \hat{u}_{xy}\,\frac{d_p}{2} \end{cases}$
$\hat{u}_{xy} = \frac{T_s}{C_f}\left[(i_x - i_y)\,(1-d_p) + I_{DC}\,(d_n - d_p)\right]$	$\hat{u}_{xy} = \frac{T_s}{C_f} d_p\,(i_x - i_y - I_{DC})$
Negative Voltage Intersections	
Origin of τ': $S_{\bar{n}z}$ $1 \rightarrow 0$	Origin of τ': $S_{\bar{n}z}$ $0 \rightarrow 1$
$\tau' = T_s \begin{cases} \sqrt{2\,\frac{u_{ref}}{\hat{u}_{yz}}\,(1-d_n)} & \text{if } u_{ref} \le \hat{u}_{yz}\,\frac{1-d_n}{2} \\ 1-\sqrt{d_n\left(1-2\,\frac{u_{ref}}{\hat{u}_{yz}}\right)} & \text{if } u_{ref} > \hat{u}_{yz}\,\frac{1-d_n}{2} \end{cases}$	$\tau' = T_s \begin{cases} \sqrt{2\,\frac{u_{ref}}{\hat{u}_{yz}}\,d_n} & \text{if } u_{ref} \le \hat{u}_{yz}\,\frac{d_n}{2} \\ 1-\sqrt{(1-d_n)\left(1-2\,\frac{u_{ref}}{\hat{u}_{yz}}\right)} & \text{if } u_{ref} > \hat{u}_{yz}\,\frac{d_n}{2} \end{cases}$
$\hat{u}_{yz} = \frac{T_s}{C_f}\left[(i_y - i_z)\,(1-d_n) + I_{DC}\,(d_p - d_n)\right]$	$\hat{u}_{yz} = \frac{T_s}{C_f} d_n\,(i_y - i_z - I_{DC})$

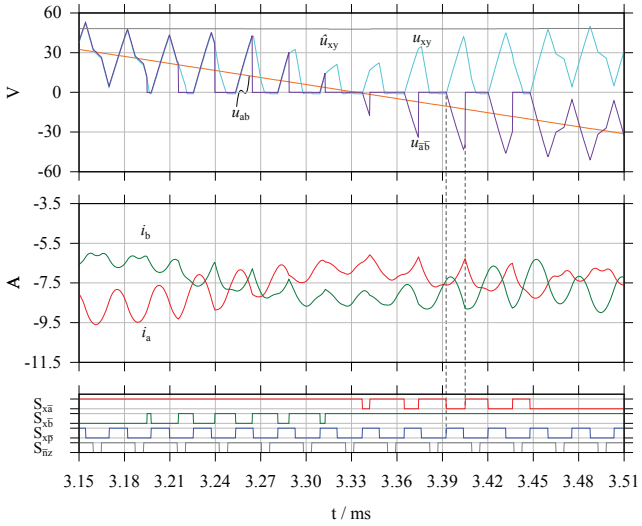

Fig. 17. Detailed simulation results for DC-to-AC power transfer and the first intersection of u_a and u_b showing the modulation of a second rectifier switch ($S_{x\bar{a}}$, $S_{x\bar{b}}$). The distortion in i_a and i_b is significantly reduced.

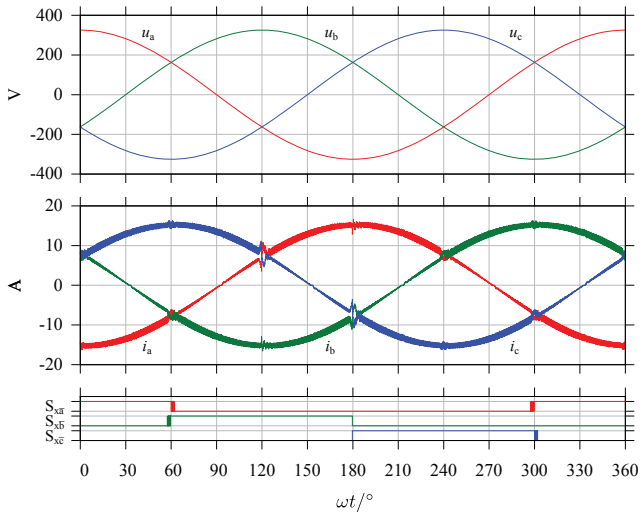

Fig. 18. Simulation results for the SWISS Rectifier specified in **Table I** with DC-to-AC power transfer. The proposed algorithm is used to mitigate the current distortions. During the intersections at $\omega t \approx 120°, 180°$ the mitigation algorithm is turned off for illustrative purposes.

which marks the beginning of the time span τ' is different than in AC-to-DC power transfer.

Fig. 18 shows simulation results for the SWISS Rectifier specified in **Table I** with 7.5 kW DC-to-AC power transfer. For illustration, the distortion compensation is disabled for the intersections at $\omega t \approx 120°$ and $\omega t \approx 180°$. It can be seen that the current distortions are significantly reduced.

V. MEASUREMENT RESULTS

In order to demonstrate the practicability of the algorithm described above, it was implemented on a bidirectional 7.5 kW prototype SWISS Rectifier. The values of all major components used in the system are given in **Table I** and were used for the presented simulation results.

A. AC-to-DC Power Transfer

Fig. 19 shows measurements taken on the hardware prototype operating with AC-to-DC power transfer. The mitigation algorithm is active during the grid voltage intersections at $\omega t \approx 60°$, $120°$ and $240°$. At $\omega t \approx 300°$ it is disabled in order to demonstrate the effect and magnitude of the current distortions in the grid current i_a. It can be seen that the amplitude of the current distortions is reduced below the switching frequency ripple of the input current.

B. DC-to-AC Power Transfer

Measurement results for DC-to-AC power transfer at nominal power are shown in **Fig. 20**. Again, the mitigation algorithm is disabled during the two intersections at $\omega t \approx 240°$ and $\omega t \approx 300°$ for comparison. Furthermore, the input filter capacitor voltage u_{xy} is shown. Note that it is positive at all times, which is in accordance with **Section IV-B**.

Fig. 21 shows detailed measurements of the first intersection of u_a and u_b at $\omega t \approx 60°$ for the same operating conditions as in **Fig. 20**. The output voltage $u_{\bar{a}\bar{b}}$ of the IVS is shown as well. It can be seen that the control algorithm turns on additional rectifier switches in order to reduce the average output voltage $u_{\bar{a}\bar{b}}$ of the IVS. Therefore, the average of $u_{\bar{a}\bar{b}}$ closely follows the grid voltage u_{ab}. Note that the grid voltage u_{ab} shows a switching frequency ripple due to the output impedance of the AC-source employed to provide the three-phase AC mains supply voltage.

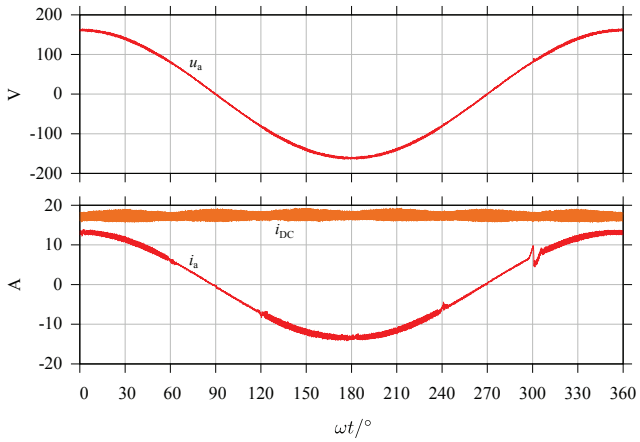

Fig. 19. Measurement results for the SWISS Rectifier prototype operated with $I_{DC} = 17.4\,A$ and $U_1 = 115\,V$. The current distortion compensation is turned off during the intersection at $\omega t \approx 300°$ for illustrative purposes.

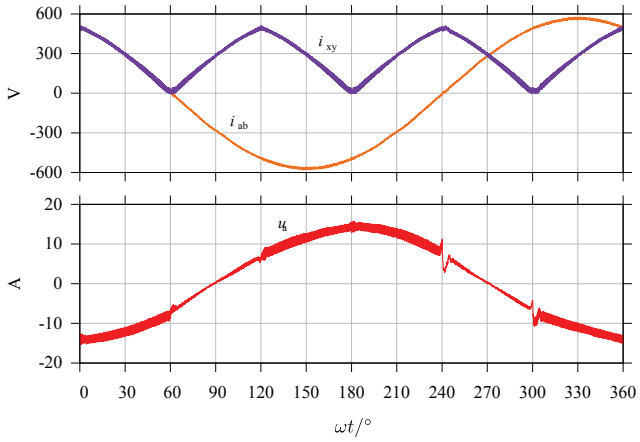

Fig. 20. Measurement results for the SWISS Rectifier prototype operated with nominal DC-to-AC power transfer. The distortion compensation is turned off during the intersection at $\omega t \approx 240°, 300°$ for illustrative purposes.

VI. Conclusion

This paper analyzes the AC input current distortion in three-phase buck-type SWISS Rectifiers which is caused by the switching frequency voltage ripple across its input filter capacitors. An analytical model is derived which allows the estimation of the distortion current's peak value and its impact on the converter's overall THD. It is shown that the current distortion's magnitude depends on the AC side filter inductance value, the ratio of switching frequency and AC grid frequency and the AC filter capacitance value.

In order to reduce the current distortion, a modification of the original SWISS Rectifier's circuit topology is proposed. By moving the AC side filter capacitors to the DC side of the input voltage selector (IVS), the commutation paths of the DC-DC converters are shortened and the conduction losses in the IVS switches are reduced. Furthermore, the DC-DC converters and the IVS can be operated independently which allows a temporary pulse width modulation of the IVS switches at the phase voltage sector boundaries in order to mitigate the input current distortions.

The modulation concept and the formulas required for its implementation are derived. It can be applied to uni- and bidirectional SWISS Rectifiers and AC-to-DC as well as DC-to-AC power transfer. Furthermore, it does not require additional sensors; the DC link current sensor and the AC grid voltage sensors, which are typically present in a SWISS Rectifier, are sufficient. In total, three multiplications, one division and one square root have to be evaluated once every switching cycle.

Simulations of various operating conditions and measurements taken on a 7.5 kW hardware prototype are proving the principle's feasibility.

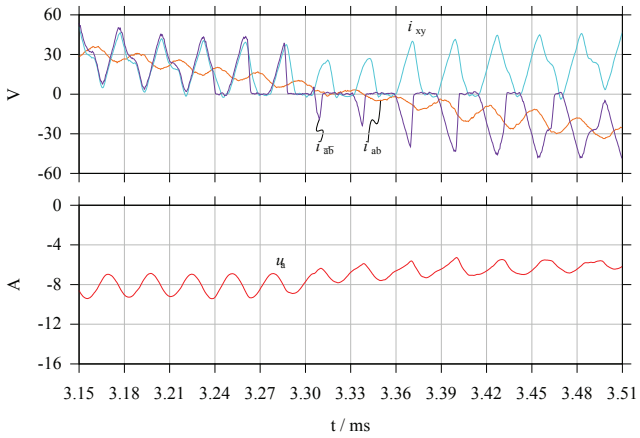

Fig. 21. Detailed results of the first grid voltage intersection of phases a and b (at $\omega t \approx 30°$) for the same configuration as in **Fig. 20**. Shown are the voltage u_{xy} of the DC side input filter capacitors, the line-to-line gird voltage u_{ab} and the output voltage $u_{a\bar{b}}$ of the IVS, as well as the grid current i_a.

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