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Conceptualization and Analysis of a Next-Generation Ultra-Compact 1.5-kW PCB-Integrated Wide-Input-Voltage-Range 12V-Output Industrial DC/DC Converter Module

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Abstract: The next-generation industrial environment requires power supplies that are compact, efficient, low-cost, and ultra-reliable, even across mains failures, to power mission-critical electrified processes. Hold-up time requirements and the demand for ultra-high power density and minimum production costs, in particular, drive the need for power converters with (i) a wide input voltage range, to reduce the size of the hold-up capacitor, (ii) soft-switching over the full input voltage and load ranges, to achieve low losses that facilitate a compact realization, and (iii) complete PCB-integration for low-cost manufacturing. In this work, we conceptualize, design, model, fabricate, and characterize a 1.5 kW, 12 V-output DC/DC converter for industrial power supplies that is required to operate across a wide 300 V–430 V input voltage range. This module utilizes an LLC-based control scheme for complete soft-switching and a snake-core transformer to divide the output current with a balanced flux among multiple secondary windings. Detailed loss models are derived for every component in the converter. The converter achieves close to 96 % peak efficiency with a power density of 337 W in^{-3} (20.6 kW dm^{-3}), excellent matching to the derived loss models, and zero-voltage switching even down to zero load. The loss models are used to identify improvements to further boost efficiency, the most important of which is the minimization of delay times in synchronous rectification, and a subsequent improved 1.5 kW hardware module eliminates nearly 25% of converter losses for a peak efficiency of nearly 97% with a power density of 308 W in^{-3} (18.8 kW dm^{-3}). Two 1.5 kW modules are then paralleled to achieve 3 kW output power at 12 V and 345 W in^{-3} (21.1 kW dm^{-3}) with ideal current sharing between the secondary outputs and no drop in efficiency from a single module, an important characteristic enabled by the novel snake-core transformer.

Keywords: resonant DC/DC converter; LLC; soft switching; PCB-integrated magnetics; wide-input-voltage range

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1. Introduction

The industrial environment of the future is increasingly electric, with factory automation and special-purpose electrified processes defining the next-generation of manufacturing environments, often referred to as Industry 4.0 [1]. Power supplies for these applications operate with highly-demanding specifications, especially on reliability and hold-up time, as mere moments of power supply downtime may translate to costly hours of downtime for the plant. For the grid-connected power supply of Figure 1a, the low-voltage output (V_o) must bridge short mains faults and, with a complete mains failure, hold-up V_o long enough for a safe shutdown of the digital and physical systems (see

Figure 1b). This is so critical for continuous line operation that batteries are integrated into commercially-available industrial power supplies in this class to extend hold-up time [2].

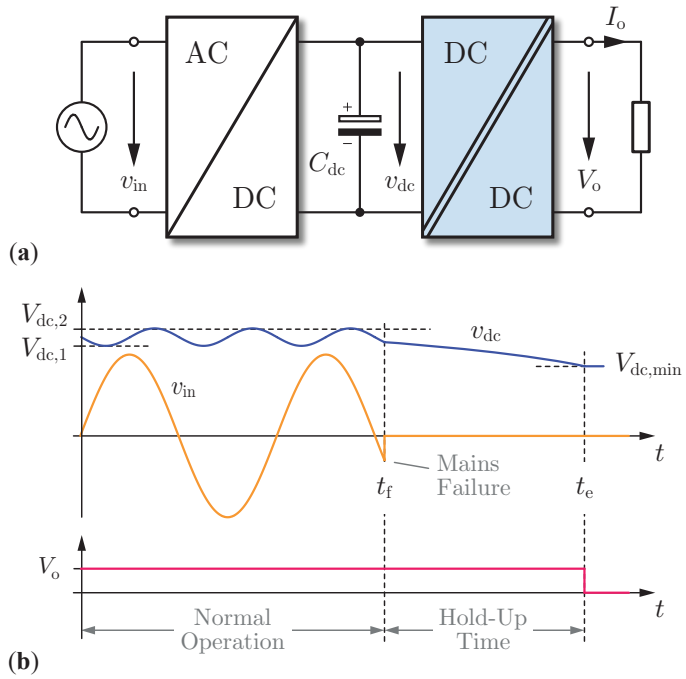

Figure 1. (**a**) Industrial power supply block diagram to convert AC-mains voltage to a high-current $V_o = 12\,V$ output; this work focused on the DC/DC converter. The requirements of the DC-link capacitor (C_{dc}) are driven by the hold-up time requirements (here, $t_e - t_f = 6\,ms$) during fault conditions, as shown in (**b**). Even with the input voltage range specified here ($V_{dc,min} = 300\,V - V_{dc,2} = 430\,V$), the DC-link capacitor accounts for nearly 15 % of the allocated system volume, indicating how critical this wide input range for the DC/DC converter is to overall system power density.

These supplies may drive, for example, CNC steppers or servo systems, and the low-voltage output must deliver hundreds of amperes of current with exacting demands that extend beyond the hold-up time requirements [3]: (i) power density, with real estate at a premium and supply cabinets already consuming space otherwise available for functional equipment, (ii) low initial and/or installation costs as the critical metric for adoption, and (iii) high and flat efficiency curves, with supplies rarely operating at full load and heat generation in cabinets driving cooling needs [2,4].

In this work, we focus on the high-step-down ratio DC/DC converters needed in these applications. The requirements of this converter module, with 1.5 kW output power at 12 V, introduce significant challenges in design when striving for ultra-high power density (targeted for $300\,W\,in^{-3}$, or $18.3\,kW\,dm^{-3}$) and full PCB-integration (including magnetics), a requirement for low-cost and high-reliability. The strict height dimension of 1.2 cm (given with other key specifications in Table 1) further drives magnetics design complexity with only very thin form factors available for these PCB-integrated components.

The hold-up time requirement ($t_e - t_f = 6\,ms$) could be met with additional converters, for example with (i) a partial-power pre-regulation converter and a fixed-voltage-ratio DC/DC converter [5], (ii) a hold-up time extension circuit [6], or (iii) a reverse-feeding concept [7]. Each of these add complexity and size in the form of an additional power stage, and we instead seek to meet the 6 ms hold-up time requirement through the combination of C_{dc} and a wide-input-voltage range DC/DC module. If we take a typical specific capacitance of $267\,\mu F\,in^{-3}$ (for box-volume, ultra-compact, 450 V electrolytic capacitors, e.g., *450USK1000MEFCSN35X55*), $C_{dc} = 1\,mF$ would already consume 15 % of the allotted

volume in a 100 W in^{-3} (6.1 kW dm^{-3}) next-generation power supply, and the DC/DC converter would need to operate from $V_{dc,min} = 300$ V to $V_{dc,2} = 430$ V, a wide-input-voltage range. We take this input voltage range as our requirement, knowing that we cannot achieve the required converter power density with any additional capacitance to narrow this range. With our power density specification prescribing such a high switching frequency that soft-switching is required, then, we encounter the major design challenge of the work: the control and topology of a wide-range, complete soft-switching DC/DC converter to meet, simultaneously, the hold-up time *and* power density specifications.

Table 1. DC/DC module design specifications.

Full-load output power (P_o)	1.5 kW
Output voltage (V_o)	12 V
Full-load output current (I_o)	125 A
Power density	300 W in^{-3} (18.3 kW dm^{-3})
Footprint ($l \times w$)	10 cm × 7 cm
Height (h)	1.2 cm
Input voltage range ($V_{dc,min} - V_{dc,2}$)	300 V–430 V
PCB-integrated	Yes
Full ZVS	Yes
Parallel-able	Yes

Indeed, upon reviewing the literature, there is no prior study that meets the demanding specifications of these next-generation Industry 4.0 power converters. In particular, wide-input-voltage range, complete soft-switching, and high-current 12 V output with PCB-integrated magnetics are rarely found together (see Table 2). Buck-based topologies support a wide-input-voltage range, but are hard-switched (over at least part of the regime) and therefore have low efficiency [8–11]. LLC-based converters are soft-switched with high efficiencies even at high switching frequencies, but are limited by a narrow input voltage range [12–17] that, in this application, would result in an unreasonably-large DC-link capacitor to meet hold-up specifications. At the extreme of narrow input voltage ranges, DC transformers ("DCX") with a fixed voltage conversion ratio require, at a minimum, a differential-power pre-regulation stage [5]. The only prior art with a wide-input range, soft-switching over the complete range, and high-current output with PCB-integrated magnetics has either a maximum efficiency of only 93 % [18] or low power density when the necessary passives are included [19] ([19] also features lower output current, which is simpler to PCB-integrate). Finally, designs with higher output voltages (e.g., $V_o = 48$ V [12,13,20]) are much simpler to PCB integrate (with 16× lower conduction losses on the secondary side) but do not meet the entrenched and ubiquitous 12 V buses that currently dominate industrial applications.

The goal here, then, is to conceptualize, design, model, and construct a next-generation industrial power supply that meets the demanding specifications of this high-reliability application while maximizing the DC/DC converter efficiency (Table 1), a combination that has not been realized previously in the literature. First, we identify a suitable low-complexity circuit topology and control scheme (Section 2.1) to operate across the wide-input-voltage range with complete soft-switching, implementing a new hybrid wide-input-range LLC control for a topology that includes a full-bridge primary and a matrix transformer for multiple high-current outputs. For each component—and especially for the PCB-integrated magnetics, including the novel snake-core transformer—we derive detailed loss and volume models that permit component-level Pareto optimizations, and present an optimal design for the 300 W in^{-3} power density target of the demonstrator module (the remainder of Section 2). In Section 3, we verify the design with a 1.5 kW demonstrator, achieving nearly 96 % DC/DC efficiency, 337 W in^{-3} power density with PCB-integrated magnetics, excellent matching to the derived loss models, and zero-voltage switching even down to zero load. In Section 4, we find the efficiency limitations for the hardware prototype and analyze the sensitivity of this barrier to component designs and architec-

tures, guiding a redesign of an improved converter module with 25 % lower total losses. In Section 5, we characterize this improved hardware demonstrator and showcase ideal current sharing among the secondary phases with two paralleled modules, a critical characteristic for high-current outputs that is uniquely enabled by the snake-core architecture. Section 6 concludes the paper with a discussion of fundamental efficiency limits for these high-output-current, wide-input-voltage range converters that will be critical to the electrification of Industry 4.0.

Table 2. Survey of published converters near the design specifications of the DC/DC module considered in this paper. Efficiency is given at nominal load ($1.0P_o$) and 50 % of nominal load ($0.5P_o$).

Ref.	Topology	Full ZVS?	v_{dc}	V_o / I_o	Power Density	Eff. ($1.0P_o$)	Eff. ($0.5P_o$)	PCB-int.?
[14,16]	LLC	Yes	380 V	12 V/83 A	700 W in^{-3}	96.5 %	97.1 %	Yes
[17]	LLC	Yes	380 V	12 V/67 A	900 W in^{-3}	97.2 %	97.6 %	Yes
[15]	LLC	Yes	200 V–420 V	12 V/83 A	—	91.2 %	96.0 %	No
[15]	PSFB	No	200 V–420 V	12 V/83 A	—	92.4 %	96.0 %	No
[21]	PSFB	Yes	270 V	22 V/68 A	—	93.2 %	96.0 %	No
[22]	PSFB	Yes	230 V–430 V	14 V/150 A	170 W in^{-3} (target)	95.0 %	96.0 %	Yes
[19]	PSFB	Yes	330 V–420 V	12 V/83 A	300 W in^{-3} (package)	97.8 %	99.1 %	Yes
[18]	Double-clamp	Yes	160 V–420 V	13.8 V/130 A	900 W in^{-3} (package)	93.0 %	93.5 %	Yes
[8]	Half-bridge	No	150 V–400 V	12 V/167 A	—	91.8 %	94.7 %	No
[9]	DAB	No	240 V–450 V	12 V/182 A	25 W in^{-3}	93.5 %	95.0 %	No
[10]	DSAB	No	350 V–410 V	12 V/25 A	≈20 W in^{-3}	95.9 %	97.0 %	Yes
[12]	LLC	Yes	280 V–380 V	48 V/2 A	≈30 W in^{-3}	94.0 %	95.0 %	Yes
[13]	Morphing LLC	Yes	100 V–400 V	48 V/17 A	—	94.3 %	—	No
[20]	PSFB	Yes	300 V–400 V	50 V/24 A	—	93.9 %	93.9 %	No
Target		Yes	300 V–430 V	12 V/125 A	300 W in^{-3}			Yes

2. DC/DC Converter Design

We first detail the design of the DC/DC converter module, which has the topology shown in Figure 2a, with the secondary split into four paralleled outputs to reduce the output current stress imposed on a single secondary winding and rectifier stage. We analyze the gain range and controllability before moving to the two most challenging passive components: the PCB-integrated transformer and primary inductor, both of which must achieve ultra-high copper utilization within the constraints of PCB fabrication methods. This copper utilization is so critical to the converter performance that intermediate test setups are built to validate the analytical approach and optimization procedures. Finally, we detail the capacitor and power semiconductor selection to complete the design analysis of this demanding wide-input-voltage range, high-output-current, PCB-integrated DC/DC converter.

2.1. Topology, Gain Analysis, and Control

As discussed in Section 1, the challenge is to combine the controllability of buck-based converters, which enables a wide-input-voltage range, with the high efficiency of LLC-based resonant topologies that feature soft-switching (and specifically zero-voltage-switching, or ZVS) across the full load and voltage ranges.

2.1.1. Topology

The topology challenges are driven by the combination of wide-input-voltage range (needed for hold-up time requirements) and complete soft-switching, as discussed in Section 1. We seek a low-complexity topology and control scheme, which eliminates approaches such as (i) DCX transformers, which require pre-regulation to fix the input voltage to the DC/DC module [5], (ii) additional hold-up time extensions circuits, which

require a full additional converter module [6], and (iii) reverse-feeding for hold-up time, which adds significant control complexity to the DC/DC module [7]. Instead, we aim to use a soft-switched LLC approach that can be controlled—with minimal complexity—across a wide gain range while maintaining soft-switching, and draw inspiration from matrix transformers used in server power supplies (e.g., [14]) to divide the high output current among multiple windings and rectifiers.

A full-bridge topology, as shown in Figure 2a, is chosen to excite the primary-side resonant tank. Relative to the half-bridge topology, the full-bridge has half of the primary-side current for a given power (with a tank excitation of $\pm v_{dc}$, rather than $\pm\frac{1}{2}v_{dc}$ for the half-bridge) and an additional control variable in the phase-shift between the two bridge legs, during which a variable-length voltage of 0 V can be applied to the tank. A center-tapped synchronous rectifier is selected for the secondary side, a topology that features a low semiconductor count, zero-voltage-switching, and no high-current output inductor. The equivalent circuit is shown in Figure 2b, including the LLC tank (C_r, L_r, and L_m), the reflected, equivalent load resistance (R_p), and the fundamental of the tank excitation (v_{AB}). The proposed converter's footprint is introduced in Figure 2c, where the matrix transformer with integrated synchronous rectifiers and output capacitors is preliminary built as a square block that sets the converter's width (w) and height (h). The PCB inductor should also be square and therefore, together with the primary-side semiconductors and control circuitry, defines the footprint's length (l).

2.1.2. Gain

For LLC converters, the fundamental-harmonic approximation (FHA) is typically used [23,24] to describe the gain, or the output-to-input voltage ratio (v_p/v_{AB}), as a function of the control variable: switching frequency (f_s). The gain as a function of switching frequency (normalized by the transformer turns ratio, n) is shown in Figure 3, where the FHA is compared to the exact solution obtained through circuit simulation for the proposed design parameters. The FHA is used primarily for the design of the unity gain point and to assess the gain in the boost region, with margin implicit because the actual gain under boost conditions is always higher than that predicted by the FHA (as shown in Figure 3). Under the FHA, the gain can be approximated as:

$$\frac{nV_o}{v_{dc}} = \frac{(m-1)\left(\frac{f_s}{f_r}\right)^2}{\sqrt{\left[m\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2 + Q^2(m-1)^2\left(\frac{f_s}{f_r}\right)^2\left[\left(\frac{f_s}{f_r}\right)^2 - 1\right]^2}} \tag{1}$$

$$f_r = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{2}$$

$$m = 1 + \frac{L_m}{L_r} \tag{3}$$

$$Q = \frac{Z_r}{R_p} \tag{4}$$

$$Z_r = \sqrt{\frac{L_r}{C_r}} \tag{5}$$

$$R_p = \frac{8n^2}{\pi^2}\frac{V_o^2}{P_o}. \tag{6}$$

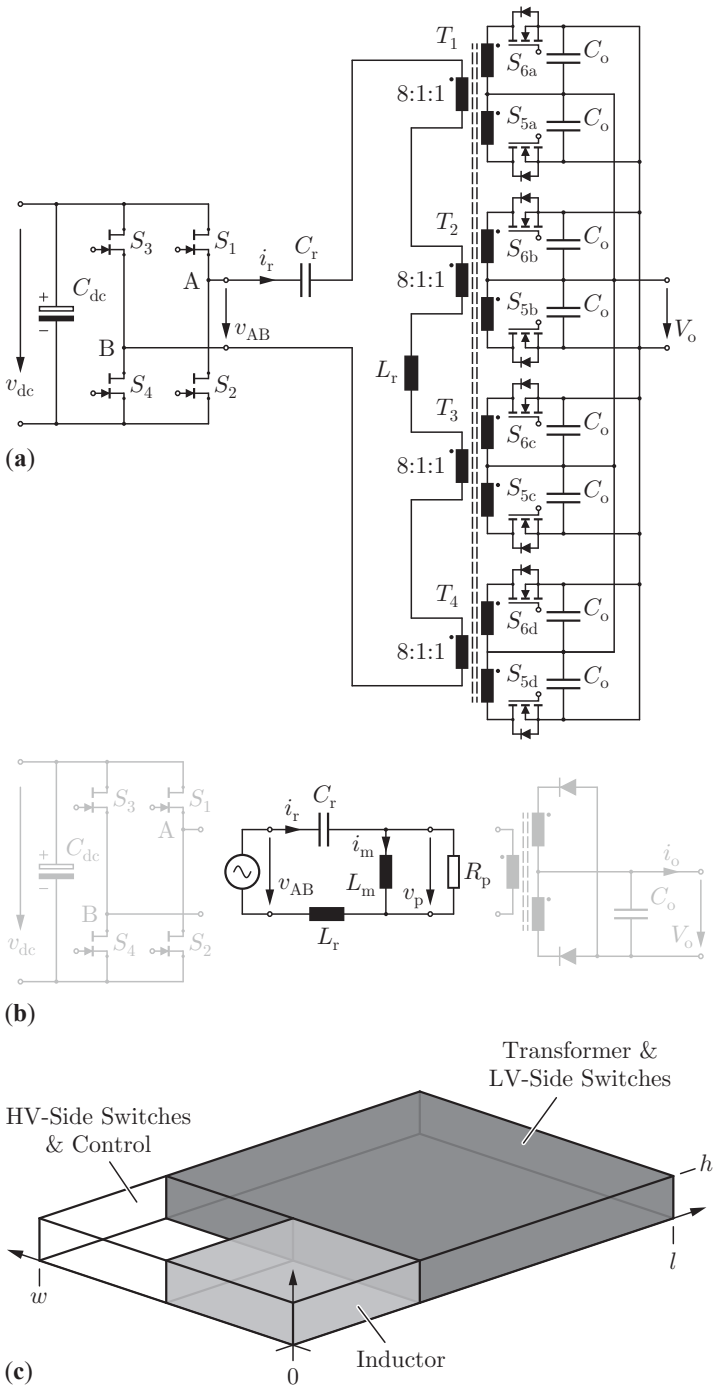

Figure 2. (**a**) Power circuit of the proposed DC/DC converter featuring GaN devices for the primary-side full-bridge, power MOSFETs operating as synchronous rectifiers on the secondary-side, and a series-input, paralleled-output, center-tapped matrix transformer. The converter operates resonantly and has the simplified circuit shown in (**b**), where the fundamental-harmonic-approximation may be used to capture the fundamental component of switched waveforms. (**c**) Proposed layout with matrix transformer, synchronous rectifiers and output capacitors as the main block defining the converter's width (w) and height (h), and the PCB inductor and primary-side full-bridge fixing the footprint's length (l).

Each parameter relates to a particular design constraint: the transformer turns ratio, n, defines the operation mode for the converter (buck, boost, or both), L_m restricts the maximum gain, L_r defines the selectivity of the tank [25] and therefore the required switching

frequency range for a given gain, and C_r is used to tune the desired resonant frequency. Each of these parameters, though, also has constraints on its selected value: n must be a multiple of the number of output stages (secondary transformers) for symmetry, L_r must be optimized for low volume, C_r must have a withstand voltage that is achievable with commercially-available capacitors, and L_m should be large to minimize the magnetizing current and the associated conduction losses.

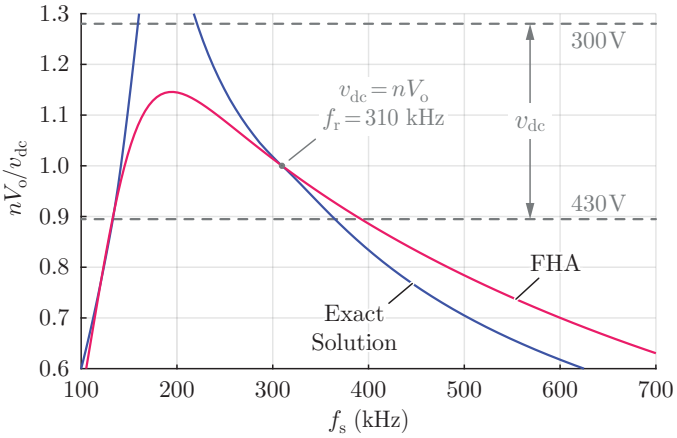

Figure 3. Graphical description of the output-to-input conversion ratio (normalized by the transformer turns ratio n) as a function of the switching frequency (control variable). The exact solution, obtained through circuit simulation, is compared to the fundamental-harmonic-approximation (FHA), where we see that the the FHA captures the correct monotonic behavior of the gain function. For the given v_{dc} range (300 V–430 V) and the parameters selected in Section 2.1, the converter operates from 210 kHz to 350 kHz.

Here, we know that a combination of buck and boost modes will be required to achieve the wide-input-voltage range, and the nominal input voltage of $v_{dc} = 400$ V is placed closed to the resonant frequency, where $f_s = f_r$ and $nV_o/v_{dc} = 1$ (see (1)). This results in $n = v_{dc}/V_o = 400\,\text{V}/12\,\text{V} = 33.33$, with $n = 32$ chosen for a symmetric design of the matrix transformer ($nV_o = 384$ V). From here, $L_r = 24$ µH is selected to compromise between inductor volume and the maximum operating frequency at light load (with the inductor design detailed in Section 2.3), mandating $L_m = 110$ µH to achieve the maximum gain at the minimum input voltage of $v_{dc} = 300$ V. A resonant frequency of 310 kHz is selected to balance the demanding efficiency and power density metrics of Table 1, which results in $C_r = 11$ nF. This design achieves full ZVS at all load and input-voltage conditions, a requirement to approach the required metrics—a hard-switching half-bridge employing *IGLD60R070D1* GaN HEMTs at $v_{dc} = 400$ V and 310 kHz would generate switching losses of one third of the allowable losses in the *complete DC/DC converter* for 96 % efficiency at 50 % load!

2.1.3. Control

Finally, returning to the goal of a simplicity of control that approaches that of buck-based converters, we propose a hybrid control loop and scheme (shown in Figure 4). Variable switching frequency control in continuous conduction mode (with the design tradeoffs between boundary and continuous conduction mode detailed in [26]) is implemented based on a comparison between the measured output voltage and requested output voltage, with the gain monotonic above the peak frequency around 200 kHz (see Figure 3). An off-the-shelf gate-driver IC with an embedded dead-time generator drives the GaN full-bridge ($g_1 - g_4$) with the corresponding PWM signals from the MCU ($s_1 - s_4$). A digital PI controller (C_{PI}) drives the sensed output voltage (V_o) to the reference value (V_o*) by adjusting the period of the MCU timer to trigger $s_1 - s_4$. When the control variable (u) has a lower value than the minimum user-defined switching period (per), the control leaves

continuous conduction mode (CCM, Figure 4b) and enters discontinuous conduction mode (DCM, Figure 4c), where the frequency is now fixed and a phase shift between s_1/s_2 and s_3/s_4 is introduced. This simple control scheme achieves the wide-input-voltage range and complete ZVS with only an isolated low-voltage measurement, a 12 V-to-3.3 V auxiliary supply, a hardware-implemented dead-time generator, and the 32-pin ST Arm Cortex M4 as the MCU.

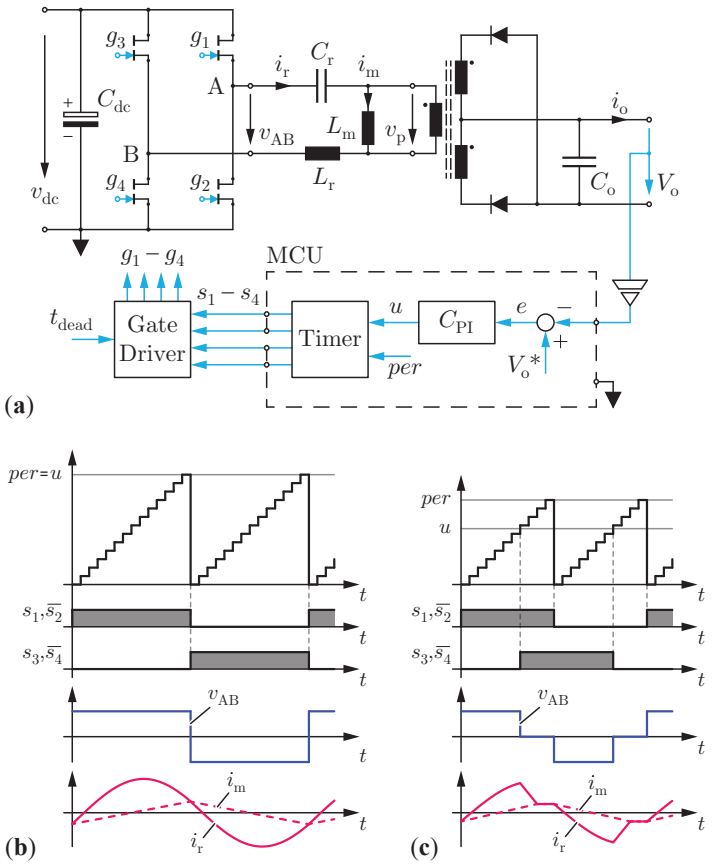

Figure 4. (**a**) Proposed control topology for the DC/DC converter, with output-voltage regulation by variable frequency using only an isolated low-voltage measurement and a low-cost, 32-pin ST Arm Cortex M4 as the MCU. (**b**) Continuous conduction mode (CCM) operation, where the digital PI controller adjusts the period of the MCU timer to trigger $s_1 - s_4$. (**c**) When the control variable (u) is lower than the minimum (user-defined) switching period (*per*), the converter enters discontinuous conduction mode (DCM), with a fixed frequency and a variable phase-shift to control the output voltage to the reference value (V_o*).

2.2. PCB-Integrated Transformer

With the topology, control techniques, and gain range determined, we turn to the design of the passive components. With 125 A at the 12 V output and the automated manufacturing requirement for full PCB integration, the multi-output transformer requires an ultra-low AC-to-DC resistance ratio (R_{ac}/R_{dc}), high copper area within the constraints of the PCB geometry, and a tight, compact layout with the synchronous rectifier. The multi-output matrix transformer approach for high-current, low-voltage outputs is known from server power supplies (e.g., [17]), but does not achieve ideal flux balancing among multiple paralleled outputs [26,27]. Here, we expand on the novel snake-core transformer concept, implementing a compact, low-loss, and balanced transformer that achieves perfect current sharing among one or many modules (as showcased later, in Section 5).

Any multi-output transformer, including the snake-core transformer, with four sub-transformers (see Figure 2a) benefits more from the PCB integration if built with side

symmetry, i.e., in a squared shape, as proposed in Figure 2c. This allows compactness of PCB windings and the shortest path for the magnetic flux (lower core losses). The transformer's side length and height are defined by the given values of width (w) and height (h) of the converter, previously specified in Table 1.

2.2.1. Winding Optimization and Losses

Firstly, the number of turns for the secondary winding (N_s) is optimized. With the winding geometry parameters shown in Figure 5a, the current density in the secondary winding is:

$$\hat{J} = \frac{\pi I_o N_s}{2A_w} \tag{7}$$

and the flux density in the core is:

$$\hat{B} = \frac{V_o}{4f_s A_c N_s}. \tag{8}$$

With the high output current requirement, a single turn ($N_s = 1$) is optimal for each secondary-side winding, with winding loss minimized at the expense of increased core loss. The optimal number of sub-transformers is selected to balance the copper and core losses. We eliminate the choices with an odd number of secondary windings, which would yield an asymmetrical structure, a complex core shape, or much higher core losses. 1 or 2 sub-transformers results in much higher copper losses, while 8 sub-transformers would yield a complicated core structure with high core losses. Therefore, for the particular constraints of this design—and especially around PCB integration, which limits the available copper thickness—a proper copper-to-core loss ratio is achieved with 4 sub-transformers, as shown later with experimental results.

This multi-output, matrix structure with 4 paralleled outputs reduces the copper loss by a factor of 4 over a single output (again at the cost of increased core losses) with the same footprint area for the secondary-side winding (A_t), as the current density reduces by a factor of 2 (see Figure 5b). Ultimately, the optimal A_w-to-A_c ratio between winding window area and core cross-section area must be selected based on a Pareto-optimization from copper and core loss models, which are developed and detailed later in this section.

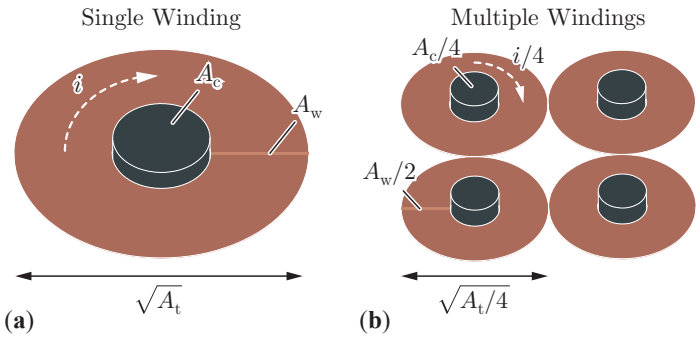

Figure 5. (**a**) Illustrative scheme of a PCB-integrated, single-turn secondary-side winding with A_w window area, A_c core cross-section area, A_t total footprint area, and current i. (**b**) Winding-loss minimization at the expense of increased core loss by means of a multi-output (matrix) structure with paralleled windings that reduces the current density by a factor of 2 for a fixed total footprint area A_t and fixed current i.

The high-current outputs must then be tightly-integrated into the remainder of the converter design. The transformer configuration, layer stackup, and secondary-side layout is detailed in Figure 6. In Figure 6a, a cutaway 3-D view shows the secondary-side semiconductors directly on top of the low-voltage windings ("LV Wind") for low termination

losses, an adjacent output capacitance (C_o) to minimize the commutation loop, and the full-bridge excitation input and chain through L_r to the high-voltage winding ("HV Wind"). The core configuration is shown in Figure 6b, with the losses and design detailed in the next sub-section. Figure 6c shows the vertical stackup and Figure 6d shows the layer-by-layer copper for the 10-layer, 2.4 mm PCB that can be fabricated using standard processes, including the low-voltage, high-current layers of TL/L2 and L9/BL, the high-voltage layers of L5/L6, and the shielding layers of L3 and L8.

The shielding layers (connected to v_{dc}-) are included to minimize the capacitance between the high-voltage and low-voltage sides of the transformer; these shielding layers, however, add common-mode capacitance that appears between the high-voltage excitation and high-voltage ground, or, analyzing the AC-equivalent circuit, add to the C_{oss} of the high-voltage switches. In order to reduce this undesired parasitic capacitance, layers L4 and L7 have been removed from the transformer's layout, increasing the distances between L5/L6 and L3/L8. From the geometry and the permittivity of FR4 ($\epsilon_r = 4.5$), we calculate $C_{\text{pri-shi}} = 550\,\text{pF}$ and measure $C_{\text{pri-shi}} = 554\,\text{pF}$ (with the bridge-legs shorted together, measured to high-voltage ground). Despite the removal of layers L4/L7, this is still a significant contribution to the C_{oss} of the selected high-voltage GaN switches and must be included in the ZVS and loss analyses.

The primary-side winding is then designed with the configuration shown in Figure 6d, with high-voltage windings around each core leg for high coupling and a balanced flux (design detailed in [27]). The total DC resistance of each multi-turn winding is:

$$R = \sum_{i=0}^{k-1} \frac{2\pi}{\sigma h_{\text{Cu}} \ln\left(r_{(\text{i}+1)}/r_{(\text{i})}\right)}, \tag{9}$$

with the optimal turn radii (see Figure 7a), adapted from [17]) as:

$$r_{(\text{i})} = \sqrt[k]{r_0^{(\text{k-i})} r_{\text{k}}^{(\text{i})}}, \tag{10}$$

where k is the number of turns per layer and per sub-transformer in the matrix structure. This optimized design is implemented for the high-voltage side windings to achieve the turns ratio (with $N_s = 1$) of $n = 32$ selected in Section 2.1, which leads to $k = 4$: 32 turns implemented in 2 PCB layers and wound around the 4 core limbs (4 sub-transformers, $T_1 - T_4$ in Figure 2a).

With the winding a critical driver of efficiency and losses, a test setup is built to validate the spiral radii optimization and expected winding resistances. An impedance analyzer in the circuit of Figure 7c measures the transformer impedance (Z_p) across frequency from the primary-side terminals with short-circuited secondary-side windings for two layer configurations: (i) both primary (HV) and secondary-side (LV) windings are built with the standard 2 oz copper thickness of 70 µm and (ii) 270 µm LV windings for reduced conduction losses. The results (shown as AC-to-DC resistance ratio) are reported in Figure 7b, with the theoretical approach well-validated by the experimental results. The measured R_{ac}/R_{dc} values across frequency are modeled by empirical linear functions (dashed lines) for later use in the winding resistance calculation.

With this same test setup, the calculated resistances of the primary and secondary windings are compared to the measured values in Table 3. Across the complete operating range of frequency, the predicted current-weighted sum of the primary and secondary resistance ($R_{\text{prim}} + n^2 R_{\text{sec}}$) is within 2 % of the measured value, indicating precise loss models for the windings that correctly describe the implemented PCB-integrated transformer and the frequency-dependent effects. The resistance of layers L2 and L9—that connect all sub-transformers in parallel (see Figure 6d)—was obtained by FEM simulations (COMSOL Multiphysics 5.4) with an error between measured and FEM-calculated values under 2 % (cf. Table 3). With the winding optimized and the loss model validated, we move to the transformer core design and loss optimization.

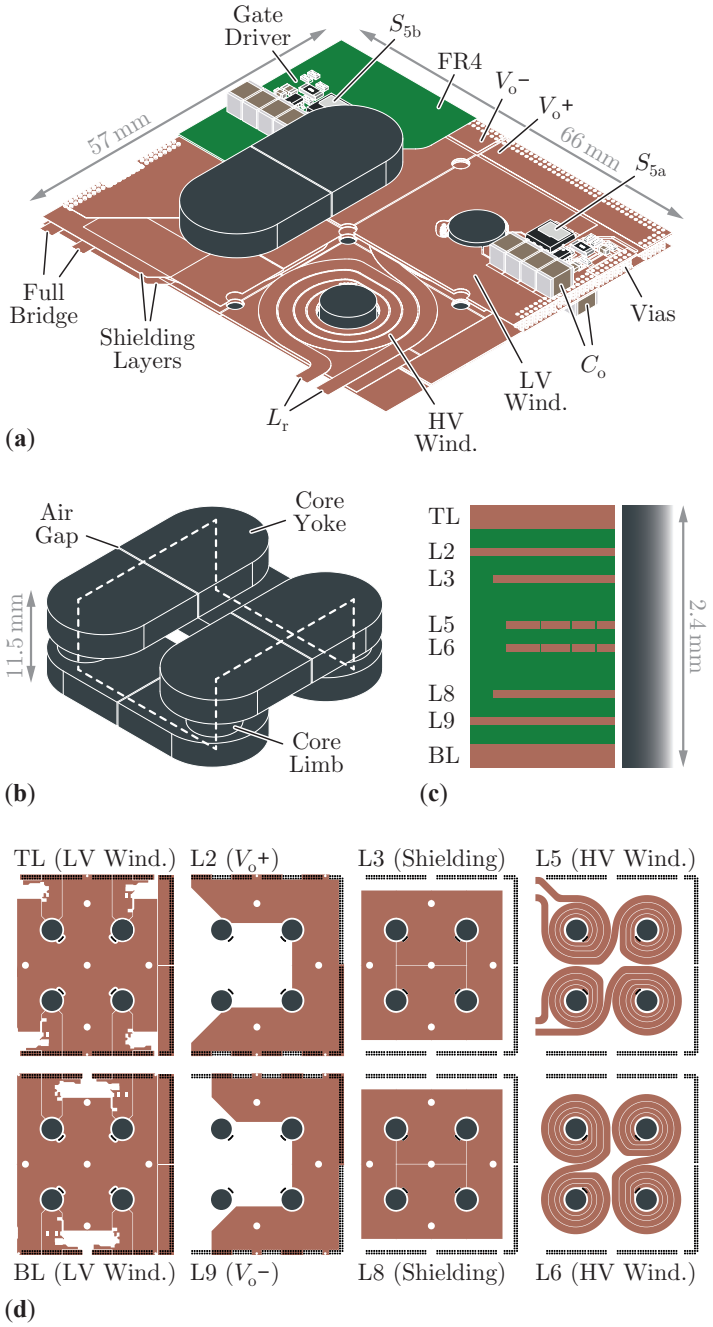

Figure 6. (**a**) The 3-D view of the snake-core matrix transformer with cutaway view of the PCB-integrated windings. The secondary-side semiconductors and output capacitors are placed directly above the low-voltage windings for low termination losses and minimization of commutation loops. (**b**) Snake core with the single path for magnetic flux highlighted with white dashed lines. (**c**) PCB layer stackup from the top (TL) to bottom layer (BL), with copper and isolation thicknesses proportional to the final design. (**d**) Layer-by-layer copper of the 10-layer layout, with layers L4/L7 empty to reduce parasitic capacitance.

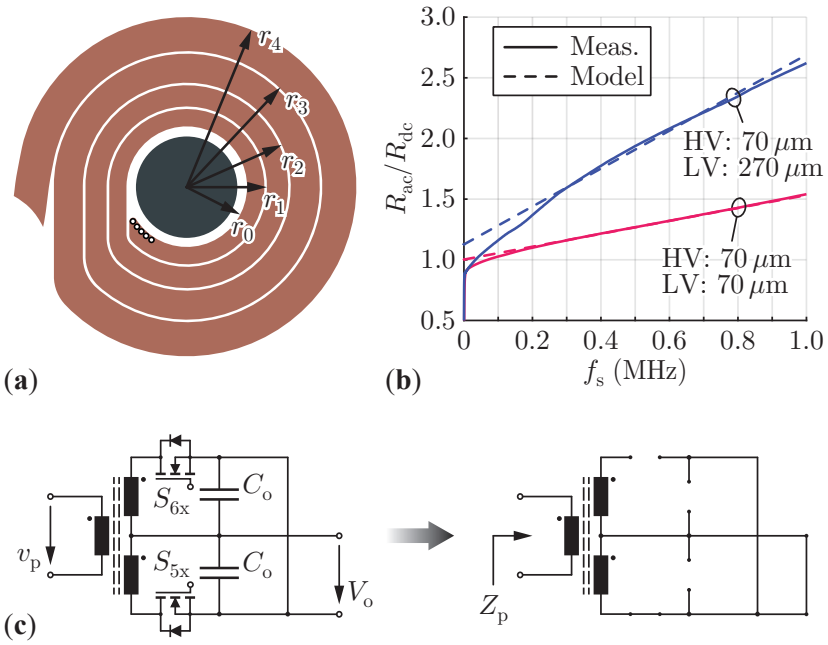

Figure 7. (**a**) Radii calculated from (10) for minimizing winding resistance. (**b**) Transformer AC-to-DC resistance ratio across frequency—measured as shown in (**c**)—with secondary-side short-circuited for two copper-thickness arrangements: 70 µm primary (HV) and 70 µm secondary-side (LV) windings, or 70 µm HV and 270 µm LV windings (with 0.2 mm copper foils soldered onto the 70 µm LV windings for experimental results). (**c**) Measurement technique for transformer resistance measurements, with measurement opens and shorts highlighted at right.

Table 3. Comparison between predicted and measured winding losses for the PCB-integrated transformer. All parameters at $T = 25\,°C$.

	Freq. (kHz)	R_{calc} **(kHz)**	R_{meas} **(mΩ)**	**Error (%)**
R_{prim}	DC	244.2	256.5	−4.8
R_{sec}	DC	0.2085	0.2166	−3.7
$R_{prim} + n^2 R_{sec}$	300	755.2	758.0	−0.4
$R_{prim} + n^2 R_{sec}$	500	892.5	906.6	−1.6
$R_{prim} + n^2 R_{sec}$	700	1030	1027	0.3
R_{L2+L9}	DC	0.03622	0.03554	1.9

2.2.2. Core Optimization and Losses

The matrix transformer is implemented with the snake-core proposed in [27] and expanded upon in [26], where the winding configuration—with a single, deterministic flux path through the high-permeability ferrite (TDK N49)—guarantees well-balanced flux among the paralleled secondary windings. The core configuration is shown in Figure 6b, with cylindrical through-PCB limbs to avoid current crowding on windings due to sharp edges, low-profile yokes following components' height, and total required air gap distributed among core yokes, calculated as:

$$l_g = \frac{\mu_0 A_{c,yoke}}{n^2 L_m}. \tag{11}$$

The core is built with different cross-sectional areas for the yokes and for the through-PCB limbs (see Table 4), with $A_{c,limb}$ selected to optimize core and winding losses for a fixed total transformer area (A_t)—Pareto optimization of Section 2.2.3—and $A_{c,yoke}$ made as large as the combination of A_t and the specified converter height would allow. We recall

that $L_m = 110\,\mu H$ and $n = 32$ were selected in Section 2.1 to meet the gain and voltage range specifications, yielding a total air gap of $l_g = 0.83\,mm$.

Table 4. Design characteristics of the optimized transformer and inductor.

	Transformer	**Inductor**
Winding width	8.6 mm	2.2 mm
Limb area ($A_{c,limb}$)	48 mm^2	36 mm^2
Yoke area * ($A_{c,yoke}$)	71 mm^2	149 mm^2
Air-gap length (l_g)	0.83 mm	0.33 mm

* at the air gap.

Eddy-current losses and hysteresis losses are included in the core loss model. The flux density in the transformer core at a given operating point is given by (8), with the yoke and limb flux densities considered separately as their cross-sectional areas are different (see Table 4), resulting in $B_{limb} = 196\,mT$ and $B_{yoke} = 143\,mT$. The losses in each piece of the snake core are then summed for the total core losses. With the flux density known, the eddy current losses are then:

$$P_{eddy} = V_c \frac{\pi f_s^2 \hat{B}^2 A_c}{4\rho}, \tag{12}$$

with $\rho = 17\,m\,\Omega$ being the N49-ferrite resistivity, and V_c the volume of each transformer piece. Hysteresis loss (P_{hyst}) also scales with V_c and is modeled as a function (P_v) of frequency (f_s), flux density ($\hat{B}$) and temperature (T):

$$P_{hyst} = V_c P_v \tag{13}$$

$$P_v = f(f_s, \hat{B}, T) \tag{14}$$

based on the manufacturer's loss data (see Figure 8). Although the flux is triangular, modeling the hysteresis loss from a sinusoidal excitation is used as a reasonable and simplifying approximation [28].

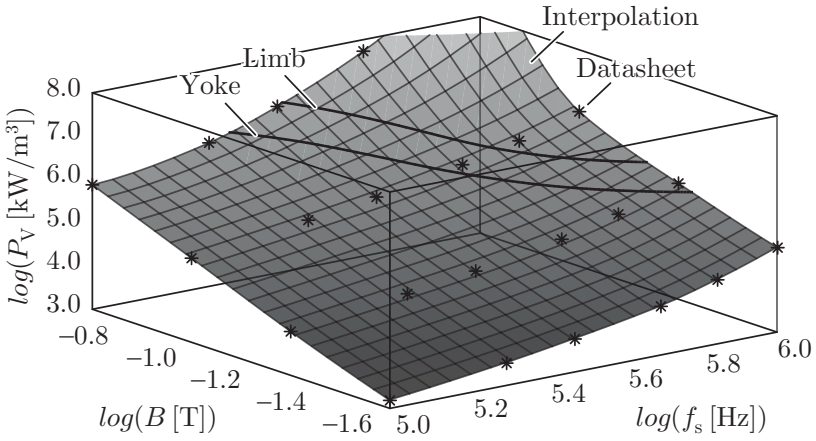

Figure 8. N49-ferrite hysteric losses (volumetric) as a function of flux density and frequency (axes in log scale). Stars are datasheet-given values, which are interpolated as inputs into continuous loss models. The frequency-dependent limb and yoke fluxes are calculated using (8) and shown with black lines on the top of the interpolation surface, indicating that core losses will decrease at higher operating frequencies due to the lower flux density.

To validate the model and the manufacturer's measurements, measured core losses with varying flux amplitude are recorded in a calorimetric chamber fixed at 35 °C using

the methodology outlined in [29] (which has a maximum loss error of less than 0.5 W). The chamber—or ambient—temperature vary from application to application (can be even cooler in datacenter racks with air-conditioning or water cooling), so the key metric considered here is the temperature on the core's surface, monitored to correctly calculate losses using the derived models. The comparison is detailed in Table 5, with the measurements matching the calculation within 10 % across all measured operating points. With the core loss model validated, we move to a Pareto optimization between transformer footprint area and losses.

Table 5. Comparison between predicted and calorimetrically-measured core losses for the PCB-integrated transformer.

	#1	#2	#3	#4
$B_{\mathbf{limb}}$ (T)	0.156	0.166	0.176	0.149
$B_{\mathbf{yoke}}$ (T)	0.113	0.121	0.129	0.148
$T_{\mathbf{core}}$ (°C)	85.9	92.4	103	105
$P_{\mathbf{hyst,limb,calc}}$ (W)	1.01	1.64	2.77	1.73
$P_{\mathbf{hyst,yoke,calc}}$ (W)	3.99	5.67	8.99	17.1
$P_{\mathbf{eddy,limb,calc}}$ (W)	0.0033	0.0038	0.0043	0.0057
$P_{\mathbf{eddy,yoke,calc}}$ (W)	0.0344	0.0391	0.0442	0.0581
$P_{\mathbf{total,calc}}$ (W)	5.04	7.45	11.8	18.9
$P_{\mathbf{total,meas}}$ (W)	4.61	6.91	10.7	17.5
Error (%)	9.3	7.8	10.3	8.0

2.2.3. Pareto Optimization and Losses

For the height-constrained transformer of Figure 2c, the total footprint area can be increased or decreased with an associated improvement or penalty on losses. Further, the area allocated to copper and magnetic core trades off winding and core losses, and a Pareto optimization is performed to select the loss-optimal design for each candidate footprint. The core design tradeoff between total transformer losses and footprint area is shown in Figure 9a for nominal load and Figure 9b for 50 % load. The designs that form the Pareto front shift materially between the two load conditions, with the selected design (footprint area of 26.4 cm^2 and full load losses of 29.2 W) representing a Pareto-optimal design at full load and a sub-optimal design at 50 % load. This indicates that the transformer design is one knob that can be tweaked to optimize for efficiency at different load conditions. Here we proceed with the Pareto-optimal design at the nominal load condition—as the whole system was designed considering full-load metrics as a first (conservative) design constraint—with the selected design marked in Figure 9a,b and detailed in Table 4. In Section 2.2, we show how selecting the optimal transformer 50 % load improves losses at light load and changes the shape of the efficiency curve.

The implemented copper and core for the PCB-integrated, snake-core transformer are shown in Figure 6b,d, respectively. With the transformer loss models proposed and validated, we move to the design and loss modeling for the PCB-integrated resonant inductor, L_r.

2.3. PCB-Integrated Inductor

Much like the transformer designed, optimized, and characterized in Section 2.2, the primary-side inductor must be PCB-integrated for compactness, manufacturability, and cost-effectiveness—but this comes with the penalty of increased losses relative to litz-wire inductors in the desired frequency range (100 kHz–1 MHz) [30]. This integration penalty—which is based on the lower fill factor, worse copper utilization (R_{ac}/R_{dc} ratio), and other geometric constraints of PCBs relative to litz wire—can be mitigated through the compensating-fringing-field concept introduced in [25], where skin and proximity effects in a PCB-based inductor are minimized by using the otherwise-parasitic fringing fields caused by the air gap in the magnetic core.

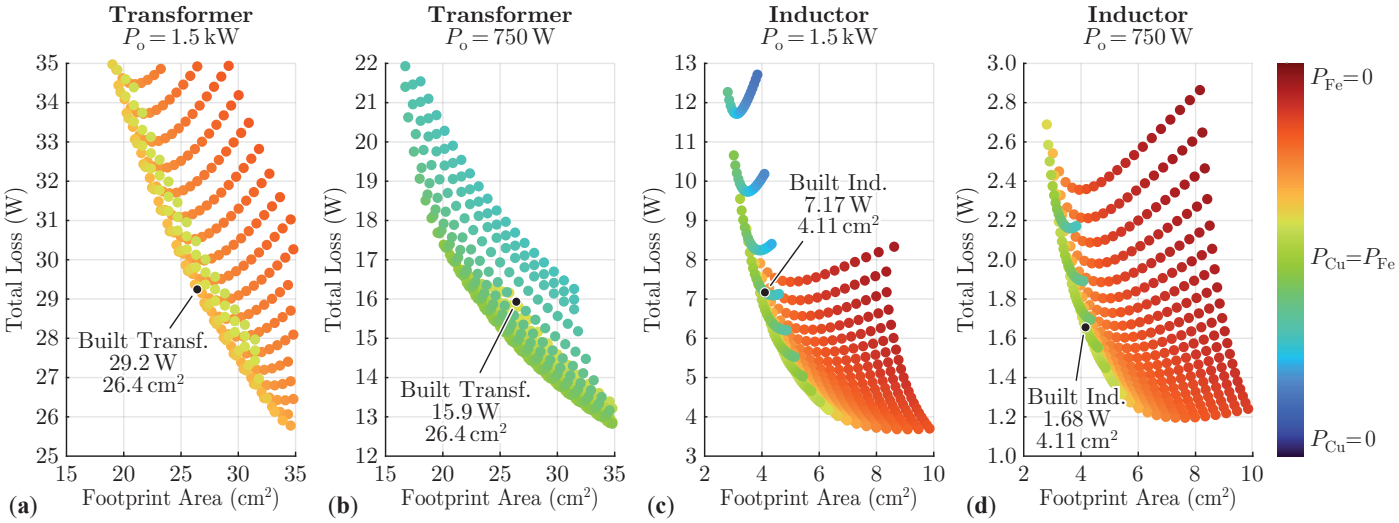

Figure 9. Pareto optimizations between total loss—sum of copper (P_{Cu}) and core (P_{Fe}) losses—and footprint area (directly related to volume) of the PCB-integrated (**a**,**b**) transformer and (**c**,**d**) inductor for (**a**,**c**) nominal and (**b**,**d**) 50 % load. The design spaces were defined by sweeping core radius and winding width values for each of the two components to trade off the winding and core area. Selected designs that were Pareto-optimized for nominal load ($P_o = 1.5\,kW$) are shown as black dots, with the design characteristics of Table 4. Note that the Pareto-optimal designs are constant between full and 50 % load for the inductor but change significantly for the transformer.

We reuse the loss models detailed in Section 2.2 and combine them with the fringing-field effects of [25] to arrive at the complete winding and core losses for the primary-side inductor, which is then Pareto-optimized for the selected value of $L_r = 24\,\mu H$ (driven by the desired gain ratio, as discussed in Section 2.1) between footprint area (directly related to volume) and total inductor losses. This optimization is shown in Figure 9c for nominal load and Figure 9d for 50 % load, where we find that, unlike the PCB-integrated transformer, the Pareto-front analysis is load-independent, with the map merely shifted down on the loss axis between nominal load and 50 % load. A footprint area of 4.11 cm^2 is selected for a primary-side inductor loss of 7.2 W at full load and 1.7 W at 50 % load. This selection represents a good trade-off between inductor footprint area and full-load losses—with enough space left for primary-side components and control circuitry (see Figure 2c), and the inductor already contributing to 12 % of total losses for a hypothetical full-load efficiency of 96 %.

The complete inductor, as implemented, is shown in Figure 10a, with a final footprint area slightly larger than the one Pareto-optimized to accommodate thermal interfaces [25]. Figure 10b shows the implemented layer-by-layer copper of the 10-layer PCB design. The selected design is marked in Figure 9c,d and detailed in Table 4.

We note here that some LLC converters utilize the leakage inductance of the transformer as the auxiliary inductance, but this approach (i) is not feasible with our required inductance of 24 µH and a PCB-integrated transformer, which has very high coupling (and accordingly low leakage inductance), (ii) would make the benefits of the fringing-field approach [25] difficult to achieve, and (iii) prevents the Pareto-optimization of the resonant inductor alone, leading to higher losses.

2.4. Capacitor and Power Semiconductor Selection

With the control, topology, and PCB-integrated magnetics designs finalized, we can move to the selection of the input, resonant, and output capacitors and the primary- and secondary-side power semiconductors. The loss contributions to our detailed model are outlined in the power semiconductor sections, while our calculations indicate that the losses from all of the capacitors are negligible.

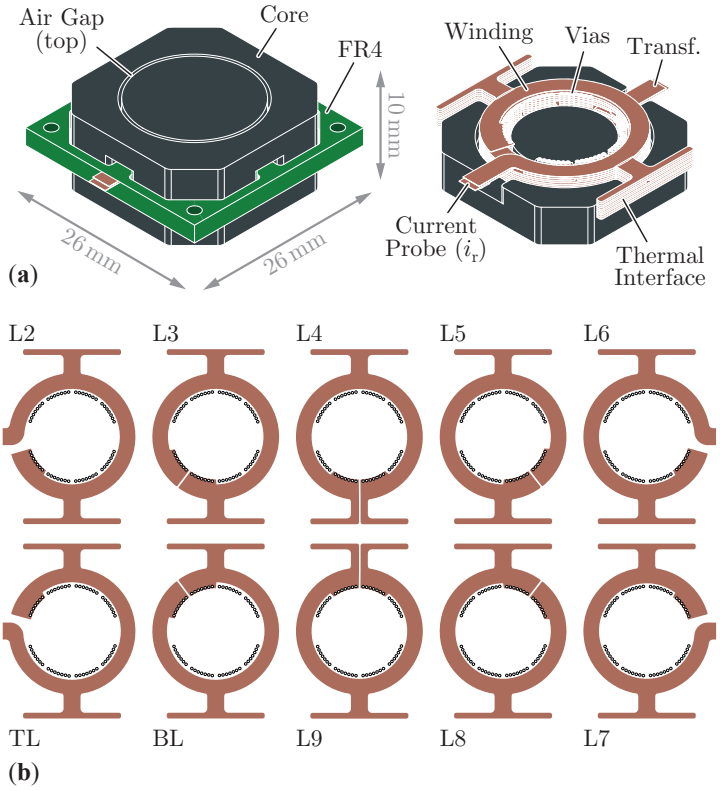

Figure 10. (**a**) The 3-D view of the primary-side inductor (L_r) with PCB-integrated windings schematically shown with cutaways. Winding heat is transferred by thermal interfaces to adjacent surfaces that can be thermally coupled to heat sinks for cooling. Following [25], air gaps are strategically placed above and underneath the windings to improve current distribution and boost efficiency. (**b**) Layer-by-layer copper of the 10-layer stackup.

2.4.1. Output Capacitor Selection

With four secondary-side sub-transformers and two windings per sub-transformer, the sheer quantity of output capacitors (eight groups) make their selection critical to the design of the converter. An analytical solution may be derived for the voltage ripple specification based on the converter parameters and the required output capacitance, as:

$$\Delta v_o = \frac{P_o}{C_o V_o}\left\{\frac{1}{2f_s}\cos\left[\sin^{-1}\left(\frac{2f_s}{\pi f_r}\right)\right] + \frac{1}{\pi f_r}\sin^{-1}\left(\frac{2f_s}{\pi f_r}\right) - \frac{1}{2f_r}\right\}. \tag{15}$$

With the output ripple specified as under 2 % in the worst-case, we select a total output capacitance of 640 µF, implemented as 4 20 µF (at 12 V) capacitors per group (*C4532X7R1C336M250KC*). This gives a worst-case full-power ripple of $\Delta v_o = 194\,\text{mV}$ ($f_s = 210\,\text{kHz}$, $v_{dc} = 300\,\text{V}$, $P_o = 1.5\,\text{kW}$) and a ripple of $\Delta v_o = 66.3\,\text{mV}$ at nominal operation ($f_s = 310\,\text{kHz}$, $v_{dc} = 400\,\text{V}$, $P_o = 1.5\,\text{kW}$).

2.4.2. Input Capacitor Selection

No analytical solution for calculating the input voltage ripple exists (the equation is transcendental), so the input capacitor value is selected from circuit simulations as $C_{dc} = 1\,\mu\text{F}$. We select four capacitors, each with $C_{dc} = 0.28\,\mu\text{F}$ at 400 V, to achieve this capacitance (*C5750X7T2W105K250KA*).

2.4.3. Resonant Capacitor Selection

As detailed in Section 2, the resonant capacitance is selected as $C_r = 11\,\text{nF}$ from the gain analysis. The resonant capacitor is implemented as 5 paralleled C0G capacitors, each contributing 2.2 nF (*CGA4F4C0G2W222J085AA*).

2.4.4. Primary-Side Semiconductors

The high-voltage power semiconductors must block up to the maximum input voltage of $v_{dc} = 430\,\text{V}$, and incur losses from conduction, resonant soft-switching, body-diode conduction, and gating, with the hard-switching contributions of Q_{oss} and VI overlap eliminated by achieving ZVS across the complete load and voltage ranges and by a fast-turn-off gate drive. To minimize the remaining loss contributions, we select the 600 V GaN HEMT *IGLD60R070D1*, with 70 mΩ nominal on-resistance and, like all GaN HEMTs, zero reverse-recovery losses. For the primary-side semiconductor modeling, the junction temperature is estimated based on load condition, with a linear spacing between 60 °C (full load) and 40 °C (10 % load). From here, the losses are straightforwardly calculated and the breakdown is reported in Section 3. *UCC21225A* gate drivers are used with bootstrap power supplies, common-mode chokes to reduce noise on these supplies, and a series capacitor to introduce a negative gate drive voltage.

2.4.5. Secondary-Side Semiconductors

The low-voltage switching stage incurs high currents and therefore must rectify synchronously, underscoring its importance to the total losses of the converter. The devices must withstand $2V_o = 24\,\text{V}$, and we select the 40 V Si MOSFET *TPW48004PL*, with a nominal on-resistance of 0.65 mΩ. The semiconductor junction temperature is again modeled based on load condition, with a linear spacing between 90 °C (full load) and 50 °C (10 % load). As we analyze in depth when searching for further improvements in Section 4, minimizing the delay of the synchronous turn-on is critical to minimizing secondary-side losses, and we use a dedicated synchronous rectifier IC (*NCP4306*) to drive the MOSFETs based on a direct v_{ds} measurement. This stage is supplied by the output voltage to fully decouple the primary and secondary sides of the converter. Again, these MOSFETs are operated under ZVS and ZCS (a natural condition of synchronous rectification) and therefore only incur conduction, body-diode, and gating losses, the contributions of which are detailed in the next section.

3. Hardware Prototype

The design detailed in Section 2 is fabricated as a 1.5 kW hardware demonstrator, and is shown in Figure 11 with the summary of the final design values and implementations given in Table 6. The DC/DC converter measures 96 mm by 66 mm by 11.5 mm, with the high-voltage switching cell highlighted in the top-right of Figure 11, the snake-core transformer in the center of the converter, and the high-current, low-voltage output to V_o in the bottom-left. This converter includes the detailed layouts of the PCB snake-core transformer (Figure 6d) and the PCB inductor L_r (Figure 10b).

Key operating waveforms are captured at nominal (Figure 12a) and 50 % (Figure 12b) load, indicating correct operation of both the high-voltage and low-voltage sides of the converter for a well-regulated output voltage of $V_o = 12\,\text{V}$. These measured waveforms show excellent agreement with circuit-simulation results, validating the model that is used as a waveform generator for the loss models. The selected control scheme maintains sinusoidal currents through the resonant network (shown with the i_r waveform captures) to minimize harmonic losses and simplify the frequency-dependent effects in the design, and soft-switching is achieved across the entire load range. The synchronous rectifier gate driver signals are shown in the bottom pane (g_5, g_6), where we see correct operation of the circuit with a simple zero-crossing detector—but an unmistakable (albeit short) time at the end of each conduction cycle (see the third pane, $v_{s,5}$ and $v_{s,6}$) where the paralleled body-diodes conduct rather than the MOSFETs. The effect of this timing mismatch sets a

loss minimum for the high-current rectification, the effects of which are investigated more deeply in Section 4.

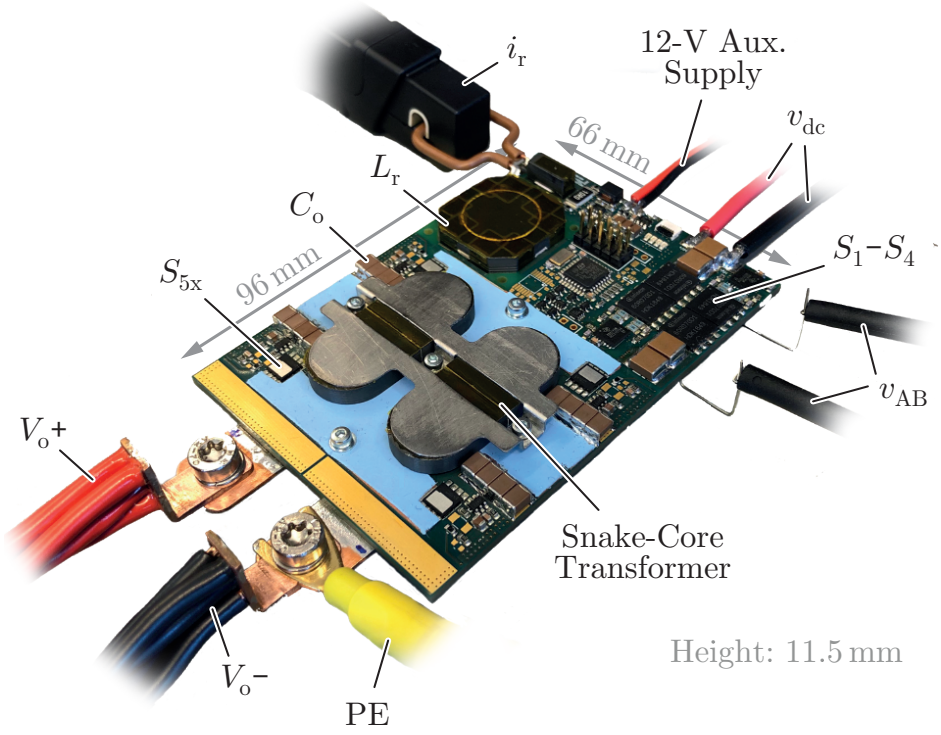

Figure 11. The 1.5 kW hardware demonstrator of the DC/DC resonant converter, measuring 96 mm × 66 mm × 11.5 mm. Key components and measurement devices are highlighted, with key values and implementations given in Table 6.

Table 6. Key design values and implementation for components in the 1.5 kW hardware demonstrator of Figure 11.

Parameter	Design Value	Implementation
$S_{1\text{-}4}$	–	600 V, 70 mΩ GaN HEMT *IGLD60R070D1*
$S_{1\text{-}4}$ gate drivers	–	*UCC21225A*
$S_{5,6}$	–	40 V, 0.65 mΩ Si MOSFET *TPW48004PL*
$S_{5,6}$ gate drivers	–	*NCP4306* and *UCC27511A*, $v_{gate} = 6$ V
L_r	24 µH	PCB-integrated, fringing-field concept [25]
C_{dc}	1 µF	4× 0.28 µF *C5750X7T2W105K250KA*
C_{out}	640 µF	32× 20 µF *C4532X7R1C336M250KC*
C_r	11 nF	5× 2.2 nF *CGA4F4C0G2W222J085AA*

The measured DC/DC efficiency, from $v_{dc} = 300$ V and $v_{dc} = 400$ V to $V_o = 12$ V, for the hardware demonstrator across output power is shown in Figure 13. The module delivers a flat and high efficiency above around 40 % of nominal load for $v_{dc} = 400$ V, with a maximum just below 96 % efficiency near 1 kW of output power. The detailed loss models developed for each component in Section 2 predict the complete converter efficiency quite accurately, with minute differences across most of the load range and less than 5 % of the loss not captured by the model at the largest variation between calculation and measurement (at nominal load). These component-level loss models, further, support a detailed breakdown of the losses that are shown for nominal and 50 % load in Figure 14.

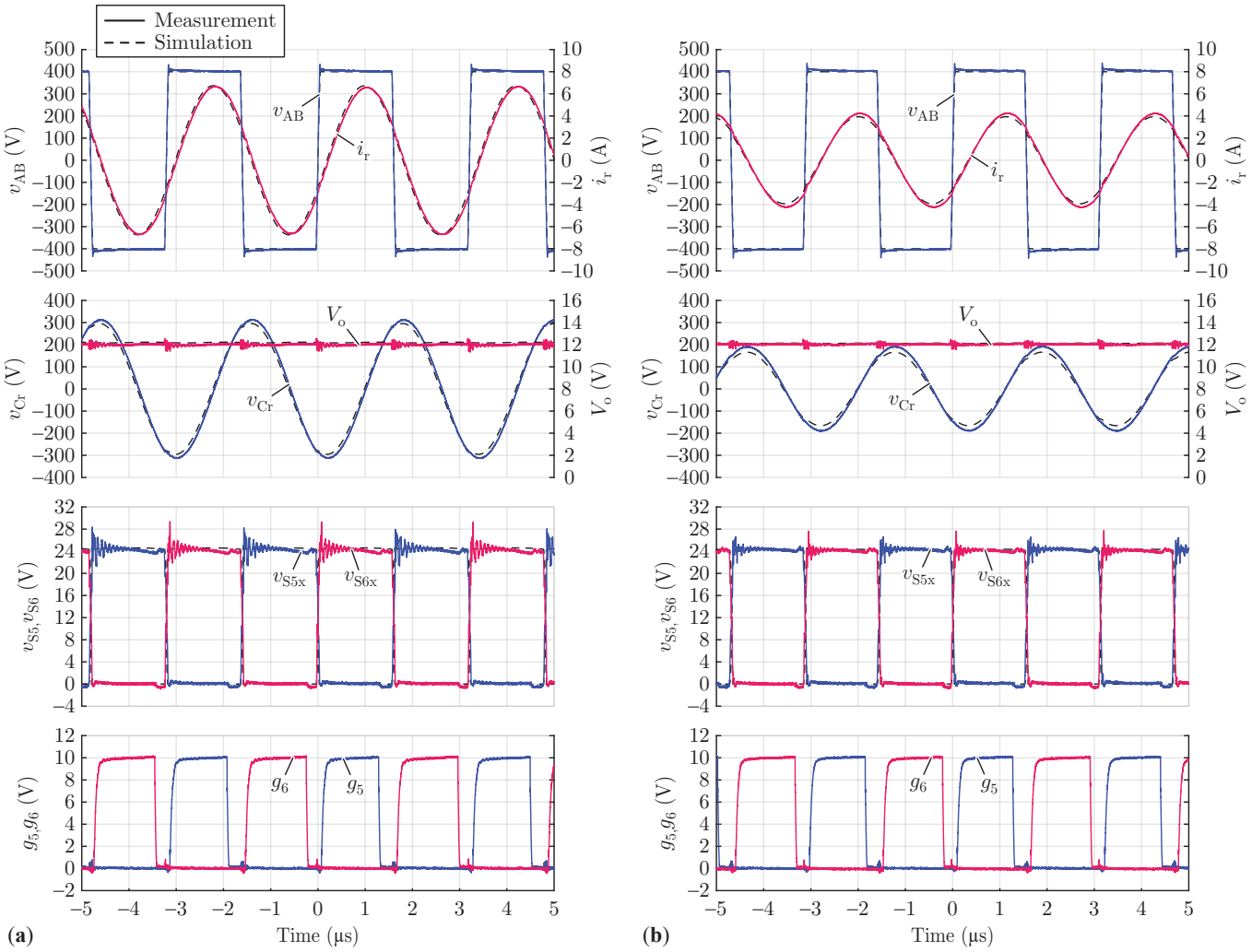

Figure 12. Key operating waveforms captured at (**a**) nominal and (**b**) 50 % load, demonstrating good agreement with circuit-simulation data (shown as dashed lines). Output voltage (V_o) is regulated at 12 V by controlling the switching frequency of v_{AB}. The sinusoidal shape of i_r minimizes harmonic losses, and synchronous rectification supports both ZVS and ZCS of the LV-side switches (drain-to-source voltages v_{S5x}/v_{S6x} commute naturally at zero current) and reduces body-diode losses by conducting most of the current through the MOSFET channel (gate signals g_5/g_6 are commanded after and before switching actions).

At full load (Figure 14a), the transformer accounts for over 40 % of the total losses, with the inductor, high-voltage logic, and GaN devices bringing the high-voltage losses to about 60 % of the total converter dissipation. The low-voltage loss breakdown, however, highlights the challenges of high-current outputs with high power density (and therefore high switching frequency). Firstly, the low-voltage tracks contribute 10 % of the losses alone, even with a careful design to maximize the copper and copper utilization in this path. Similarly, the synchronous rectifier diode alone accounts for 16.5 % of total converter losses, despite conducting for less than 10 % of the on-time! At high switching frequencies and high output currents, the speed of the sensing, control, and gating of the synchronous rectifier switches is a major performance driver, and Section 4 analyzes efficiency limits as this delay decreases.

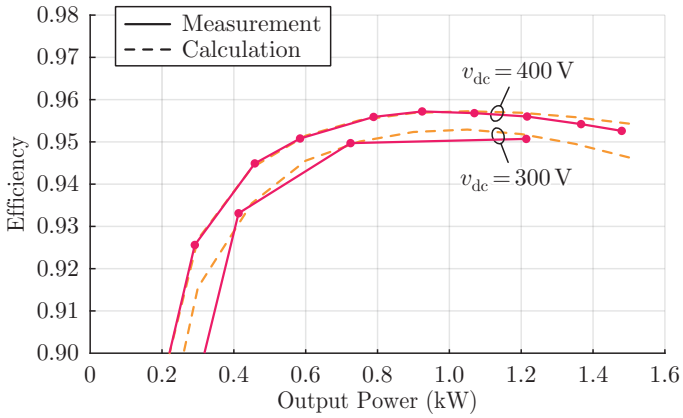

Figure 13. DC/DC calculated and electrically-measured efficiencies from input ($v_{dc} = 300\,V, 400\,V$) to output ($V_o = 12\,V$) at different load conditions and two input voltages, including all loss components.

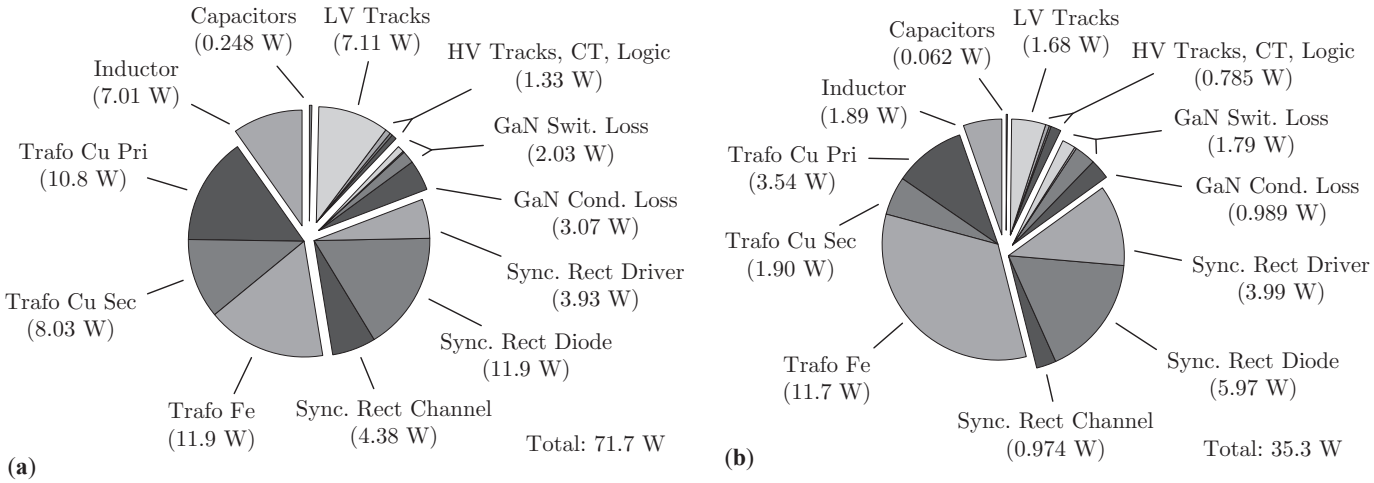

Figure 14. (**a**) Full- and (**b**) 50 %-load loss budgets for the DC/DC converter with $v_{dc} = 400\,V$ and $V_o = 12\,V$. Transformer, synchronous rectifiers and HV-side components/PCB tracks represent the three groups of loss contributors. Transformer losses accounts for 43 % and 49 % of the total losses at full and 50 % load, respectively. Synchronous rectification is the second element with highest loss, achieving nearly 30 % of the total losses in both load conditions.

At 50 % load (Figure 14b), as expected, the current-independent (or nearly current-independent) losses represent a larger fraction of the total loss budget, including the transformer core losses (33 % of total losses), the GaN switching losses, and the synchronous rectifier gating losses. The synchronous rectifier diode losses remain at around 1/6 of the total losses, with these VI losses simply related to the ratio of the forward drop to the output voltage and the percent of the period in which the diode conducts.

A thermal image of the converter at nominal load and nearly steady-state is shown in Figure 15. A small fan was used to blow air on the surface of the converter (air speed of approximately $1\,m\,s^{-1}$) and keep the temperature within limits. The high-current output results in a relatively-hot low-voltage side of the converter—with losses from the transformer winding, transformer core, low-voltage tracks, and synchronous rectifier—but the maximum temperature remains below 71 °C. The hottest components are the gate drivers for the synchronous rectifier switches, which each dissipates around 0.5 W in a small package that is located in a hot environment. In a commercial application, heat sinks should be installed to conduct heat from the hot surfaces of the transformer windings either onto a cooling plate or into air.

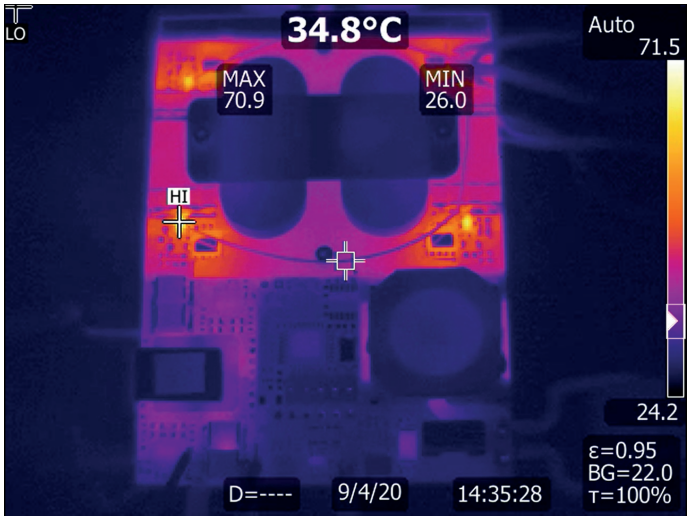

Figure 15. Thermal image of the converter at steady-state and $P_o = 1.5\,\text{kW}$ with forced cooling. The hottest component (71 °C) is the gate driver for the synchronous rectifier switches, which each dissipate around 0.5 W.

4. Efficiency Barriers

We combine simplified control techniques, novel PCB-integrated passive components, and detailed loss optimizations to showcase an efficient, power-dense, and wide-input-voltage-range DC/DC converter for industrial power supplies with stringent hold-up time and manufacturability requirements. This module achieves a flat efficiency curve with a peak of nearly 96 % and a power density of $337\,\text{W in}^{-3}$ with (i) only PCB-integrated magnetic components, (ii) soft-switching across the entirety of the operating envelope, and (iii) a wide-input-voltage range that achieves the hold-up time requirements while minimizing the volume of the DC-link bulk capacitor. Finally, the detailed loss models permit component- and converter-level optimizations, and we leverage these extensive models to identify the barriers to higher efficiency that may be overcome with a next-generation module. These improvements are evaluated in two distinct categories - firstly, we reevaluate operating parameters and converter design approaches, which may be optimized by the power electronics engineer. Secondly, we analyze what key component advances would improve efficiency, improvements that will likely be considered as *inputs* to the power electronics design.

Firstly, the selections of transformer turns ratio, switching frequency, and primary-side bridge configuration are revisited in Figure 16. The transformer turns ratio, we recall, determines the required gain range but also drives losses as its selection defines whether the converter nominally operates near resonance or away from resonance. Figure 16a confirms that $n = 32$ is the optimal choice for efficiency across load, with lower turn counts especially penalized as the load is increased through higher conduction losses. The nominal switching frequency, characterized by the tank resonant frequency, can also be optimized across load range, as shown in Figure 16b, where we see that increasing the resonant frequency to $f_r = 500\,\text{kHz}$ can eliminate around 10 % of the losses at 50 % load. These models, though, exclude the extra losses incurred by the non-idealities in synchronous rectification timing, when the body diode conducts, and $f_r = 300\,\text{kHz}$ remains the ideal nominal switching frequency when these losses are included. Finally, a half-bridge decreases the number of semiconductors relative to a full-bridge, accruing gains in both area and number of devices in the conduction path, but the full-bridge has a more flexible control scheme (CCM and DCM operation are both possible, as shown in Figure 4) and less primary-side current. The half-bridge efficiency is marginally higher at light load, as shown in Figure 16c, but the full-bridge outperforms on an efficiency basis above around 75 % load and improves the

control scheme. In all three cases, the converter-scale improvements tap out at around 96 % peak DC/DC efficiency, and we turn to explore component-level improvements to push down losses.

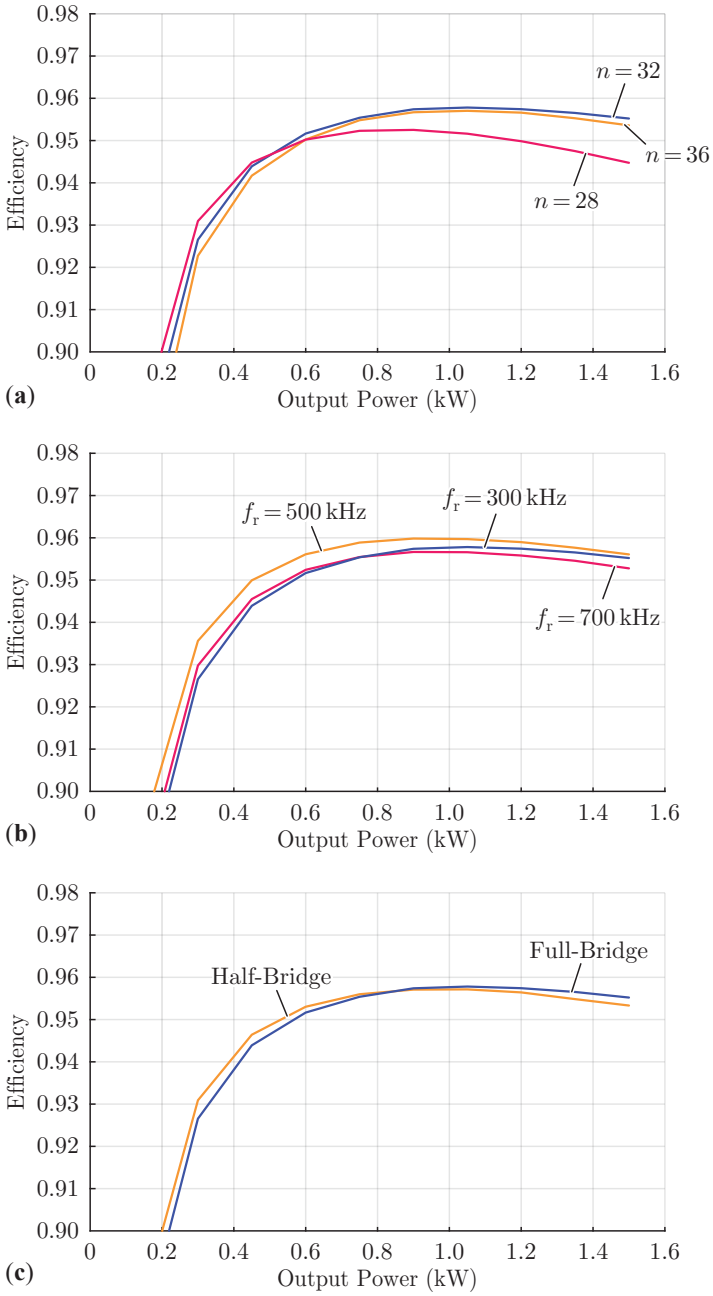

Figure 16. Calculated efficiencies at $v_{dc} = 400$ V and $V_o = 12$ V, highlighting optimal choices for (**a**) turns ratio ($n = 32$) and (**b**) resonant frequency ($f_r = 500$ kHz). Due to the non-ideal synchronous rectification, body-diode conduction losses increase at higher frequencies (practical behavior not captured by the loss models), which actually makes $f_r = 300$ kHz the best choice to maximize efficiency. (**c**) A HV half-bridge switching-stage (that prevents DCM operation) does not improve efficiency over the full-bridge, even though n is cut by half.

As we detail in Figure 14, the transformer and synchronous rectifier are the primary loss drivers across the load range, and are accordingly the components in which we first seek to reduce losses. Firstly, the transformer cross-sectional area can be increased in the limbs and yokes to lower the core losses at the expense of increased winding losses (with a

fixed total volume). This benefit is shown in Figure 17, which highlights the Pareto front for 50 % load, recalling from Figure 9b that the selected transformer was optimized at nominal load and was sub-optimal at light load. This design change increases the peak efficiency at light load, where core losses dominate over conduction-related losses, by up to 1 %, as shown with the case labeled (i) in Figure 18a.

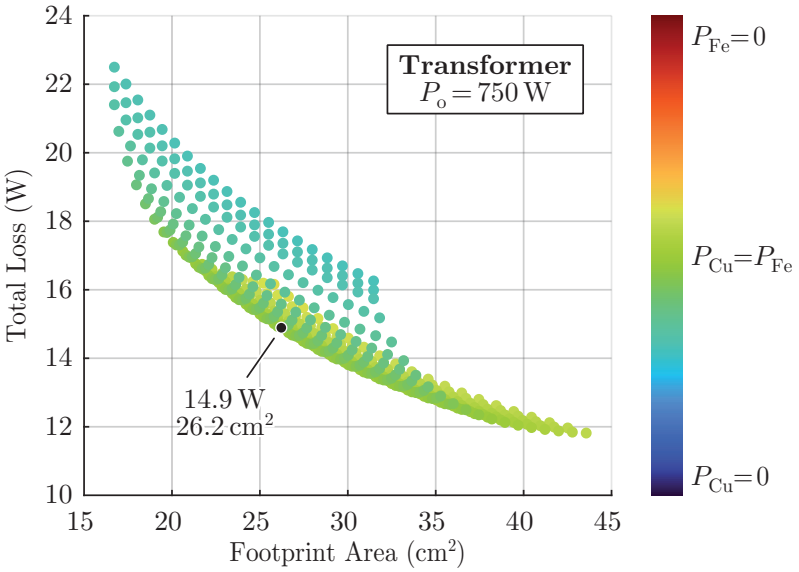

Figure 17. Transformer Pareto front optimized at 50 % load by increasing limb and yoke cross-sectional areas according to case (i) of Figure 18a, which shows that 8.11 W/6.59 W of core/winding losses is optimal on Figure 18b.

Even larger gains can be realized in the synchronous rectifier; replacing the low-voltage MOSFETs with the new 40 V MOSFET from Infineon, *IQE013N04LM6*, reduces the driver losses by 5×, from nearly 4 W to 0.8 W, by dropping the gate driver voltage from 12 V to 6 V and requiring a lower gating charge (recalling $P_{gate} = f_s C_{gate} V_{drive} V_{gate}$). This improvement is shown as case (ii) in Figure 18a. Finally, as discussed previously, reducing the body-diode conduction time significantly improves converter efficiency; cutting this time by 50 %, in combination with the other two improvements, pushes the efficiency over 96.5 %, as shown by case (iii). Close-to-ideal synchronous rectification, though, is difficult to achieve at high switching frequencies with existing discrete components; speeding this sense and actuation might require either integrated synchronous rectifier ICs or, at a minimum, Kelvin-source connections on high-current MOSFETs to support direct v_{ds} measurements. The loss breakdown at 50 % load with these three improvements is shown in Figure 18b, with the total losses reduced from 35.3 W (Figure 14b) to 26.4 W, driven by reductions in transformer core losses (3.6 W), synchronous rectifier gate driver losses (3.2 W), and synchronous rectifier body diode losses (4.5 W).

With the key module-level improvements characterized and identified—and, indeed, improvements identified that can eliminate 26 % of the total converter losses—we move to fabricate and characterize an improved 1.5 kW module in the next Section. With this improved demonstrator, we subsequently leverage the snake-core transformer to achieve ideal current sharing with two paralleled modules for an output power of 3 kW.

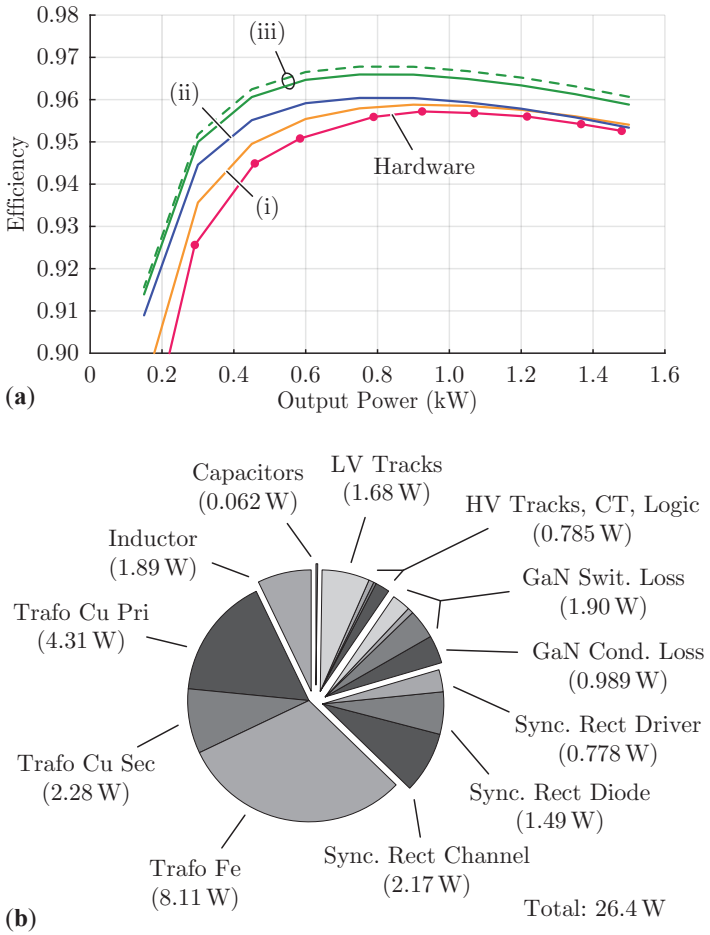

Figure 18. (**a**) Calculated efficiencies (i,ii,iii) as result of a series of improvements for comparison with the prototype's measured efficiency ("Hardware"): (i) larger limb and yoke cross-sectional areas for reduced core losses; (ii) new LV-side switch (*IQE013N04LM6*) with lower gate charge and triggered by a lower gate voltage using an LDO (6 V instead of 12 V); and (iii) 50 % lower body-diode conduction time (dashed line shows the ideal case of no body-diode conduction). (**b**) Loss budget of case (iii) at 50 % load.

5. Paralleled and Next-Generation DC/DC Modules

5.1. Next-Generation DC/DC Module

Firstly, a next-generation DC/DC module is fabricated with the critical changes proposed in Section 4 to improve efficiency. The updated module includes, with references to Figure 2 and a component summary in Table 7:

- New LV-side switches ($S_{5,6}$), with *IQE013N04LM6* featuring lower gate charge and driven by a 6 V gate voltage (supplied by a LDO) rather than a 12 V gate voltage;
- An updated rectifier integrated circuit (*SRK2001A*), that reduces the body diode conduction time by up to 25 %;
- Larger transformer limb (65 mm^2) and yoke (93 mm^2) cross-sectional areas (see Table 4 for previous values), which lowers core losses but also slightly reduces power density through a larger core height.

This updated converter is shown as "Module 1" in Figure 19, and measures 89.5 mm × 66.0 mm × 13.5 mm, for an 8.6 % reduction in power density to 308 W in^{-3}. This minor reduction in power density, though, accompanies a large increase in efficiency across the load range, as shown in Figure 20: at 10 % load, the efficiency increases from 87.2 % to 92.3 %, and at 50 % load, total converter losses are reduced by the predicted 26 % for an efficiency increase from 95.6 % to 96.7 % (see Figure 21 for a detailed loss budget).

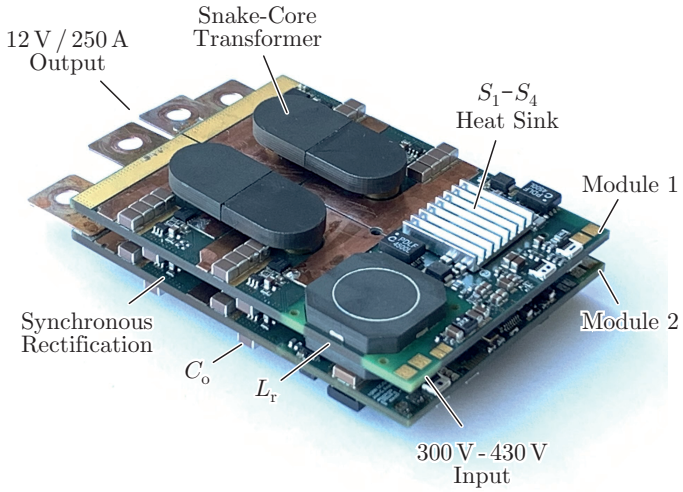

Figure 19. Next-generation DC/DC module (key values and implementations given in Table 7), measuring 89.5 mm × 66.0 mm × 13.5 mm (308 W in^{-3}), shown with two modules combined in an input-parallel output-parallel (IPOP) configuration to reach 3 kW output power at 250 A of output current and measuring 89.5 mm × 66.0 mm × 24.1 mm (345 W in^{-3}). The snake-core transformer enables ideal current sharing between the phases and modules with reduced core losses from the single flux path and shared transformer core between the two modules.

Table 7. Key design values and implementation for components in the *Improved* 1.5 kW hardware demonstrator of Figure 19.

Parameter	Design Value	Implementation
$S_{1\text{-}4}$	–	600 V, 70 mΩ GaN HEMT *IGLD60R070D1*
$S_{1\text{-}4}$ gate drivers	–	*UCC21225A*
$S_{5,6}$	–	40 V, 1.35 mΩ Si MOSFET *IQE013N04LM6*
$S_{5,6}$ gate drivers	–	*SRK2001A* and *1EDN7511B*, $v_{gate} = 6$ V
L_r	24 µH	PCB-integrated, fringing-field concept [25]
C_{dc}	1 µF	4× 0.28 µF *C5750X7T2W105K250KA*
C_{out}	640 µF	32× 20 µF *C4532X7R1C336M250KC*
C_r	11 nF	5× 2.2 nF *C3216C0G2J222J115AA*

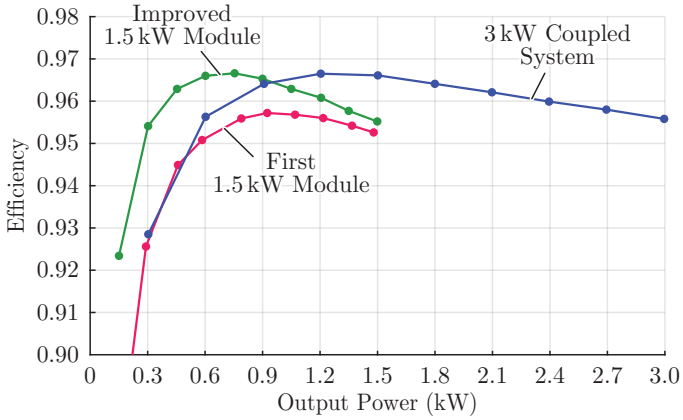

Figure 20. DC/DC electrically-measured efficiencies from input ($v_{dc} = 400$ V) to output ($V_o = 12$ V) at different load conditions, including all loss components. The improved DC/DC module achieves higher efficiency than the original module at all load conditions, and the paralleled 3 kW converter achieves higher efficiency from reduced core losses at power levels below 1.5 kW.

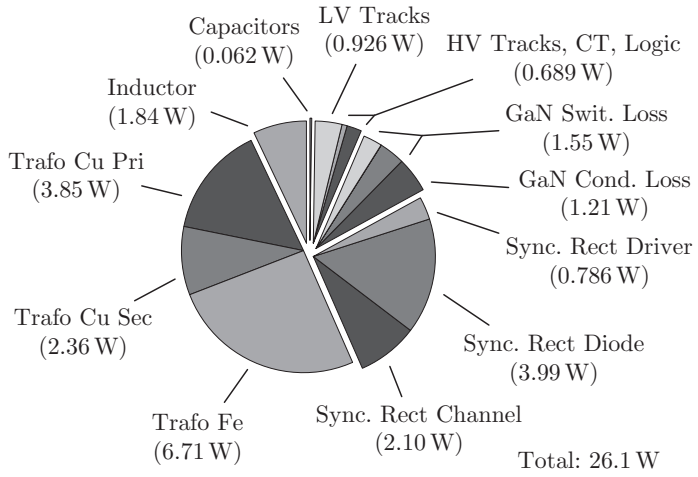

Figure 21. Experimental loss budget at 50 % load of the "Improved 1.5 kW Module" of Figure 20 ("Module 1" in Figure 19), with $v_{dc} = 400$ V and $V_o = 12$ V, confirming the expected performance improvements calculated in Figure 18b.

5.2. Paralleled DC/DC Modules

With the improvements identified in Section 4 demonstrated in hardware for a significant increase in overall efficiency, we move to coupling two modules to highlight one key benefit of the snake-core transformer—ideal current sharing—and reach 3 kW of output power, demonstrating a path to higher output powers and currents with the modular approach.

The modules could be coupled in four configurations, with the input connections configured as "input series" (IS) or "input parallel" (IP) and the outputs independently configured as "output series" (OS) or "output parallel" (OP). The output series configurations (ISOS and IPOS) are not preferred for high-output-current applications, as each module is only configured to half of the total output voltage and therefore each module must provide the full output current. An input-series-output-parallel (ISOP) configuration features natural current sharing [31], at the expense of higher input currents per module and, for this application, switches rated to the awkward and non-commercial voltage level of 300 V.

In this application, then, the input-parallel-output-parallel (IPOP) module coupling is preferred, with simple scaling at the expense of complications in power sharing, where even minor mismatches in resonant tank impedance leads to poor current sharing between modules [32]. To work around this fundamental problem, which is especially pernicious at high output currents, a few concepts can be considered. Firstly, digital or analog output current controllers that force equal power sharing through modulation are possible, but require additional sensing circuits, control loops, and computational power and complexity. In [33,34], coupled inductors are used to force equal current sharing, but these cannot be arbitrarily modularized and cannot benefit from the fringing-field approach used here [25] to realize high-efficiency PCB inductors. Finally, the resonant capacitors or inductors can be electrically connected [32,35], which achieves good power balancing with a simple implementation but does not improve the power density or core losses.

The proposed snake-core transformer, however, fundamentally solves the power sharing issue that bedevils IPOP modularity, with a single flux path that forces ideal magnetic coupling between modules for even power sharing, lower core losses, and a *boost* in power density for a single core shared between two modules. The two-module topology is shown in Figure 22, highlighting the direct magnetic coupling through a single flux path between the two modules.

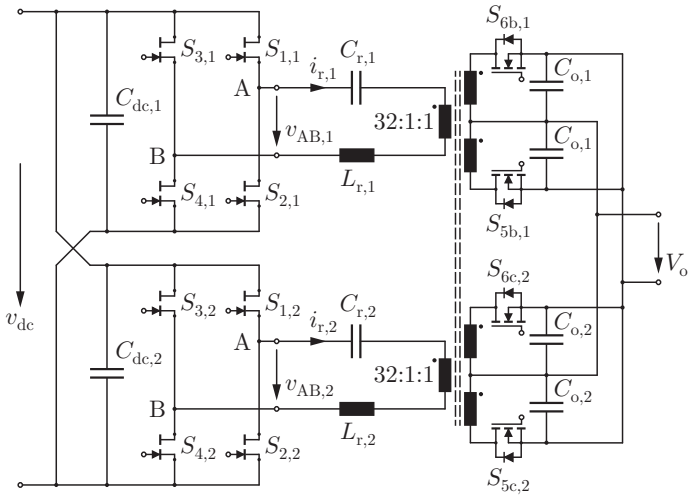

Figure 22. Simplified power circuit of the proposed input-parallel output-parallel (IPOP) combined DC/DC converter, with the snake-core transformer shared for a single flux path between the two modules that results in ideal current sharing, lower core losses, and improved power density. The converter utilizes GaN devices for the primary-side full-bridge and the updated *IQE013N04LM6* power MOSFETs operating as synchronous rectifiers on the secondary-side.

This single flux path—the critical innovation of the snake-core—can be visualized through an equivalent circuit model of the magnetic reluctance, shown in Figure 23 for a conventional matrix transformer (Figure 23a) and for the snake-core transformer (Figure 23b). With a high-permeability core, the snake-core transformer can be modeled with a single flux path through each winding, so mismatches in the number of turns or core reluctances cannot affect the current sharing between phases or modules. With the matrix transformer, alternatively, additional flux paths exist across the core yokes, so even small mismatches (in turns or reluctance) can result in major current imbalances, and, potentially, to operational instability.

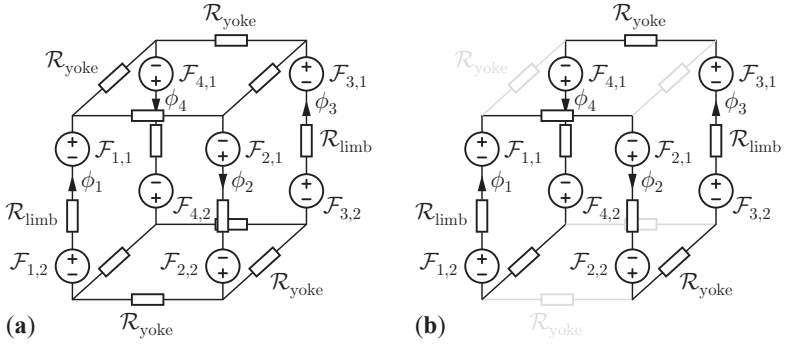

Figure 23. Magnetic circuits for (**a**) a conventional matrix transformer and (**b**) the proposed snake-core transformer, with the magnetomotive forces of the windings ($\mathcal{F}$) and core reluctances ($\mathcal{R}$) highlighted, assuming the permeability of the core is sufficiently high to ignore reluctance paths through the air. The snake-core transformer has only a single path for the flux, guaranteeing identical flux through every winding and resulting in ideal current sharing. The conventional matrix transformer has multiple flux paths, and small turns or reluctance mismatches therefore result in poor current sharing and, potentially, operation instability.

The benefits of the snake-core transformer, and by association the reluctance model, are validated in situ by artificially unbalancing the reluctance in one core leg of a matrix transformer with the addition of around 10 % more air gap. In Figure 24a, the snake-core transformer maintains ideal current sharing between the phases and modules with the

same flux penetrating all windings, while in Figure 24b,c, a traditional matrix transformer is tested, resulting in poor current sharing (especially during and near switching transitions) and signs of instability *even before the artificial air gap is added*. In real-world conditions, then, with variations in core materials and PCB manufacturing processes inevitable, the snake-core transformer uniquely provides a straightforward and reliable path to module coupling for high-current outputs.

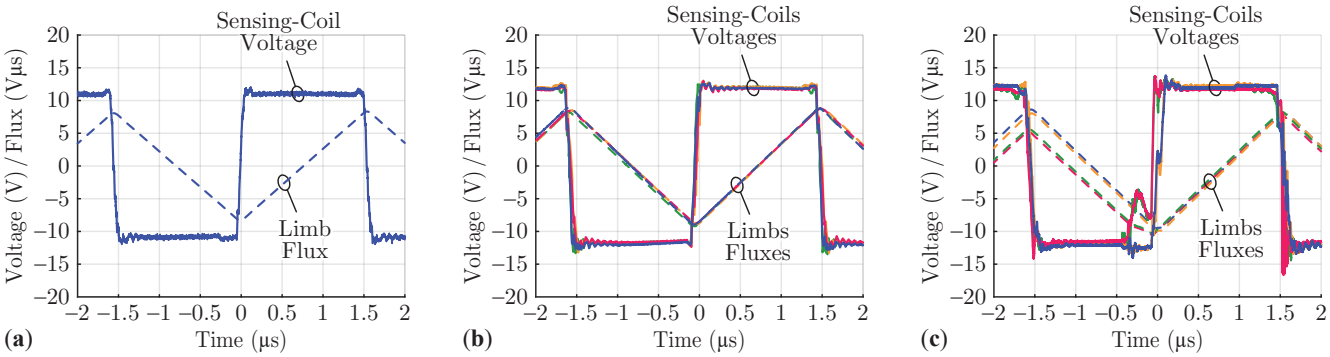

Figure 24. Measured induced voltages and limb fluxes (measured by sensing coils wound around the core limbs) for (**a**) the proposed snake-core transformer , and for the conventional matrix transformer with (**b**) balanced and (**c**) unbalanced reluctances, through the addition of an larger air gap in one leg. Output power is 40 % load for all test conditions.

The two paralleled modules are implemented in Figure 19, with the transformer core shared for higher power density and reduced core losses. The measured efficiency for the combined 3 kW DC/DC converter is given in Figure 20 as the "3 kW Coupled System", with the expected gains in efficiency from reduced core losses boosting the 1.5 kW efficiency by half percentage point at light load. The paralleled converter reaches nearly 97 % peak efficiency and outputs 250 A at 12 V for 3 kW output power, paving the way to higher-current applications for the next-generation industrial environment.

6. Conclusions

Compact, reliable, and efficient power supplies are critical to unlocking the electrification of Industry 4.0, including power for CNC steppers, servo motor drives, and, as the power is scaled, for charging electrified material handling systems like forklifts and tuggers. These industrial power supplies must be realized under a challenging set of specifications, including long hold-up times that result in a wide-input-voltage range, complete PCB-integration with limited available heights, and high output currents at low voltages.

In this work, we conceptualize, analyze, and demonstrate a 1.5 kW, 12 V-output DC/DC converter module for industrial applications. This converter achieves nearly 96 % peak efficiency with a power density over 300 W in^{-3} (18.3 kW dm^{-3}) while achieving the application-specific requirements: complete PCB integration, soft-switching over the entire operating range, and a wide-input-voltage from 300 V to 430 V. This demonstrator met the key requirements, but further component- and converter-level improvements were subsequently identified using the detailed loss models derived in the design optimization stage. We implement the key improvements, including expanding the snake-core-transformer core area and improving the synchronous rectifier speed and device selection, and eliminate 25 % of the total converter losses in a second-generation demonstrator that achieves nearly 97 % peak efficiency. Finally, the benefits of the proposed snake-core transformer are showcased by paralleling two DC/DC modules with ideal current sharing among the secondary outputs—which cannot be achieved with conventional matrix transformers—for 3 kW output power with an *improvement* in efficiency over a single module and a power density of 345 W in^{-3} (21.1 kW dm^{-3}).

To keep pushing Industry 4.0 towards its increasingly-electric future, power supplies that are soft-switched, wide-input-voltage range, fully PCB-integrated, efficient, power

dense, and high-output-current are required. This work highlights key innovations — with experimental demonstrations—that unlock these critical power requirements, with a particular emphasis on the snake-core transformer innovation to support modular power scaling with ideal current sharing.

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