A Semiconductor Area Based Assessment of AC Motor Drive Converter Topologies

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***Abstract* - In order to find the optimal converter topology for a given ac motor drive, as defined by its mission profile, suitable assessment criteria have to be applied. A new semiconductor chip area based approach is proposed to compare and assess different motor drive converter topologies. It determines the total semiconductor chip area based on the drive's operating point and the optimal partitioning of the transistor and diode chip areas. This approach not only provides a distinct figure-of-merit for comparison but also enables the semiconductor costs of different converter topologies to be determined. The chip area based comparison has been successfully used to assess three 3-phase ac-dc-ac converter topologies for a 15 kW (20 HP) motor drive. It is shown that the Voltage DC-Link Back-to-Back Converter based drive provides the best overall performance in terms of chip area, cost, efficiency, and available nominal torque.**

I. INTRODUCTION

The development of reliable, efficient, and cost effective variable frequency drive converters, which are optimally matched to the drive's mission profile, is demanding due to the large number of design parameters. Starting typically with the mapping of the drive requirements to the torque-speed plane, selecting the motor type and possibly the gear system, the design engineer is then faced with the task to analyze and compare different converter topologies in order to find the optimal topology for the given application.

The core components of any power electronic converter are the power semiconductors (including their packaging) [1]. They not only determine the key performance figures such as efficiency, power density, switching frequency range, and partly EMI emissions but also contribute to the overall converter costs by approximately 25-30% [2]. Therefore, for any converter topology comparison a figure-of-merit (FOM) is essential that assesses the power semiconductor cost to converter performance relationship. Different methods for semiconductor related comparisons have been presented in the literature. A commonly used method is to compare different converter topologies by determining the losses at different operating points using the same semiconductors for all topologies, as given in [3]. The semiconductors have to be selected such that they fulfill the ratings of all compared converters topologies and therefore are not matched to the individual topologies. Another possibility, presented in [4], is to perform the comparison based on the thermal stress of the power semiconductors. In this method the rating of the compared converter topologies is adapted depending on the operating point in order to not exceed the thermal limits of the semiconductor devices. The general limitation with these methods is that the semiconductor chip area required by the different converter topologies is not considered.

In this paper a Semiconductor chip Area based motor drive Converter Comparison (SAC^2) is presented, which utilizes a semiconductor model including packaging data. This method avoids the above mentioned limitations, allows for optimal selection of the semiconductors with respect to the topology and the operating point, and finally provides a common FOM for comparison: the required total semiconductor chip area.

To provide a more in-depth understanding of the suggested approach, a description of the comparison method, including an overview of the semiconductor model, is given in **section II**. In **section III** this approach is then applied to compare three different converter topologies: a Voltage DC-Link Back-to-Back Converter (VLBBC), a Current DC-Link Back-to-Back Converter (CLBBC), and an Indirect Matrix Converter (IMC), shown in **Fig.1**. Methods to determine the accuracy of the approach are summarized in **section IV**. This paper concludes in **section V** with a discussion of the achievable results and the merits of the SAC^2.

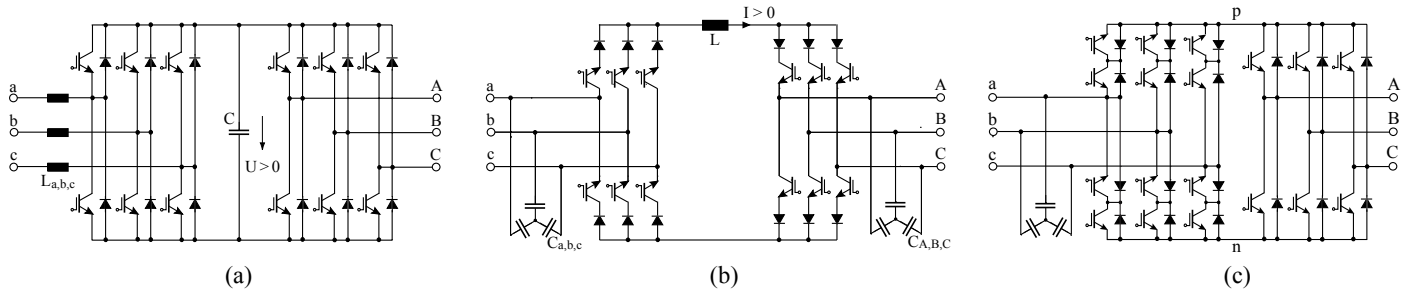

Fig. 1: Compared motor drive converter topologies: (a) VLBBC, (b) CLBBC, and (c) IMC.

II. Description of The Comparison

A. Basic Concept

The basic concept can be best explained with **Fig.2(a),** depicting a PWM modulated IGBT with an anti-parallel diode, which is a standard semiconductor configuration in many motor drive converters. The IGBT and diode current rating is proportional to the (active) chip area. Depending on the applied voltage u, the average and the rms values of the current i, the current direction and the switching frequency (modulation scheme), the IGBT and diode are loaded differently. This consequently leads to unequal semiconductor losses for the IGBT and diode chip. The total power loss is dissipated through the power module base plate to the heat sink, as shown in **Fig.2(b)**, with the resulting thermal resistance $R_{th,JS}$ being dependent on the chip area and the module assembly. For a given level of semiconductor losses $P_{L,Semi}$ and a heat sink temperature T_S, the resulting average junction temperature T_J can be calculated (the thermal capacitances are not considered, as explained in section III) as

$$T_J = T_S + R_{th,JS} \cdot P_{L,Semi} \,. \tag{1}$$

The important point is that if the same semiconductor IGBT and diode chip configuration of a power module is implemented in different converter topologies and analyzed regarding losses, it is most likely that for one topology e.g. the IGBT chip is over- and the diode chip is under-dimensioned whereas for an another topology it may be vice versa. That is exactly where the SAC[2] provides benefits. The implemented algorithm, shown in **Fig.3**, determines the minimum required semiconductor area for the individual IGBT and diode chips for a given converter topology and operating point such that the maximum average IGBT and diode junction temperatures $T_{J,T/D}$ are equal or less than a predefined maximum value $T_{J,max}$. This does not only guarantee optimal chip area partitioning and semiconductor material usage but also provides a common basis for converter topology comparisons. Furthermore, the chip area data can be directly used to determine the semiconductor costs.

B. Semiconductor Model

The prerequisite of the semiconductor area based converter comparison is a sufficiently accurate semiconductor model. In a first step, the model is developed for the latest generation of Infineon Trench & Field Stop 1200 V IGBTs (IGBT4) and 1200 V EMCON 4 diodes, both rated for a maximum junction temperature of 175°C. The presented procedure can be applied to any semiconductor technology.

The individual semiconductor parameters are derived based on a statistical analysis of the power module datasheets and manufacturer data. The extracted data is fitted to a set of

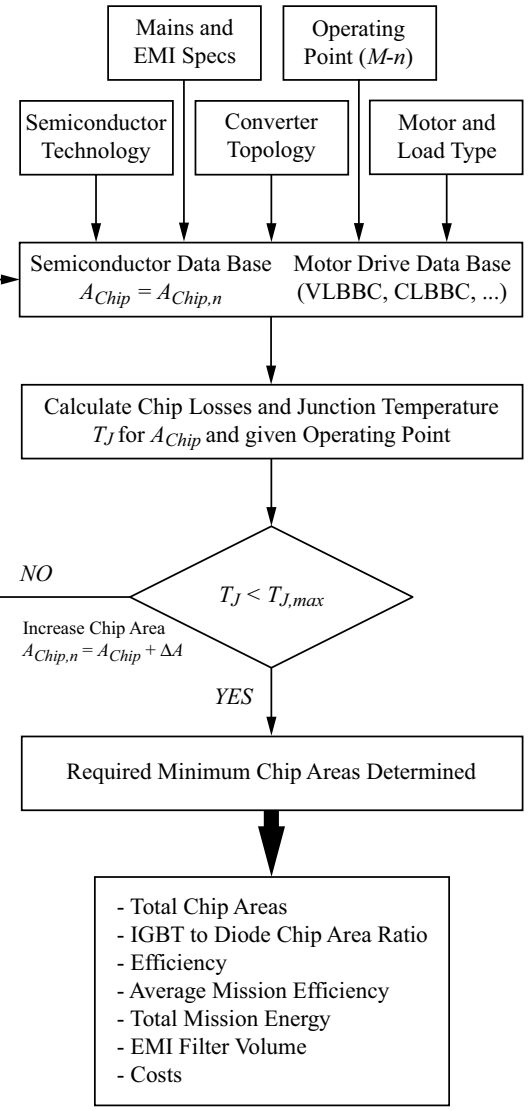

Fig. 3. Converter evaluation flowchart showing the algorithm to determine the chip areas. This algorithm is performed for all IGBT and diode chips individually. The chip areas are initialized with 0.

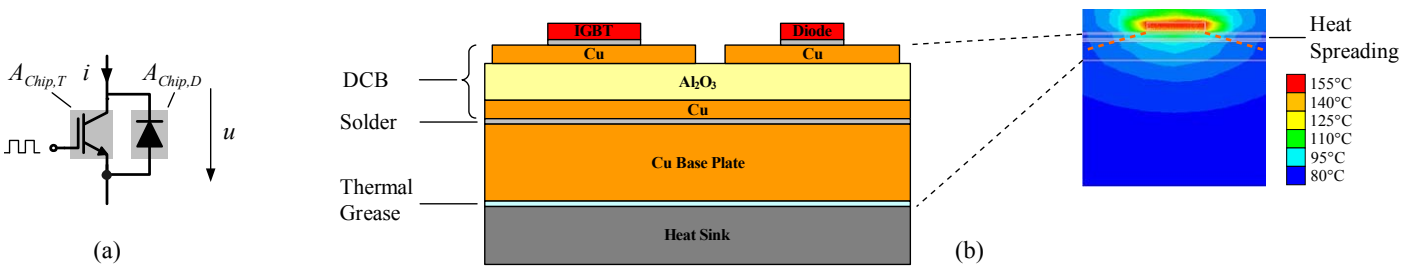

Fig. 2:(a) Standard IGBT diode configuration. (b) Considered module assembly with thermal simulation showing the heat spreading.

voltage, current, chip area, and temperature dependent model equations that are based on semiconductor theory [5-7]. For reasons of conciseness only the key relationships of the semiconductor model for the maximum junction temperature of 150°C are presented in this paper. To begin with, a relationship between the nominal semiconductor chip current rating I_N and the chip area A_{Chip} is required, which is shown in **Fig.4**. This can be approximated with a set of linear equations for the IGBT (2) and the diode (3) chips

$$A_{Chip,T} = 0.95\,\frac{\text{mm}^2}{A}\cdot I_N + 3.2\,\text{mm}^2 \quad (2)$$

$$A_{Chip,D} = 0.47\,\frac{\text{mm}^2}{A}\cdot I_N + 3.6\,\text{mm}^2\,. \quad (3)$$

In order to model the thermal properties, the dependency between the chip area and the resulting thermal resistance from junction to heat sink $R_{th,JS}$ is needed. The chip area dependent thermal resistance (4), depicted in **Fig.5**, is derived based on manufacturer data for a standard power module assembly with a 3 mm Cu base plate and 380 µm Al_2O_3 DCB ceramic substrate, and has been verified by thermal simulations (Fig.2(b))

$$R_{th,JS} = 23.94\,\frac{\text{K}}{W\text{mm}^2}\cdot A_{Chip}^{-0.88}\,. \quad (4)$$

The IGBT and diode on-state parameters, which are used to determine the semiconductor conduction losses, are modeled with a nominal chip area A_{Chip} dependent forward voltage drop $U_{CE/F}$ and differential resistance $r_{T/D}$. The resulting IGBT $P_{C,T}$ and diode chip $P_{C,D}$ conduction losses can then be calculated according to (5) and (6)

$$P_{C,T} = U_{CE}\left(A_{Chip,T}\right)\cdot I_{T,avg} + r_T\left(A_{Chip,T}\right)\cdot I_{T,rms}^2 \quad (5)$$

$$P_{C,D} = U_F\left(A_{Chip,D}\right)\cdot I_{D,avg} + r_D\left(A_{Chip,D}\right)\cdot I_{D,rms}^2\,. \quad (6)$$

The IGBT switching loss energy per switching transition are modeled as a function of the chip area $A_{Chip,T}$, the switched collector current I_C, and the switched collector-emitter voltage U_{CE} for turn-on and turn-off independently. **Fig.6** depicts, as an example, the turn-on energy loss for two switched voltage levels as a function of the nominal chip current rating and the switched collector current. By multiplying the energy loss by the switching frequency f_S the IGBT switching losses $P_{S,T}$ can be determined (7)

$$P_{S,T} = f_S\cdot\left[E_{on,T}\left(A_{Chip,T}, I_{CE}, U_{CE}\right) + E_{off,T}\left(A_{Chip,T}, I_{CE}, U_{CE}\right)\right]. \quad (7)$$

The diode reverse recovery energy losses are approximated as a function of the diode chip area A_{Chip}, the forward current I_F, and the applied reverse voltage U_B, assuming a constant current fall-time. The diode reverse recovery losses $P_{rr,D}$ can then be calculated according to (8)

$$P_{rr,D} = f_S\cdot E_{rr,D}\left(A_{Chip,D}, I_F, U_B\right). \quad (8)$$

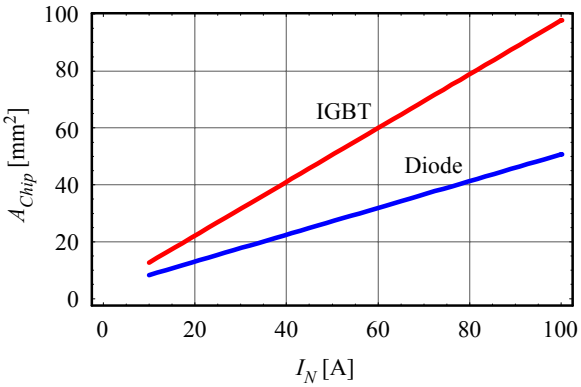

Fig. 4. IGBT and diode chip area A_{Chip} as a function of the nominal chip current I_N, scaled for the specified temperature conditions.

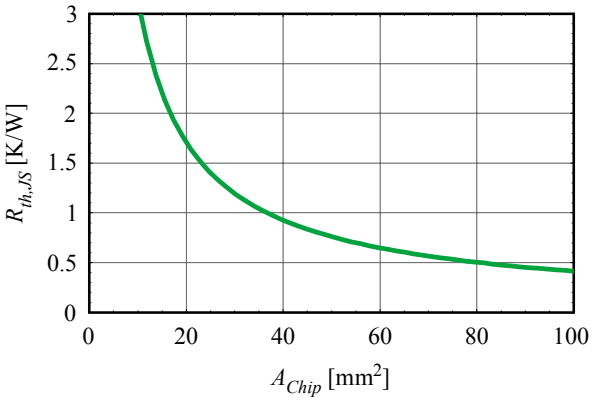

Fig. 5. Resulting thermal resistance $R_{th,JS}$ between junction and heat sink as a function of the chip area A_{Chip}.

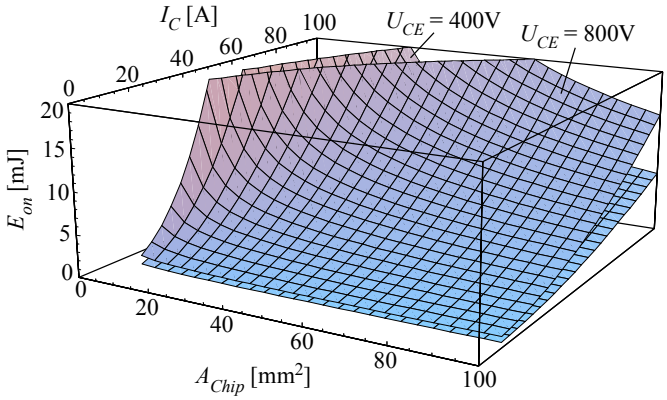

Fig. 6. IGBT turn-on switching energy loss as a function of the collector-emitter voltage U_{CE}, the collector current I_C, and the chip area A_{Chip}.

III. Chip Area Based Assessment

A. Motor Drive System Design

The SAC^2 is calculated for three bidirectional three-phase converter topologies (Fig.1) that are designed to supply a gear-less elevator traction drive: the Voltage DC-Link Back-to-Back Converter (VLBBC), the Current DC-Link Back-to-Back Converter (CLBBC), and the Indirect Matrix Converter (IMC).

Gearless traction drives are typically applied for "high speed" elevators with a speed greater than 2.5 m/s (500 feet per minute [8]) where bidirectional operation is desirable. In this paper a vector controlled permanent magnet synchronous machine (PMSM) is considered. The application example of an elevator drive system has been selected for several reasons:

- With a focus on environmental friendliness, efficiency, and compactness, elevator drive systems provide an interesting application area for alternative converter topologies to the standard voltage-source type converters, such as Matrix Converters or Current Source Converters, as presented in [9, 10].
- The elevator mission profile comprises all of the converter design relevant operating points, from electrical stand-still (f_2 = 0 Hz) to nominal electrical output frequency ($f_2 = f_{2,N}$) at full load current.

The individual power converters are designed for a 400 V / 50Hz three-phase mains system and have a nominal output power level of 15 kVA. In order to provide a control margin, the nominal output power can be provided at 90% of the maximum output voltage $U_{2,max}$.

The input and output stage switching frequency of the VLBBC and CLBBC are selected to be identical. For the IMC the input stage switching frequency is half the output stage switching frequency, which is inherently determined by its modulation scheme [11]. The considered output stage switching frequencies are 8 kHz and 32 kHz.

Since the nominal output voltage and output current of the individual topologies varies the load machine (PMSM) parameters are matched to the topology in order to guarantee a fair comparison. It is further assumed that the output current ripple of the VLBBC and the IMC is identical for a given output stage switching frequency. The key converter design specifications are summarized in Tab.I.

B. Modulation

For the considered topologies it is assumed that space vector modulation is applied. The space vector modulation scheme implemented for the VLBBC and the CLBBC is described in [12] (Fig.6(b) and Fig.9(b) respectively). The selected modulation scheme for the IMC is explained in [12] (Fig.17(a)) and it implements zero current commutation of the input stage. Therefore, the input stage switching losses of the IMC can be neglected.

All modulation schemes considered clamp the switch configuration with the largest commutation voltage and/or the switch carrying the largest current in order to minimize the switching losses.

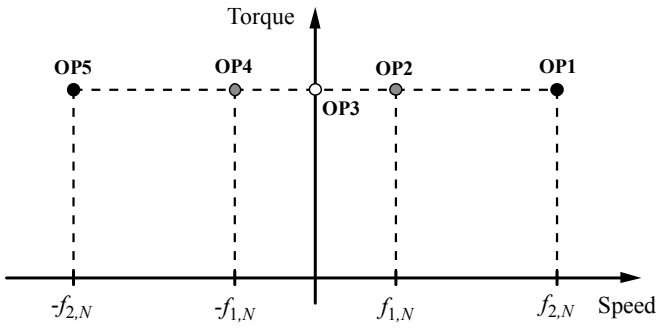

Fig. 7. Design relevant operating points in the torque-speed plane.

C. Operating Points

Fig.7 depicts design relevant operating points for bidirectional motor drives that have been identified in the torque-speed plane. For symmetry reasons it is sufficient to consider only two quadrants.

- OP1/OP5: motor/generator operation at nominal output current $I_{2,N} \sim M_N$ (proportional to the nominal torque M_N), nominal electrical output frequency $f_2 = f_{2,N}$, and nominal output power $P_{2,N}$ = 15 kW.
- OP2/OP4: motor/generator operation at nominal output current and an electrical output frequency equal to the input mains frequency: $f_2 = f_{1,N}$.
- OP3: motor operation at nominal output current and electrical stand-still f_2 = 0 Hz. At this operating point it is assumed that the output voltage is restricted to 3% of the topology dependent maximum output voltage level. This allows for modeling the ohmic voltage drop of the PMSM at stand-still and nominal current.

All converter input stages are controlled to operate at unity power factor. Due to the PMSM load the output phase displacement Φ_2 is assumed to be 0° for motor operation and 180° for generator operation.

In the following analysis the VLBBC, the CLBBC, and the IMC are compared for the characteristic operating points OP1, OP3, and OP5. The operating points OP2 and OP4 are shown for the sake of completeness since for the Conventional Matrix Converter (CMC) [11] the semiconductor stresses significantly increase for these operating conditions. However, including the CMC in the SAC^2 is out of the scope of this paper.

As previously stated the thermal capacitances of the chips are neglected. This is an acceptable simplification for the considered topologies as the electrical frequencies vary in a range of 50 Hz to 150 Hz and therefore the junction temperature variation is comparatively small. For electrical stand-still the thermal capacitances can be neglected in any case.

Table I: Converter Design Specification Summary

	VLBBC	**CLBBC**	**IMC**
Nominal Input Voltage	$U_{1,N}$ = 230 V, $f_{1,N}$ = 50 Hz	$U_{1,N}$ = 230 V, $f_{1,N}$ = 50 Hz	$U_{1,N}$ = 230 V, $f_{1,N}$ = 50 Hz
DC-Link	Capacitive, $U_{DC,N}$ = 700 V	Inductive, $I_{DC,N}$ = 35.3 A	No energy storage
Nominal Output Quantities (90% of $U_{2,max}$)	$U_{2,N}$ = 256 V, $I_{2,N}$ = 19.6 A, $P_{2,N}$ = 15 kW, $f_{2,N}$ = 150 Hz	$U_{2,N}$ = 201 V, $I_{2,N}$ = 24.9 A, $P_{2,N}$ = 15 kW, $f_{2,N}$ = 150 Hz	$U_{2,N}$ = 175 V, $I_{2,N}$ = 28.6 A, $P_{2,N}$ = 15 kW, $f_{2,N}$ = 150 Hz
Switching Frequency	f_S = 8 kHz / 32 kHz	f_S = 8 kHz / 32 kHz	f_S = 8 kHz / 32 kHz

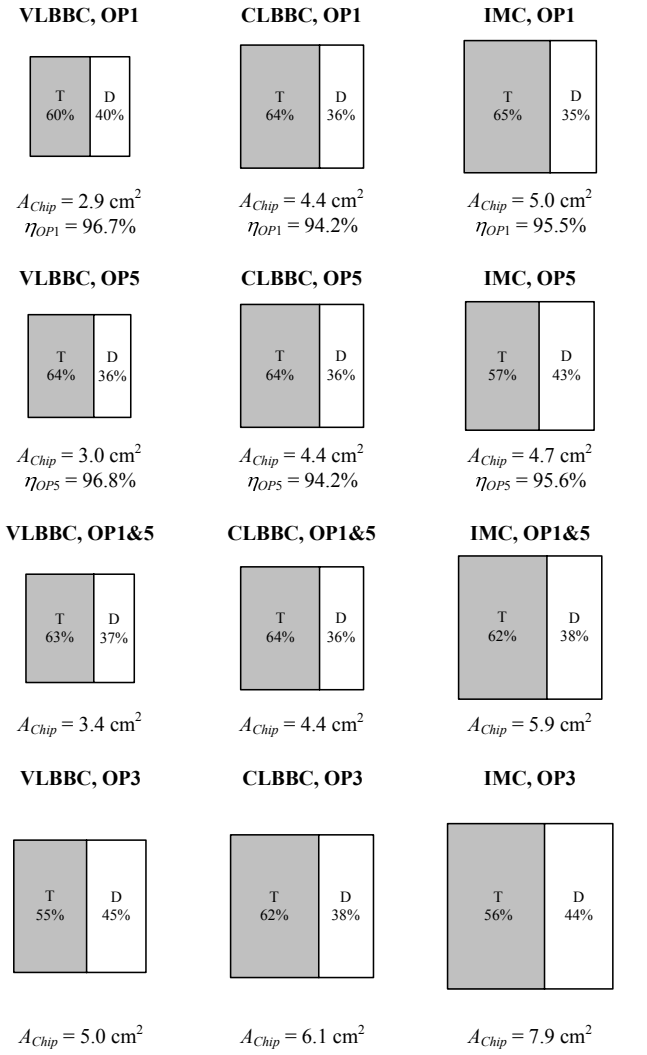

Fig. 8. VLBBC, CLBBC, and IMC semiconductor chip area requirements for a switching frequency f_S = 8 kHz.

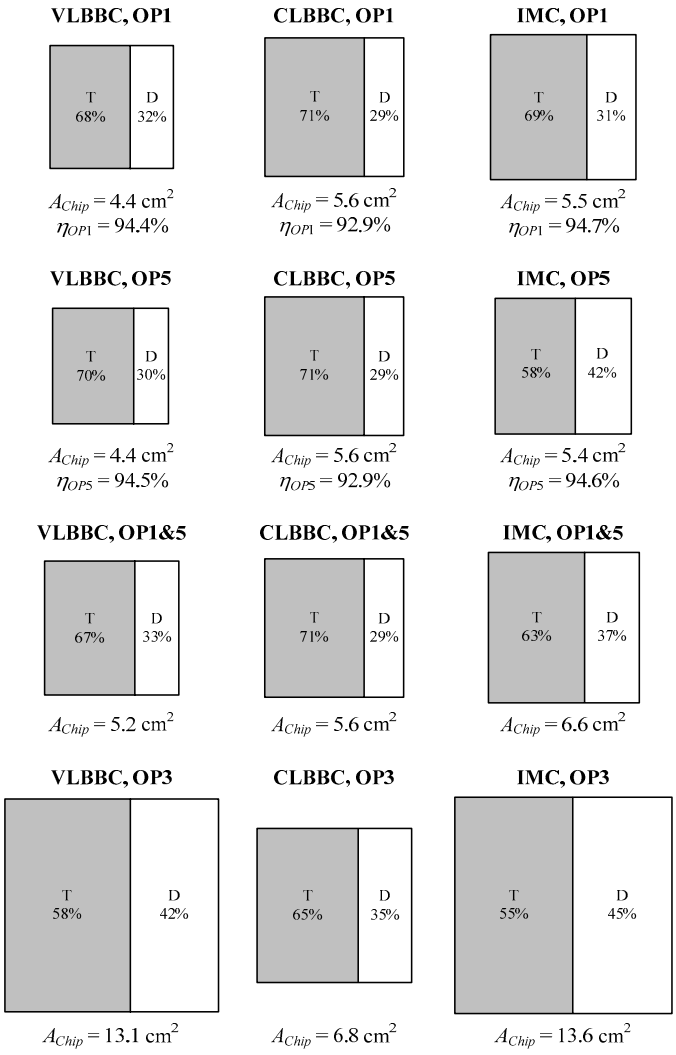

Fig. 9. VLBBC, CLBBC, and IMC semiconductor chip area requirements for a switching frequency f_S = 32 kHz.

D. Semiconductor Area Comparison

The suggested SAC[2] is applied for OP1, OP3, and OP5 to determine the minimum semiconductor chip area for the VLBBC, the CLBBC, and the IMC (designed according to Tab.1). The average maximum junction temperature of all semiconductor chips is limited to $T_{J,max}$ = 150°C, assuming a heat sink temperature of T_S = 80°C. The comparison is performed as follows:

- In a first step the semiconductor area requirements are calculated for OP1 and OP5.
- Then the maximum semiconductor chip area of OP1 and OP5 is determined, denoted as OP1&5. With this chip area design the junction temperature limit can be fulfilled for motor as well as generator operation.
- Finally, the maximum chip area required to operate the converter at OP3 (nominal output current and electrical stand-still) and OP1&5 is calculated.

Fig.8 and **Fig.9** visualize the required silicon chip areas for a switching frequency of 8 kHz and 32 kHz respectively. The total chip areas are represented by individual squares for the different operating points, showing the partitioning between the IGBT (T) and diode (D) chip area. In addition, the achieved converter efficiency is given for OP1 and OP5. As can be seen in Fig.8, for a switching frequency of 8 kHz the VLBBC is the most economical topology regarding semiconductor usage for all operating points followed by the CLBBC and then the IMC. Furthermore, the VLBBC has the highest efficiency. The IMC has the second highest and the CLBBC the lowest efficiency. For the design according to OP1&5 the chip area for the VLBCC is 60% of the required chip area of the IMC.

In Fig.9 the chip area data are presented for a switching frequency of 32 kHz. For the operating points OP1, OP5, and OP1&5 the VLBBC requires again the smallest chip area. In terms of efficiency the IMC has a higher efficiency than the VLBBC followed by the CLBBC. It is important to note that the comparatively small chip area of the CLBBC for OP3 is due to the low output voltage level (low commutation voltage). Therefore, the output stage switching losses of the CLBBC are

low and thus the chip area only slightly increases compared with OP1&5. Contrary to the CLBBC the output stage commutation voltage for the IMC and VLBBC equals the actual DC-link voltage leading to high output stage switching losses and an increase in chip area of the output stage semiconductors for OP3.

The small chip area for the VLBBC can be explained by its lower nominal output current compared with the CLBBC and the IMC. Due to its DC-link voltage of 700 V the considered 1200 V power semiconductors are also much better utilized in terms of blocking voltage compared with the CLBBC and IMC where the maximum reverse voltage is only 566 V. The large chip area required for the IMC has several reasons. Firstly, as a result of the reduced input to output voltage transfer ratio (86%) [11] the IMC has the highest nominal output current of all considered topologies and therefore requires a larger chip area for the output stage power devices compared to the VLBBC. Secondly, in view of the VLBBC and the CLBBC, the IMC requires 18 IGBTs and diodes instead of 12.

E. Efficiency and Switching Frequency Relationship for OP1

In **Fig.10** the converter efficiency is plotted for OP1 (motor operation) over a switching frequency range of 8 kHz to 32 kHz with steps of 4 kHz. For each switching frequency value the minimum chip area is determined according to the algorithm in Fig.3 ($T_{J,max}$ = 150°C, T_S = 80°C). As previously stated in the low switching frequency range the VLBBC has the highest efficiency. For switching frequencies above 25 kHz the IMC becomes more attractive in terms of efficiency compared with the VLBBC. However, the IMC still needs a larger chip area than the VLBCC. The lower reduced efficiency for the IMC (c.f. VLBBC) for increasing switching frequency originates from the negligible switching losses of the IMC input stage. The CLBBC features the lowest efficiency over the whole switching frequency range, as always 4 IGBTs and 4 diodes conduct the DC-link current.

The efficiency of the IMC and CLBBC could be increased by replacing the serial connections of IGBT and diode by Reverse Blocking IGBTs.

F. Maximum Torque for Given Total Chip Area

The next aspect to be investigated is on how much torque (M_{max}), can be achieved with the different motor drives for OP1 and OP3 if the same total chip area is used and is optimally partitioned for all converter topologies. For that purpose the VLBBC, the CLBBC, and the IMC are designed for OP1&5 and a switching frequency of 8 kHz and 32 kHz using a total chip area of 5.9 cm^2 This corresponds exactly the determined chip area for the IMC for OP1&5 at f_S = 8 kHz. Consequently, the IMC is considered as the reference system and defines the nominal torque M_N (100%) for OP1 at f_S = 8 kHz. The maximum torque at OP1, which is proportional to the maximum output current, is determined by performing the optimization algorithm (see Fig.3) for steadily increasing output currents. The maximum torque at OP3 is reached, when any junction temperature reaches $T_{J,max}$ = 150°C for the inital chip design of OP1&5. In **Fig.11** and **Fig.12** the maximum achievable torque M_{max} normalized to the nominal torque M_N is plotted for OP1 and OP3 for a switching frequency of 8 kHz and 32 kHz respectively. (The dashed curves between OP1 and OP3 are linear approximations, as the thermal capacitances are not considered.) The option of alternating every pulse period the output stage free-wheeling state of the VLBBC or IMC at OP3

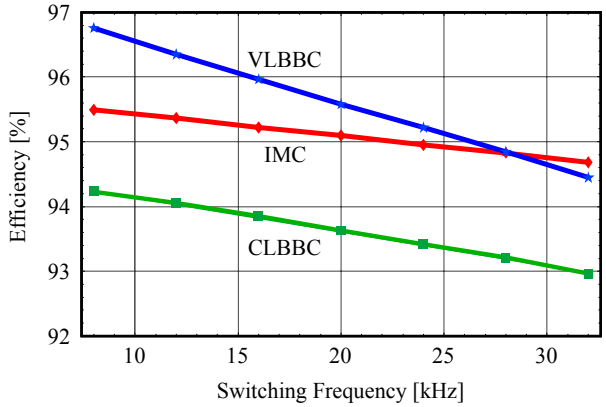

Fig. 10. Efficiency vs. switching frequency for OP1.

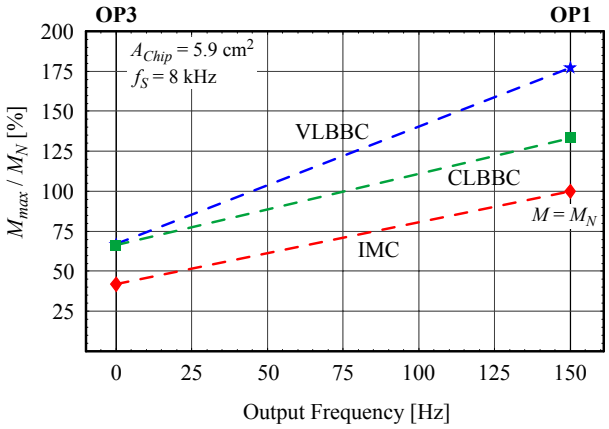

Fig. 11. Normalized maximum torque M_{max}/M_N for OP1 and OP3 for A_{Chip} = 5.9 cm^2 and f_S = 8 kHz.

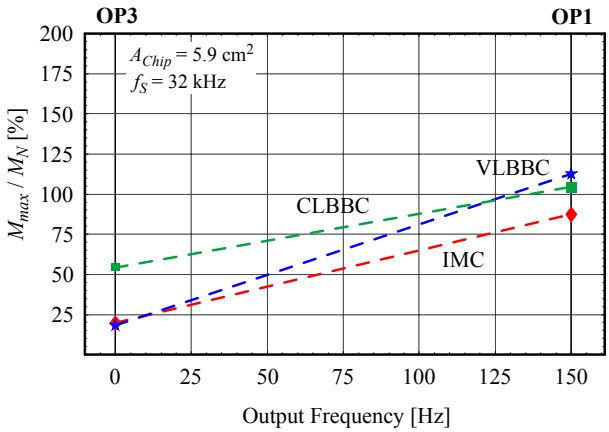

Fig. 12. Normalized maximum torque M_{max}/M_N for OP1 and OP3 for A_{Chip} = 5.9 cm^2 and f_S = 32 kHz.

and thus reducing the semiconductor losses is not considered. By comparing the results it can be seen that at OP1 the VLBBC drive provides a higher torque than the CLBBC and the IMC. At OP3 the VLBCC is superior to the IMC for a switching frequency of 8 kHz. For $f_S = 32$ kHz the available torque for the motor drive with the VLBBC and IMC is similar and approximately 3 times lower compared with the CLBBC. By applying more advanced modulation strategies it is possible to increase the torque of the IMC at OP3. However, this does not increase the available torque at OP1. The high stand-still torque capability of the CLBBC drive is due to low output voltage resulting in lower switching losses in the output stage (as explained in subsection III.D).

IV. Error Estimation

An estimate of the error in the FOM given by the proposed SAC^2 is essential as the approach is based on analytical loss calculations and models. Absolute and relative errors can be identified. The absolute error corresponds to the actual difference from the predicted performance indicators, such as efficiency, chip area, and torque, when compared to a real hardware system implementation. The relative error, on the contrary, is associated with the difference of the performance indicators between the individual topologies. Ongoing research is focusing on the verification of the SAC^2 accuracy. There are basically two methods under investigation:

- The individual topologies are implemented using commercially available power modules. The SAC^2 algorithm is parameterized with the corresponding power module data in order to determine critical operating points, where the junction temperature reaches the desired maximum value. The converter is then operated at these critical operating points. By measuring the chip temperatures the accuracy of the SAC^2 method can be verified.
- The operating point and power module chip area data generated by the SAC^2 algorithm are utilized in a numerical electro-thermal simulation of the converter topologies. The simulation result of the junction temperature is then compared with the desired maximum junction temperature (defined in the SAC^2 algorithm). The difference gives a measure of the accuracy.

In general, the SAC^2 is not intended to provide highly accurate absolute results but rather provides a FOM for topology assessment with low computational effort.

V. Conclusions

In this paper a semiconductor chip area based converter comparison (SAC^2) has been presented to assess different ac motor drive converter topologies. It has been applied to determine the required semiconductor chip area based on latest generation 1200 V Si IGBT and diode technology. Three bidirectional 15 kVA (20 HP) three-phase converter topologies are considered for characteristic operating points of an elevator traction drive. The result of the analysis is a figure-of-merit that indicates the power semiconductor chip area (cost) to converter performance.

In terms of semiconductor chip area the VLBBC drive provides the most economical solution. The VLBBC has the highest efficiency for switching frequencies below 25 kHz. The CLBBC requires approximately 30% more chip area than the VLBBC for a switching frequency of 8 kHz (10% more for 32 kHz) and has the lowest efficiency of all considered converter topologies. Its advantage compared with the VLBBC and IMC is the high torque capability at stand-still with respect to the utilized chip area. The IMC drive requires the largest semiconductor chip area, which is approximately 70% larger compared with the VLBBC for a switching frequency of 8 kHz (25% larger for 32 kHz). The benefit of the IMC is the higher efficiency, compared with the VLBBC and CLBBC, for switching frequencies above 25 kHz.

Based on the results of the SAC^2 for the analyzed switching frequency range and semiconductor technology the VLBBC drive is the topology to select when the semiconductor chip area (cost), efficiency, and achievable nominal torque are considered together.

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