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Full-SiC Integrated Power Module based on Planar Packaging Technology for High Efficiency Power Converters in Aircraft Applications

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Abstract

Compact, light-weight, efficient and reliable power converters are fundamental for the future of *More Electrical Aircraft* (MEA). Core elements supporting the electrification of the aerospace industry are power modules (PMs) employing exclusively SiC MOSFETs. In order to fully exploit the high switching speeds enabled by SiC, and to address the challenges arising from the parallelization of power devices, novel PM concepts must be investigated. In this paper, highly symmetrical layouts, low inductance planar interconnection technologies, and integrated buffer capacitors are explored to realize a high efficiency, fast-switching, and reliable full-SiC PM for MEA applications. A comprehensive assessment of a number of performance metrics against state-of-the-art full-SiC PMs demonstrates the benefits of the proposed design approach and manufacturing technologies. Moreover, by integrating temperature and current sensors, intelligent functions, which are crucial for the safe application of power electronics in MEA, are added to the developed PM. In this context, the use of MOSFETs' *Temperature Sensitive Electrical Parameters* for online junction temperature estimation is demonstrated, allowing for non-invasive, i.e. without the need for dedicated sensors, thermal monitoring. Additionally, a highly compact gate driver, reducing the overall system volume and complexity, is designed and integrated in the housing of the PM. Finally, switching waveforms are measured during operation of the PM at 500 V and 200 A, proving the performance improvement enabled by the low inductance layout, the integrated snubber, and the gate driver.

1 Introduction

The *More Electrical Aircraft* (MEA) concept targets the replacement of mechanic, pneumatic, and hydraulic systems of commercial aircraft with electric power converters and actuators, aiming for decreased fuel consumption and emissions reduction, as well as increased reliability and lower maintenance effort. An electric power demand of 1.6 MVA is planned for the next generation of commercial aircraft, justifying the interest of the power electronics community in MEA. In particular, the *Horizon2020* European Project 636170 - *Integrated, Intelligent Modular Power Electronic Converter* (I^2MPECT) [1], building on the expertise in device packaging, thermal management, converter design, and reliability analysis of European industry and academia, intended to demonstrate significant advances in terms of power-to-weight ratio and efficiency of power converters for MEA. The primary goal was the realization of a *Power Electronic Building Block* (PEBB) consisting of a $>98\,\%$ efficient three-phase (3-Φ) 45 kW DC/AC inverter, achieving a power-to-weight ratio of 10 kW/kg, three times higher than for nowadays available solutions.

Core elements for the development of an efficient and light-weight PEBB are the power modules (PMs), since they actively perform the power conversion, thus are responsible for the main fraction of the occurring losses, and therefore define the overall system performance and cooling requirements [2, 3]. Promising enabler of a high efficiency and compact power conversion are wide band-gap (WBG) semiconductors; due to their maturity, silicon-carbide (SiC) MOSFETs are currently the preferred technology in PMs. However, their characteristic high switching speeds require low inductance layouts to ensure homogeneous load current sharing and to mitigate switching node over voltage and oscillation after a switching transition. Possible countermeasures to these challenges are the integration of buffer capacitors into the PM to achieve symmetric and minimized parasitic power loop inductances, and the integration of the gate driver circuit to limit gate loop inductances [4].

Moreover, safe and uninterrupted operation of PMs is a fundamental prerequisite in high reliability applications, such as the aerospace industry; therefore, the packaging technology of SiC dies is of major importance [5]. In particular, the lifetime of PMs is significantly affected by their operating conditions, e.g. by the absolute temperature and temperature variations, which result in thermo-mechanical stress [6]. The online measurement and/or estimation of dies' junction temperature is therefore essential for the health monitoring of a PM [7]. Direct temperature measurements are typically impractical due to the necessity of physical contact between the dies and a sensor. Hence, non-invasive indirect temperature estimation methods using *Temperature Sensitive Electrical Parameters* (TSEPs) have been extensively researched on both Si and SiC devices [8]. Although many demonstrators have been proposed, practical solutions in realistic converters are not readily available.

Accordingly, this paper summarises the design steps resulting in the realisation of a full-SiC PM based on planar packaging technology, featuring integrated snubber capacitors, an integrated gate driver, and successfully applying non-invasive temperature estimation concepts. The PM is developed for a $>98\,\%$ efficient 45 kW PEBB aiming to facilitate a standardization process in power electronics for MEA. **Section 2** provides the specifications of the PM, presents preliminary design considerations and its general structure focusing on the adopted planar packaging technology. **Section 3** illustrates a practical solution for the temperature monitoring of power converters employing SiC MOSFETs in realistic operating conditions, supported by experimental results on the realized PM. **Section 4** introduces the designed gate driver before discussing switching waveforms measured on the PM in a double pulse test

(DPT) setup. Finally, **Section 5** concludes the paper.

2 Power Module Design

The system level specifications of the 3-Φ DC/AC inverter reported in **Table 1** support a preliminary analysis of the PM, which consists of a single-phase bridge-leg. The most significant design considerations are discussed in the first part of this section, before presenting estimated efficiency curves associated to the optimized hardware. Further investigations concerning the topology selection, and the design of the input and output filters are presented in [9]. In the second part of this section, the planar packaging technology at the basis of the manufacturing process of the PM is discussed in detail. Finally, the realized hardware is compared to state-of-the-art products.

2.1 Preliminary Considerations

A half-bridge topology is chosen for the PM to reduce the number of dies and to minimize its lateral dimension, the complexity of driving/wiring, as well as the overall cost. The nominal DC-link voltage V_{DC}, considering a safety margin, defines the minimum voltage rating of the power semiconductors to be integrated in the PM, while the high output current of the application at hand (see **Table 1**) makes devices with low on-state resistance $R_{ds,on}$ values preferable. Accordingly, the 1.2 kV 25 mΩ CPM2-1200-0025B [10] SiC MOSFET is selected. The minimal cooling capability available in the aircraft power bay limits the semiconductor loss budget of each single-phase PM to $150\,W = 0.01\,{}^{P_{out}}/_{3}$, corresponding to a PM efficiency $\eta = 99\,\%$. Additionally, the minimum switching frequency of the 3-Φ inverter is fixed at $f_{sw,min} = 30\,kHz$ to guarantee sufficient control dynamics [11], given the relatively high AC output frequency $f_{out} = 400\,Hz$.
The first degree-of-freedom in the realization of the PM is identified in the number N of dies to be connected in parallel to form each switch. For this reason, the estimated conduction losses P_{cond} and switching losses P_{sw} are calculated at the nominal operating point, i.e. at ${}^{P_{out}}/_{3} = 15\,kW$, for different values of N, with $f_{sw} = f_{sw,min}$, and considering a sinusoidal output current, i.e. neglecting the high frequency current ripple; in particular,

$$P_{cond} = \frac{R_{ds,on}(100\,°C)}{N} I_{out,RMS}^2, \tag{1}$$

is assumed for the conduction losses, while

$$P_{sw} = f_{out} N \sum_{\forall T_{sw} \in T_{out}} \left[k_0 + \left(k_1 \frac{I_{sw}}{N} \right) + k_2 \left(\frac{I_{sw}}{N} \right)^2 \right] \tag{2}$$

is derived for the switching losses. In (2), an appropriate value of switched current I_{sw} is selected for each switching period T_{sw} from the sampling of the output current i_{out}; thus, the dissipated switching energy E_{sw} is calculated in each T_{sw} and all contributions in one AC output period T_{out} are summed. Finally, the total switching energy is multiplied with f_{out}, determining P_{sw}. The coefficients $k_0 = 154\,\mu J$, $k_1 = 5.81\,V\mu s$, and $k_2 = 181\,\Omega ns$ are determined experimentally from switching loss measurements performed on a half-bridge featuring one of the selected power semiconductors per switch [4]. The results of these calculations are reported in **Fig. 1**, where also the total losses $P_{tot} = P_{sw} + P_{cond}$ are indicated (yellow). It is interesting to notice how P_{cond} (blue) drops inversely proportional to N as expected, while P_{sw} (red) features different trends with respect to N (and does not increase proportionally to it), depending on the dominant term in the sum in (2). Nevertheless, P_{tot} appears practically flat for $N \geq 6$, hence $N = 6$ is selected to minimise cost and size of the PM. Moreover, with $N = 6$, the loss budget of 150 W is already reached with $f_{sw} = f_{sw,min}$, hence f_{sw} is fixed to 30 kHz. Separate anti-parallel SiC Schottky diodes are not considered, since their benefit is not yet proven [12].
The described loss models are considered as well to calculate the expected η of the PM with $N = 6$ for different values of f_{sw} and $I_{out,RMS}$. The results of this procedure are summarized in **Fig. 2**. In particular, **Fig. 2(a)-(b)** offer a cross-sectional view of the 3D plot shown in **Fig. 2(c)** in

Table 1 Nominal operating point of the analysed three-phase DC/AC inverter.

	Description	Value
V_{DC}	DC-link voltage	540 V
f_{out}	AC output frequency	400 Hz
$V_{out,RMS}$	RMS AC output voltage	115 V
$I_{out,RMS}$	RMS AC output current	130 A
P_{out}	3-Φ output power	45 kW

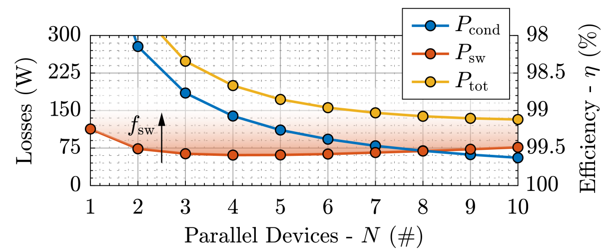

Figure 1 Semiconductor loss breakdown, i.e. conduction losses P_{cond} (blue), switching losses P_{sw} (red) and total losses P_{tot} (yellow), in dependence of the number N of dies connected in parallel to form each switch in the PM.

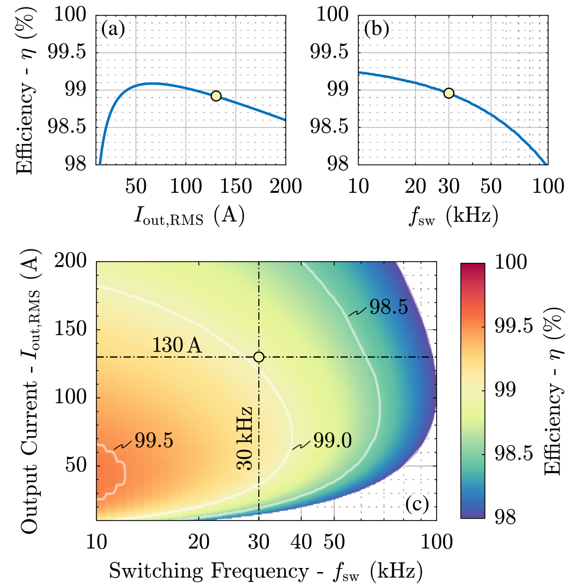

Figure 2 Efficiency η of the optimized PM ($N = 6$) for different values of switching frequency f_{sw} and RMS value of the output current $I_{out,RMS}$ ($P_{out} = 345\,I_{out,RMS}$[A] W). **(a)-(b)** Cross-sectional view of the η-map shown in **(c)** for $f_{sw} = 30\,kHz$ and $I_{out,RMS} = 130\,A$ ($P_{out} = 45\,kW$), respectively.

case of $f_{sw} = 30\,\text{kHz}$ and nominal output power, respectively. Thus, **Fig. 2(a)** provides an indication of the partial load efficiency of the PM, while **Fig. 2(b)** highlights how $\eta > 99\,\%$ can be achieved only with $f_{sw} \leq 30\,\text{kHz}$ as expected, which ultimately limits the possible downsizing of the filter elements. A further increase of f_{sw}, e.g. up to $100\,\text{kHz}$, would come at the expense of an efficiency reduction ($\eta = 98\,\%$), i.e. of a higher cooling requirement.

2.2 General Description

In addition to the described power stage formed by six SiC MOSFETs per half-bridge side, a *RC-C* snubber is added at the input of the PM between the DC terminals with the aim of reducing the power loop inductance, i.e. of limiting switching node over voltage, and of damping the oscillations between the external DC-link capacitors and the fast switching devices. A detailed study on the design of the snubber network is carried out in [4].
The temperature of the PM is measured with two PTC temperature sensors [13] directly mounted on the substrate. Additionally, a shunt resistor [14] is used for measuring the output current. The complete PM layout is shown in **Fig. 3**, where all mentioned components are visible. The highly symmetric layout aims to evenly distribute the load current between the parallel dies, for conduction and during switching operation. The size of the PM and the requirement to provide input and output terminals at its short sides are constraints originating from the converter system design and result in relatively long DC bus-bars.

2.3 Planar Packaging Technology

In order to fully exploit the fast-switching capability of SiC MOSFETs, low power loop inductance values are crucial. The use of planar packaging technologies to eliminate aluminum (Al)-bond wires is the key to achieve low inductive PM designs [15]. In particular, a variation of the Siemens SIPLIT® technology [16] is used in this work. At the core of this technology, a thin insulation material separates the substrate copper (Cu) from a second metal layer. The second metal layer is obtained by a Cu electrodeposition process, while the structuring of the Cu layer is achieved in a photo-lithography step. The thickness of the Cu layer can be adjusted within a wide range to fulfill the requirements of the PM. In this case, a thickness of $75\,\mu\text{m}$ is selected. Additionally, in contrast to the original SIPLIT® technology, the process of the insulation material deposition and the epoxy-based material itself are altered. In particular, the insulation material is applied in an additive printing process and allows for high operating temperatures, i.e. well above $150\,°\text{C}$. Moreover, the PM is covered only with a top-insulation film as final coating to provide a terminal protective layer against electrical arcing, dirt and humidity, since there is no need for the conventional silicone gel. The SiC MOSFETs are attached to a silicon nitride (Si_3N_4) active metal brazed (AMB) substrate by a pressure assisted silver sintering process. The SMD capacitors and resistors forming the snubber network, the PTCs, as well as the shunt resistor, the bus bars, and the contact sleeves are soldered with a conventional lead-free soldering process. This soldering process is also applied for attaching the AMB substrate to the Cu baseplate. A schematic representation of the overall PM structure is depicted in **Fig. 4**, while the final hardware, including all components and the housing, is shown in **Fig. 5**.

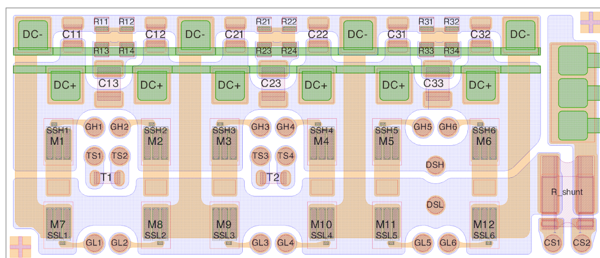

Figure 3 Layout of the I²MPECT PM highlighting the routing of the planar copper tracks and the placement of the different components on the substrate.

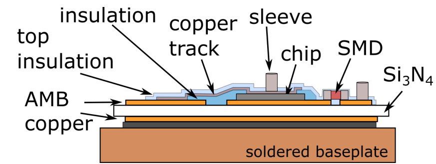

Figure 4 Schematic cross-section of the PM showing the different layers and components/materials considered during the manufacturing process.

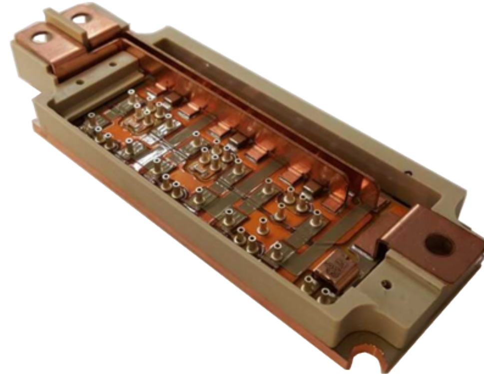

Figure 5 Picture of the I²MPECT PM. The DC input and AC output terminals are placed at the opposite short sides. Contact sleeves are used for inserting e.g. press-fit pins to contact the gate driver board.

2.4 Comparison to State-of-the-Art

Until 2024, the compound annual growth rate (CGAR) of SiC power devices is predicted to approach $30\,\%$ [22]. Confirming this trend, nowadays, more and more full-SiC PMs are available on the market, both from well established IGBT PM manufactures, e.g. Infineon and Semikron, as well as from manufactures of SiC semiconductors, e.g. Cree and ROHM. **Table 2** compares selected parameters of off-the-shelf full-SiC PMs with the I²MPECT PM described in this paper. All PMs in **Table 2** have an half-bridge structure and a voltage rating of $1200\,\text{V}$, while their current ratings range from $200\,\text{A}$ to $631\,\text{A}$, and their $R_{DS,on}$ values vary from $2.5\,\text{m}\Omega$ to $7.5\,\text{m}\Omega$. Only three out of the five analysed PMs feature external anti-parallel SiC-Schottky diodes and/or a baseplate. The presence of the baseplate and its material influence the volume and the weight of the PM, respectively; however, the heat-spreading enabled by the baseplate significantly increases the power dissipation capability of the PM. The size of the I²MPECT PM approaches the benchmark PM from Cree [17], but several additional features are integrated in its case, i.e. two temperature sensors, a current

Table 2 Comparison of different 1200 V half-bridge full-SiC PMs [17–21].

Manufacturer Part Number	Cree CAS325M12HM2	ROHM BSM300D12P2E001	MicroSemi MSCMC120AM03CT6LIAG	Infineon FF6MR12W2M1	Semikron SK250MB120SCTE2	I^2MPECT
Max. DC Current (A) @ $T_j = 175\,°C$	444	300	631	200	249	381[a]
$R_{DS,on}$ (mΩ) @ $T_j = 25\,°C$	3.7	7.3	2.5	5.6	7.5	4.2
Max. Power (W) @ $T_c = 25\,°C$	1500	1875	2780[a]	457[a]	1000[a]	1270[a]
Inductance (nH)	5	13	3	8	6	0.55[c]
Diodes[b]	w/	w/	w/	w/o	w/o	w/o
Baseplate	AlSiC	Cu	Cu	w/o	w/o	Cu
Volume (cm^3)	79	160	114	43	43	81
Weight (g)	140	349	320	39	35	177

[a] calculated [b] anti-parallel SiC Schottky [c] w/ snubber, 15 nH between DC+ and DC- terminals w/o snubber

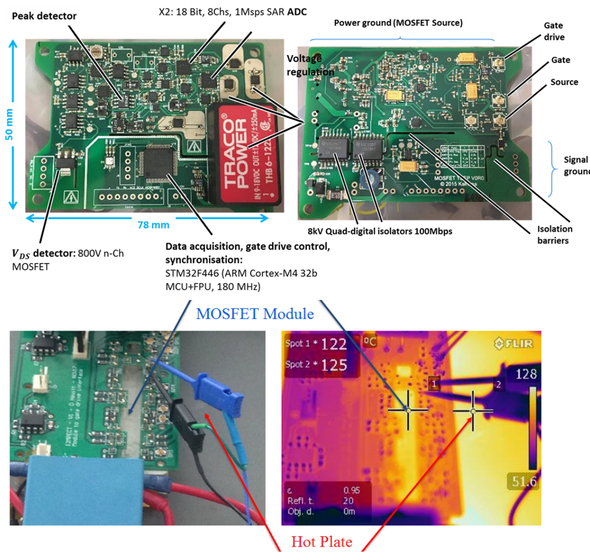

Figure 6 TSEPs data acquisition board and view of the PM operated at 125 °C.

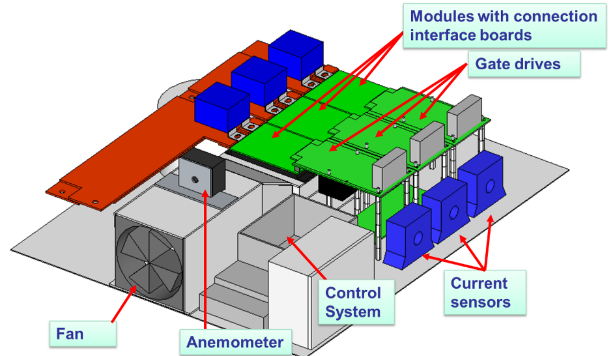

Figure 7 Power converter prototype considered for the validation of the TSEP monitoring procedure.

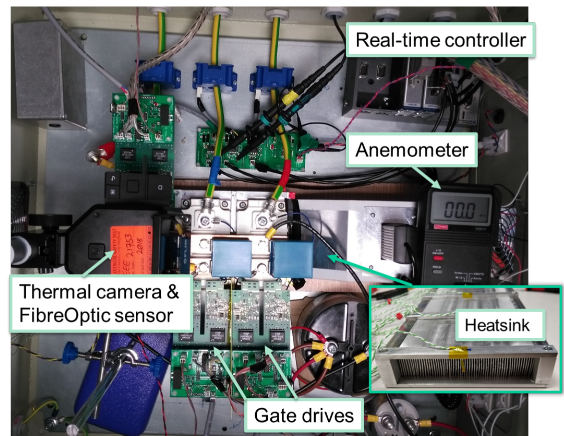

Figure 8 Test rig considered for the validation of the TSEP monitoring procedure.

sensor, a snubber network, individual gate and source contacts as well as two integrated gate driver printed circuit boards (PCBs). The integration of the snubber reduces the stray inductance of the I^2MPECT PM to 0.55 nH (according to simulation), significantly lower than the state-of-the-art.

3 Real-Time Temp. Monitoring

A number of studies have been published on the use of TSEPs for SiC power devices. In [23], it is demonstrated that the quasi-threshold voltage v_{th} and the on-state voltage $v_{DS,on}$ show good sensitivity to temperature variation and linearity over a wide operating range. A practical data acquisition and TSEP monitoring board are presented in [23] and shown in **Fig. 6**. Convenient circuit implementation for triggering the measurement and transferring them to a suitable analog-digital converter (ADC) are also discussed in [23]. Here, the application to the real-time monitoring of the PM in a realistic power converter is demonstrated. A series of DPTs are conducted at controlled junction temperatures T_j in order to characterize v_{th} and $v_{DS,on}$ as functions of T_j. Hence, calibration tables to be used as look-up tables, i.e. to correlate the measured quantities to T_j in a real-time implementation, are built. Since $v_{DS,on}$ is a function of both on-state current i_{DS} and temperature, a 2D look-up table is constructed. A prototype converter using the PM described in this paper is realized for the purpose of validating the proposed TSEP monitoring solution in a realistic application, as illustrated in **Figs. 7** and **8**.

The converter is operated in steady state with $f_{sw} = 20\,kHz$, controlling $I_{out} = 90\,A$ at $f_{out} = 200\,Hz$ into an R-L load. The temperature on the MOSFET surface is measured directly using a thermal camera (FLIR ETS320) and a fibre optic temperature measurement system (a Opsens Coresens GSX-2-N module and an OTF-F temperature sensor) for comparison with the proposed TSEP concept

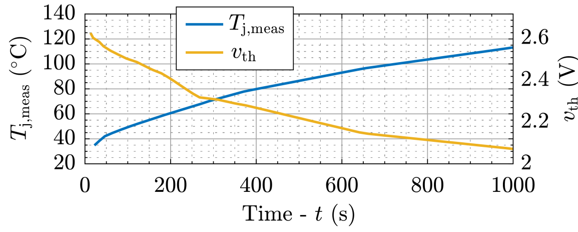

Figure 9 Measured threshold voltage v_{th} (yellow) for varying device temperature T_j (blue).

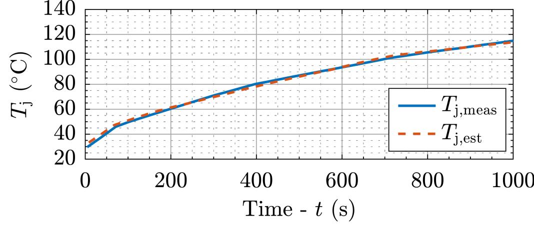

Figure 10 Measured $T_{j,meas}$ (blue) and estimated $T_{j,est}$ (red) device temperatures using v_{th} as TSEP.

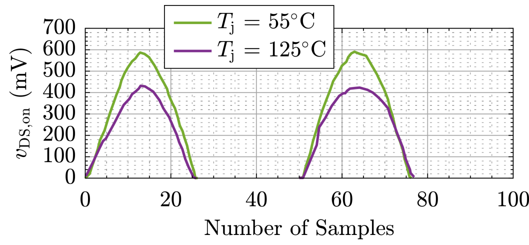

Figure 11 Measured on-state voltage $v_{DS,on}$ at two different T_j.

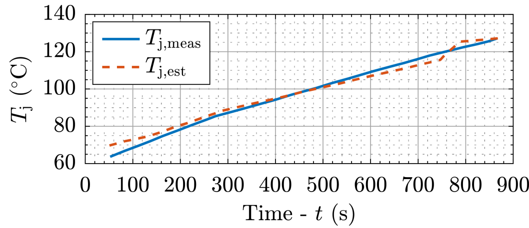

Figure 12 $T_{j,meas}$ (blue) and $T_{j,est}$ (red) using $v_{DS,on}$ as TSEP.

and validation of the proposed methodology. Exemplary results of the TSEP monitoring are illustrated in **Figs. 9-12**. In particular, **Fig. 9** shows the measured v_{th} over a period of about 17 min. The temperature estimated by the reverse look-up table $T_j(v_{th})$ is shown in **Fig. 10**, demonstrating a worst case error of less than 4 K. Similarly, **Fig. 11** shows the measured real-time $v_{DS,on}$ during positive current conduction, while **Fig. 12** shows the estimated temperature using the reverse look-up table $T_j(v_{DS,on}, i_{DS,on})$. The results demonstrate that both v_{th} and $v_{DS,on}$ are suitable TSEPs for SiC power devices, however, the isolation difficulties in the measurement of $v_{DS,on}$ and its current dependence, make v_{th} the most viable solution for a simpler and lower cost monitoring system.

4 Switching Performance

The operation of the full-SiC PM presented in **Section 2** is validated in this section, after introducing the designed gate driver.

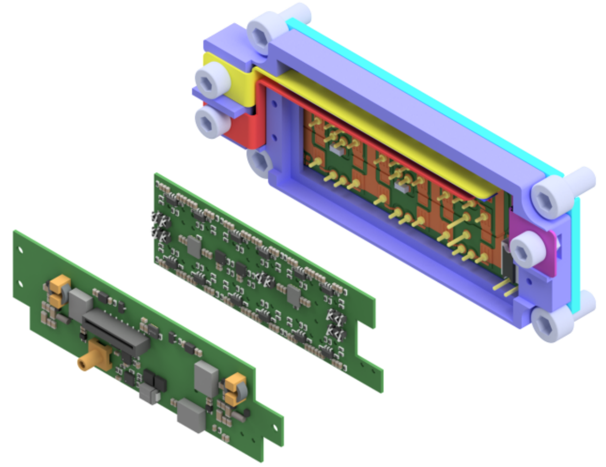

Figure 13 Exploded view of the PM with the two gate driver boards. Both PCBs are integrated into the housing.

4.1 Gate Driver

Commercial gate drivers for PMs typically offer a single connector to the PM and are mounted on top of it, hence they suffer from large and asymmetric parasitic gate loop inductances and lead to a significant volume increase. Differently, the designed gate driver circuit is integrated in the housing of the PM, and its functionalities are distributed in two compact PCBs to fully utilize the available space. The two PCBs are shown together with the PM in a 3D model in **Fig. 13**.

The inner board contains two (one per side) isolated gate driver ICs [24], each of them connected to six (one per die) dedicated push-pull current amplifiers [25]. This distributed driving approach ensures symmetric and minimized gate loop inductances. Thus, symmetric current sharing is facilitated also during the switching transitions. Furthermore, high driving currents are obtained, which ultimately enable high switching speeds.

The outer board hosts the sensing circuitry, e.g. substrate temperature, output current and on-state voltage measurements, and other secondary functionalities, e.g. power isolation and generation of the required supply voltage levels. Finally, a connector is placed to communicate with the external control board, which provides the main supply voltage and the PWM gate signals.

4.2 Double Pulse Test Measurement

To prove the proper functioning of the designed PM and to reveal the improvement enabled by the integration of the snubber, DPT measurements are performed on the realised hardware. In the DPTs, $V_{DC} = 500$ V and I_{out} is increased up to 200 A. The switch node voltage v_{sw} is measured across the high-side MOSFETs with a 120 MHz differential probe (LeCroy HVD3106). The on- and off-state gate voltages are 22 V and -5 V, respectively. The drain current i_{sw} of the high-side MOSFETs is measured with a Rogowski-coil-based sensor (PEM CWT6UM) at the DC+ terminal. An inductor of 140 µH is connected to the AC terminal to control I_{out}.

The results of the successful DPTs, performed with and without the snubber on the same setup, are depicted in **Fig. 14**. First, the functioning of the realised PM at its nominal operating conditions is confirmed. Moreover, **Fig. 14** highlights how the use of the snubber greatly improves

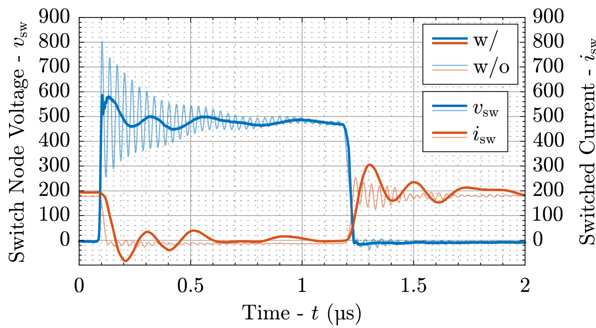

Figure 14 Switched voltage v_{sw} (blue) and current i_{sw} (red) waveforms measured on the PM with integrated gate driver. The figure shows a comparison of switching 200 A at $V_{DC} = 500$ V with and without snubber.

the switching behaviour of the PM. The turn-off overvoltage spike is strongly reduced from approximately 300 V to 90 V, i.e. is 70 % lower, at the same switching speed. Additionally, the amplitude of the voltage oscillations is greatly decreased and fades out in less than 400 ns, i.e. in less than 3 % of an average on-time. This allows to operate the PM with higher voltage safety margins or at a higher V_{DC} values, i.e. to reduce the conduction losses, or to switch it at higher switching speeds, thus reducing the switching losses.

5 Conclusion

High efficiency, reliability and power density are the key cornerstones for the further electrification of air transport. Meanwhile, SiC MOSFETs are emerging as the semiconductor of choice for power conversion in demanding applications; however, there is a lack of standardised PEBBs suitable for the aerospace industry, which limits the applicability of this promising technology.
The design procedure and performance of the compact and light-weight full-SiC PM with integrated snubber, gate driver, and sensing technologies demonstrated in the *Horizon2020* European Project - I^2MPECT are summarised in this paper. For the realization of the PM, a novel planar packaging technology, based on the Siemens SIPLIT® process, is employed. This approach offers significant benefits in terms of switching performances due to the avoidance of wire-bonding; moreover, it allows high temperature operation, thanks to a novel insulation material which replaces the traditional silicone gel coating. Comparative assessments against a number of commercially available full-SiC PMs demonstrate the advantages enabled by the proposed solutions in a number of key performance metrics, including low $R_{DS,on}$ and low parasitic inductance values, and high power-to-weight ratio. Additionally, significant progress in integration technologies are validated by means of experiments on the PM. The PM is operated up to 500 V and 200 A, focusing on the performance of the integrated snubber and gate driver including the sensing functions. Moreover, a novel online temperature measurement solution for health-monitoring, based on TSEPs, is successfully evaluated. The obtained results pave the way for the realization of a highly compact and reliable WBG PEBB, which can be the foundation for further adoption of SiC technologies in MEA, ultimately providing a best-in-class solution contributing to next-generation clean and reliable aerospace industry products.

6 Acknowledgement

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