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Stability and Robustness Analysis of $\mathrm{d}/\mathrm{d}t$-Closed-Loop IGBT Gate Drive

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***Abstract*—Closed-loop IGBT switching trajectory control by means of an active IGBT gate drive (AGD) ensures an operation of the IGBT in the SOA and enables the minimization of switching delays, switching losses and EMI.**

In this paper the closed-loop control of $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ by the use of an AGD is investigated on the basis of control-oriented small signal IGBT modeling and the analysis of IGBT module parasitics. Therewith, analytical stability considerations are carried out employing root-locus plots. Furthermore, the transfer functions for different closed-loop controlled IGBT modules are analyzed in dependency of their parameter variations and parasitic inductances. A closed-loop AGD prototype is used to experimentally test, verify and comparatively evaluate the switching behavior of the different considered IGBT modules.

I. Introduction

IGBT modules are widely used in clamped inductive load (hard) switching voltage source power electronic converters, cf. Fig. 1 (a), such as inverters for drives or switched mode power supplies, wherefore the equivalent circuit depicted in Fig. 1 (b) can be considered to investigate the switching behavior.

Contrary to state of the art passive gate driving topologies, the closed-loop control of the IGBT's switching trajectories by means of an active gate drive (AGD) concept compensates the parameter dependencies and non-linearities of the IGBT [1]. This enables accurately specified current- and voltage waveforms of the IGBT at hard switching for the entire operating and temperature range. As a consequence, this ensures the operation of the IGBT in the safe operating area (SOA), i.e. with limited diode reverse recovery current at turn-on and turn-off overvoltage, and enables to minimize the switching delays, the switching losses and the EMI.

Controlling the current- and / or voltage time derivatives, i.e. $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$, is a promising concept to achieve a high bandwidth closed-loop switching trajectory control [1–10]. Since the current and voltage slopes are basically separated at hard switching, in previous work [1] a concept based on [8, 9] was proposed, where both $\mathrm{d}/\mathrm{d}t$-control loops are joined using a common PI-control amplifier, that is controlling $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ as well as $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$. The block diagram of this proposed $\mathrm{d}/\mathrm{d}t$-closed-loop AGD is depicted in Fig. 2. This approach operates without detection and triggering of the active control loop, which otherwise is needed for the case of individual control loops [6, 7], and thus enables a very simple, fast and efficient way of controlling $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$.

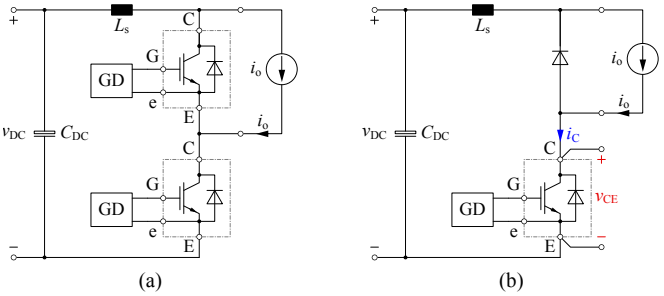

Fig. 1: (a) IGBTs with anti-parallel diodes in voltage source half-bridge configuration feeding a current impressing, i.e. inductive, load. (b) Corresponding equivalent circuit for the commutation from the IGBT to the opposite diode and vice versa; L_s considers the commutation loop inductance.

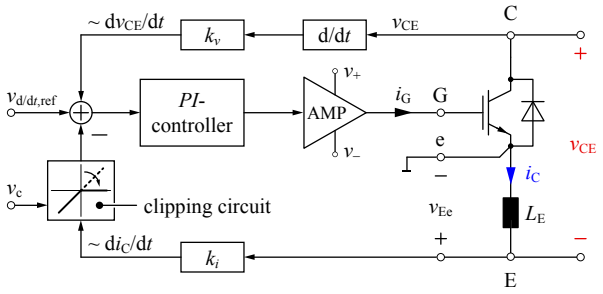

Fig. 2: Block diagram of the basic proposed closed-loop active gate drive concept with joined $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control loops [1].

In order to verify and ensure the operation of the AGD's $\mathrm{d}/\mathrm{d}t$-closed-loop switching trajectory control in the whole load current range and for devices of different manufacturers, the stability and robustness with regard to the parameter dependencies must be investigated. Since the control depends on the measurement and control circuitry of the AGD, the IGBT's characteristics and the parasitics, control-oriented models of the AGD and the IGBT are used in this paper as a basis for the stability analysis. Subsequently, the parasitics of different IGBT modules will be compared and their physical reason will be pointed out. By means of modeling the $\mathrm{d}/\mathrm{d}t$-closed-loop AGD, the IGBTs and the parasitics, small signal transfer functions will be derived for the current- and voltage slopes of

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$A_{\mathrm{DC,OP}}$	$f_{\mathrm{T,OP}}$	$f_{\mathrm{c,AMP}}$	τ_V	τ_I
100 dB	350 MHz	100 MHz	1 ns	1 nH

TABLE I: Parameter values of the AGD circuit.

the switching transients, in order to evaluate the control bandwidth, stability and robustness for the different IGBT modules. Finally, experimental measurements of different IGBT modules being actively controlled by means of a prototype of the $\mathrm{d}/\mathrm{d}t$-closed-loop AGD are used to verify the stability considerations made.

II. Control-oriented modeling

Key issue of any closed-loop control is system stability. In order to analyze the $\mathrm{d}/\mathrm{d}t$-closed-loop switching trajectory control regarding stability and robustness, models of the proposed AGD and the IGBT are needed. Considering the non-linearity of the IGBT behavior, a small signal approach is suitable for this kind of analysis [11–17]. Corresponding models are described out in the following.

A. Model of the closed-loop gate drive

The PI-controller of the $\mathrm{d}/\mathrm{d}t$-closed-loop AGD, cf. Fig. 2, is composed of a high-bandwidth operational amplifier, whose transfer function can be modeled as

$$G_{\mathrm{OP}} = \frac{A_{\mathrm{DC,OP}}}{s\frac{A_{\mathrm{DC,OP}}}{2\pi f_{\mathrm{T,OP}}} + 1}, \tag{1}$$

where $A_{\mathrm{DC,OP}}$ denominates the DC-gain of the amplifier and $f_{\mathrm{T,OP}}$ the transit frequency. Since the operational amplifier is wired in a non-inverting PI-configuration, cf. [1], the transfer function of the PI-controller is given by

$$G_{PI} = \frac{G_{\mathrm{OP}}(sP + I)}{s(G_{\mathrm{OP}} + P) + I}, \tag{2}$$

where P denominates the proportional gain and I defines the integral part Is^{-1}. The output amplifier, that is used to provide the needed output current, can be modeled as low-pass filter, i.e.

$$G_{\mathrm{AMP}} = \frac{1}{s\frac{1}{2\pi f_{\mathrm{c,AMP}}} + 1}. \tag{3}$$

Positive $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback is used since the IGBT has an inverting characteristic for the voltage slope which is provided by means of an RC-high-pass filter,

$$H_{V,\mathrm{HP}} = \tau_V \frac{s}{s\tau_V + 1}, \tag{4}$$

where the time constant $\tau_V = R_V C_V$ corresponds to the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback gain, k_v, cf. Fig. 2, and specifies the corner frequency, $f_{\mathrm{c},V} = \frac{1}{2\pi\tau_V}$, of the high-pass filter. The voltage drop across the parasitic emitter bonding inductance, L_{E}, cf. Fig. 2, is utilized as the negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback,

$$H_{I,\mathrm{HP}} = \tau_I s, \tag{5}$$

where a $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback gain of $-\tau_I = -k_i L_{\mathrm{E}}$ results. The corresponding parameters related to the AGD circuit's transfer functions are provided in Table I.

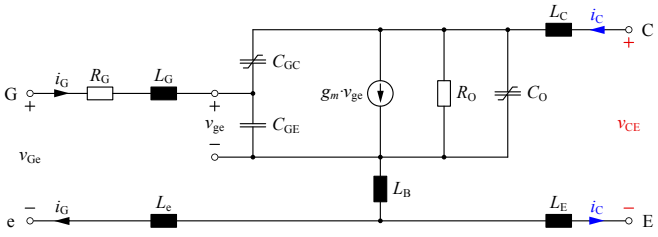

Fig. 3: Small signal IGBT model valid in the active region with parasitic inductances of the bond wires and / or the electrical terminals.

B. Control-oriented IGBT model

A small signal IGBT model for the active operating region as used in [11–17] and shown in Fig. 3 can be employed as a basis for the investigation of the $\mathrm{d}/\mathrm{d}t$-closed-loop switching trajectory control.

By means of this IGBT model, the transfer functions from the gate voltage, $V_{\mathrm{Ge}}(s)$, to the collector-emitter voltage, $V_{\mathrm{CE}}(s)$, and to the collector current, $I_{\mathrm{C}}(s)$, can be derived. Since the boundary conditions for the switching trajectories, that are defined by the clamped inductive load switching circuit as shown in Fig. 1, are different for the voltage- and current slope, the transfer functions are derived separately in the following.

1) Interval of $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control: In this interval, i.e. for the voltage slope, i_{C} is impressed by the inductive load, cf. Fig. 1, and is therefore assumed to be constant. Accordingly, the transfer function from the gate voltage to the collector-emitter voltage based on Fig. 3 can be calculated as per [14, 15],

$$G_V = \frac{V_{\mathrm{CE}}}{V_{\mathrm{Ge}}} = \frac{a_3 s^3 + a_2 s^2 + a_1 s + a_0}{b_3 s^3 + b_2 s^2 + b_1 s + b_0}, \tag{6}$$

with the coefficients

$$\begin{aligned}
a_0 &= -g_m R_{\mathrm{O}} \\
a_1 &= R_{\mathrm{O}} C_{\mathrm{GC}} \\
a_2 &= L_{\mathrm{B}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
a_3 &= L_{\mathrm{B}} R_{\mathrm{O}} C_{\mathrm{t}} \\
b_0 &= 1 \\
b_1 &= R_{\mathrm{O}}(C_{\mathrm{GC}} + C_{\mathrm{O}}) + R_{\mathrm{G}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
b_2 &= R_{\mathrm{O}} R_{\mathrm{G}} C_{\mathrm{t}} + (L_{\mathrm{Ge}} + L_{\mathrm{B}})(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
b_3 &= R_{\mathrm{O}} C_{\mathrm{t}}(L_{\mathrm{Ge}} + L_{\mathrm{B}}) \\
C_{\mathrm{t}} &= C_{\mathrm{GE}} C_{\mathrm{GC}} + C_{\mathrm{GE}} C_{\mathrm{O}} + C_{\mathrm{GC}} C_{\mathrm{O}},
\end{aligned} \tag{7}$$

which is in accordance with [14, 15] and is given here for the sake of completeness and easier reference. The inductances in the gate path can be joined according to $L_{\mathrm{Ge}} = L_{\mathrm{G}} + L_{\mathrm{e}}$.

2) Interval of $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control: In this interval, i.e. for the current slope, v_{CE} is clamped by the diode to the DC-link, cf. Fig. 1, and is thus assumed to be constant. Accordingly, the transfer function from the gate voltage to the collector current

based on Fig. 3 is

$$G_I = \frac{I_\mathrm{C}}{V_\mathrm{Ge}} = \frac{c_3 s^3 + c_2 s^2 + c_1 s + c_0}{d_4 s^4 + d_3 s^3 + d_2 s^2 + d_1 s + d_0}, \quad (8)$$

with the coefficients

$$\begin{aligned}
c_0 &= g_m R_\mathrm{O} \\
c_1 &= -R_\mathrm{O} C_\mathrm{GC} \\
c_2 &= -L_\mathrm{B}(C_\mathrm{GE} + C_\mathrm{GC}(1 + g_m R_\mathrm{O})) \\
c_3 &= -L_\mathrm{B} R_\mathrm{O} C_\mathrm{t} \\
d_0 &= R_\mathrm{O} \\
d_1 &= L_\mathrm{CE} + L_\mathrm{B}(1 + g_m R_\mathrm{O}) + R_\mathrm{G} R_\mathrm{O}(C_\mathrm{GE} + C_\mathrm{GC}) \\
d_2 &= R_\mathrm{G}(L_\mathrm{CE} + L_\mathrm{B})(C_\mathrm{GE} + C_\mathrm{GC}(1 + g_m R_\mathrm{O})) \\
&\quad + R_\mathrm{O}(C_\mathrm{GE}(L_\mathrm{B} + L_\mathrm{Ge}) + C_\mathrm{GC}(L_\mathrm{CE} + L_\mathrm{Ge}) \\
&\quad + C_\mathrm{CE}(L_\mathrm{CE} + L_\mathrm{B})) \\
d_3 &= R_\mathrm{G} R_\mathrm{O} C_\mathrm{t}(L_\mathrm{CE} + L_\mathrm{B}) \\
&\quad + L_\mathrm{t}(C_\mathrm{GE} + C_\mathrm{GC}(1 + g_m R_\mathrm{O})) \\
d_4 &= L_\mathrm{t} R_\mathrm{O} C_\mathrm{t} \\
C_\mathrm{t} &= C_\mathrm{GE} C_\mathrm{GC} + C_\mathrm{GE} C_\mathrm{O} + C_\mathrm{GC} C_\mathrm{O} \\
L_\mathrm{t} &= L_\mathrm{CE} L_\mathrm{Ge} + L_\mathrm{CE} L_\mathrm{B} + L_\mathrm{Ge} L_\mathrm{B},
\end{aligned} \quad (9)$$

where the inductances in the power- and gate paths can be joined according to $L_\mathrm{CE} = L_\mathrm{C} + L_\mathrm{E}$ and $L_\mathrm{Ge} = L_\mathrm{G} + L_\mathrm{e}$.

C. Transfer functions

On the basis of the derived AGD and IGBT models, the block diagrams representing the voltage- and current slope control are depicted in Fig. 4. Accordingly, the open-loop transfer functions from the reference signal to the voltage and current time derivative values are given by

$$G_{V,\mathrm{OL}} = \frac{V_{\mathrm{d}v/\mathrm{d}t}}{V_{\mathrm{d}/\mathrm{d}t,\mathrm{ref}}} = G_{PI} G_\mathrm{AMP} G_V H_{V,\mathrm{HP}}, \quad (10)$$

$$G_{I,\mathrm{OL}} = \frac{V_{\mathrm{d}i/\mathrm{d}t}}{V_{\mathrm{d}/\mathrm{d}t,\mathrm{ref}}} = G_{PI} G_\mathrm{AMP} G_I H_{I,\mathrm{HP}}. \quad (11)$$

Out of that, the corresponding closed-loop transfer functions based on positive $V_{\mathrm{d}v/\mathrm{d}t}$ and negative $V_{\mathrm{d}i/\mathrm{d}t}$ feedback can be derived,

$$G_{V,\mathrm{CL}} = \frac{G_{V,\mathrm{OL}}}{1 - G_{V,\mathrm{OL}}}, \quad (12)$$

$$G_{I,\mathrm{CL}} = \frac{G_{I,\mathrm{OL}}}{1 + G_{I,\mathrm{OL}}}. \quad (13)$$

As will be shown later, the parasitic inductances of an IGBT module are key parameters regarding the closed-loop $\mathrm{d}/\mathrm{d}t$-controllability. For that reason, the mechanical setup and the corresponding parasitic inductances of three IGBT modules from different manufacturers will be investigated and compared in the next section.

III. IGBT Module Construction and Parasitics

Parasitic inductances of an IGBT module are typically undesired; on the one hand, the total inductance in the power path L_pp, that is basically the sum of the low-side and high-side IGBT's parasitic inductances L_C, L_B and L_E according to Fig. 3, contributes to the stray inductance, L_s, in the commutation path, which is directly proportional to the overvoltage at the IGBT's turn-off transients. On the other hand, as will be shown, the inductance in the gate loop L_gl, that corresponds to the sum of L_G, L_B and L_e referred to the IGBT model of Fig. 3, is negatively affecting the achievable control bandwidth of the closed-loop IGBT gate drive.

Main physical reason of an IGBT module's parasitic inductances is the mechanical setup consisting of the screw terminals for the power connections, the gate drive terminals and the internal wiring, e.g. via bond wires. Three IGBT half-

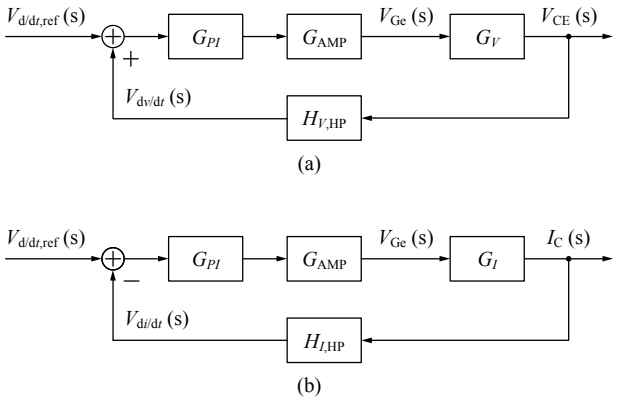

Fig. 4: Block diagram representation of the closed-loop (a) voltage- and (b) current slope control. G_{PI} corresponds to the PI-controller, G_AMP to the output amplifier, G_V and G_I to the small signal transfer functions of the IGBT and finally $H_{V,\mathrm{HP}}$ and $H_{I,\mathrm{HP}}$ to the high-pass feedbacks according to equations (2) to (9).

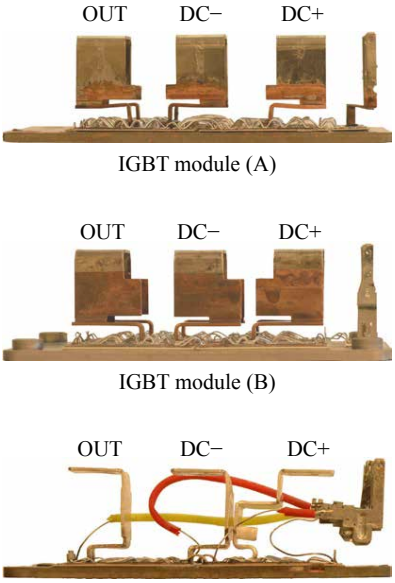

Fig. 5: Side view of the disassembled half-bridge IGBT modules of manufacturers (A) - (C) with visible construction of the screw terminals for the power connections.

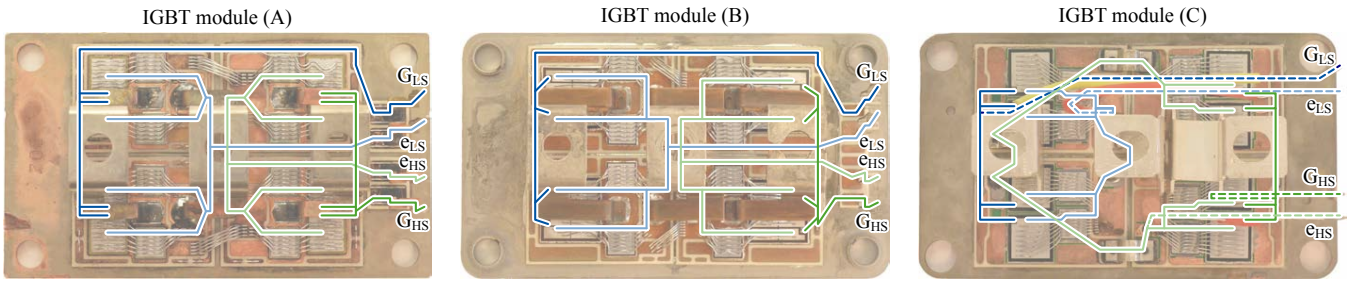

Fig. 6: Top view of the half-bridge IGBT modules of manufacturers (A) - (C) with highlighted the gate- and auxiliary emitter connections (solid: bond wire connections; dashed: silicon insulated cabling).

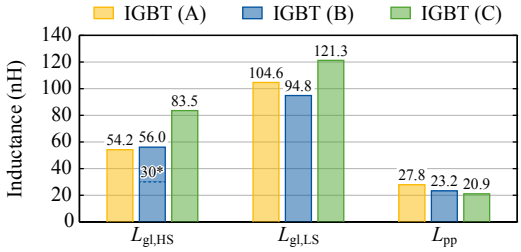

Fig. 7: Measured gate loop inductances between the gate and auxiliary emitter terminals for the high-side IGBT, $L_{\mathrm{gl,HS}}$, and low-side IGBT, $L_{\mathrm{gl,LS}}$, as well as the total inductance in the power path, L_{pp}, i.e. from the DC+ to the DC- connector (with a straight connection of both terminals for closing the measurement loop), for the different IGBT modules (A), (B) and (C). *In case a low-inductance coaxial connection to the foot ends of the terminals, i.e. a direct connection to the corresponding pads of the DBC would be used, the parasitic gate loop inductance could be considerably reduced, as shown for module (B)*.

bridge modules from different manufacturers in the $1.2\,\mathrm{kV}$ class with current ratings of $400 - 450\,\mathrm{A}$ (all in $62\,\mathrm{mm}$ housing) have been disassembled, in order to illustrate and compare their mechanical setups and parasitic inductances.

Fig. 5 depicts the construction of the IGBT module's power terminals which are a main reason for the parasitic inductance in the power path, L_{pp}. It's apparent that the DC+ and DC− terminals of modules (A) and (B) are located side by side, whereas a coplanar, i.e. low-inductive, layout is employed for module (C). According to the measured inductance values depicted in Fig. 7, module (C) exhibits the lowest L_{pp} value as a result of it's coplanar layout and module (A) shows the largest value for L_{pp} due to the parallel layout with large geometrical distance.

The module's internal gate and auxiliary emitter wirings are highlighted in Fig. 6, to compare the different manufacturing approaches. Bond wires are employed for modules (A) and (B) to interconnect the gate drive terminals and the IGBT chips resulting in similar values of the gate loop inductances, cf. Fig. 7. Module (C) uses, in addition to the bond wires, silicon insulated cables for the connection from the module terminals to the baseplate, what results in additional wiring loops and thus increased gate loop inductances.

Since the gate drive terminals are located next to the high-side IGBT and diode chips, the gate loop of the low-side IGBT is considerably larger than the one for the high-side device as depicted in Fig. 6. Accordingly, larger values result for the measured low-side gate loop inductance, $L_{\mathrm{gl,LS}}$, than for the high-side inductance, $L_{\mathrm{gl,HS}}$, as shown in Fig. 7.

In order to investigate and experimentally verify the impact of reduced parasitic gate loop inductance on the closed-loop control, the high-side gate drive terminals of module (B) have been bypassed by a low-inductive coaxial connection. Therewith, $L_{\mathrm{gl,HS}}$ of module (B) was reduced by $26\,\mathrm{nH}$ and / or $46\,\%$ as illustrated in Fig. 7. This modified module is henceforth denominated as module (B).

IV. Stability Analysis

A fundamental property of the proposed closed-loop AGD is that both $\mathrm{d}/\mathrm{d}t$-control loops are joined using a common PI-control amplifier, that is controlling the current and voltage slopes subsequently and / or individually, since they are basically separated on time at switching of inductive load currents. This also allows to independently investigate the closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control, under the condition that the PI-controller parameters are identical for both control loops.

In order to determine the closed-loop transfer functions, the IGBT model parameter values according to Fig. 3 are required and will thus be given in the following.

A. Small signal IGBT model parameters

All parameter values are summarized in Table II. On the basis of the IGBT's data sheet, the values for the transconductance, g_m, at an average switched current of $200\,\mathrm{A}$, the gate capacitance,

$$C_{\mathrm{GE}} = C_{\mathrm{ies}} - C_{\mathrm{res}}, \tag{14}$$

and the Miller capacitance,

$$C_{\mathrm{GC}}(v_{\mathrm{CE}}) \approx C_{\mathrm{GC,ref}} \sqrt{\frac{v_{\mathrm{CE,ref}}}{v_{\mathrm{CE}}}}, \tag{15}$$

at an average switched voltage of $300\,\mathrm{V}$ can be extracted. The output capacitance,

$$C_{\mathrm{O}} = C_{\mathrm{oes}} - C_{\mathrm{res}} \tag{16}$$

is assumed to be smaller by a factor of 10 than C_{GC}. R_{O} is typically not specified in the data sheet, thus a typical value for an $1.2\,\mathrm{kV}$, $400\,\mathrm{A}$ IGBT [11] is used. R_{G} and L_{E}

	g_m(S)	R_G(Ω)	L_B(nH)	L_E(nH)	L_C(nH)	L_G(nH)	L_e(nH)	C_{GE}(nF)	C_{GC}(nF)	C_O(nF)	R_O(Ω)
IGBT (A)	200	2	1	2.1	11	27.1	27.1	34.9	0.61	0.06	50
IGBT (B)*	200	2.05	1	3.85	6.75	15	15	26.9	0.32	0.03	50
IGBT (C)	200	1.62	1	3.2	6.25	41.7	41.7	23	0.87	0.09	50

TABLE II: Parameter values of the high-side IGBTs (A), (B)* and (C).

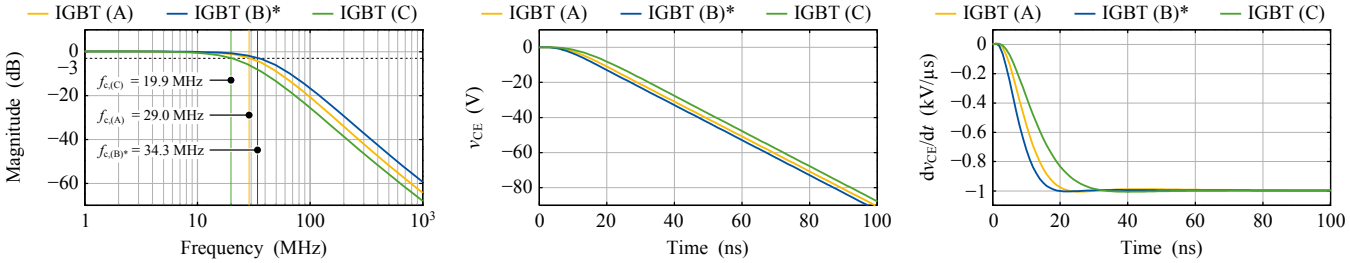

Fig. 8: Bode diagram, and v_{CE} and $\mathrm{d}v_{CE}/\mathrm{d}t$ step responses for a reference value step from 0 to $-1\,\mathrm{kV}/\mu\mathrm{s}$ for the closed-loop $\mathrm{d}v_{CE}/\mathrm{d}t$ control with the PI parameters according to Table III.

	P	I
IGBT (A)	3.75	$12.9 \cdot 10^7$
IGBT (B)*	1.34	$8.57 \cdot 10^7$
IGBT (C)	5.93	$14.5 \cdot 10^7$

TABLE III: PI parameter values for the high-side $\mathrm{d}v_{CE}/\mathrm{d}t$ control of modules (A), (B)* and (C).

have been measured for the high-side IGBTs by means of an impedance analyzer. The measured gate loop inductance, $L_{gl,HS}$, cf. Fig. 7, is assumed to be equally split to L_G and L_e. Further, L_B was estimated and L_C is assumed to be

$$L_C \approx L_{pp}/2 - L_B - L_E. \tag{17}$$

B. Closed-loop transfer functions

By means of the IGBT parameters, the closed-loop $\mathrm{d}/\mathrm{d}t$-transfer functions can be evaluated in dependency of the controller parameters. In a first step, the PI-controller was adjusted individually for each module to achieve a $\mathrm{d}v_{CE}/\mathrm{d}t$ control without overshoot in the step response. The P and I values for the different modules are given in Table III and the corresponding Bode diagram and step responses of the $\mathrm{d}v_{CE}/\mathrm{d}t$ control are depicted in Fig. 8.

As can be observed, a larger gate loop inductance, $L_{gl,HS} = L_G + L_e$, demands for higher P- and I values of the controller, in order to achieve the desired step response, and results in lower closed-loop control bandwidth, f_c. This behavior can be explained by the fact that the PI-controller is implemented by an operational amplifier with limited gain-bandwidth product. A higher controller gain, that is needed at larger gate loop inductance, reduces the control bandwidth, and in addition, leads to an increased applied gate voltage amplitude. Since in practice the output voltages of the operational- and the output amplifiers are limited to the supply voltages, v_+ and v_-, i.e. $\pm 15\,\mathrm{V}$, another (non-linear) reduction of the control dynamics may occur. For the sake of simplicity, this effect is not considered in this paper.

The PI-controller for the $\mathrm{d}i_C/\mathrm{d}t$ control is the same as for the $\mathrm{d}v_{CE}/\mathrm{d}t$ control, however the control loops are different in both cases. On the basis of the optimized $\mathrm{d}v_{CE}/\mathrm{d}t$ control, the closed-loop transfer function for the current slope control, $G_{I,CL}$, can be evaluated. The corresponding Bode diagram and step responses of the $\mathrm{d}i_C/\mathrm{d}t$ control are depicted in Fig. 9 (a). Since the controller is optimized for the $\mathrm{d}v_{CE}/\mathrm{d}t$ control, an unsatisfying performance of the $\mathrm{d}i_C/\mathrm{d}t$ control results, that is close to or even beyond the limit of stability as can be seen in Fig. 9 (a). In the following, two different solutions to overcome the problem of having only one PI-controller, that is used to control the two different $\mathrm{d}/\mathrm{d}t$-loops, are presented.

On the one hand, the controller can be optimized for the more sensitive, i.e. less stable, loop. In the present case, this would mean to adjust the PI-controller for the $\mathrm{d}i_C/\mathrm{d}t$ loop. Therewith, an optimal $\mathrm{d}i_C/\mathrm{d}t$ control could be achieved with the drawback that the control bandwidth of the $\mathrm{d}v_{CE}/\mathrm{d}t$ control would be below it's optimal value.

On the other hand, a degree of freedom is to add a gate- or Miller capacitance close to the IGBT chip, whereby the effective values for C_{GE} and C_{GC} would correspond to the sum of the IGBT's internal and the external capacitance values. Since i_C is controlled via the gate voltage and v_{CE} depends on the Miller capacitance's voltage, adding additional capacitance acts as low-pass filter to the corresponding loop. In the present case, the PI-controller could be adjusted for a fast $\mathrm{d}v_{CE}/\mathrm{d}t$ control and the $\mathrm{d}i_C/\mathrm{d}t$ loop could be adapted by means of additional gate capacitance to get a desired control behavior.

The performance of such a modification of the closed-loop $\mathrm{d}i_C/\mathrm{d}t$ control is depicted in Fig. 9 (b). Since the two control loops are decoupled at inductive switching, no interference of adding gate capacitance to the $\mathrm{d}v_{CE}/\mathrm{d}t$ control can be observed. The disadvantages of this solution are the increased gate drive charge and the difficulty to insert a capacitor close to the chip in practice.

C. Parameter variations

A verification of the control's robustness can be performed by investigating the impact of IGBT and controller parame-

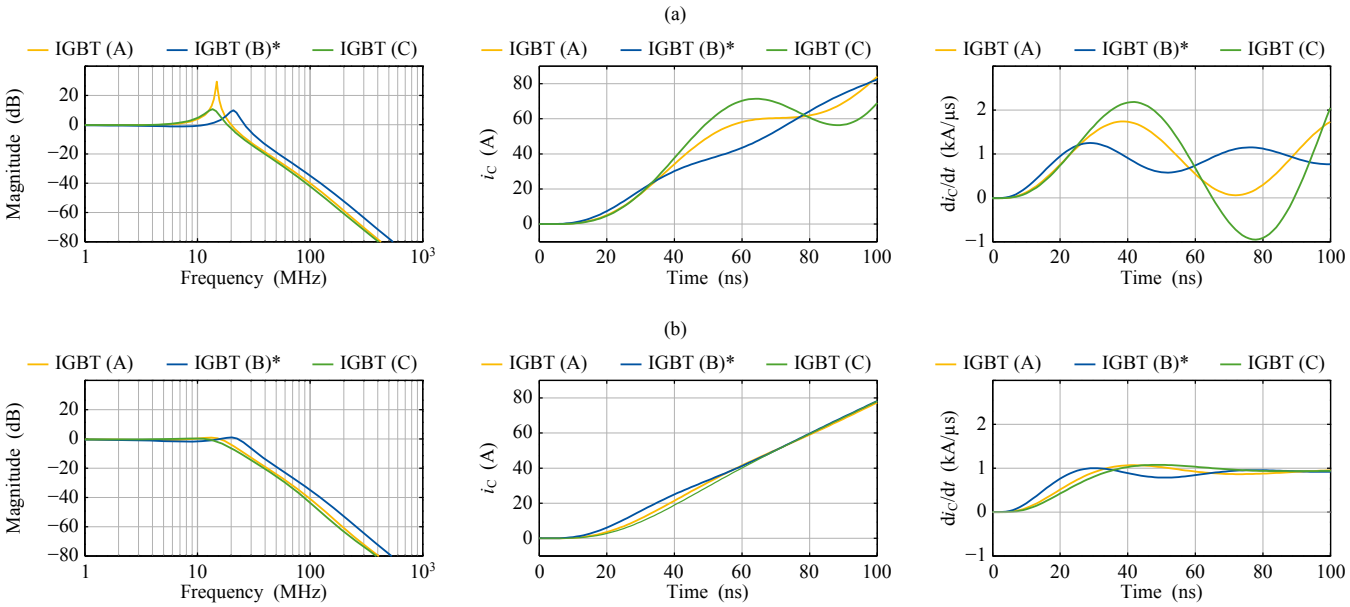

Fig. 9: Bode diagram, and i_C and di_C/dt step responses for a reference value step from 0 to $1\,\mathrm{kA}/\mu\mathrm{s}$ for the closed-loop di_C/dt control with the PI-controller optimized for the dv_{CE}/dt control. (a) without and (b) with increased gate-emitter capacitance, i.e. $C_{GE,(A),ext.} = 143\,\mathrm{nF}$, $C_{GE,(B)*,ext.} = 38\,\mathrm{nF}$ and $C_{GE,(C),ext.} = 230\,\mathrm{nF}$.

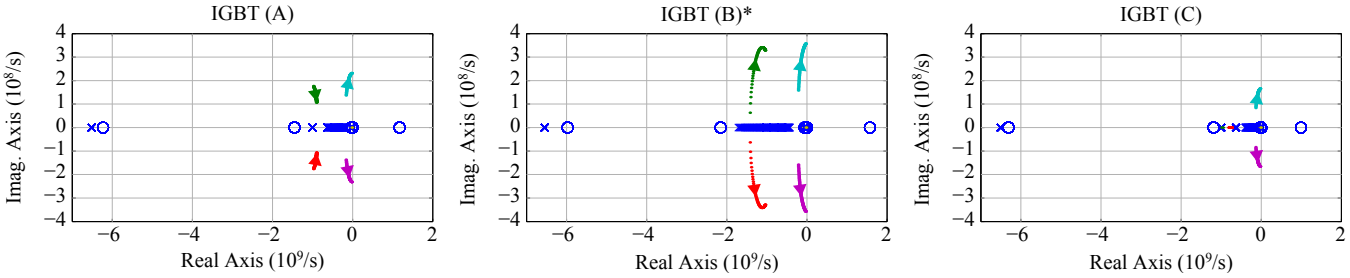

Fig. 10: Root locus plots for an increase of the controller's P-gain from 1 to 4-times the nominal value.

ter variations. According to Nyquist's stability criterion, the stability of a closed-loop system is given, if all poles of the corresponding open-loop transfer function are located in the open-left s-half plane.

To investigate the sensitivity of the controller, the root-locus plots of the dv_{CE}/dt loop for an increase of the P-gain up to 4-times the nominal value are depicted in Fig. 10. It can be seen for all IGBT modules, that the control is very close to the stability limits for the upper value of P. From the controller's side, there should accordingly not be a concern regarding stability, since in practice the P-gain is properly adjusted initially and then kept constant.

For the robustness analysis of the control with respect to the IGBT's parameters, root-locus plots of the dv_{CE}/dt loop for reduced Miller capacitance, cf. Fig. 11, and of the di_C/dt loop for increased transconductance, cf. Fig. 12, are evaluated.

Reducing the Miller capacitance down to 25 % of the nominal value as worst case assumption for high values of v_{CE} leads to a shifting of the pivotal poles of the dv_{CE}/dt control towards the right s-half plane, but the system is still stable. For the di_C/dt loop, the dominant poles are also shifted towards the right s-half plane for a 4-times higher transconductance, and therewith the system gets close to instability. Since this high value for g_m exceeds the specified values in the data sheets by far, no stability issues need to be expected in practice.

V. Experimental Results

By means of a closed-loop di_C/dt and dv_{CE}/dt AGD prototype, cf. Fig. 14, double pulse tests have been performed to obtain the hard switching waveforms for the different 1.2 kV, $400-450$ A IGBT modules. In Fig. 13, the turn-on waveforms for a variation of the load current i_o are depicted. IGBT module (B)*, expected to exhibit highest control bandwidth, shows the most accurately controlled di_C/dt and dv_{CE}/dt values. Slight oscillations are observable for module (A) and the controllability of module (C) is most demanding due to the high gate loop inductance and accordingly reduced control bandwidth. This result is in accordance with the expected behavior, i.e. the larger the gate loop inductance, L_{gl}, the lower the allowed gain of the controller for ensuring a stable operation and the less accurate and / or less stable the control.

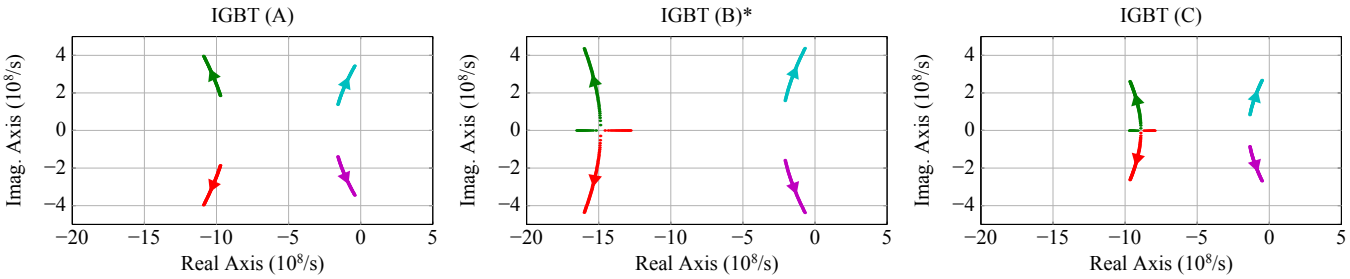

Fig. 11: Root locus plots (poles only) of the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control related to Fig. 8 for a decrease of the IGBT's Miller capacitance C_{GC} from nominal value, cf. Table II, down to a scaling factor of 0.25.

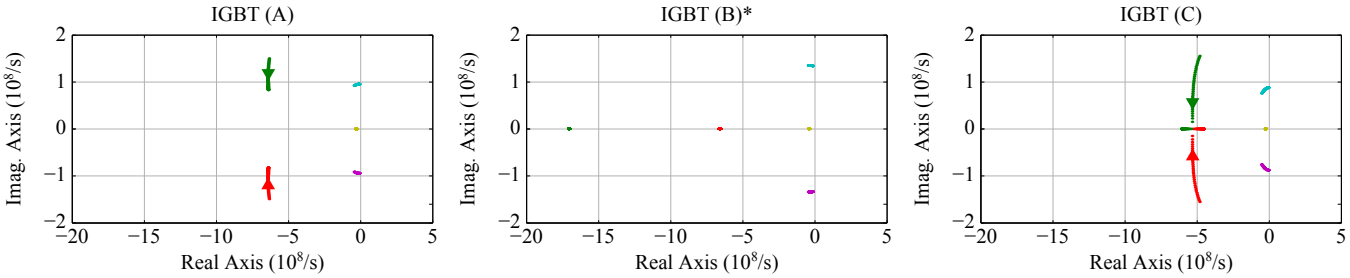

Fig. 12: Root locus plots (poles only) of the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control related to Fig. 9 (b) for an increase of the IGBT's transconductance g_m from nominal value, cf. Table II, up to a scaling factor of 4.

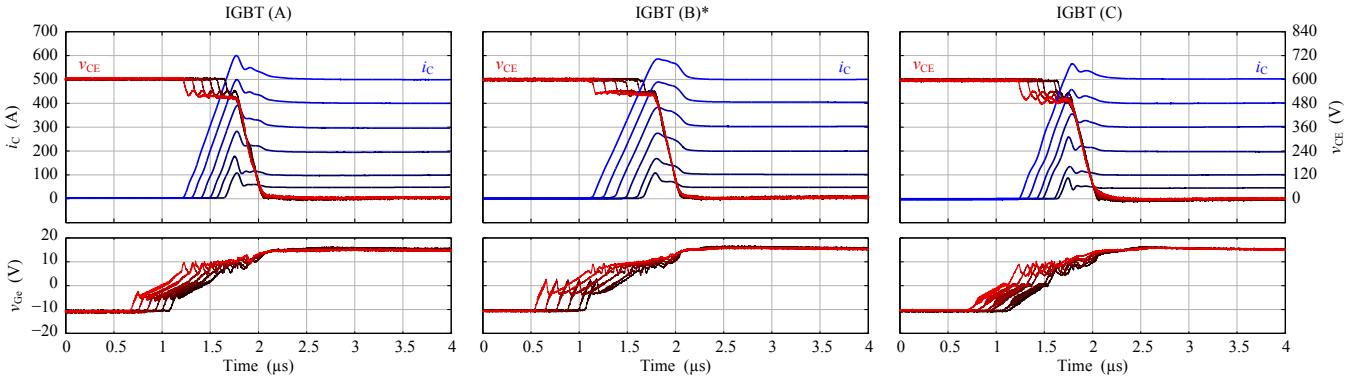

Fig. 13: Measured closed-loop controlled turn-on waveforms at $1\,\mathrm{kA}/\mu\mathrm{s}$, $-2\,\mathrm{kV}/\mu\mathrm{s}$ of the IGBT modules (A), (B)* and (C).

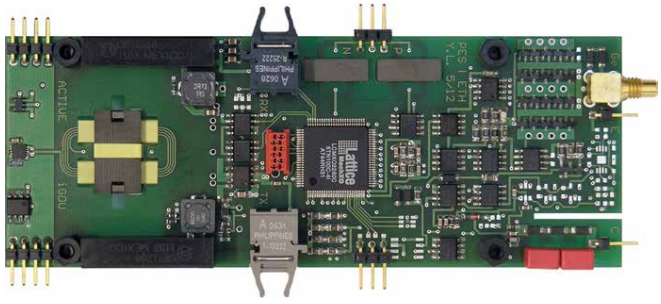

Fig. 14: Prototype of the active IGBT gate drive; PCB dimensions: 50 mm x 133.3 mm and / or 1.97 in x 5.25 in

In addition, the closed-loop control was also tested for a 1.2 kV, 300 A IGBT module containing SiC-diodes (module (E)), and compared to an IGBT module comprising conventional Si-diodes (module (D)). The corresponding comparative measurements are shown in Fig. 15. It can be summarized, that the control is highly accurate and stable for both modules, i.e. for the conventional module and the module with SiC-diodes.

VI. Conclusion

The main contribution of this paper is the investigation and verification of the stability and robustness of a closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ IGBT gate drive based on small signal control-oriented models. Experimental measurements of the closed-loop switching trajectories and the investigation on the parasitics of different IGBT modules confirm the results of the theoretical stability analysis. The small signal approach allows to analyze the stability around a specific operating point, whereas an IGBT model considering the non-linear IGBT parameters and dependencies is needed, in order to investigate the stability in the large signal domain.

Future work in this area will be related to the analysis of

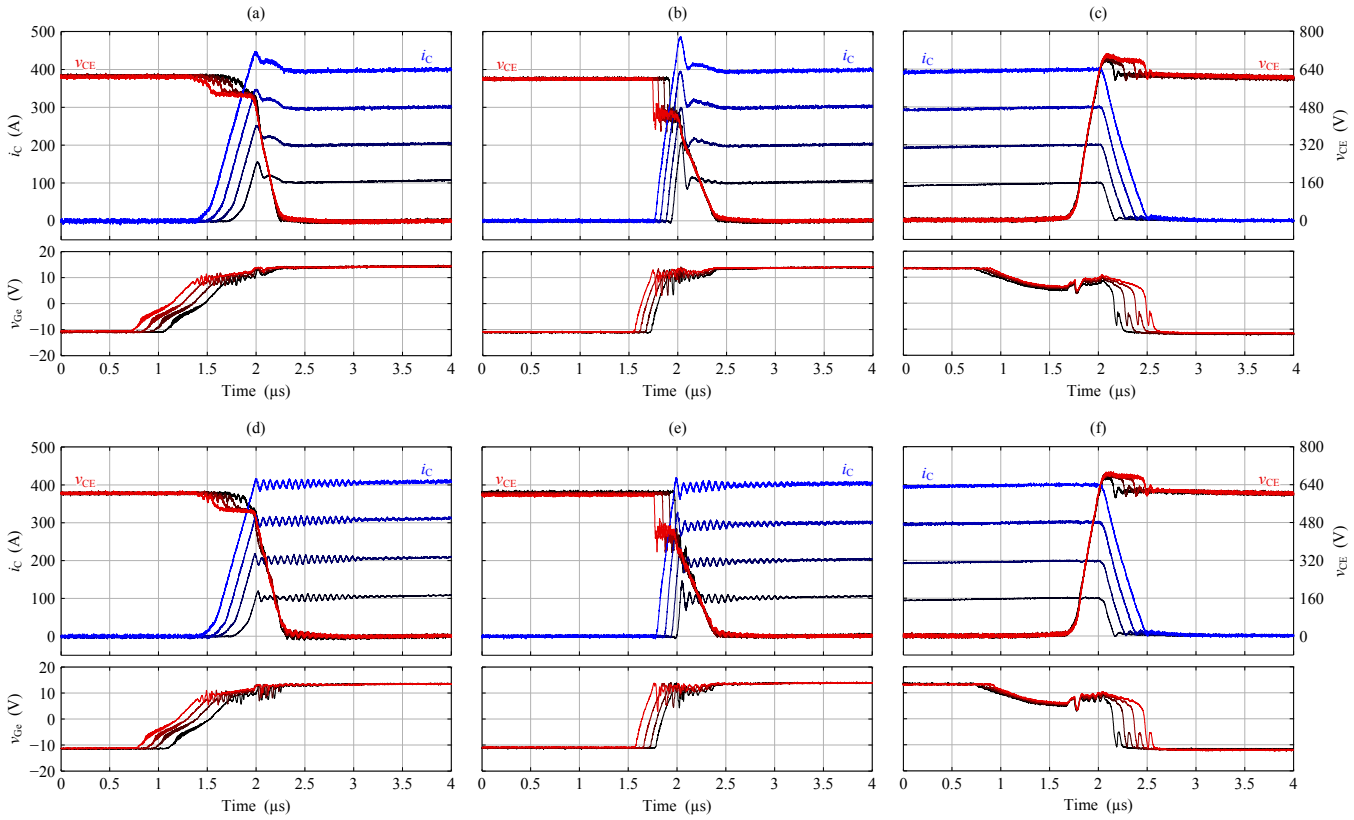

Fig. 15: Measured closed-loop controlled waveforms for (a,b,c) conventional Si-diode Si-IGBT module (D) and (d,e,f) SiC-diode Si-IGBT module (E). Turn-on at (a,d) $1\,\mathrm{kA}/\mu\mathrm{s}$, $-2\,\mathrm{kV}/\mu\mathrm{s}$ and (b,e) $2\,\mathrm{kA}/\mu\mathrm{s}$, $-1\,\mathrm{kV}/\mu\mathrm{s}$. Turn-off at (c,f) $-1\,\mathrm{kA}/\mu\mathrm{s}$, $2\,\mathrm{kV}/\mu\mathrm{s}$.

the interaction between the high- and low-side AGD to achieve optimal control of the IGBTs in a bridge-leg configuration and to an application of the gate drive concept to series connected IGBTs.

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