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***Abstract*— In this paper, total performance of two $20\,\mathrm{kVA}$ UPS realizations based on different design processes are compared in terms of losses and volumes. One of the design process employs a multi-objective optimization approach and Pareto analysis for selecting optimal design parameters. The other design process employs traditional industrial design approach. Employing the multi-objective optimization approach and Pareto analysis in the design process enables comparison and selection of suitable combinations of power semiconductor device for achieving minimum semiconductor losses. Thus, not only lower semiconductor losses but also lower heat sink volumes are achieved. In addition, it also enables selection of suitable magnetic material and design parameters, switching frequencies and relative current ripple, for reducing losses and volumes of inductors. As a result, the total volume of realized system based on the optimized design is $47\,\%$ less than the other realization. On the other hand, costs are considered as one of the most important performance index in the industrial application. Challenges for including systematic costs analysis into the design process are also discussed.**

I. Introduction

A demand for improvement of the power converter system's efficiency and power density has been kept increasing since last decades. In addition, for the industrial application, not only the efficiency and the power density of the power converter itself, but also development lead-time of the power converter is required to be reduced. Typical development process of the power converter system in the industrial application is consist of several prototype hardware production, evaluation and design improvement process. For example, a first prototype is built in order to perform basic evaluation, such as a switching test or a thermal test, and to find a problem to be solved for second prototype. Over heating of power semiconductors, inductors or capacitors could be one of such a problem to be found and localized. In the worst case, not only second but also third prototype has to be built and evaluated again when the second prototype didn't satisfy the required specification or performance, such as the efficiency and power density. Since required specification and performance is keep increasing, it is getting more difficult to design the power converter system within the limited lead-time. In order to satisfy the both of high performance and short lead-time of the development, the performance oriented design optimization of power converter system is getting more important to be discussed and applied for industrial applications.

The optimization of power converter systems is a multi-domain procedure [1], which considers thermal effects and limitations besides electric and / or magnetic characteristics of active and passive power components. Early implementations of power converter optimizations are limited to the optimization with respect to a single performance index, e.g. power density ρ or efficiency η [2]–[4]. Single-objective converter optimizations, however, often yield unsatisfying remaining converter characteristics, i.e. a converter optimized for high power density may generate high losses, due to increasing losses of high power density magnetic components. Thus, the multi-objective optimization of a PFC rectifier based on the η-ρ Pareto front is proposed in [5]. This Pareto front identifies the highest efficiency for a given power density (and vice versa) and can be used as basis for initial decisions concerning the converter design parameters.

In the previous work [6], a $20\,\mathrm{kVA}$ Uninterruptible Power Supply (UPS) system has been designed and realized based on the multi-objective optimization approach and Pareto analysis. On the other hand, Fujielectric has been developed same $20\,\mathrm{kVA}$ UPS based on the traditional industrial design approach. In this paper, total performance of two $20\,\mathrm{kVA}$ UPS realizations based on different design approaches are compared in terms of losses and volumes. In **Section II**, application system and specifications of realized UPS system are summarized. In **Section III**, the employed multi-objective optimization procedure in [6] is briefly summarized and the optimization results are described. In **Section IV**, losses and volumes distribution of two UPS system realizations are compared in detail. In addition, measured efficiency, realized

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TABLE I
REQUIRED SPECIFICATIONS.

Input line-to-line RMS voltage	V_{in}	400 V
Input frequency	f_{in}	50 Hz
Output line-to-line RMS voltage	V_{out}	400 V
Output frequency	f_{out}	50 Hz
Nominal apparent output power	S_{out}	20 kVA
DC link voltage	V_{dc}	720 V
Battery voltage	V_{bt}	360 V

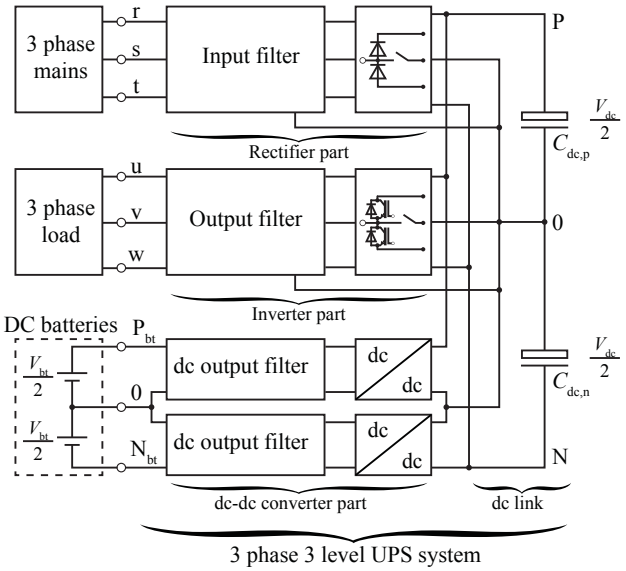

Fig. 1. Simplified circuit schematic of the UPS power unit including input and output filters.

power density and cost distribution are also compared and discussed. In **Section V**, main benefit and some challenges of the multi-objective optimization approach for industrial applications are discussed.

II. APPLICATION SYSTEM AND SPECIFICATIONS

Required specifications of the realized UPS power unit is shown in **Tab. I**. **Fig. 1** shows simplified circuit schematic of the UPS power unit. A three-level T-type topology is employed for both input rectifier and output inverter. The T-type NPC topology requires one bi-directional switch per phase between output and neutral point. There are two different way to realize the bi-directional switch [7]–[10] as shown in **Fig. 2**. Employed realizations of bi-directional switch and specifications of the power semiconductor switch for optimized design and industrial design are discussed in **Section IV**. Employed topology for input and output filters are also discussed in Section IV.

III. OPTIMIZATION PROCEDURE

A system-level multi-optimization procedure for three-phase three-level T-type UPS system is introduced in [6]. A flow-

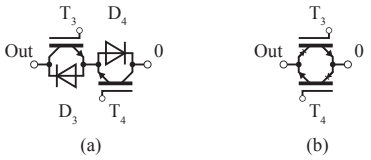

Fig. 2. Possible realization of the bi-directional switch, (a) anti-series connection of two IGBTs including Free-Wheeling-Diodes (FWDs), (b) anti-parallel connection of two RB-IGBTs.

chart of the optimization procedure is shown in **Fig. 3**. The switching frequency f_{sw} is considered one of the variable in the design design space of the converter system. The optimization procedure calculates losses and volumes of power components (e.g. power semiconductors with cooling system, inductors and capacitors) at each design point and sums up losses and volumes for all power components in order to calculate total losses and volumes of the converter system. This procedure is iterated until all combination of design variable are swept.

At the end of the optimization procedure, two performance indices, total efficiencies and power densities, are calculated at each design point. These values of performance index are plotted in the performance space as shown in **Fig. 4**. This is the procedure to translate or project the converter design information in the design space into the performance space. The main benefit of projecting lots of converter design into the multi-dimensional performance space is that makes easier comparison of trade-off between multiple performance indices and clear decision making.

As a result, the switching frequency of $16\,\mathrm{kHz}$ was selected for total efficiency of $96.2\,\%$ at power density of $2.3\,\mathrm{kVA/dm^3}$ when the ambient temperature of $55\,^{\circ}\mathrm{C}$ was considered. At same time, several combinations of the power semiconductor and four different magnetic core materials are considered in the optimization procedure. Based on the result in [11], the anti-parallel connection of Si RB-IGBTs with SiC Schottky Barrier Diodes (SBDs) is selected for the rectifier part, and the anti-series connection of Si IGBTs with SiC SBDs is selected for the inverter part. For the magnetic component, the Amorphous material at relative high frequency current ripple of $20\,\%$ is selected as a most suitable combination for achieving low losses and volumes [6], [12]. Selected design parameters of the optimized converter is summarized and compared with the industrial design parameters in **Tab. II**.

IV. COMPARISON OF UPS SYSTEM WITH AND WITHOUT OPTIMIZATION

Tab. III shows calculated loss distribution at nominal output power and loss measurement results. Switching losses of the power semiconductor is lower for optimized design since SiC SBD at lower switching frequency is employed. However,

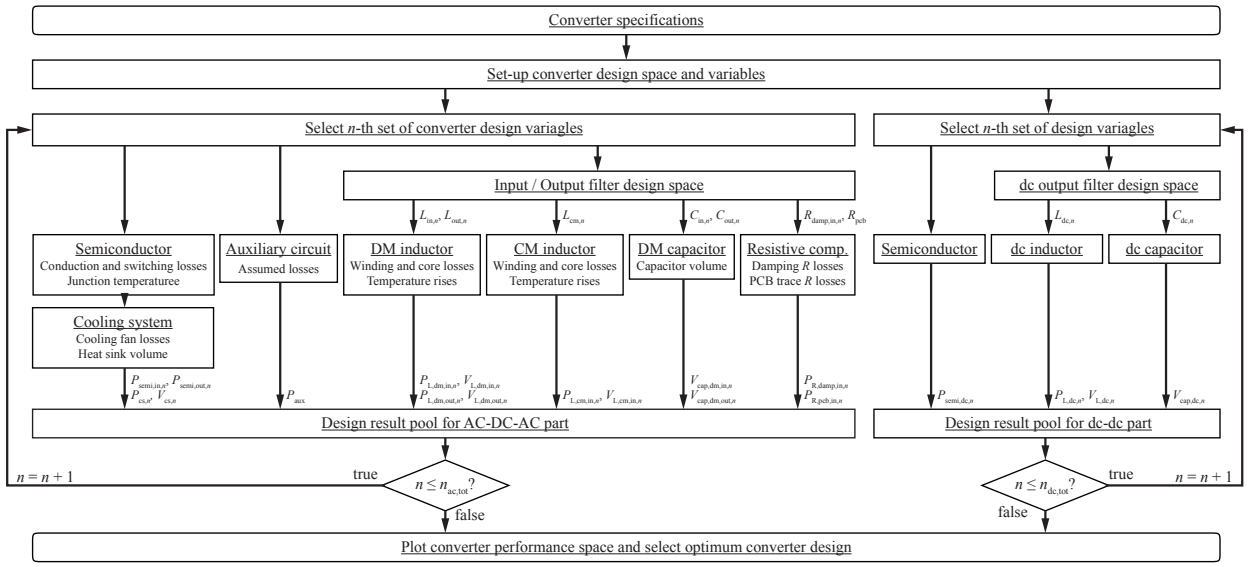

Fig. 3. Flow-chart of the system-level optimization procedure for three-phase three-level T-type UPS system.

TABLE II

SUMMARY OF DESIGN PARAMETERS.

Switching frequencies

	Optimized design	Industrial design
Inverter and Rectifier	16 kHz	20 kHz
dc-dc converter	16 kHz	40 kHz

Selected poser semiconductors

	Optimized design	Industrial design
Rectifier	1200 V SiC SBD	1200 V Si Diode
	600 V Si RB-IGBT	600 V Si RB-IGBT
Inverter	1200 V Si IGBT	1200 V Si IGBT
	1200 V SiC SBD	1200 V Si Diode
	600 V Si IGBT	600 V Si RB-IGBT
	600 V SiC SBD	-
dc-dc converter	600 V Si IGBT	600 V Si IGBT
	600 V SiC SBD	600 V Si Diode

Selected filter components

		Optimized design	Industrial design
Input filter	Topology	Two-stage LC	Single-stage LCL
	EMI filter	Included	Not included
	High frequency side inductor	Amorphous	Iron powder
	Low frequency side inductor	Amorphous	Ferrite
	Common-mode inductor	Nanocrystalline	-
	Filter capacitor	Film	Film
Output filter	Topology	Two-stage LC	Single-stage LCL
	EMI filter	Not included	Not included
	High frequency side inductor	Amorphous	Iron powder
	Low frequency side inductor	Amorphous	Ferrite
	Filter capacitor	Film	Film
dc-dc converter	high frequency side inductor	Amorphous	Iron powder
	dc link capacitor	Film	Electrolytic

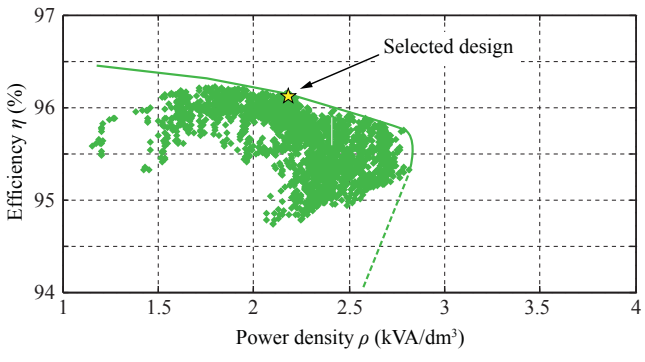

Fig. 4. Plotted converter design points into the η-ρ performance space and the selected design point.

slightly higher conduction losses are calculated as a result of employing higher on voltage drop of SiC SBDs than Si diodes and series connection of two IGBTs including FWDs for bi-directional switch in the inverter part. Since total semiconductor losses are lower for optimized design, power consumption of cooling system is also lower. Auxiliary circuits, including DSPs and gate drivers, provide fixed amount of loss which is not depended on operating point of output power. Winding losses of filter inductor is higher for optimized design due to relatively low switching frequency and, therefore, higher inductance values are required. However, core losses are lower for optimized design because of amorphous material was selected. Resistive components, including PCB traces, cables, magnetic contactors, fuses, damping resistors and discharge re-

TABLE III
CALCULATED LOSS DISTRIBUTION AND LOSS MEASUREMENT RESULT.

Components	Items	Optimized	Industrial	Difference (Optimized/Industrial)
Power semiconductors	Switching	112.5 W	262.7 W	42.8%
	Conduction	285.2 W	237.2 W	120.2%
Cooling system	Fans	25.9 W	63.4 W	40.9%
Auxiliary circuits	DSPs, Gate drivers	23.9 W	36.9 W	64.7%
Filter inductors	Winding	82.6 W	48.7 W	169.7%
	Core	75.4 W	90.0 W	83.7%
CM inductors	Winding	42.3 W	0.0 W	-
	Core	2.3 W	0.0 W	-
Resistive components	PCB traces and cables	26.8 W	34.9 W	76.7%
	Magnetic contactor	10.7 W	10.0 W	107.7%
	Fuses	5.4 W	6.8 W	78.6%
	Damping and discharging resistors	16.0 W	12.1 W	131.8%
Total calculated losses		708.9 W	802.7 W	88.3%
Total calcculated conversion efficiencies		96.58%	96.14%	-
Total measured losses		728.3 W	730.0 W	99.8%
Total measured conversion efficiencies		96.49%	96.48%	-

sistors at dc link, generate considerable amount of loss. Based on the calculated losses at room temperature, total conversion efficiencies of 96.6 % and 96.1 % are expected for optimized design and industrial design, respectively. Measurement result shows that same conversion efficiency of 96.5 % is achieved for both designs.

Tab. IV shows volume distribution based on calculated boxed volumes of power components. Achieved total boxed volumes and power densities of realized UPS power unit are also shown. The optimized design achieved very compact cooling system volume compare with the industrial design. Comparably lower semiconductor losses and volume optimization procedure of heat sink design contribute this achievement. On the other hand, volumes of inductor are higher for the optimized design due to relatively lower switching frequencies. Filter capacitors has almost has same volume, however, lower volumes of the dc link capacitor was achieved with industrial design because of the selected capacitor type. The electrolytic capacitor is selected for industrial design and it has smaller volume than film capacitor at same capacitance and rated voltage [2]. The calculated total volume based on component volumes shows that the optimized design achieves 15 % smaller volume than the industrial design at lower operating switching frequency. Main contribution of this achievement was made by cooling system. However, the total boxed volume of the realized hardware is drastically increased by factor of 3 to 4. This is due to existence of other component, such as magnetic contactors, fuses, current sensors, connectors, cables, enclosures, PCBs and other auxiliary circuits. In addition, there is lots of free spaces between components due to keep clearance, smooth air flow or not optimized placements of the component. As a result, achieved power densities of the realized hardware are $0.91\,\mathrm{kVA/dm^3}$ and $0.48\,\mathrm{kVA/dm^3}$ for the optimized design and the industrial design, respectively.

Tab. V shows relative cost distribution of realized UPS power units. Since industrial designed UPS power unit is designed for math production, absolute total cost is about 10 times lower than optimized UPS power unit which was realized as a demonstrator. Therefore, only relative cost distribution of components are shown here. Please note that the cost information was converted into USD first then cost distribution was analysed. Nearly half of total cost was contributed by inductors for both designs. Especially, the amorphous material is more expensive than the iron powder or the ferrite material [13]. Relative cost of the power semiconductors in the optimized design is lower than the value in the industrial design, however, this is because of relatively higher cost of inductors and PCBs for the optimized design. Basically, employing SiC devices requires higher cost [14]–[16] than Si devices. The cost of PCB is much higher for the optimized design due to too little number of production compare with the industrial design.

V. DISCUSSION

The analysis of loss distribution shows that the semiconductors still contributes more than half, about 60 %, to the total losses. In order to dissipate that huge amount of losses, boxed volume of the cooling system in the industrial design contribute more than 60 % to the total components volume.

TABLE IV
CALCULATED VOLUME DISTRIBUTION AND ACHIEVED POWER DENSITY.

Component	Item	Optimized	Industrial	Difference (Optimized/Industrial)
Cooling system	Heat sink + fans	1.37 dm^3	6.22 dm^3	22.0%
Inductors	Filter inductors	2.49 dm^3	2.01 dm^3	123.9%
	CM inductors	1.22 dm^3	0.00 dm^3	-
	dc inductors	1.37 dm^3	0.37 dm^3	371.7%
Capacitors	Filter capacitors	0.52 dm^3	0.46 dm^3	112.4%
	dc link capacitors	1.55 dm^3	1.00 dm^3	155.5%
Total boxed volume (only components)		8.52 dm^3	10.06 dm^3	84.7%
Total power density (only components)		2.35 kVA/dm^3	1.99 kVA/dm^3	-
Total boxed volume (realized hardware)		22.03 dm^3	41.68 dm^3	52.9%
Total power density (realized hardware)		0.91 kVA/dm^3	0.48 kVA/dm^3	-

TABLE V
RELATIVE COST DISTRIBUTION.

Component	Optimized	Industrial
Power semiconductors	13.8%	17.6%
Cooling system	3.7%	5.2%
Inductors	48.5%	44.1%
Capacitors	6.1%	13.0%
Gate drivers	5.5%	15.0%
PCBs	22.5%	5.0%
Total	100.0%	100.0%

However, the volume difference of the cooling system between the optimized design and the industrial design is bigger than the loss difference of the semiconductors. This is due to lower cooling coefficient of the forced cooling system in the industrial design. Cooling fans are mounted on the inlet of the enclosure, therefore, flow volume of the air path through the air channel of the heat sink is lowered. In addition, since semiconductor losses are calculated at worst case of junction temperature in order to avoid over heating, heat sink volume is typically over sized in the industrial design. On the other hand, relative cost contribution of power semiconductors and cooling system is less than 20 % for the optimized design and less than 25 % for the industrial design. It means that power semiconductors and cooling system has high contribution to the losses and volumes.

Inductors contribute about 20 % to the total losses for both designs, but it has higher contribution to the total volumes. Especially, the optimized design has higher share of the inductor volumes due to considerably reduced volumes of the cooling system. In addition, inductors have considerably high contribution of more than 40 % to the total costs. Even relatively cheaper materials, such as the iron powder and ferrite, are selected for the industrial design, relative cost to the total cost is almost same with the optimized design. Capacitors has relatively lower contribution than inductors to the total volumes and costs.

Other components, such as DSPs, gate drivers and resistive components, are also contributing to the total loss. Typically, losses of these components are neglected, however, analysis result shows that total losses of these components are not negligible. In the optimization procedure, volumes of these components are also neglected. In addition, contribution of these components to the total costs is more than 20 % for both designs, therefore, it is also not negligible. One of challenge of the optimization approach is that to include analytical volume and cost estimation model of these non major components.

Tab. VI summarize contribution characteristics of each component to losses, volumes and costs. From the comparison result of volume distribution between calculated values and realized hardware, contribution of free space to the total volume seems to be high. Unfortunately, no analytical approach to model and reduce the volume has been introduced. However, it is possible to define power components' boxed size and optimize it as small as possible in the early stage of the design process by applying the analytical optimization approach. There for it is also possible to maximize the period for optimize placement of the components in order to minimize unnecessary free space. It is other benefit of the optimization approach for industrial application. On the other hand, advanced integration technologies, will be strongly required for reducing volume of free space.

VI. CONCLUSION

In this paper, comparison on losses, volumes and costs of two different design of 20 kVA three-phase three-level UPS system are compared. The system level multi-objective optimization approach was employed for one of the design,

TABLE VI
SUMMARY OF CONTRIBUTION CHARACTERISTICS.

Component	Losses	Volumes	Costs
Power semiconductors	High	Low	Moderate
Cooling system	Moderate	High	Low
Inductors	Moderate	Moderate	High
Capacitors	Low	Moderate	Moderate
Other components	Moderate	Moderate	Moderate
Free space	Nothing	High	Nothing

and the other one was designed based on traditional industrial design approach. As a result, 47 % smaller total volume at same conversion efficiency of 96.5 % with the optimized design has been confirmed. Detailed comparison and analysis of the performance indices have shown that inductors have high contribution to the total cost. In addition, not negligible contribution of auxiliary circuit components to the total losses, volumes and costs, are found. Such components are including gate drivers, magnetic contactors, fuses, cables and PCBs. An analytical losses, volumes and cost models for these auxiliary components has to be considered in the future. Also, it was found that free space has high contribution to the volume of realized hardware. In order to push power density boundary of the industrial application, optimized components placement and the advanced integration technology will be mandatory to apply.

REFERENCES

[1] H. Ohashi, "Research Activities of the Power Electronics Research Centre with Special Focus on Wide Band Gap Materials," in *Proc. of the 4^{th} International Conference on Integrated Power Systems (CIPS)*, pp. 1–4, 2006.

[2] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM Converter Power Density Barriers," in *Proc. of the Power Conversion Conference (PCC)*, pp. 9–29, 2007.

[3] U. Badstuebner, J. Biela, and J. W. Kolar, "Power Density and Efficiency Optimization of Resonant and Phase-Shift Telecom DC–DC Converters," in *Proc. of the 23^{rd} Annu. IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 311–317, 2008.

[4] U. Badstuebner, J. Biela, B. Faessler, D. Hoesli, and J. W. Kolar, "An Optimized $5\,\mathrm{kW}$, $147\,\mathrm{W/in^3}$ Telecom Phase-Shift DC–DC Converter with Magnetically Integrated Current Doubler," in *Proc. of the 24^{th} Annu. IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 21–27, 2009.

[5] J. Biela and J. W. Kolar, "Pareto Optimal Design and Performance Mapping of Telecom Rectifier Module Concepts," in *Proc. of the Power Conversion and Intelligent Motion (PCIM)*, 2010.

[6] H. Uemura, F. Krismer, Y. Okuma, and J. W. Kolar, "η-ρ Pareto Optimization of 3-Phase 3-Level T-Type AC–DC–AC Converter Comprising Si and SiC Hybrid Power Stage," in *Proceedings of the International Power Electronics Conference - ECCE Asia (IPEC 2014)*, May 2014.

[7] M. Schweizer, I. Lizama, T. Friedli, and J. W. Kolar, "Comparison of the Chip Area Usage of 2-level and 3-level Voltage Source Converter Topologies," in *Proc. of the 36^{th} Annu. Conf. of the IEEE Ind. Elec. Society (IECON)*, (Phoenix, USA), November 2010.

[8] M. Takei, Y. Harada, and K. Ueno, "600V-IGBT with Reverse Blocking Capability," in *Proc. of 2001 Int. Symp. on Power Semiconductor Devices and ICs*, (Osaka, Japan), pp. 413–416, 2001.

[9] A. Lindemann, "A New IGBT with Reverse Blocking Capability," in *Rec. of the 9th European Conf. on Power Elec. and Appl. (EPE)*, pp. 27 – 29, Aug. 2001.

[10] M. Otsuki and Y. Seki, "The Authentic Reverse Blocking IGBT (RB-IGBT) Technologies for Bi-directional switching applications," in *PCIM Brasil Conference*, 2012.

[11] H. Uemura, F. Krismer, and J. W. Kolar, "Comparative Evaluation of T-Type Topologies Comprising Standard and Reverse-Blocking IGBTs," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, 2013.

[12] R. M. Burkart, H. Uemura, and J. W. Kolar, "Optimal Inductor Design for 3-Phase Voltage-Source PWM Converters Considering Different Magnetic Materials and a Wide Switching Frequency Range," in *Proceedings of the International Power Electronics Conference - ECCE Asia (IPEC 2014)*, May 2014.

[13] R. Burkart and J. W. Kolar, "Component Cost Models for Multi-Objective Optimizations of Switched-Mode Power Converters," in *Proc. of the IEEE Energy Conversion Congress and Exposition (ECCE USA)*, 2013.

[14] J. Biela, M. Schweizer, S. Waffler, and J. W. Kolar, "SiC versus Si—Evaluation of Potentials for Performance Improvement of Inverter and DC–DC Converter Systems by SiC Power Semiconductors," *IEEE Trans. on Industrial Electronics*, vol. 58, pp. 2872–2882, 2011.

[15] R. O. Nielsen, L. Torok, S. Munk-Nielsen, and F. Blaabjerg, "Efficiency and Cost Comparison of Si IGBT and SiC JFET Isolated DC/DC Converters," in *Proceedings of the 39th Annual Conference of the IEEE Industrial Electronics Society (IECON 2013)*, 2013.

[16] M. G. H. Aghdam and T. Thiringer, "Comparison of SiC and Si Power Semiconductor Devices to Be Used in 2.5 kW DC/DC Converter," in *International Conference on Power Electronics and Drive Systems (PEDS 2009)*, 2009.