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***Abstract*—This Paper proposes a novel Dual Three-Phase Active Bridge (D3AB) PFC rectifier topology for a 400 V dc distribution system, which features galvanic isolation, bidirectional power conversion capability, a high level of component integration, and can be dimensioned with respect to high efficiency. In the course of a comprehensive and in-depth analytical investigation, the working principle of the D3AB PFC rectifier is described in order to enable converter modelling and the derivation of mathematical expressions and limitations needed for converter design and optimization. The developed converter models are verified by means of circuit simulations. An overall optimization of a system with 400 V line-to-line input voltage, 400 V dc output, and $P_{\text{out}} = 8\,\text{kW}$ rated power with respect to efficiency and power density reveals the feasibility of a full-load efficiency of 98.1% and a power density of $4\,\text{kW/dm}^3$ if SiC MOSFETs are used. The finally presented design is found to achieve efficiencies greater than $98\,\%$ for $P_{\text{out}} > 1.7\,\text{kW}$.**

I. Introduction

Recent efforts with regard to a more sustainable electric power generation propose the installation of distributed dc microgrids in order to effectively utilize distributed renewable energy sources [1]. A dc microgrid architecture typically incorporates dc sources (e.g. photovoltaic, fuel cell), energy storages (e.g. batteries), and loads (e.g. household appliances, IT equipment, electric vehicles) and employs an isolated bidirectional rectifier system to establish energy transfer between the dc grid and the three-phase ac mains.

This paper evaluates a novel topology of a grid-connected, bidirectional, and isolated three-phase power factor corrected (PFC) rectifier with a rated power of $P_{\text{out}} = 8\,\text{kW}$ and further specifications as listed in **Tab. I**, which fulfills the requirements of bidirectional conversion capability and galvanic isolation with very low complexity. Due to the versatility of the proposed system, it is suitable for various further applications including PFC rectifiers for common dc bus architectures as, for example, used in efficiency-optimized multi-axis drive systems [2], where it is reasonable to consider advanced rectifier topologies to define the electric potential of a dc terminal, include a battery to buffer outages, etc. Furthermore, the system could e.g. be implemented for battery chargers of plug-in hybrid electric vehicles [3].

Conventional realizations of three-phase and isolated ac–dc rectifiers are two-stage solutions, with grid-side rectifiers and series-connected isolated dc–dc converters [4], [5], [6]. Two-stage converter systems feature the advantages of decoupled functional parts, at the cost of higher expected losses due to the high number of power components in the current path. State-of-the-art research with regard to more efficient converter topologies reveals various solutions that combine PFC functionality, galvanic isolation, and voltage conversion in a single stage. In this context, isolated single-stage PFC rectifiers, based on isolated Swiss-forward or matrix-type topologies [7], [8], [9], represent suitable but complex solutions. With regard to reduced converter complexity, a direct connection of the high frequency (HF) transformer of a single-phase dc–dc converter to a three-phase PFC rectifier is proposed in [10], which, due to the asymmetry of the converter, is considered more viable for lower power levels. Further level of integration is achieved with a topology with coupled input inductors proposed in [11]. There, the isolated dc port is immediately coupled at the ac port in order to reduce the number of power components in the current path and achieve increased efficiency. The required coupled inductors and the high number of IGBTs (24), though, render the presented converter structure comparably complex.

TABLE I: Specifications of the D3AB PFC rectifier.

Nominal mains line-to-phase voltage (rms value)	$V_{\text{ac}} = 230\,\text{V}$
Mains frequency	$f_{\text{m}} = 50\,\text{Hz}$
Nominal output dc voltage, port 1 (not isolated)	$V_{\text{dc1}} = 800\,\text{V}$
Nominal output dc voltage, port 2 (galv. isolated)	$V_{\text{dc2}} = 400\,\text{V}$
Nominal output power	$P_{\text{out}} = 8\,\text{kW}$

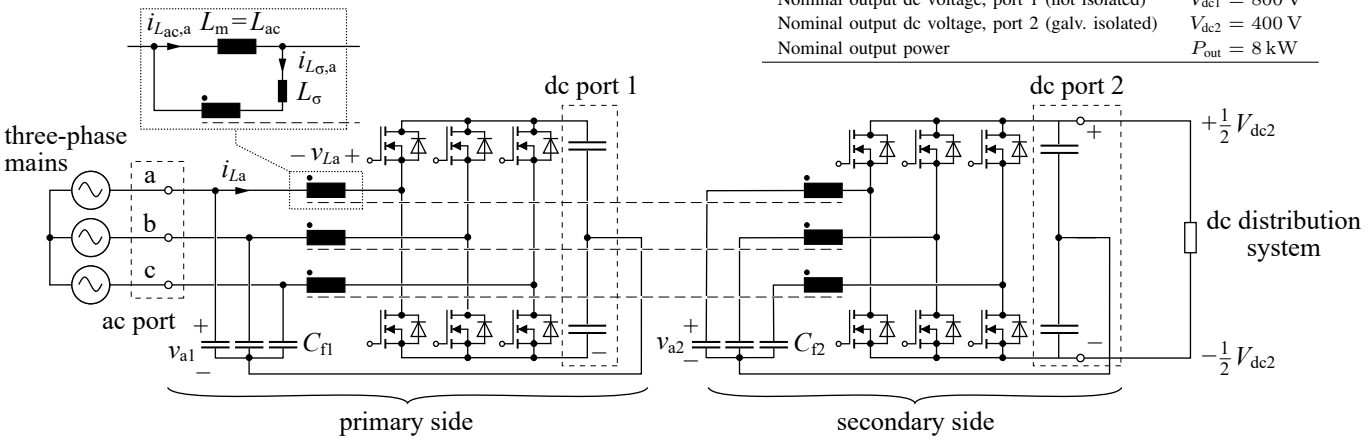

Fig. 1: Proposed bidirectional converter topology with a three-phase ac input port, a dc output port 1 and an isolated dc output port 2.

This paper proposes a novel isolated bidirectional Dual Three-Phase Active Bridge (D3AB) PFC rectifier topology, depicted in **Fig. 1**, that aims for high level of integration and, for this, integrates the functionalities of PFC inductors and HF transformers. Thus, the system essentially combines the functionalities of a bidirectional three-phase PFC rectifier and a three-phase Dual Active Bridge (DAB) converter and provides three power ports, i.e, the ac (input) port, a dc (output) port without isolation, and an isolated dc (output) port. With a total of twelve power MOSFETs, and since the two-level three-phase rectifier structure facilitates the use of conventional 6-pack power modules, the proposed structure features reduced realization complexity compared to state-of-the-art solutions. The paper is organized as follows. **Section II** presents a comprehensive description of the proposed converter system and, for this purpose, first investigates the properties of a single-phase version of the system and then extends the analysis to the three-phase system. Subsequently, **Section III** summarizes results of a converter optimization with respect to efficiency and power density. **Section IV**, finally, evaluates a selected design of the D3AB PFC rectifier with regard to losses, volumes, and efficiency in order to assess the suitability of the proposed concept for the given application.

II. Operating principle

The input inductors, L_{ac}, of a conventional three-phase PFC rectifier without galvanic isolation (and filter capacitors connected to the dc output midpoint, i.e., the primary-side part of the converter depicted in Fig. 1), are subject to an inductor voltage, v_L, with nearly zero local average value, $\langle v_L \rangle \approx 0$ (angle brackets denote the average over one switching period), but large HF spectral components at the switching frequency ($f_{\mathrm{s}} = 35\,\mathrm{kHz}$) and multiples thereof. For the purpose of illustration, **Fig. 2(a)** depicts the instantaneous and local average values of the voltage across the input inductor of phase a over one mains period for rated operation according to Tab. I and **Fig. 2(b)** shows the corresponding spectrum. The proposed isolated converter topology is derived based on the idea that the input inductors are replaced by transformers in order to take advantage of the applied HF voltages. The secondary-side windings are connected to a second three-phase PFC rectifier, which, in combination with the transformers' stray inductances L_σ, realizes a converter structure similar to a three-phase DAB converter. It is worth to note that Fig. 1 illustrates only one possible realization of the D3AB PFC rectifier. Variations of this concept may only use differential or common mode voltage components for energy transfer and/or employ different three-phase transformers, e.g., with delta-connected windings on the secondary side [12].

In this work, the corresponding power transistors at the converter's primary and secondary sides operate with same duty cycles. For this reason,

$$\frac{v_{\{\mathrm{a,b,c}\}1}}{V_{\mathrm{dc1}}} = \frac{v_{\{\mathrm{a,b,c}\}2}}{V_{\mathrm{dc2}}} \tag{1}$$

applies. The gate signals of the six corresponding primary- and secondary-side transistors are subject to a common phase shift, φ, in order to facilitate output power control at dc port 2.

Based on the assumption that the capacitances of the split dc-link are sufficiently large to achieve negligible fluctuations of the dc-link capacitor voltages, the analysis can be confined to the single-phase system with separated input inductor and HF transformer shown in **Fig. 3**. With this modification

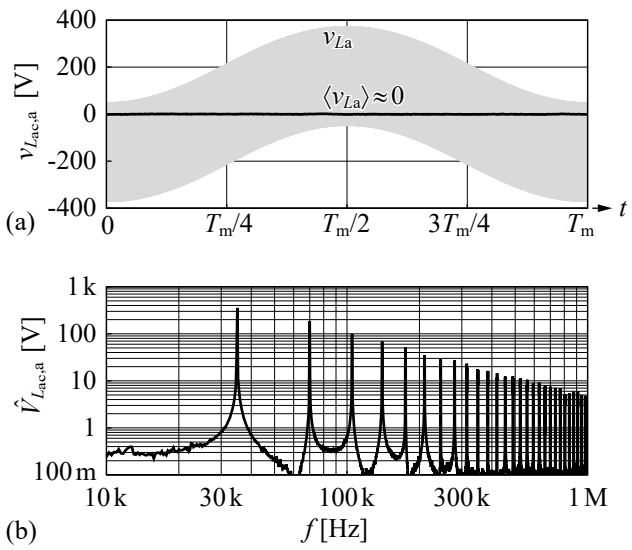

Fig. 2: (a) Instantaneous and local average values of the voltage across L_{ac}; (b) spectrum of v_{La} (operating parameters according to Tab. I, $f_{\mathrm{s}} = 35\,\mathrm{kHz}$).

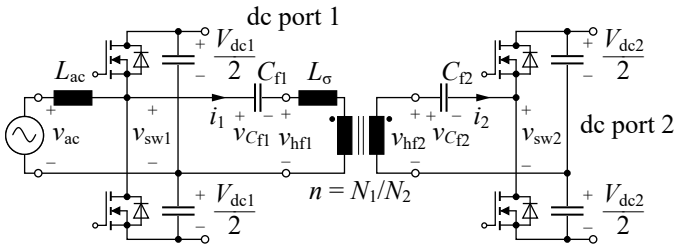

Fig. 3: Single-phase system with input inductor L_{ac}, primary- and secondary-side low-frequency blocking and filter capacitors C_{f1} and C_{f2}, and HF transformer.

a comprehensible description of the operating principle is feasible and the derived results can be directly applied to the three-phase converter of Fig. 1. The converter of Fig. 3 has been documented with regard to dc–dc operation, for $D_1 = D_2 = 0.5$ [13] and arbitrary (but equal) duty cycles, $0 < D = D_1 = D_2 < 1$ [14]; its extension to a dc–dc converter with a three-phase HF dc-link is investigated in [15]. Section II-A revisits its main operating principles for dc–dc operation in order to allow for a comprehensible extension to ac–dc operation of single- and three-phase PFC rectifier systems in Sections II-B and II-C, respectively.

A. Single-phase system at dc–dc operation

Fig. 4 illustrates voltage and current waveforms simulated for the single-phase converter system of Fig. 3 at a selected operating point. The ac input voltage, v_{ac}, changes slowly with respect to the switching period, T_{s}, and can thus be considered as constant during one switching period. The converter features four degrees of freedom for the control of the output power, i.e., switching frequency, f_{s}, input- and output-side duty cycles D_1 and D_2, and phase shift angle, φ.

The filter capacitors C_{f1} and C_{f2} are blocking the dc voltage components, $V_{C\mathrm{f1}}$ and $V_{C\mathrm{f2}}$, in order to avoid saturation of the transformer core. Thus, the HF voltages,

$$v_{\mathrm{hf1}} = v_{\mathrm{sw1}} - V_{C\mathrm{f1}}, \tag{2}$$

$$v_{\mathrm{hf2}} = v_{\mathrm{sw2}} + V_{C\mathrm{f2}}, \tag{3}$$

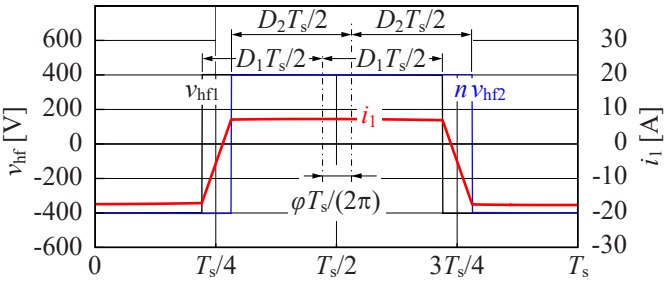

Fig. 4: Definitions of D_1, D_2, and φ using simulated waveforms of v_{hf1}, v_{hf2}, and i_1 over one switching period, T_s. Considered operating conditions: $f_s = 35\,\text{kHz}$, $L_\sigma = 58\,\mu\text{H}$, $n = 2$, $v_{ac}(t) = 325\,\text{V}\sin(t\,2\pi 50\,\text{Hz})$, $t = 5\,\text{ms}$, $V_{dc1} = 800\,\text{V}$, $V_{dc2} = 400\,\text{V}$, and $\varphi = 22°$.

result at the HF transformer of the DAB, cf. Fig. 3. The analysis of the lossless converter is similar to the analysis of a conventional DAB converter. For $D = D_1 = D_2$, the expression for the output power is

$$P_{1\phi} = \frac{nV_{dc1}V_{dc2}}{2f_sL_\sigma}\frac{\varphi}{2\pi}\left(2D(1-D) - \frac{|\varphi|}{2\pi}\right), \tag{4}$$

which is found to be valid for

$$\frac{|\varphi|}{2\pi} < \min(D, 1-D). \tag{5}$$

Fig. 5 evaluates (4) with respect to different duty cycles and phase shift angles. A close inspection of the curves in Fig. 5 reveals that maximum power results for a phase shift angle that meets condition (5). For a given duty cycle, the expression

$$P_{1\phi,max} = \frac{nV_{dc1}V_{dc2}\varphi^2_{P1\phi,max}}{8\pi^2 f_sL_\sigma} \tag{6}$$

with

$$\varphi_{P1\phi,max} = 2\pi D(1-D) \tag{7}$$

applies for maximum power. As with all DAB converters, the inductor L_σ limits the maximum output power.

B. Single-phase system at ac–dc operation

The investigated system is operated with ac input voltage,

$$v_{ac}(t) = V_{m,pk}\sin(2\pi f_m t), \tag{8}$$

cf. **Fig. 6(a)** and therefore, the above presented derivations for dc–dc operation need to be extended accordingly. For the sake of brevity, basic sinusoidal modulation is considered, i.e., the input and output stages apply a time-varying duty cycle,

$$D_1 = D_2 \approx \frac{1}{2}\left(1 + \frac{v_{ac}(t)}{V_{dc1}/2}\right), \tag{9}$$

in order to achieve a sinusoidal phase current with unity power factor.

Fig. 6(b) shows the calculated waveform of the primary-side current i_1 over a mains period, for $\varphi = 22° = \text{constant}$. The filter capacitors C_{f1} and C_{f2} are blocking the low-frequency (LF) voltage components and with (1) and (9),

$$\langle v_{Cf1}\rangle(t) = \frac{V_{dc2}}{V_{dc1}}\langle v_{Cf1}\rangle(t) = v_{ac}(t) \tag{10}$$

applies. For this reason, the HF transformer currents are subject to LF offsets caused by superimposed LF capacitor currents,

$$i_{lf1} = C_{f1}\frac{\mathrm{d}\langle v_{Cf1}\rangle}{\mathrm{d}t}, \qquad i_{lf2} = C_{f2}\frac{\mathrm{d}\langle v_{Cf2}\rangle}{\mathrm{d}t}, \tag{11}$$

cf. **Fig. 6(c)**. Thus, the analytical investigation for dc–dc operation presented in Section II-A is extended with respect to the time varying duty cycle and the capacitor currents. The

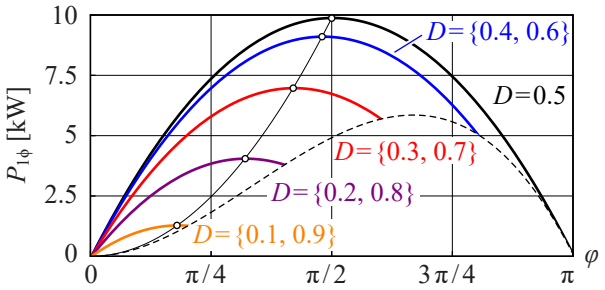

Fig. 5: Average power over one switching period as a function of the phase shift angle φ, for different values of $D = D_1 = D_2$, $f_s = 35\,\text{kHz}$, $L_\sigma = 58\,\mu\text{H}$, $n = 2$, and dc voltages according to Tab. I. The thin black line denotes the trajectory of maximum power and the dashed line denotes the delimitation of the validity range of (4), according to (5).

respective analysis reveals that the superimposed LF capacitor currents have no impact on the current power level, for which

$$\langle p_{1\phi}\rangle = P_{1\phi,dc} + P_{1\phi,ac,pk}\cos(4\pi f_m t) \tag{12}$$

$$P_{1\phi,dc} = \frac{nV_{dc1}V_{dc2}}{2f_sL_\sigma}\frac{\varphi}{2\pi}\left[\frac{1}{2} - \left(\frac{V_{m,pk}}{V_{dc1}}\right)^2 - \frac{|\varphi|}{2\pi}\right], \tag{13}$$

$$P_{1\phi,ac,pk} = \frac{nV_{dc1}V_{dc2}}{2f_sL_\sigma}\frac{\varphi}{2\pi}\left(\frac{V_{m,pk}}{V_{dc1}}\right)^2, \tag{14}$$

is derived.

According to (12), (13), and (14) and for constant phase shift angle φ,

$$\frac{|\varphi|}{\pi} = \frac{1}{2} - \left(\frac{V_{m,pk}}{V_{dc1}}\right)^2 - \sqrt{\frac{\left(V_{dc1}^2 - 2V_{m,pk}^2\right)^2}{4V_{dc1}^4} - \frac{8f_sL_\sigma P_{1\phi,dc}}{nV_{dc1}V_{dc2}}}, \tag{15}$$

the local average of the instantaneous power of the single-phase PFC rectifier, $\langle p_{1\phi}\rangle$ is a sinusoidal function with twice the mains frequency, amplitude $P_{1\phi,ac,pk}$, and dc offset $P_{1\phi,dc}$. In this regard, a detailed analysis reveals that power limitation relevant for the design of L_σ occurs at the maximum values of $|v_{ac}|$, since the maximum possible output power decreases considerably for duty cycles approaching 0 or 1, cf. Fig. 5. With this and expressions (6) and (7), the useful range for φ is limited to

$$\frac{|\varphi|}{2\pi} < \frac{1}{4} - \left(\frac{V_{m,pk}}{V_{dc1}}\right)^2 \tag{16}$$

and with (13), a condition for L_σ results,

$$L_\sigma < \frac{nV_{dc1}V_{dc2}}{8f_sP_{1\phi,dc}}\left[\frac{1}{4} - \left(\frac{V_{m,pk}}{V_{dc1}}\right)^2\right]. \tag{17}$$

C. Three-phase system

It would be straight-forward to use three of the single-phase rectifiers given in Fig. 3 to realize an isolated three-phase PFC rectifier system. With dedicated input inductors, L_{ac}, and DAB transformers, however, the resulting system would require increased total converter volume, since it would not take advantage of the HF voltage applied to the input inductors. For this reason, the remaining part of the paper solely considers the topology of Fig. 1. Nevertheless, the results derived in Sections II-A and II-B directly apply, merely the waveforms of the input currents, $i_{L\{a,b,c\}}$, change, due to the superposition of the currents through L_{ac} and L_σ,

$$i_{L\{a,b,c\}} = i_{Lac,\{a,b,c\}} - i_{L\sigma,\{a,b,c\}}. \tag{18}$$

Fig. 7 depicts characteristic waveforms obtained from circuit simulation using operating conditions and settings

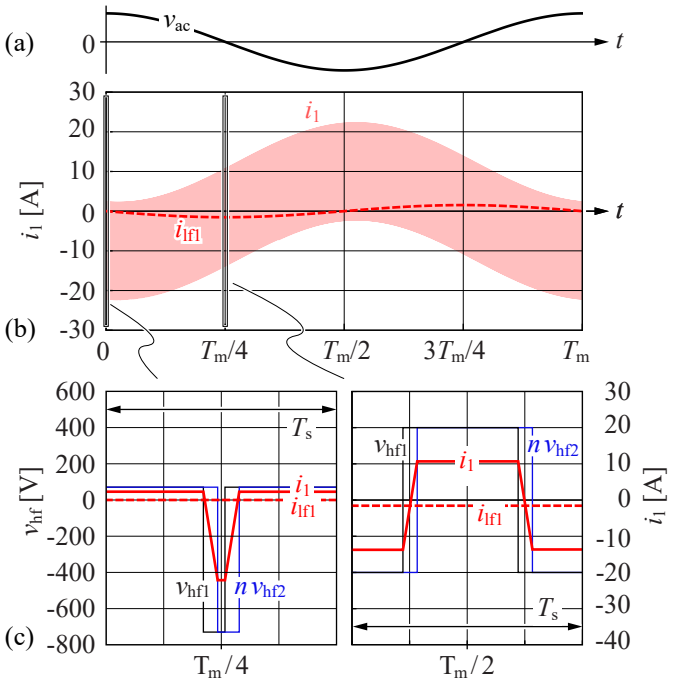

Fig. 6: Voltage and current waveforms determined for the single-phase system. (a) Sinusoidal input voltage over a mains period T_m. (b) Primary-side transformer current i_1 over a mains period. (c) i_1 and primary- and secondary-side HF transformer voltages v_{hf1} and v_{hf2} over a switching period T_s at $t = T_m/4$ and $t = T_m/2$, respectively.

according to Tables I and III. According to Figs. 7(a) and (b), the three-phase voltages are phase shifted by 120° and the primary- and secondary-side capacitor voltages are proportional, cf. (10). Fig. 7(c) illustrates the input currents, $i_{L\{a,b,c\}}$, at rated power and reveals that, with the considered value of L_{ac}, Zero Voltage Switching (ZVS) is partly lost at the primary side.[1] Detailed waveforms of the input currents at $t = 0$ and $t = 5\,\mathrm{ms}$ are shown in Fig. 7(d) and clearly disclose the superposition of $i_{L_{ac,a}}$ and $i_{L_{\sigma,a}}$ according to (18). Fig. 7(e) illustrates the time-varying output power levels of each phase, $\langle p_{1\phi\{a,b,c\}} \rangle$, which are sinusoidal and phase shifted by 120°. For this reason, constant total power results,

$$P_{out} = 3P_{1\phi,dc}. \tag{19}$$

It is worth mentioning that the output power of each phase is maximal at the zero crossing of the corresponding phase voltage, which is due to $D = 0.5$, cf. (4). Furthermore, with the considered specifications and converter settings, the amplitude of the sinusoidal characteristic superimposed on $\langle p_{1\phi\{a,b,c\}} \rangle$ is less than its average value ($1.6\,\mathrm{kW} < 2.7\,\mathrm{kW}$).

III. Optimized Converter Design

In this Section, the investigated D3AB PFC rectifier is optimized with regard to efficiency and power density; the optimization objective is maximum power density at a converter efficiency of 98%. The implemented optimization procedure employs analytical expressions to calculate the component currents, which have been verified at different operating points using a circuit simulator, revealing a high accordance with errors of less than 2%. With known currents, the below listed component models are evaluated with regard to losses and volumes:

[1] Full ZVS requires a minimum current, which is indicated in Fig. 7(c) and described in Section III-A.

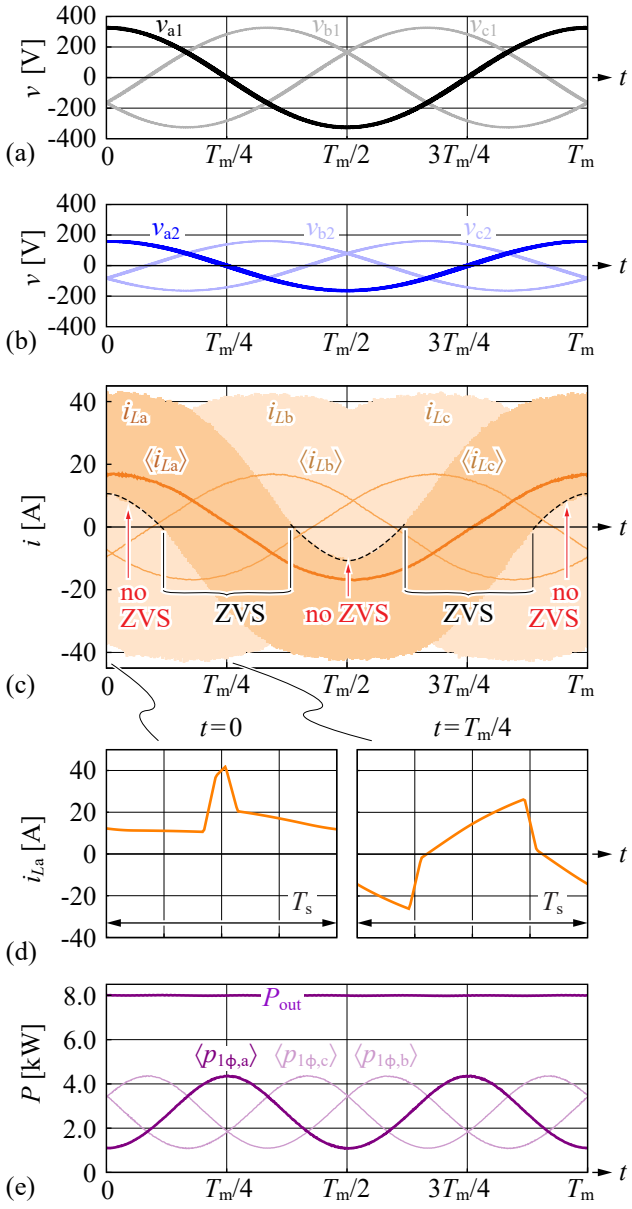

Fig. 7: Simulation results for the operating conditions and settings according to Tables I and III: (a) primary-side capacitor voltages; (b) secondary-side capacitor voltages; (c) input currents (= primary-side transformer currents; cf. Fig. 1); (d) magnified input current of phase a during $0 < t < T_s$ and $5\,\mathrm{ms} < t < 5\,\mathrm{ms} + T_s$, revealing the input current of the PFC rectifier (with current ripple) and the superimposed HF DAB transformer current, which shows a deviation from the ideal shape that originates from the series resonant circuit formed with L_σ and the filter capacitors C_{f1} and C_{f2}; (e) local average values of the instantaneous power levels of each phase and total output power.

- Semiconductors and cooling system in Section III-A,
- Magnetic components in Section III-B,
- Capacitors in Section III-C,
- EMI filter, gate drivers, and control in Section III-D.

A fully generalized converter optimization would feature a great number of open design parameters. Due to given specifications, known converter characteristics, and/or available components, however, a great number of design parameters can be readily defined. In this regard, V_{dc1} is set to 800 V in order to feature reasonable duty cycles with sufficient margins to 0 and 1, cf. (9), and still enable the use of power semiconductors with a blocking voltage of 1200 V.

Furthermore, it is known that DAB converters achieve most efficient operation for $V_{\mathrm{dc1}}/(nV_{\mathrm{dc2}}) \approx 1$. Thus, with regard to the specified output voltage, $V_{\mathrm{dc2}} = 400\,\mathrm{V}$, the turns ratio is set to $n = N_1/N_2 = 2$. Furthermore, (17) limits the maximum value of L_σ for given output power. The considered converter inductance is set to 80% of the maximum value,

$$f_\mathrm{s} L_\sigma = 80\%\,(f_\mathrm{s} L_\sigma)_\mathrm{max} = 80\%\,\frac{nV_{\mathrm{dc1}}V_{\mathrm{dc2}}}{8P/3}\left[\frac{1}{4} - \left(\frac{V_{\mathrm{m,pk}}}{V_{\mathrm{dc1}}}\right)^2\right],$$

to ensure controllability of the converter.

A. Semiconductors and cooling system

SiC power MOSFETs are used on the primary and secondary sides in order to take advantage of their low conduction and switching losses. Initial calculations of semiconductor losses reveal that low conduction and switching losses are achievable if single $25\,\mathrm{m\Omega}/1200\,\mathrm{V}$-devices (C2M0025120D by Cree) and $10\,\mathrm{m\Omega}/900\,\mathrm{V}$-devices (C3M0010090K by Cree) realize each switch on the primary and secondary sides, respectively. Using devices with increased on-state resistances would be possible with regard to the devices' rated currents and losses, however, reduced efficiencies would result. Conversely, the use of multiple MOSFETs connected in parallel would attain only limited improvements that may not justify the increased effort.[2]

The conduction losses are calculated based on the devices' on-state resistances at junction temperatures of 125°C,

- C2M0025120D ($25\,\mathrm{m\Omega}/1200\,\mathrm{V}$): $R_{\mathrm{DS,on},1} = 38\,\mathrm{m\Omega}$,
- C3M0010090K ($10\,\mathrm{m\Omega}/900\,\mathrm{V}$): $R_{\mathrm{DS,on},2} = 13\,\mathrm{m\Omega}$.

The calculation of the switching losses is based on measured switching losses for the considered devices from [16], [17] and depicted in **Fig. 8**. The considered polynomials are

$$E_\mathrm{sw} = \begin{cases} 233\,\mu\mathrm{J} - 15.1\,\frac{\mu\mathrm{J}}{\mathrm{A}}\,I_\mathrm{D} + 281\,\frac{\mathrm{nJ}}{\mathrm{A}^2}\,I_\mathrm{D}^2 & \forall \quad I_\mathrm{D} \le 0.53\,\mathrm{A}, \\ 12\,\mu\mathrm{J} + 212\,\mu\mathrm{J}\left(\frac{2.3\,\mathrm{A} - I_\mathrm{D}}{1.77\,\mathrm{A}}\right)^2 & \forall\ 0.53\,\mathrm{A} < I_\mathrm{D} < 2.3\,\mathrm{A}, \\ 17.1\,\mu\mathrm{J} - 2.53\,\frac{\mu\mathrm{J}}{\mathrm{A}}\,I_\mathrm{D} + 136\,\frac{\mathrm{nJ}}{\mathrm{A}^2}\,I_\mathrm{D}^2 & \forall \quad I_\mathrm{D} \ge 2.3\,\mathrm{A}. \end{cases} \tag{20}$$

for the $25\,\mathrm{m\Omega}/1200\,\mathrm{V}$-device, for operation with $800\,\mathrm{V}$ and $T_\mathrm{j} = 125°\mathrm{C}$ and

$$E_\mathrm{sw} = \begin{cases} 164\,\mu\mathrm{J} - 4.48\,\frac{\mu\mathrm{J}}{\mathrm{A}}\,I_\mathrm{D} + 2.85\,\frac{\mathrm{nJ}}{\mathrm{A}^2}\,I_\mathrm{D}^2 & \forall \quad I \le 1.2\,\mathrm{A}, \\ 3.4\,\mu\mathrm{J} + 155\,\mu\mathrm{J}\left(\frac{2.8\,\mathrm{A} - I_\mathrm{D}}{1.6\,\mathrm{A}}\right)^2 & \forall\ 1.2\,\mathrm{A} < I < 2.8\,\mathrm{A}, \\ 964\,\mathrm{nJ} + 837\,\frac{\mathrm{nJ}}{\mathrm{A}}\,I_\mathrm{D} + 10.1\,\frac{\mathrm{nJ}}{\mathrm{A}^2}\,I_\mathrm{D}^2 & \forall \quad I \ge 4.5\,\mathrm{A}. \end{cases} \tag{21}$$

for the $10\,\mathrm{m\Omega}/900\,\mathrm{V}$-device ($V_\mathrm{DS} = 400\,\mathrm{V}$, $T_\mathrm{j} = 70°\mathrm{C}$). Negative values of the instantaneous drain current during switching, I_D, denote switching operations where ZVS cannot be attained, i.e. turn-on losses occur, and $I_\mathrm{D} > 0$ denote switching operations where ZVS is in principle feasible. However, a minimum current is required for ZVS to fully charge and discharge the MOSFET's output capacitances. In this regard, the second polynomials in (20) and (21) represent partial ZVS that are approximated based on quadratic interpolations for a dead time interval of 200 ns. Remark: since the MOSFETs are used without external capacitors increasing C_oss, the very low loss property of ZVS is lost at high positive currents, due to turn-off losses (approximately at $I_\mathrm{D} > 20\,\mathrm{A}$ in Fig. 8).

[2]Even increased switching losses would result on the primary side, due to time intervals where turn-on losses occur, cf. Fig. 7. As a result, optimal designs would employ increased current ripples.

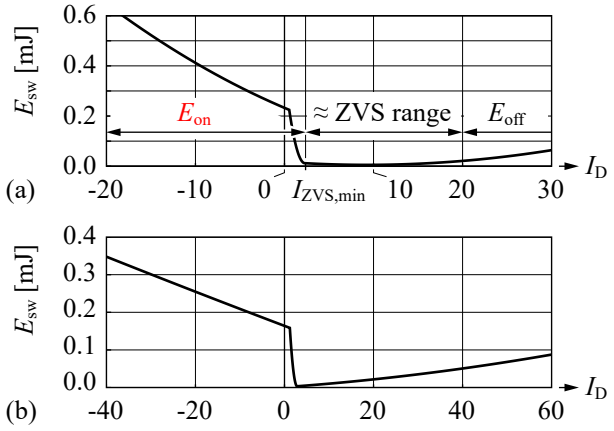

Fig. 8: (a) Switching losses of the $25\,\mathrm{m\Omega}/1200\,\mathrm{V}$ SiC MOSFET C2M0025120D for operation with $800\,\mathrm{V}$ and $T_\mathrm{j} = 125°\mathrm{C}$ and (b) the $10\,\mathrm{m\Omega}/900\,\mathrm{V}$ SiC MOSFET C3M0010090K for operation with $400\,\mathrm{V}$ and $T_\mathrm{j} = 70°\mathrm{C}$, with respect to the drain current, I_D, at the switching instant. Both Figures depict measured results from [16], [17] for $I_\mathrm{D} < 0$ and $I_\mathrm{D} > I_\mathrm{ZVS,min}$. For $0 \le I_\mathrm{D} \le I_\mathrm{ZVS,min}$ the switching losses for partial ZVS are interpolated for an assumed dead time interval of 200 ns.

TABLE II: Expressions used for scaling all lengths, areas, and volumes of the considered magnetic components (based on two stacked E 55/28/21 cores).

Core volume	$V_\mathrm{c} = 435 \times 10^{-3} V_\mathrm{box}$
Core cross section	$A_\mathrm{c} = 206 \times 10^{-3} V_\mathrm{box}^{2/3}$
Available winding cross section of coil former	$A_\mathrm{w} = 95.2 \times 10^{-3} V_\mathrm{box}^{2/3}$
Height of core window	$h_\mathrm{w} = 158 \times 10^{-3} V_\mathrm{box}^{1/3}$
Width of core window	$A_\mathrm{w} = 631 \times 10^{-3} V_\mathrm{box}^{1/3}$
Average turn length	$l_\mathrm{avg} = 2.64 V_\mathrm{box}^{1/3}$
Open surface to ambient	$A_\mathrm{open} = 5.51 V_\mathrm{box}^{2/3}$

The volume of the cooling system for power semiconductors with total losses of $P_\mathrm{semi,total}$ is considered by means of a Cooling System Performance Index (thermal conductance per volume), $CSPI$, of $13\,\frac{\mathrm{W}}{\mathrm{dm^3\,K}}$ and a considered temperature difference between heat sink and ambient of $\Delta T_\mathrm{hs-a} = 50°\mathrm{C}$,

$$V_\mathrm{cooling\ system} = \frac{P_\mathrm{semi,total}}{\Delta T_\mathrm{hs-a} \times CSPI}. \tag{22}$$

B. Magnetic components

This paper uses a unified scaled model for all magnetic components. The scaled model is parameterized according to the geometrical properties of the transformers realized in [8], which are compose of two stacked E 55/28/21 cores (boxed volume, V_box, is $200\,\mathrm{cm^3}$) and achieve efficiencies of 99.6% for an isolated three-phase PFC rectifier with a rated power of 7.5 kW. For a given value of V_box, all lengths, areas, and volumes of the magnetic component are determined according to the expressions listed in **Tab. II**. The input inductors/transformers of the D3AB PFC rectifier and the DAB converter inductors, L_σ, are considered separately in order to take the additional volumes and losses due to L_σ into account.

The employed component model calculates the core losses with the improved Generalized Steinmetz Equation (iGSE) [18] and the Steinmetz parameters

$$k = 1.02,\ \alpha = 1.4745,\ \text{and}\ \beta = 2.6607 \tag{23}$$

for the considered N95 ferrite core material (extracted for $f = 25\,\mathrm{kHz}$, $B_\mathrm{pk} = 300\,\mathrm{mT}$, and $T_\mathrm{c} = 80°\mathrm{C}$ with a software tool provided by TDK/EPCOS [19]). The copper losses are

determined using simplified expressions for HF skin- and proximity effects derived in [20], which assume a distributed air gap. The computation of the copper losses considers the first 30 harmonic components of each conductor current; the conductors employ HF litz wires with single strand diameters of $0.1\,\mathrm{mm}$.

The automated design procedure further takes an effective copper area of $38\% \times A_\mathrm{w}$ (A_w is the cross section of the core window, cf. Tab. II), a copper temperature of $100°\mathrm{C}$, a maximum flux density of $300\,\mathrm{mT}$, and a maximum temperature rise of the component's surface of $50°\mathrm{C}$ into account. The surface temperature rise is approximated according to [21],

$$\Delta T = \left(\frac{P/1\,\mathrm{mW}}{A_\mathrm{open}/1\,\mathrm{cm}^2} \right)^{\frac{1}{1.1}} \times 1°\mathrm{C} < 60°\mathrm{C}. \tag{24}$$

In a first step, the design procedure scans a wide range of values for V_box in order to determine a boxed volume that leads to a design close to the thermal limitation, $V_\mathrm{box,0}$. For this purpose, geometric sequences are used for V_box with common ratios of 0.5 (initial coarse scan starting from $V_\mathrm{box} = 10\,\mathrm{dm}^3$) and 1.1 (subsequent fine scan). For each given value of V_box an inner loop determines the optimal number of turns with respect to minimum total losses. In case of the input inductors/transformers, the available cross section of the core window is divided to the windings of primary and secondary sides such that same current densities result. Finally, the air gap length is determined to achieve the specified inductance.

Losses of magnetic components decrease with increasing volume. For this reason, the copper and core losses are calculated for further 29 magnetic components with increasing boxed volumes according to

$$V_{\mathrm{box},i} = V_\mathrm{box,0} \times 1.1^i \quad \forall \quad i \in \{1, 2, 3, \dots\ 29\} \tag{25}$$

and for optimized numbers of turns. The resulting volumes, losses, and design configurations (e.g. numbers of turns) are stored and the data transferred to the main converter optimization procedure.

C. Capacitors

The capacitors of the considered converter are subject to relatively high currents. In order to still achieve high power density, ceramic and film capacitors have been selected, which are listed below:

- C_f1: 1×B32754C2106K000 (film capacitor, $10\,\mu\mathrm{F}$, $250\,\mathrm{Vac}$, $12\,\mathrm{A}$, EPCOS),
- C_dc1: 1×CeraLink™ SP500 (ceramic capacitor, $12\,\mu\mathrm{F}$, $400\,\mathrm{Vdc}$, $41\,\mathrm{A}$, EPCOS),
- C_f2: 25×KR355WD72W125MH01 (ceramic cap., $0.85\,\mu\mathrm{F}$ at $163\,\mathrm{V}$, $450\,\mathrm{Vdc}$, $\approx 2\,\mathrm{A}$ at $50\,\mathrm{kHz}$, Murata),
- C_dc2: 1×CeraLink™ SP500 (same as C_dc1; note: capacitance drops to $8.4\,\mu\mathrm{F}$ at $200\,\mathrm{V}$).

The total volume of all capacitors is $160\,\mathrm{cm}^3$, which includes an additional volume of $30\,\mathrm{cm}^3$ for damping networks, an electrolytic output capacitor ($120\,\mu\mathrm{F}$, $450\,\mathrm{Vdc}$), and two SMD inductors that decouple the electrolytic capacitor from the CeraLink™ capacitors (C_dc2). The final design suggested by optimization has been successfully tested with comprehensive circuit simulation, using the above capacitance values, revealing only minor differences in terms of rms values and losses (conduction, switching, and core). It is worth to note that the optimization does not consider capacitor losses, due to their comparably low contribution to the total losses.

D. Remaining components

The volumes and losses of EMI filter, gate drivers, and control have been adopted from [22], due to similar specifications and optimization objectives:

$$P_\text{EMI filter} = 5\,\mathrm{W} \tag{26}$$
$$P_\text{gate drivers} + P_\text{control} + P_\text{fan} = 12\,\mathrm{W}, \tag{27}$$
$$V_\text{EMI filter} = 0.35\,\mathrm{dm}^3, \tag{28}$$
$$V_\text{gate drivers} + V_\text{control} = 0.3\,\mathrm{dm}^3, \tag{29}$$
$$V_\text{total} = 1.15 \sum V_i, \tag{30}$$

i.e., 15% of the volume is considered to be unused.

E. Optimization

Based on the above considerations and assumptions, it is found that the switching frequency, f_s, the input current ripple,

$$r = \frac{\Delta I_{L\mathrm{ac,pkpk}}}{\frac{2P}{3V_\mathrm{m,pk}}} = \frac{\Delta I_{L\mathrm{ac,pkpk}}}{I_\mathrm{m,pk}}, \tag{31}$$

and the considered boxed volumes of the magnetic components remain for optimization of efficiency and power density. The considered settings are defined with

$$f_\mathrm{s} \in \{23,\ 27,\ 35,\ 47,\ 72,\ 140\}\mathrm{kHz}, \tag{32}$$
$$r \in \{30,\ 50,\ 75,\ 100,\ 125,\ 150,\ 175,\ 200,\ 225,\ 250,\ 275,\ 300\}\%, \tag{33}$$

where the listed switching frequencies are preselected with regard to small volume EMI filters (cf. Fig. 12 in [23]). The sets defined for f_s and r lead to 72 different settings. Furthermore, 900 combinations of different designs result for the input inductors/transformers and the DAB inductors (30 for each, cf. Section III-B) for given values of f_s and r, which, in total, yields 64800 results. **Fig. 9** depicts the corresponding results and discloses the η-ρ Pareto front for the investigated converter system.

The orange star in Fig. 9 marks the selected operating point, which achieves $\eta = 98.1\%$ and $\rho = 4\,\mathrm{kW/dm}^3$ at $f_\mathrm{s} = 35\,\mathrm{kHz}$, $r = 175\%$, and for magnetic components with maximum power density, i.e., operated at their thermal limitation. The resulting Pareto-optimal design points reveal increasing efficiency for decreasing power density, which is directly related to the similar η-ρ characteristics of magnetic components. From a detailed inspection of the design points on the Pareto front it becomes apparent that design points with Pareto-optimal power density and very high efficiency are obtained for reduced switching frequencies (switching losses, core losses) and reduced current ripples (rms currents, conduction and copper losses, core losses; reduced switching frequencies overcompensate the increases of switching losses by reason of reduced current ripples).

The red triangles in Fig. 9 mark results with constant switching frequency of $35\,\mathrm{kHz}$, magnetic components with maximum power densities, and different values of r. It can be observed that reduced power densities and efficiencies result for $r < 175\%$. The reduced power densities are mainly addressed to increased boxed volumes of the PFC input inductors and the reduced efficiencies originate from both, the PFC input inductors due to the required increased energy storage capability and the semiconductors on the primary side, which generate increased switching losses due to an increase of the region where ZVS is lost, cf. Fig. 7. Slightly reduced converter volumes are feasible for $r > 175\%$, however, the efficiency quickly decreases by reason of large rms currents.

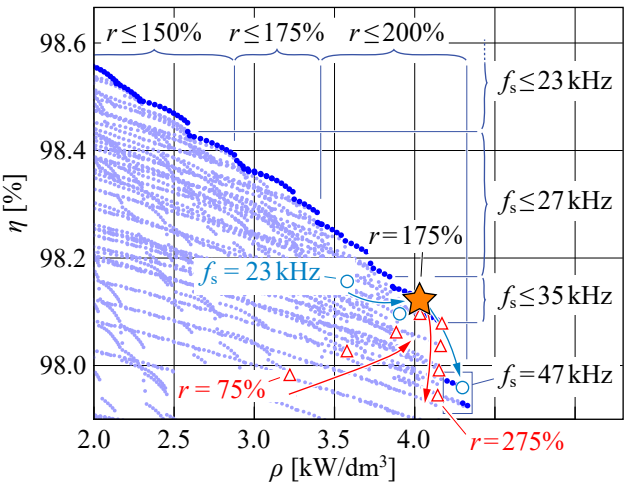

Fig. 9: Efficiencies, power densities, and η-ρ Pareto front determined for the D3AB PFC rectifier.

The cyan circles mark results with constant current ripple of 175%, magnetic components with maximum power densities, and different switching frequencies. It can be seen that a considerably reduced switching frequency of 23 kHz still facilitates a relatively high power density of 3.6 kW/dm^3. In this regard it is found that Pareto-optimal designs with very high efficiencies not only require reduced switching frequencies and power densities but also magnetic components with increased boxed volumes.

IV. Discussion of Design Result

Tab. III lists the design results at the selected operating point identified in Fig. 9 and **Figs. 10(a)** and **(b)** depict the corresponding component losses and volumes, respectively. According to Fig. 10(a), more than half of the total losses are attributed to the semiconductor losses which are mainly generated in the power MOSFETs on the primary side. A reduction of the primary-side conduction losses could be achieved by increasing the corresponding chip sizes, which, however, would increase the switching losses. The magnetic components generate one third of the losses; here, losses mainly occur in the windings of the input inductors, which are already operated with maximum flux densities of 300 mT, i.e., a further increase of the core losses is not feasible.

Approximately two thirds of the converter volume are required for passive components (magnetics, capacitors, EMI filter). Due to comparably low semiconductor losses (84 W at rated power), a cooling system with a comparably small volume can be employed, e.g., using double-sided cooling a small fan with an edge length of 30 mm, which is found to enable the realization of a cooling system with the calculated low volume of 130 cm^3 and still provides a sufficiently large base plates to accomodate all 12 MOSFETs.

Fig. 11(a) and **(b)** depict the calculated characterists of efficiency and selected components' losses with respect to the output power and reveal that $\eta > 98\%$ is feasible for $P_{\text{out}} > 2.3\,\text{kW}$. According to Fig. 11(b), substantial conduction losses and losses in the magnetic components remain at very low power, due to the inductor current ripples. However, increasing switching losses are observed for decreasing output power and $P_{\text{out}} < 2\,\text{kW}$. A close investigation reveals that the currents during switching of the secondary-side MOSFETs are insufficient for ZVS, cf. **Fig. 12(a)** and Fig. 8(b). ZVS could

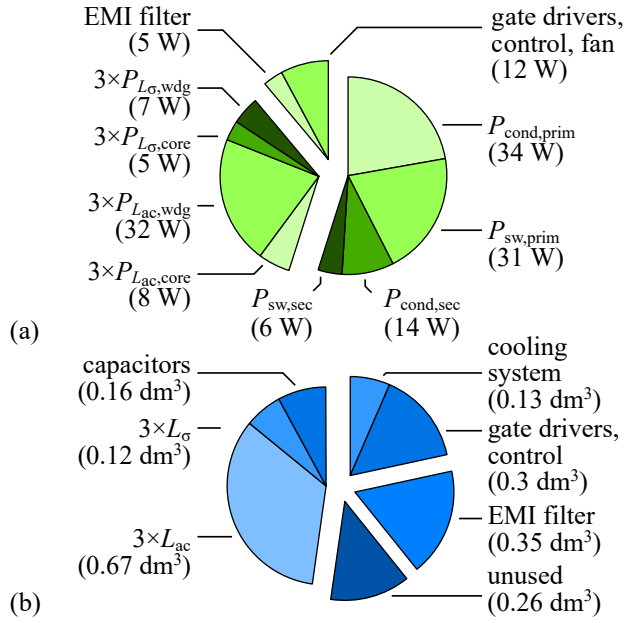

Fig. 10: (a) Component losses and (b) volumes for the selected design point with $\eta = 98.1\%$ and $\rho = 4\,\text{kW/dm}^3$.

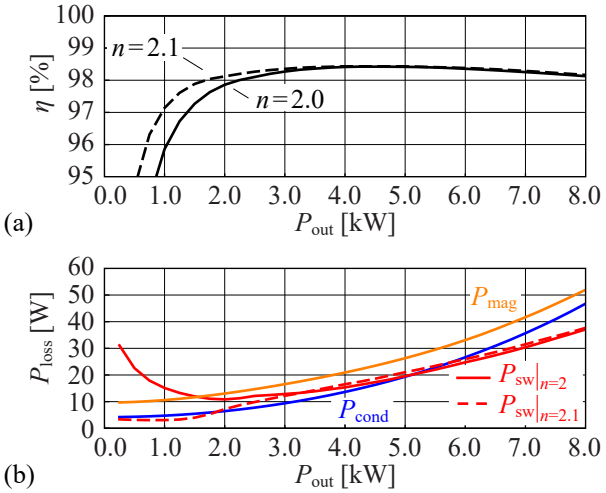

Fig. 11: (a) Total converter efficiency and (b) characteristics of selected components' losses with respect to output power.

be attained if three inductors would be placed in parallel to the three transformers' secondary windings. According to the results of an analytical investigation of the equivalent circuit of a transformer, however, the same effect can be achieved for a slight adjustment of the transformers' turns ratios, from $n = 2$ to $n = 2.1$, cf. **Fig. 12(b)**. With this minor adjustment, a substantial efficiency improvement is achieved at low output power levels, i.e., $\eta > 98\%$ for $P_{\text{out}} > 1.7\,\text{kW}$.

V. Conclusion

This paper proposes and analyzes a novel three-level and three-port isolated and bidirectional PFC rectifier topology (D3AB PFC rectifier), which can be realized with standard 6-pack power modules on the primary and secondary sides, employs integrated input inductors and HF transformers, and/or features galvanic isolation and high efficiency. The given in-depth description of the working principle of the D3AB PFC rectifier allows the derivation of key expressions needed

TABLE III: Summary of results for the selected converter design, cf. Fig. 9.

General results and rms currents	
Switching frequency	$f_s = 35\,\mathrm{kHz}$
Current ripple	$r = 175\%$
Calculated efficiency at rated load	$\eta = 98.1\%$
Calculated total power density	$\rho = 4\,\mathrm{kW/dm^3}$
Transformer rms current, prim. and sec. sides	$I_{\mathrm{tr1,2}} = \{17.2\,\mathrm{A}, 19.2\,\mathrm{A}\}$
MOSFET rms currents,prim. and sec. sides	$I_{\mathrm{T,prim,sec}} = \{12.2\,\mathrm{A}, 13.6\,\mathrm{A}\}$
Magnetic input inductor/transformer L_{ac}	
Inductance	$L_{\mathrm{ac}} = 195\,\mu\mathrm{H}$
Boxed volume	$V_{\mathrm{box}} = 223\,\mathrm{cm^3}$
Number of turns, prim. and sec. sides	$N_{1,2} = \{20, 10\}$
Air gap length	$l_{\mathrm{air}} = 1.9\,\mathrm{mm}$
Conductors, prim. and sec. sides (HF litz wires)	$\{547, 610\} \times 0.1\,\mathrm{mm}$
Copper losses	$P_{\mathrm{w}} = 10.6\,\mathrm{W}$
Core losses	$P_{\mathrm{c}} = 2.5\,\mathrm{W}$
Calculated temperature rise	$\Delta T = 44°\mathrm{C}$
DAB inductor L_σ/n^2 (placed on the secondary side)	
Inductance	$L_\sigma = 14.5\,\mu\mathrm{H}$
Boxed volume	$V_{\mathrm{box}} = 41\,\mathrm{cm^3}$
Number of turns	$N = 9$
Air gap length	$l_{\mathrm{air}} = 1.7\,\mathrm{mm}$
Conductor: HF litz wire	$610 \times 0.1\,\mathrm{mm}$
Copper losses	$P_{\mathrm{w}} = 2.4\,\mathrm{W}$
Core losses	$P_{\mathrm{c}} = 1.8\,\mathrm{W}$
Calculated temperature rise	$\Delta T = 44°\mathrm{C}$

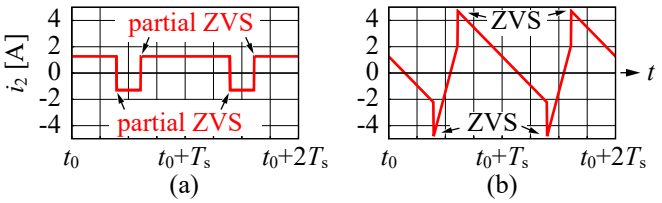

Fig. 12: Calculated current at the transformer's secondary side for $P_{\mathrm{out}} = 500\,\mathrm{W}$, $t_0 = 2.5\,\mathrm{ms}$, operating conditions and parameters according to Tab. I and Tab. III, and different turns ratios: (a) $n = 2$, (b) $n = 2.1$.

to design the converter system with respect to optimized performance values, e.g. efficiency and power density, which serves as a basis for the converter optimization presented in the second part of this paper. According to the calculated results, a full-load efficiency of 98.1% and a power density of $4\,\mathrm{kW/dm^3}$ can be achieved for the PFC rectifier if SiC MOSFETs are used ($25\,\mathrm{m\Omega}/1200\,\mathrm{V}$ and $10\,\mathrm{m\Omega}/900\,\mathrm{V}$ devices on primary and secondary sides, respectively). The presented design is found to achieve efficiencies greater than $98\,\%$ for $P_{\mathrm{out}} > 1.7\,\mathrm{kW}$.

The discussions given in this paper are confined to the basic structure, operating behavior, and design of the new topology. Further research will focus on the investigation of prospective efficiency and/or power density improvements that can be achieved with modified topologies and alternative control schemes that take advantage of currently unused degrees of freedom of the considered converter system. Corresponding examples include realizations where only CM or DM components are utilized for energy transfer and alternative control schemes with non-constant values of the phase shift and different duty cycles, $D_1 \neq D_2$.

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