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Novel Highly Efficient/Compact Automotive PCB Winding Inductors Based on the Compensating Air-Gap Fringing Field Concept

J. Schäfer,
D. Bortis,
J. W. Kolar

Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

Novel Highly Efficient/Compact Automotive PCB Winding Inductors Based on the Compensating Air-Gap Fringing Field Concept

Jannik Schäfer, *Student Member, IEEE,* Dominik Bortis, *Member, IEEE,* and Johann W. Kolar, *Fellow, IEEE*

***Abstract*—Especially in the automotive sector, the design of power electronic converters is subject to extreme cost pressure. Consequently, each component needs to be optimized regarding material and manufacturing cost. The latter is especially important for magnetic components, as the expensive wire-wrapping process has a significant impact on the overall production costs. In this paper, a new inductor concept is proposed, where the winding is directly integrated into the printed-circuit-board, while at the same time the usually large high-frequency conduction losses are mitigated. This is achieved by using the fringing field around a single air gap or several (distributed) air gaps for compensating the adverse magnetic skin and proximity fields within the winding. Consequently, low AC to DC resistance ratios are achieved and the required copper cross-section of the winding can effectively be reduced. Furthermore, a thermal model for the PCB winding is derived, which allows for designing PCB windings close to the thermal limit and therefore inductors with very high power densities are obtained. Finally, the findings of this paper are verified by experimental measurements and a simplified design sequence is described.**

***Index Terms*—printed-circuit-board (PCB) winding, inductor design, magnetic field compensation.**

I. Introduction

In the last decade, a rising demand for electric vehicles (EVs) emerged out of the continuing trend towards greater electrification in transportation, driven by the increasing environmental awareness of the end customers. Therefore, especially in the automotive sector with its enormous commercial potential, an exceedingly competitive market evolved. The low achievable profit margins in this area demand for more and more cost-effective solutions, while at the same time better performances need to be achieved. Consequently, each component of the vehicle needs to be optimized in terms of cost, efficiency and power density in order to develop competitive products.

Besides the mechanical drive train, the most important components in state-of-the-art EVs are the various power electronic converter systems of the energy distribution grid, as e.g. battery chargers, DC/AC inverters and DC/DC step-down converters. Hence, there is a large potential for cost saving by using optimized designs and converter topologies. However, all these systems have one operating condition in common: They are charging or are powered from a battery and are therefore required to handle a varying input and/or output voltage [1]–[4]. These varying voltages impede the design of such systems, as in contrast to converters with a fixed input to output voltage transfer ratio, where the voltage adoption can effectively be achieved by e.g. a transformer with an appropriate turns ratio, a converter system with variable voltage transfer ratio in principle demands for an energy storage element, i.e. a capacitor and/or an inductor, which absorbs the changing voltage difference between the input and the output voltage.

There are two different passive energy storage elements which can be used for this purpose: On the one hand, capacitors as used in so-called switched capacitor converters (SCCs) [5], [6] or hybrid SCCs, if a voltage regulation is required [7], [8], and on the other hand, inductors as used in almost all classical topologies like buck, boost and buck-boost converters [9], [10]. Even though capacitors achieve a higher energy density, which

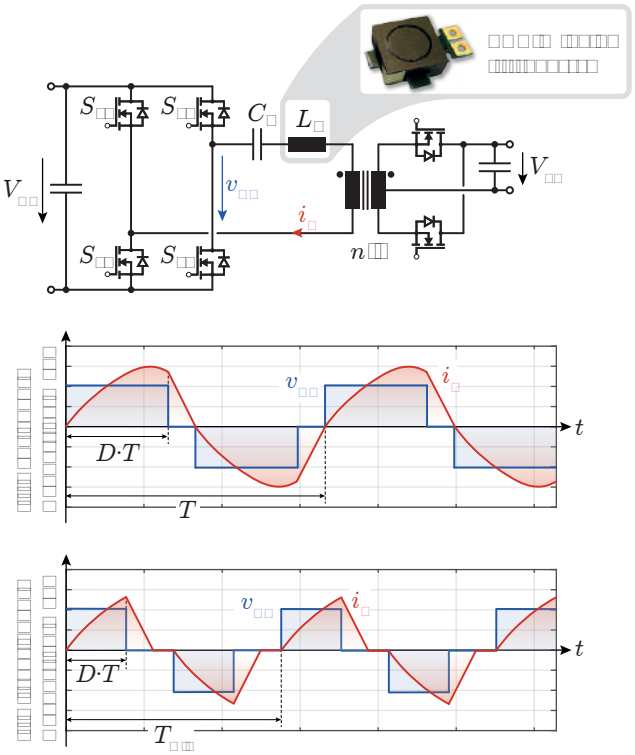

Fig. 1. Series-resonant converter topology for a 3 kW, 500 V → 15 V DC/DC step-down converter. The converter is operated in continuous conduction mode (CCM) for high power levels and discontinuous conduction mode (DCM) for low output power values.

J. Schäfer, D. Bortis and J. W. Kolar are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology, Zurich 8092, Switzerland (e-mail: schaefer@lem.ee.ethz.ch; bortis@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

TABLE I. Specifications of a 3 kW HV/LV Step-Down Converter for Automotive Applications.

Input Voltage	V_{HV}	250 V...500 V
Output Voltage	V_{LV}	10.5 V...15 V
Output Power	P_{out}	0 W...3 kW
Coolant Temperature	T_{A}	80 °C

makes them the more promising energy storage element in power-dense applications, the usually large number of switches needed in SCC topologies in combination with a comparably poor reliability of such systems make them less attractive for automotive applications, where reliability is key for all system components. Consequently, inductors are still widely used in industrial converter systems in order to ensure simplicity and reliability.

Unfortunately, the utilization of conventional inductors in a power electronic system significantly increases the overall manufacturing costs, as the wire-wrapping process complicates the production severely. Furthermore, following the trend towards higher switching frequencies in converter systems, expensive litz wire windings need to be used instead of solid conductor windings, as solid conductors are prone to high-frequency (HF) effects, i.e. suffer from high skin and proximity losses.

In transformers, for example, these effects can be circumvented by integrating the windings directly into a printed-circuit-board (PCB) [11], [12]. Thus, the wire-wrapping process is omitted, and, due to the coplanar arrangement of the primary and secondary windings, the HF effects in the windings are effectively mitigated.

Even though the winding of an inductor can also be integrated into the PCB, the mitigation of the HF effects is much more difficult in this case, as there is no secondary winding and/or anti-parallel current flow, which would compensate the proximity fields in the winding. Consequently, either a distributed or quasi-distributed air gap as proposed in [13] should be used, which tries to minimize the impact of the fringing field around the air gap on the inductor winding, or a different magnetic field compensation concept can be used, as firstly introduced in [14], which utilizes the fringing field around the air gap in a beneficial way. This paper now shows how this magnetic field compensation concept can be applied to a practical implementation of a PCB-winding inductor, which will finally be employed in a 500 V to 15 V, 3 kW series-resonant step-down converter for automotive applications. This converter stage is usually used to transfer power from the main high-voltage (HV) battery of an EV to the auxiliary low-voltage (LV) battery, according to typical specifications as summarized in **Tab. I**. As most promising topology, the series-resonant converter of **Fig. 1** is chosen for this application, due to its various advantages compared to other non-resonant topologies: On the one hand, the current within the converter is almost sinusoidal for high output power values, whereby its low harmonic content minimizes the HF conduction losses in the magnetic components, and at the same time reduces the EMI filtering effort. On the other hand, the secondary-side switches are operated as synchronous rectifiers only, whereby zero-voltage-switching (ZVS) and zero-current-switching (ZCS) are guaranteed over the full operating range. This is especially important for low-voltage high-current applications (up to 280 $\mathrm{A_{pk}}$ in this case), where switches with large silicon areas and therefore large Q_{oss} need to be employed. Without ZVS conditions, the large output capacitance charges of these switches would lead to considerable switching losses. Even though ZVS minimizes the switching losses, ZCS is equally important, as the switch-internal di/dt for actively switched currents induces significant over-voltages across the parasitic inductance of the semiconductor packages. Thus, without ZCS, semiconductors with larger breakdown voltages and therefore higher specific on-state resistances would need to be employed. Consequently, a synchronous rectifier is the most efficient topology for low-voltage high-current converter output ports.

Unfortunately, one of the biggest weaknesses of resonant converter systems is the operation with input-output voltage ratios which do not correspond to their effective transformation ratio n, which is given by the ratio of the number of turns of the transformer windings ($n = \frac{N_{\mathrm{HV}}}{N_{\mathrm{LV}}}$). Hence, the difference between the input voltage V_{HV} and the primary side referred output voltage $n \cdot V_{\mathrm{LV}}$ is directly applied across the resonant tank, which has a very low impedance if the converter is operated close to its resonant frequency. Consequently, in order to control the power flow through the resonant tank, its impedance needs to be increased by selecting a switching frequency of the converter above the resonant frequency. As shown in **Fig. 2**, the required increase in frequency $f_{\mathrm{sw,0\to x}}$ for a certain required impedance Z_{LC} highly depends on the ratio between L and C of the resonant tank. Hence, with a larger resonant inductance, a lower switching frequency range is required and therefore also the switching losses and the HF conduction losses of the converter are reduced. However, a large inductance also means a large volume of the inductor, whereby the overall power density of the converter is reduced. The optimal inductance value is therefore a tradeoff between

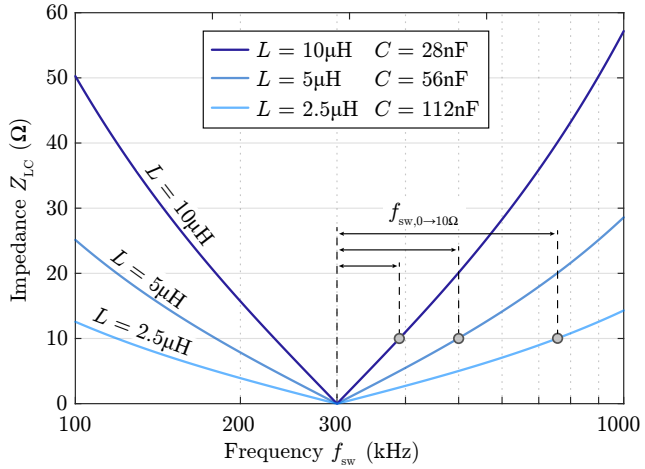

Fig. 2. Three impedance curves of different resonant tanks with the same resonance frequency of 300 kHz are shown. Additionally, the required frequency range $f_{\mathrm{sw,0\to 10\Omega}}$ for an increase of the tank impedance Z_{LC} from 0 Ω to 10 Ω is illustrated.

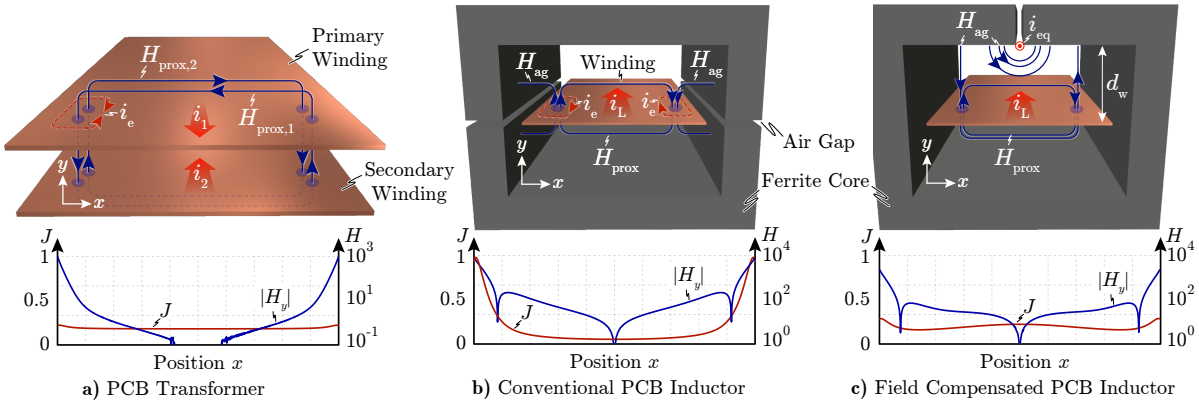

Fig. 3. Magnetic field distributions and the corresponding normalized current densities J and vertical magnetic field components H_y of **a)** a PCB-winding transformer with coplanar arrangement of the two windings, **b)** a conventional PCB-winding inductor with the air gap in the same physical layer as the winding and **c)** the proposed PCB-winding inductor design, where the air gap is arranged perpendicularly to the windings.

TABLE II. Specifications of the Optimized Series-Resonant Inductor.

Inductance	L	$6.8\,\mu\mathrm{H}$
Max. RMS Current	$I_\mathrm{L,RMS}$	$17.9\,\mathrm{A_{RMS}}$
Peak Current	$I_\mathrm{L,pk}$	$25.2\,\mathrm{A_{pk}}$
Switching Frequency	f_sw	300 kHz...720 kHz

efficiency and power density of the converter.

For the application at hand, the optimal inductor should comply with the specifications given in **Tab. II**, that are found by means of a multi-objective optimization of the overall converter system, which is out of the scope of this paper.

Considering **Tab. II**, one has to note that the classical approach of using the leakage inductance of the transformer as a series-resonant inductor cannot always be used efficiently, as e.g. in this case the achievable leakage inductance values of PCB transformers are much lower then the required value of $6.8\,\mu\mathrm{H}$. Of course, there are different design strategies where such large leakage inductances could be achieved [15], but these are only obtained by introducing a poor coupling between the primary and secondary transformer windings, such that the mutual compensation of the proximity fields of the two windings is lost and the HF losses are significantly increased.

Therefore, the only reasonable way to achieve large inductance values is the utilization of an external inductor, whose appropriate design is described in this paper, resulting in a highly-efficient and compact PCB-winding inductor.

In **Section II**, the applied magnetic field compensation concept for the PCB-winding inductor [14] is shortly revisited based on a single layer PCB winding, where a special focus is put on its practical implementation. Subsequently, the impact of using multiple PCB layers on the quality of the field compensation is discussed in **Section III** and the performance as well as the applicability of the concept is proven by means of experimental measurements in **Section IV**. In **Section V**, the thermal model of the PCB-winding inductor is analyzed in detail and a thermally enhanced inductor design is proposed and verified, again by means of experimental measurements. The derived design guidelines are then summarized in **Section VI**, based on an exemplary design sequence of the previously mentioned series-resonant inductor. Finally, **Section VII** concludes the findings of this paper.

II. Field Compensation Concept

In this section, the derivation of the previously introduced compensating fringing field concept (CFFC) [14] is shortly revisited, in order to facilitate the understanding of the possibilities and limitations of this design strategy in real applications. Starting with the simplified magnetic field distribution in a conventional PCB-winding transformer (cf. **Fig. 3a**)), it can be seen that, based on Ampere's law, each winding induces a HF magnetic field H_prox around itself. This magnetic field penetrates the conductor of the other winding, whereby significant eddy currents i_e would be induced, resulting in an increased AC-resistance of the windings and therefore in high conduction losses. Fortunately, the currents in the two transformer windings are flowing in opposite directions, whereby the two HF magnetic fields $H_\mathrm{prox,1}$ and $H_\mathrm{prox,2}$ are heading in opposite directions as well. Thus, for magnetically well coupled transformers, where the currents in the two windings generate almost equal magneto-motive forces, the two magnetic fields mutually compensate each other, resulting in almost negligible eddy current induction and therefore AC to DC resistance ratios of almost one.

In inductors, however, this inherent field compensation is not given, as there is only a current flow in one direction (cf. **Fig. 3b)**). Consequently, the HF magnetic field H_prox is penetrating the conductor perpendicularly to its surface, whereby significant eddy currents i_e are induced. These induced currents effectively reduce the copper cross-section of the winding utilized for current conduction (as analytically derived in [14]), and therefore increase the AC resistance significantly. In conventional PCB-winding inductors, this effect becomes even worse, since the fringing field H_ag around the air gap generates an additional vertical magnetic field component inducing additional eddy currents, if the air gap is placed in the same physical layer as the winding (as given e.g. for

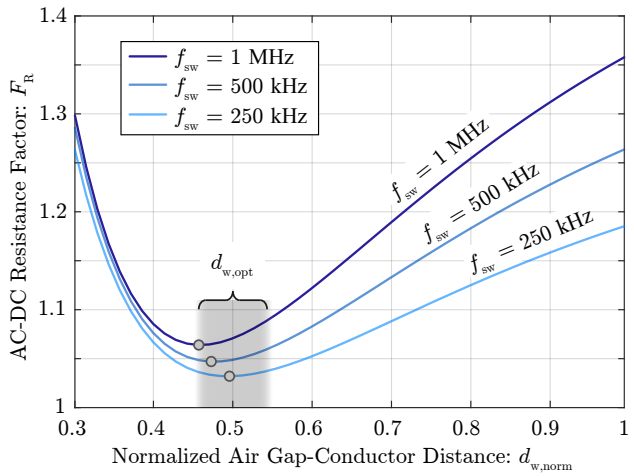

Fig. 4. AC to DC resistance ratios of the conductor for three different frequencies f_{sw} in an arrangement according to **Fig. 3c)** for a variable distance d_w between the air gap and the conductor.

pot cores and ELP cores). In practical applications, the air gap is therefore usually placed as far as possible from the winding, in order to minimize the impact of the fringing field on the conductor. Moreover, there were different approaches presented to further reduce the effect of the fringing field on the inductor winding, as e.g., avoiding the air gap completely by building air coil inductors for HF applications [16], placing the air gap in the corner of the winding window [17], or distributing the total air gap among many small air gaps [18]. Consequently, all conventional approaches for designing efficient and power-dense PCB-winding inductors have one thing in common: they try to minimize the impact of the fringing field around the air gap on the PCB winding as far as possible, either by minimizing the magnitude of the fringing field inside the winding window (distributed air gap), or by maximizing the distance between the air gap and the winding. The proposed PCB-winding inductor design concept, however, does not avoid the penetrating fringing field H_{ag} in the winding, but rather uses it to compensate the vertical field components H_{prox} within the winding. This compensation can be achieved by a simple relocation of the air gap to the top of the winding [13], as shown in **Fig. 3c)**. In this arrangement, the fringing field around the air gap acts like the proximity field of an equivalent current with magnitude $i_{eq} = -i_L$ located at the position of the air gap [19]. Hence, a transformer-like magnetic field distribution is achieved and the HF conduction losses can effectively be mitigated.

However, as shown in [14], the quality of the field compensation highly depends on the distance between the air gap and the conductor d_w (cf. **Fig. 4**), as well as on the number of air gaps N_{ag}. The following rules of thumb can be derived for straight conductors in an inductor arrangement according to **Fig. 5**:

$$d_{w,opt} = \frac{b_w}{2 \cdot N_{ag}} \qquad d_{ag,opt} = \frac{b_w}{N_{ag}}, \tag{1}$$

where b_w and $d_{ag,opt}$ denote the width of the conductor and the optimal distance between multiple air gaps, respectively. Hence, with more air gaps, the core can be placed closer to the winding, leading to a more power-dense inductor design. However, the complexity of the core manufacturing increases with the number of air gaps too, which is why N_{ag} should be chosen to be as small as possible, while still complying with the required power density of the component.

In most practical applications, the inductor windings are not straight, but rather of circular shape in order to minimize the winding length. However, the very same design guidelines can also be used for circular conductor arrangements, as long as the ratio between the outer and the inner radius of the conductor is not exceeding a value of approximately 2, as anyway given in almost all practical applications. For all other ratios, the accurate values for $d_{w,opt}$ should be used, as given in [14].

Besides the circular shape, there is usually more than one turn required in practical applications, in order to achieve a certain required inductance. For this reason, the influence of multiple turns of a PCB winding on the effectiveness of the compensating fringing field concept (CFFC) is investigated in the following section.

III. Multi-Turn PCB Winding

In a practical application, the number of turns of an inductor is usually larger than one, whereby either multiple tracks on one PCB layer, multiple PCB layers with one track each, or a combination of both needs to be used. Ideally, only a single PCB layer with a spiral winding should be employed, as this layer can be placed in the ideal distance $d_{w,opt}$ to the air gap, whereby AC to DC resistance ratios of close to one can again be achieved. Additionally, there

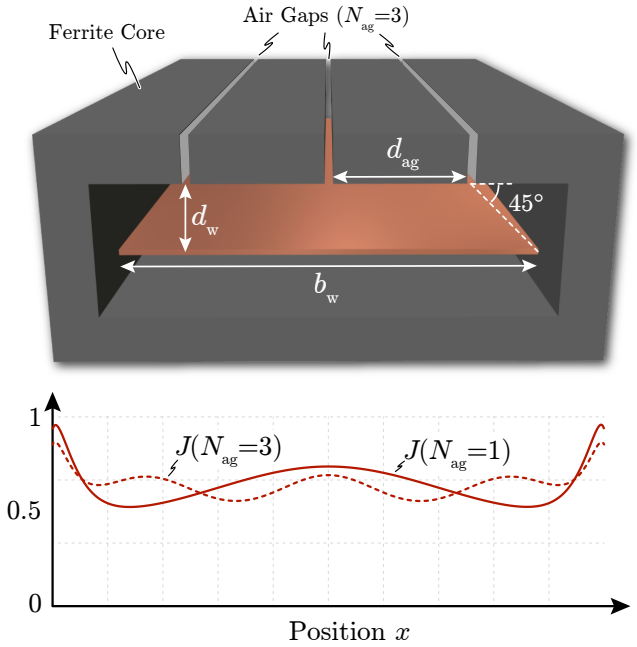

Fig. 5. Optimal arrangement of a PCB-winding inductor with three air gaps. The cutting surfaces of the core are colored in light gray in order to ensure good visibility of the air gap placement. In addition, the normalized current density distribution of a single air gap ($N_{ag} = 1$) and triple air gap ($N_{ag} = 3$) arrangement are shown.

is no need for layer transitions within the winding and vias can therefore be completely omitted. However, in high power applications, the limited height of a PCB copper layer ($35\,\mu\mathrm{m}...105\,\mu\mathrm{m}$) demands for large track widths, in order to carry the currents through the winding with a reasonable current density ($\leq 100\,\mathrm{A\,mm^{-2}}$). For a single turn winding, this inherently would result in a large total winding width $b_{\mathrm{w,SL}}$ and therefore huge overall inductor dimensions.

The only possibility to reduce the winding width, while at the same time keeping a certain maximum current density, is the utilization of multiple helical PCB layers, as shown in **Fig. 6**. Hence, compared to a single-layer spiral winding, in a multi-layer helical winding there is only a single turn per layer, where the individual turns are interconnected through vias in vertical direction. Consequently, each layer of the PCB can be used for the winding, whereby the ratio between the width of a multi-layer winding $b_{\mathrm{w,ML}}$ and the width of the equivalent single-layer winding $b_{\mathrm{w,SL}}$ is inversely proportional to the number of PCB layers N_{layer} used, according to $\frac{b_{\mathrm{w,ML}}}{b_{\mathrm{w,SL}}} = \frac{1}{N_{\mathrm{layer}}}$.

Even though the transition between the layers should ideally be done with blind and buried vias within the winding, this is usually not possible due to cost reasons. Thus, through-hole vias need to be used, which can either be placed at the inner or outer edge of the winding. However, the inner location should be preferred, as it is more efficient due to the shorter total winding length.

The layer transition with through-hole vias, however, requires a certain overlap between two consecutive turns, such that multiple vias can be used for the layer transition and the maximum current per via is not exceeded. Consequently, the effective winding length per layer $l_{\mathrm{w,eff}}$ is reduced (cf. **Fig. 6**), whereby the number of turns per layer N_{pL} is always smaller than one. Thus, if a vertically aligned termination is required, which means that the beginning of the winding needs to be exactly at the same position as its respective end, the total number of turns N_{L} will always be lower than the number of PCB layers N_{layer}, as for $N_{\mathrm{L}} = N_{\mathrm{layer}}$, an N_{pL} value of exactly one would be required. This, however, would only be possible with vias at the inner and outer radius of the winding, yielding a significantly reduced available copper cross-section of the winding for a certain given b_{w}. The optimal number of turns of such a PCB-winding inductor, which results in the best copper utilization, is therefore given as

$$N_{\mathrm{L}} = N_{\mathrm{layer}} - 1. \tag{2}$$

For large required inductance values, it is of course also possible to use multiple turns per layer, however, this inherently demands for vias at the inner and outer radius of the winding, as the positions of the layer transitions are alternating between inner radius and outer radius of the winding as well. Thus, the total width of the PCB winding is further increased, as at least $1\,\mathrm{mm}$ is required for the vias and their necessary clearance to the adjacent turns. Especially for small winding widths b_{w}, this has a large influence on the overall power density of the inductor. Hence, the multi-layer helical winding with single

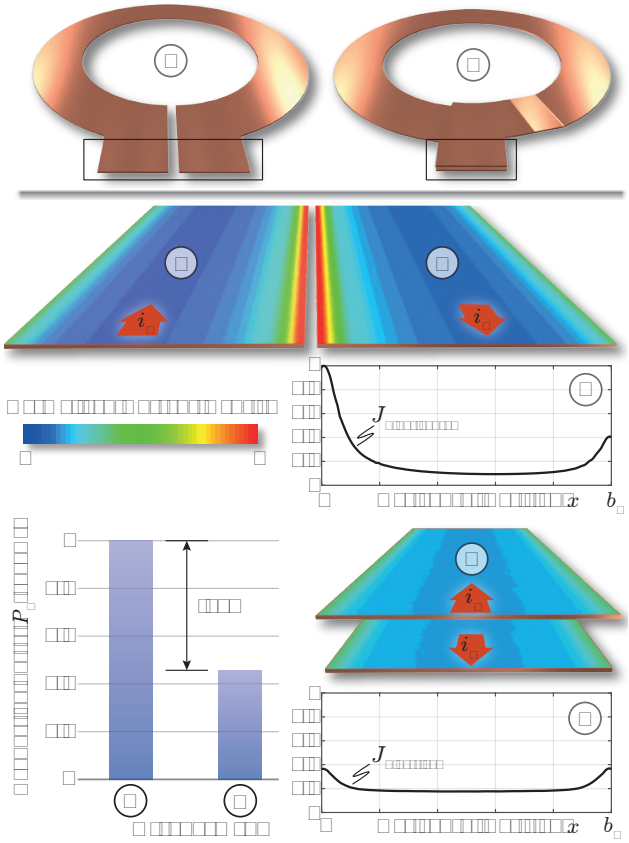

Fig. 7. FEM-simulated current densities in a horizontal (H) and a vertical (V) parallel termination for a frequency of $500\,\mathrm{kHz}$ and a track width of $5\,\mathrm{mm}$. The normalized conduction losses P_{n} of the two possible terminations are shown as well.

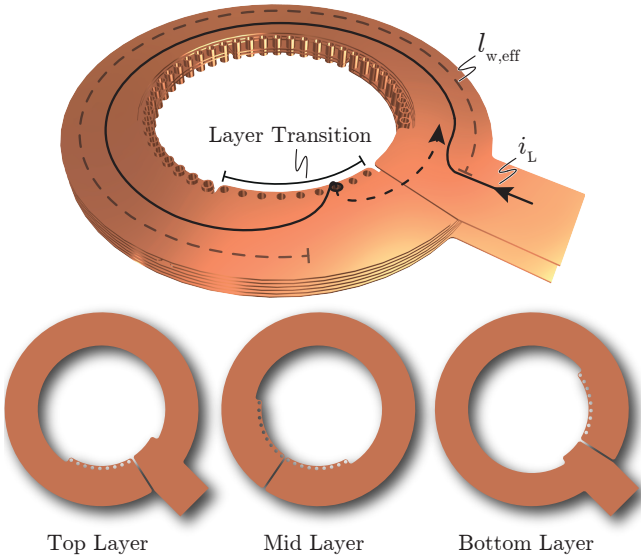

Fig. 6. Design of a multi-layer PCB winding with single turns on each layer and through-hole vias for the transitions between the layers and/or interconnections of the turns. Additionally, the shapes of the different copper layers are shown, where it needs to be mentioned, that all the inner layers (Mid Layer) look the same just rotated by a certain rotation angle, which is why it is shown only once.

turns per layer should be preferred whenever possible.

Finally, it is important to pay attention to the termination of the PCB winding, as otherwise, significant conduction losses might arise. As known from PCB-winding transformers, a vertically aligned arrangement, with two conductors on top of each other, is the most efficient way of carrying anti-parallel currents in PCBs. Consequently, the same arrangement should be used in the winding termination too, as the two currents in an inductor termination are heading into opposite directions as well (cf. **Fig. 7**). Hence, assuming a track width of e.g. $5\,\mathrm{mm}$ and a frequency of $500\,\mathrm{kHz}$, a vertically aligned termination Ⓥ saves $65\,\%$ of conduction losses compared to a lateral parallel termination Ⓗ. This reduction of losses originates from the fact, that two currents flowing into opposite directions physically attract each other, whereby in arrangement Ⓗ, most of the current is flowing at the inner edges of the terminals only and the respective effective copper cross-section is significantly reduced. In contrast, in arrangement Ⓥ, the mutual attracting force between the two terminal currents yields a slight current displacement in vertical direction only, whereby still an almost homogeneous current density in horizontal direction can be found, and the effective copper cross-section is not significantly reduced. For this reason, a vertical aligned termination should always be used if in any way possible (cf. **Fig. 6**).

So far, only the design of a multi-turn PCB winding has been discussed, but the influence of multiple layers on the quality of the CFFC has not yet been investigated. This is done in the next section.

A. Field Compensation in Multi-Layer PCB Windings

In the previous section, it has been shown that a reasonable power density of the component can often only be achieved by using multiple PCB layers for the inductor winding. However, this inherently results in non-homogeneous magnetic field distributions within the winding, as each layer is located at a different distance d_w from the air gap(s). Consequently, the proximity effect between the layers starts to play an important role, as it amplifies the inhomogeneities of the current densities within the PCB tracks. This is illustrated in **Fig. 8** based on a four-layer PCB example, where the first layer is located in a distance $d_\mathrm{w,opt}$ from the air gap. In the first graph, the simulated current densities of the four PCB tracks are shown, without taking into account the proximity effect among the tracks, i.e. the current distribution of each track is simulated independent from the others. Hence, they were simulated one after the other, whereby only the skin field and fringing field were considered. Thus, almost homogeneous current densities are achieved, as predicted by the analysis of the previous section. The effectiveness of the field compensation can also be quantified by the ratio between the total conduction losses in the four PCB tracks in the field-compensated arrangement (P_comp), thus, the arrangement shown in the figure, and the losses arising in the same PCB tracks operated as an air coil (P_air) without an air gap in the near vicinity of the conductors. However, if the proximity effect is considered, where the complete system is simulated simultaneously, the current densities of **Fig. 8b)** are found. There is still a certain compensating effect visible, but due to the proximity effect, most of the fringing field of the air gap is "shielded" by the top layer, whereby its compensating effect on the mid layers is reduced. Still, the conduction losses of this arrangement are $33\,\%$ lower than the losses of the same PCB winding without a core (operated as air coil), proofing the benefits of the proposed CFFC. Nevertheless, the effectiveness of the field compensation can further be enhanced by using two air gaps, one above and one below the PCB, as shown in **Fig. 8c)**. Splitting the air gap reduces the magnetically effective number of PCB layers by half, due to the symmetry of the arrangement around the horizontal axis. Thus, the proximity effect can significantly be reduced, which means, in terms of conduction losses, a reduction by almost $50\,\%$ compared to the air coil. It should be noted, that the optimal distance $d_\mathrm{w,opt}$ between the air gap and the top/bottom layer of the

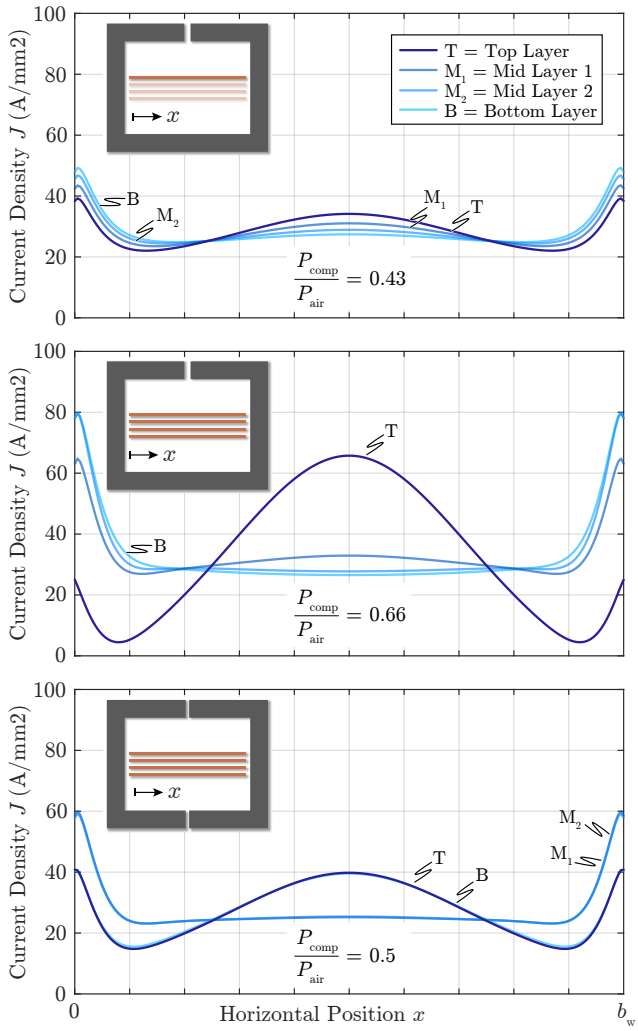

Fig. 8. Simulated current densities in a four-layer PCB for **a)** a single air gap and all layers simulated independently from each other, one at a time (neglecting the proximity effect), **b)** a single air gap and all layers simulated simultaneously (real situation) and **c)** a dual air gap arrangement with simultaneously simulated PCB layers. Additionally, the occurring conduction losses are always compared to the one arising in the PCB without a magnetic core (air coil).

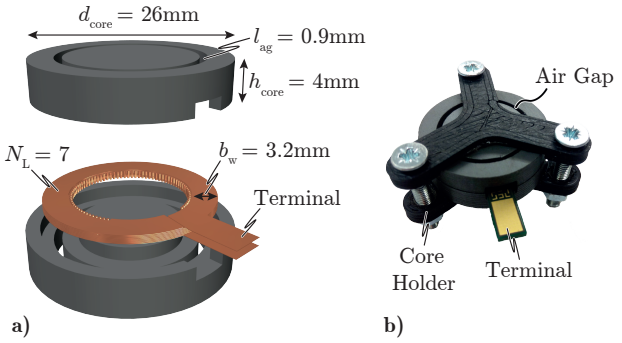

Fig. 9. a) 3D model of the practical implementation of a 6.8 µH multi-layer PCB-winding inductor using the proposed field compensation concept, by means of a ferrite core with two air gaps and **b)** picture of the assembled inductor with a 3D-printed core holder.

PCB winding does not change if the air gap is split into two air gaps above and below the PCB winding. This follows from the symmetry of the arrangement, as in a first approximation, the upper air gap can be considered to be responsible for the compensation of the upper half of the PCB layers and the lower air gap for the lower half of the PCB layers, respectively. Consequently, for PCB windings with more than one layer, the dual air gap arrangement should be used, where the optimal distance between the PCB and the air gaps can still be calculated according to (1). Hence, the top and the bottom layers should always be placed in the optimal distance $d_{w,opt}$ to the respective air gap, as can be proven by means of FEM simulations.

In the following section, the benefits of the proposed multi-layer PCB-winding arrangement are experimentally verified and finally compared to state-of-the-art solutions.

IV. Experimental Verification

In this section, the proposed PCB-winding inductor concept is experimentally verified by means of an inductor designed according to the specs given in **Tab. II**. The number of copper layers in the PCB is in this case given by the application with $N_{layer} = 8$, which is why the inductor is ideally designed with $N_L = 7$ turns, such that through-hole vias for the layer transitions and a coplanar termination can be used. However, the optimal number of turns depends on the required specifications and does not always match $N_{layer} - 1$, which would result in the best copper-utilization. For this reason, N_L should be chosen according to an η-ρ-optimization, which considers both, the winding losses as well as the core losses of the inductor and is based on well-known equations for calculating the different loss components [20]. This optimization is briefly explained in **Section VI**, which is why only the dimensions of the finally selected inductor design are given here. The optimal dimensions such as winding width b_w, air gap length l_{ag} and core cross-section A_C directly result from the aforementioned η-ρ-optimization and are summarized in **Fig. 9**.

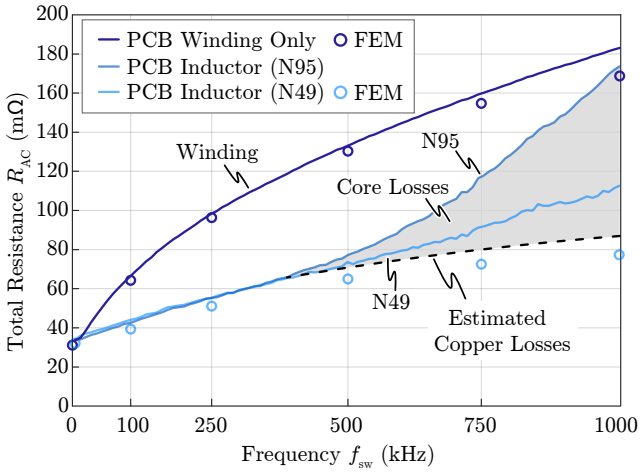

Fig. 10. Total winding resistance of the PCB winding only (air coil), the fully assembled inductor with a core made of N95, and the same inductor but with a core made of N49 ferrite material. All three measurements were taken using an impedance analyzer.

In order to verify the findings of the previous sections, the impedance of both, the PCB winding without a core (air coil), as well as the PCB winding with the proposed core arrangement were measured. The measurement results of the total winding resistance are shown in **Fig. 10**, whereby a good agreement between the FEM simulations and the measurements can be found. Two observations have to be noted: On the one hand, in the frequency range of interest (300 kHz...720 kHz), the effectiveness of the CFFC is clearly visible, as the winding resistance of the assembled PCB-winding inductor is reduced by almost 50 % compared to the air coil. The reduction of the winding resistance originates from the fact, that in contrast to the air coil, in the assembled inductor the fringing field around the air gap effectively counteracts the skin and proximity fields within the PCB winding. On the other hand, the influence of the core material on the overall inductor losses, especially for high frequencies, becomes noticable, i.e. already constitutes half of the total inductor loss at around 1 MHz for N95. Hence, the eddy-current losses (the hysteresis losses are negligible when measuring the impedance with an impedance analyzer) in the core made of N95 ferrite material are significantly higher then the ones arising in exactly the same core but made of N49 ferrite material. Consequently, the effect of an improperly chosen core material is directly visible in the AC-resistance measurement of an inductor, whereby a careful selection of an appropriate core material is key for high efficiency applications.

In order to consider the hysteresis losses in the ferrite core as well, the same components have been excited in a calorimeter with a sinusoidal current of 5 A_{pk} at a frequency of 500 kHz. In order to compare the proposed design concept to state-of-the-art solutions, an additional core arrangement has been measured, with exactly the same dimensions as shown in **Fig. 9**, but instead of two air gaps, i.e. one air gap on top and another air gap at the bottom of the winding, the air gaps are located in the same physical layer as the PCB winding (cf. **Fig. 11** Ⓒ). The results are shown in **Fig. 11**, where the ratio between winding and core losses are estimated based on the impedance measurements of **Fig. 10**, as in a calorimetric setup only the total losses of a device can be measured. The benefits of the proposed CFFC are obvious: even though the inductance

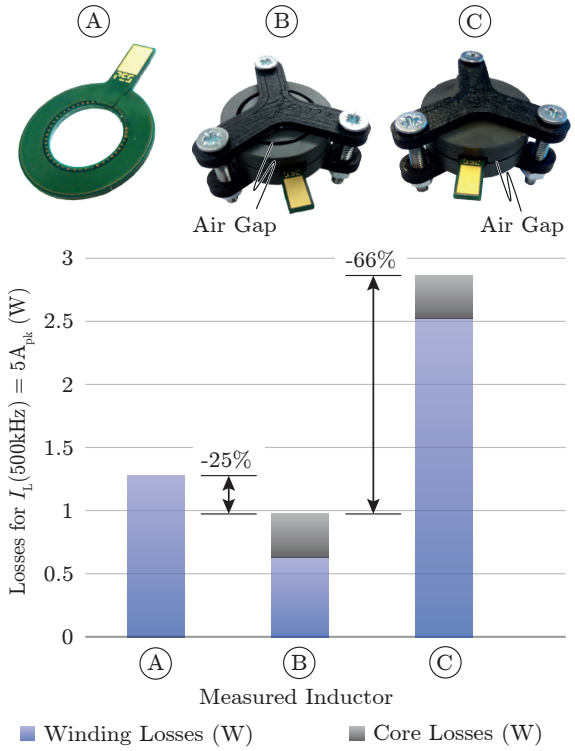

Fig. 11. Calorimetric loss measurements of Ⓐ the PCB winding only, with an inductance of 700 nH, Ⓑ the proposed PCB-winding inductor design (N49) with an inductance of 6.7 µH and Ⓒ the conventional design approach with the air gap in the same physical layer as the PCB (6.8 µH).

of the field compensated inductor Ⓑ is 10 times larger then the one of the air coil Ⓐ, the overall losses can be reduced by 25 %. Of course this ratio changes with current, as the winding losses scale quadratically with the current, while the core losses show an i_L^{β} dependency, where β denotes the according Steinmetz parameter [20] of the core material. Nevertheless, the ratio between the conventional inductor Ⓒ and the field compensated inductor Ⓑ does not change significantly with the current amplitude, whereby for the same inductance L, 66 % of the total losses can be saved by the proposed field compensation concept.

However, there is one major drawback of this concept compared to conventional inductor core arrangements: The air gap is directly given by the manufactured core and can hardly be changed afterwards (cf. **Fig. 9**). Thus, the only possible adjustment of the inductance in the given arrangement is the increase of the total air gap by separating the two core halves, whereby an additional small air gap in the same physical layer as the winding results. However, as previously mentioned, the fringing field around this air gap would increase the conduction losses of the winding, whereby it should be avoided at all costs. Fortunately, the air gaps in inductors employing the CFFC are usually large, whereby possible inaccuracies during the manufacturing of the cores do not affect the inductance significantly and the resulting inductance values are quite consistent.

In the proposed PCB-winding inductor of **Fig. 9**, the allowable RMS current is strongly limited due to the poor thermal

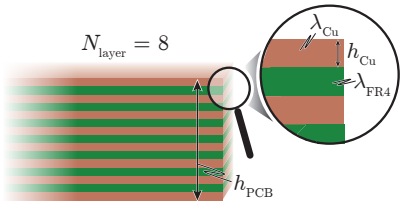

Fig. 12. Sketch of an eight-layer PCB with all the definitions used to introduce an effective thermal conductivity λ_{eff} of a PCB (cf. Eqs. (3-5)).

conductivity of the PCB, in combination with the terminal of the winding as the only possible thermal interface between the winding and the heat sink. Consequently, a thermally enhanced PCB winding inductor design is required, which will be introduced in the next section.

V. Thermally Enhanced Inductor Design

Even though the CFFC can significantly reduce the occurring conduction losses in a PCB-winding inductor, these losses can hardly be dissipated in the initially proposed PCB-winding design. In order to improve the thermal interface between the winding and the heat sink, the thermal model of the existing PCB winding needs to be derived first. For this reason, an equivalent thermal conductivity λ_{eff} of a PCB in horizontal direction is defined [21] according to

$$\lambda_{eff} = r_{PCB}\lambda_{Cu} + (1 - r_{PCB})\lambda_{FR4}, \tag{3}$$

with

$$r_{PCB} = \frac{A_{Cu}}{A_{FR4} + A_{Cu}} = \frac{N_{layer} \cdot h_{Cu}}{h_{PCB}}, \tag{4}$$

where λ_{Cu}, λ_{FR4}, h_{Cu} and h_{PCB} denote the thermal conductivity of copper, the thermal conductivity of FR4, the height of a copper layer and the total height of the PCB, respectively (cf. **Fig. 12**). Using this effective thermal conductivity, the thermal resistance R_{th} of a piece of PCB can be calculated according to

$$R_{th} = \frac{l_w}{\lambda_{eff} \cdot b_w \cdot h_{PCB}}, \tag{5}$$

where l_w denotes the length and b_w the width of the considered PCB part, as shown in **Fig. 13**. The same calculation method can now be used to estimate the temperature distribution in the PCB winding, based on the thermal model shown in **Fig. 14**. In order to simplify the calculations, a homogeneous loss density q_W within the winding is assumed, which is calculated according to

$$q_W = \frac{P_W}{2\pi}, \tag{6}$$

where P_W denotes the total arising conduction losses in the winding. It should be noted, that for simplicity reasons q_W and all further parameters are normalized with respect to 2π instead of $2\pi r_W$, as only the angular dependency of the temperature is of interest and a constant temperature in radial direction is assumed. Besides q_W, a constant thermal "per-length" resistance $r_{th,W}$ of the winding is defined, which is calculated according to

$$r_{th,W} = \frac{1}{2\pi}\left(\frac{2r_W\pi}{\lambda_{eff} \cdot b_W \cdot h_{PCB}}\right). \tag{7}$$

Furthermore, as shown in **Fig. 14**, an infinite number of heat sources and thermal resistances along the winding are assumed, which are finally connected to the ambient temperature T_A through a single additional thermal resistance $R_{\mathrm{th,T}}$, which represents three individual components: The thermal resistance of the terminal of the winding, the thermal resistance of the thermal interface material between the winding terminals and the heat sink, and finally, the thermal resistance from the heat sink to the ambient. The employed thermal interface material (TIM) between the winding terminals and the heat sink provides a tight thermal connection and at the same time ensures the required isolation between them, as otherwise the heat sink would short circuit the winding.

As the total generated power loss has to flow through $R_{\mathrm{th,T}}$, this thermal resistance needs to be particularly small, as otherwise a significant temperature drop across $R_{\mathrm{th,T}}$ would be induced.

Based on the aforementioned quantities and the thermal model of **Fig. 14**, the angle-dependent PCB temperature T_W can be calculated, according to

$$T_\mathrm{W}(\varphi) = T_\mathrm{A} + R_{\mathrm{th,T}} \cdot P_\mathrm{W} + \int_0^\varphi q_\mathrm{W} r_{\mathrm{th,W}}(\pi - \varphi)\mathrm{d}\varphi. \quad (8)$$

Hence, the following temperature profile can be found

$$T_\mathrm{W}(\varphi) = T_\mathrm{A} + R_{\mathrm{th,T}} \cdot P_\mathrm{W} + q_\mathrm{W} r_{\mathrm{th,W}} \cdot \varphi \left(\pi - \frac{\varphi}{2}\right). \quad (9)$$

As an example, **Fig. 15** shows the temperature profile within the PCB winding of **Fig. 9** and **Fig. 14** for 6 W of conduction losses and an ideal heat sink with a temperature of 25 °C connected to the winding terminal. As shown in the figure, the calculated temperatures are in good agreement with the FEM-simulated temperatures, even though the calculation is based on various simplifications.

The thermal bottlenecks of the initial PCB-winding design can now be identified with (9) and **Fig. 15**: One the one hand, there is a large temperature drop across the winding terminals (55 °C), as the total losses have to flow through a narrow piece

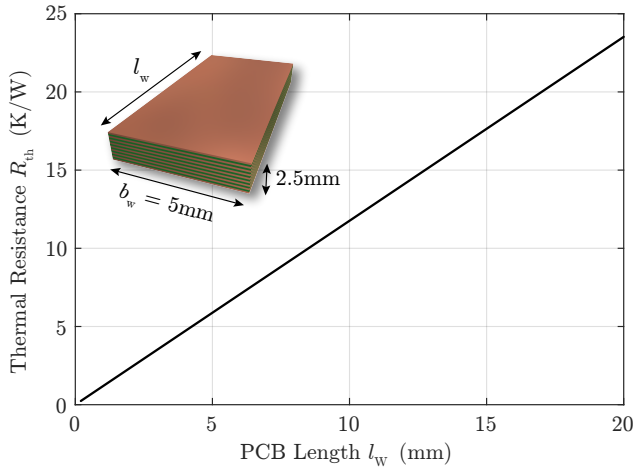

Fig. 13. Thermal resistance of a piece of an eight-layer 70 µm PCB with a width of 5 mm, a height of 2.5 mm and a variable length l_w.

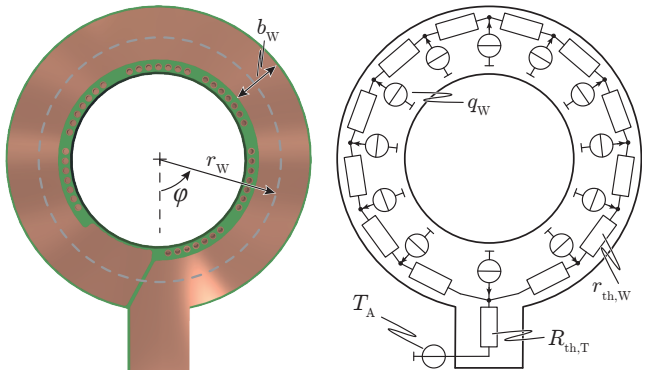

Fig. 14. Thermal model of the initially proposed multi-layer PCB-winding design.

of PCB with a comparably large thermal resistance, according to

$$T_\mathrm{W}(\varphi = 0) = T_\mathrm{A} + R_{\mathrm{th,T}} \cdot P_\mathrm{W} \quad (10)$$

(cf. $l_\mathrm{w} = 8$ mm in **Fig. 13**). On the other hand, the temperature gradient is increasing for smaller φ, as there is more and more heat flux accumulated along the winding, which needs to flow through $r_{\mathrm{th,W}}$ towards the terminals. Therefore, in order to thermally improve the design, more thermal interfaces should be used, whereby the total heat flux is distributed among multiple thermal terminals and at the same time the mean length of the thermal path for the heat flux from its origin to the heat sink is reduced. Such a thermally enhanced design is shown in **Fig. 16**, where three additional thermal interfaces are used. These additional thermal interfaces do not carry any current, as they are fully isolated from the aluminum heat sink by means of a thermal interface material, but they provide a thermally conductive path from the actual PCB winding to the aluminum heat sink. Consequently, only one quarter of the total heat flux flows through each terminal and the mean length of the thermal path is reduced by a factor of four as well.

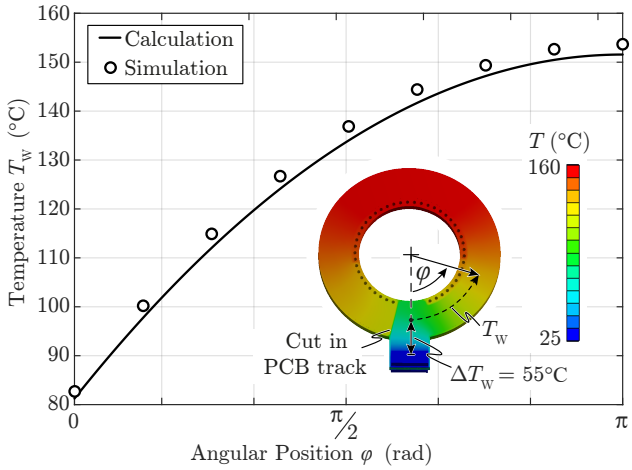

Fig. 15. Temperature profile for the PCB winding shown in **Fig. 9** and **Fig. 14** for 6 W of total losses. Additionally, the corresponding FEM simulation is shown.

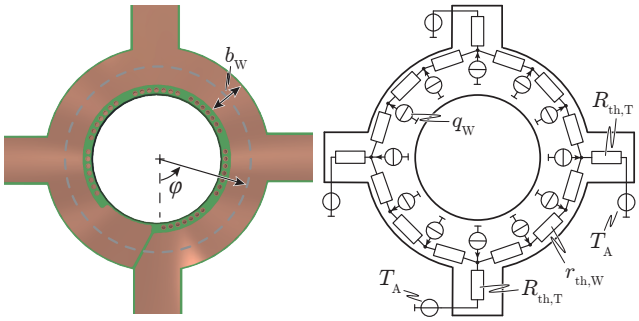

Fig. 16. Thermal model of a thermally enhanced multi-layer PCB winding with four thermal interfaces.

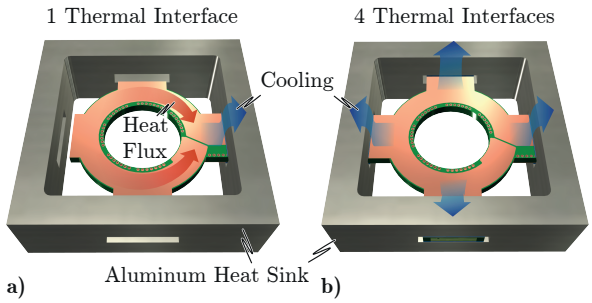

Fig. 18. Experimental test setups of **a)** a PCB winding with only a one thermal interface at the electric winding terminals, and **b)** the same winding but with four thermal interfaces.

Similar to (9), the following angle-dependent PCB temperature T_W can be derived for the thermally enhanced winding design:

$$T_W(\varphi) = T_A + R_{th,T} \cdot \frac{P_W}{4} + \frac{q_W r_{th,W}}{4} \cdot \varphi\,(\pi - 2\varphi)\,, \quad (11)$$

which is valid for $\varphi \in (0, \frac{\pi}{2})$ and is periodically repeating (cf. **Fig. 17**). The calculated temperature profile is again in good agreement with the FEM simulations. However, due to the necessary cuts in the copper layers, there are always some hot spots in the winding, which need to be considered when designing a PCB winding close to the thermal limit. For most applications, however, it is sufficient to add a safety margin of $\approx 10\,°C$ to the maximum calculated PCB temperature.

The comparison of the temperature profiles (9) and (11) reveals the benefits of additional thermal interfaces on the temperature distribution within the winding, as the temperature drop across $R_{th,T}$ is approximately reduced to one fourth, or more generally, to $\frac{1}{N_T}$ of the initial value, where N_T denotes the number of thermal terminals. Furthermore, the maximum temperature difference within the winding is even reduced to $\frac{1}{N_T^2}$ of the initial value (which can be explained considering the lower thermal resistance besides the lower heat flux), allowing for much higher loss densities and therefore much higher RMS currents in the winding. Consequently, the number of required thermal interfaces for a certain given maximum PCB temperature can be calculated based on

$$T_{W,max} = T_A + R_{th,T} \cdot \frac{P_W}{N_T} + \frac{q_W r_{th,W} \pi^2}{2 N_T^2}. \quad (12)$$

In addition to the enhanced thermal properties of the winding, multiple thermal interfaces improve the mechanical stability of the inductor as well, whereby a high vibration resistance is achieved, which is especially important in automotive applications.

In order to experimentally verify the derived thermal model, PCB windings with the same dimensions as given in **Fig. 9**, but with either one or four thermal interfaces were designed and tested. The corresponding test setups are shown in **Fig. 18**, where the winding arrangement without enhanced cooling is thermally connected to the quadratic aluminum heat sink only at the electric winding terminals (cf. **Fig. 18a)**), while the thermally improved winding configuration is connected to the heat sink via four thermal interfaces (cf. **Fig. 18b)**),

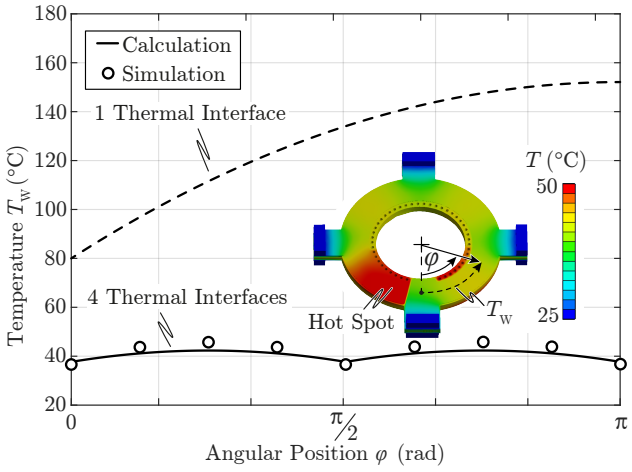

Fig. 17. Temperature profile of the thermally enhanced PCB winding (4 thermal interfaces) for 6 W of total losses. Additionally, the corresponding FEM simulation is shown.

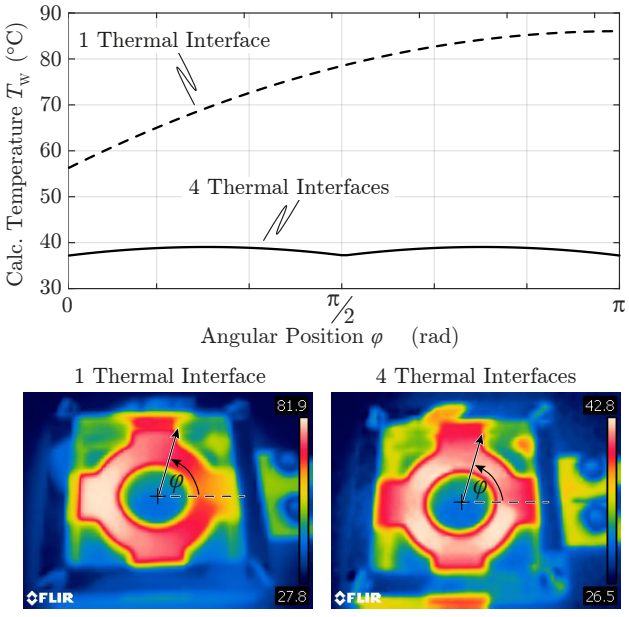

Fig. 19. Calculated thermal profiles of the inductors shown in **Fig. 18**, for total winding losses of 3.5 W. Additionally, the corresponding thermal images of the measured inductors are shown for the same amount of losses.

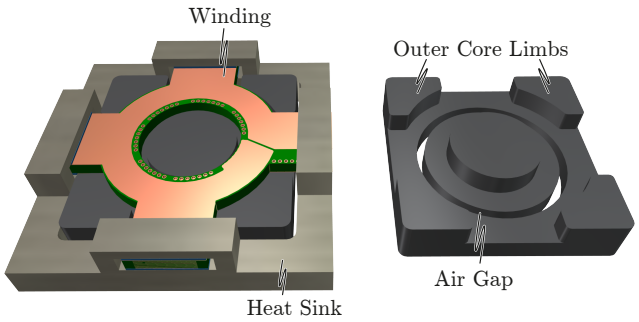

Fig. 20. 3D model of the adapted ferrite core shape for a winding with four thermal interfaces.

as indicated by the blue arrows. The quadratic aluminum heat sink is then screwed to a water-cooled aluminum base plate, as in a real EV application. In **Fig. 19**, the calculated and the measured PCB temperatures are shown for 3.5 W of conduction losses induced by a sinusoidal current of 500 kHz from a power amplifier. Based on the thermal images (aquired using an infrared camera FLIR), a high accuracy of both, the predicted peak temperatures (based on (11), peak temperatures of 86 °C and 39 °C are expected) as well as the measured temperature profiles can be observed. The slightly lower measured temperatures originate from the additional natural convection of the PCB windings, which is neglected in the proposed thermal model. However, as soon as the ferrite core is placed around the PCB winding, the contribution to the cooling due to natural convection will almost vanish. Consequently, the proposed simple thermal model can efficiently be used to optimize the thermal design of PCB winding inductors.

However, due to the additional lateral thermal interfaces of the winding, the shape of the ferrite core needs to be adapted as well. In order to compensate for the reduced core cross-section of the outer limb (due to the cut-outs around the thermal interfaces), the total core dimensions need to be slightly increased, such that the saturation flux density of the ferrite material is not exceeded. For power density reasons, this is ideally done by changing the outer shape of the core to a square, according to **Fig. 20**. In this way, the boxed volume of the inductor is not significantly increased, but rather more efficiently used. Hence, almost homogeneous magnetic flux densities within the inner and outer limbs are again achieved. Even though the return path for the magnetic flux in the outer limbs is not concentric anymore, the fringing field around the air gap does not change, as the uniform circular air gap inherently yields a radially symmetric field distribution. Consequently, the field compensation within the winding is not affected by the shape of the outer limbs.

So far, only the winding has been considered for the thermal model of the inductor. However, there are of course also core losses generated during operation, which need to be dissipated as well. In contrast to conventional inductors, the cores of the proposed inductor design concept cannot be directly attached to an aluminum heat sink, as the fringing field around the air gap would induce substantial eddy current losses in the aluminum of the heat sink. For this reason, a free space between the top and/or the bottom surface of the inductor cores and any conductive material around the inductor should be left. Consequently, there are only two possible ways to dissipate the arising core losses: On the one hand, natural or forced convection can be used, which, however, limits the allowable core losses due to a comparably low power dissipation capability. On other hand, thermally conductive epoxy resin can be used for potting the complete inductor, whereby the core pieces are thermally attached to the PCB winding and the core losses can therefore be dissipated through the thermal interfaces of the winding. Consequently, the thermal interfaces would need to be enlarged in order to dissipate both, the winding as well as the core losses of the inductor. However, due to the complexity of this arrangement, the thermal model would be far more complicated and is therefore usually directly solved by means of FEM. For this reason, it is not discussed any further in this paper.

In the following section, the electromagnetic and thermal design process of the inductor is shortly summarized and explained considering the series-resonant inductor for the application mentioned in the beginning of this paper.

VI. Design Guidelines

In this section, the simplified design process of a PCB-winding inductor is explained, based on the specifications given in **Tab. II**. As mentioned earlier, the PCB of the application has eight copper layers with a height of 70 µm each. Consequently, from a copper utilization point of view, the ideal number of turns would be $N_\mathrm{L} = 7$, as explained in **Section III**. However, depending on the application, it might be better to increase or decrease the number of turns N_L, in order to find the most appropriate inductor design, even though the copper utilization would be slightly worse. For this reason, N_L is varied during the optimization of the inductor, in order to explore the widest possible design space and find the best suited inductor design. In the following, a number of turns of $N_\mathrm{L} = 7$ is assumed (which in this specific case is also the optimum) in order to give the reader a certain impression on the geometrical dimensions, which can be expected for inductors employing the CFFC.

Thus, based on N_L, the minimum core cross-section $A_\mathrm{C,min}$ can be calculated, which is used in order to avoid saturation of the ferrite core:

$$A_\mathrm{C,min} = \frac{L \cdot I_\mathrm{pk}}{N_\mathrm{L} \cdot B_\mathrm{sat}} = \frac{6.8\,\mu\mathrm{H} \cdot 25.2\,\mathrm{A}}{7 \cdot 0.35\,\mathrm{T}} = 70\,\mathrm{mm}^2. \quad (13)$$

Hence, the minimum radius of the inner core limb is

$$r_\mathrm{C,min} = \sqrt{\frac{A_\mathrm{C,min}}{\pi}} = 4.7\,\mathrm{mm}. \quad (14)$$

This value is of course only a lower limit and in most cases not the optimal choice regarding losses. Thus, this value is iteratively increased during the design process in order to find the optimal dimension.

Based on the core radius r_C, the mean winding length l_W for a certain winding width b_W can be calculated according to

$$l_\mathrm{W} = N_\mathrm{L} \cdot 2\pi \cdot \left(r_\mathrm{C} + d_\mathrm{via} + \frac{b_\mathrm{W}}{2} \right), \quad (15)$$

where d_{via} denotes the additional required radius due to the clearance between the core and the PCB winding as well as the width of the vias of the layer transitions. As a first guess, a value of $d_{\mathrm{via}} = 1\,\mathrm{mm}$ can be used for applications with voltages $\leq 500\,\mathrm{V}$ within the winding. Consequently, the simplified DC-resistance R_{DC} of the winding is calculated according to

$$R_{\mathrm{DC}} = \frac{l_{\mathrm{W}}}{\sigma_{\mathrm{Cu}} \cdot b_{\mathrm{W}} \cdot h_{\mathrm{Cu}}}, \tag{16}$$

where σ_{Cu} denotes the electrical conductivity of copper. In order to estimate the effectively occurring conduction losses in the winding, the AC to DC resistance ratio needs to be known. Even though this is ideally calculated by means of FEM simulations of the total inductor, a very good estimate can be found in **Fig. 21**, where the FEM-simulated AC to DC resistance ratios for 4, 6 and 8 layer PCB pieces are shown. These ratios are independent of the actual winding width b_{W}, and are valid if the air gaps are placed above and beneath the winding according to (1).

The core losses of the inductor, however, are derived based on the inductor current waveforms and the core dimensions, which are calculated such that the same flux density in the inner and outer core limbs is achieved (cf. **Fig. 22**). Hence, based on the estimated conduction losses in the PCB winding and a certain number of thermal interfaces N_{T}, the minimum width of the thermal interfaces b_{th} can be calculated, which keeps the peak temperature within the winding below the maximum allowed PCB temperature (cf. Eqn. (12)). Using this value, the side length of the core l_{C} can be calculated according to the simplified equation

$$l_{\mathrm{C}} = b_{\mathrm{th}} + \sqrt{\pi r_{\mathrm{C}}^2 + 2r_{\mathrm{out}}^2 - b_{\mathrm{th}}\sqrt{4r_{\mathrm{out}}^2 - b_{\mathrm{th}}^2}}, \tag{17}$$

or using the exact solution given in Appendix A, which results in the same peak flux density in the inner and outer core limbs. Based on these core dimensions, the iGSE is finally applied to estimate the occurring core losses according to [20].

Hence, in order to find the most appropriate solution for a certain application, the two parameters r_{C} and b_{W} are varied and the corresponding core and conduction losses are calculated. This results in a performance Pareto plot, where the total losses and the characteristic length l_{C} of the core of the different designs are illustrated (cf. **Fig. 23**).

For the application at hand, the most power dense inductor should be chosen, which does not exceed the maximum allowable losses of $P_{\mathrm{W}} = 23\,\mathrm{W}$ for a maximum inductor current of $I_{\mathrm{L,RMS}} = 17.9\,\mathrm{A_{RMS}}$. The value for P_{W} originates from an overall optimization of the converter system with respect to power density and a targeted full-load efficiency of $\eta = 95\,\%$. The corresponding optimal inductor dimensions and the assembled component are shown in **Fig. 24**. It should be noted, that even though the two connectors of the inductor prototype are horizontally aligned, the terminals of the induc-

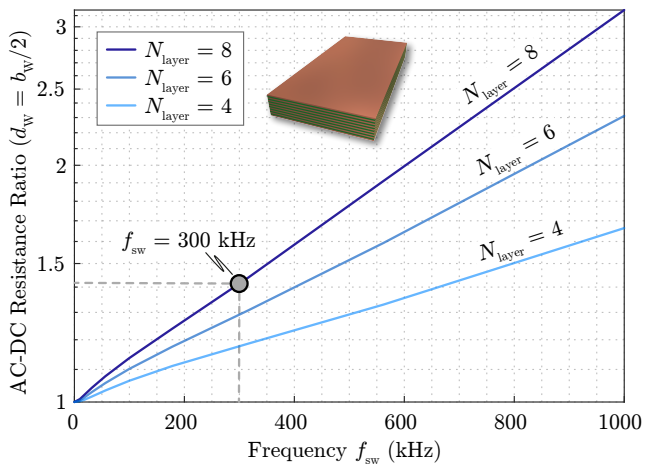

Fig. 21. AC to DC resistance ratios of inductor windings implemented in 4, 6 and 8 layer PCBs for an air gap placement according to (1).

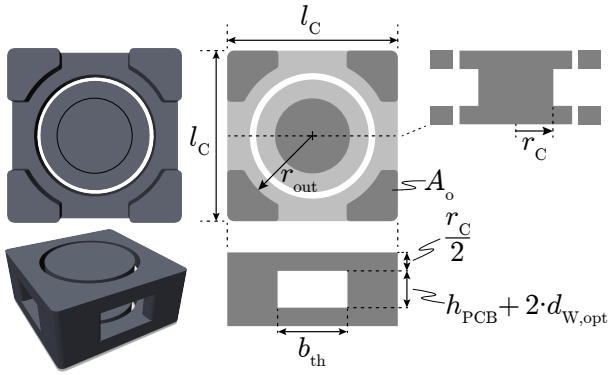

Fig. 22. Minimum core dimensions which are required to avoid saturation of the core material along the complete magnetic path.

TABLE III. Specifications and Parameters of the PCB Winding Inductor shown in **Fig. 24**.

Water Cooling	T_{A}	80 °C
Thermal Interface Resistance	$R_{\mathrm{th,T}}$	$9.5\,\mathrm{K\,W^{-1}}$
Thermal Resistance of Winding	$r_{\mathrm{th,W}}$	$10.6\,\mathrm{K\,W^{-1}}$
Max. PCB Temperature	$T_{\mathrm{W,max}}$	150 °C

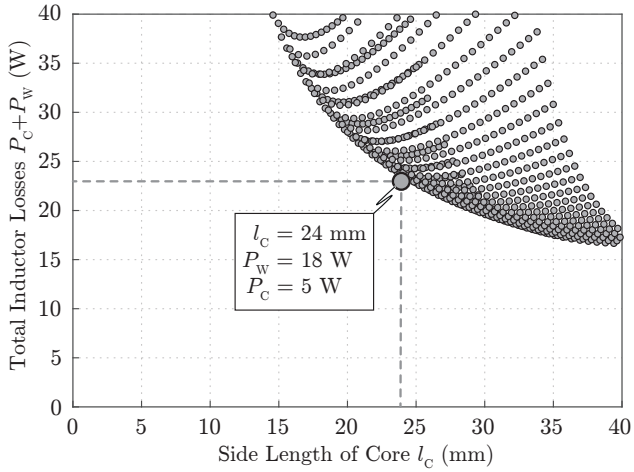

Fig. 23. Pareto optimization of a PCB-winding inductor according to the specifications given in **Tab. II**. Additionally, the chosen design is shown with its loss composition and the side length of the ferrite core.

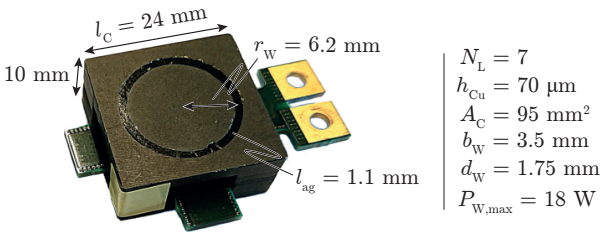

Fig. 24. Practically implemented 6.8 µH PCB-winding inductor with a CNC-milled ferrite core made out of N49 material.

tor are still vertically aligned along most of the terminal (the transition between the vertically and the horizontally aligned termination was only necessary to facilitate the connection of the inductor to the impedance analyzer and would not be required in a real application).

Based on these inductor dimensions, a 3D model of the inductor has been created and the frequency-dependent resistance of the winding has been simulated by means of Ansys Maxwell (cf. **Fig. 25**). The current density distribution of the first PCB layer clearly reveals the impact of the air gap on the inductor current, as the attracting force of the fringing field on the current yields a current crowding along the air gap, which counteracts the natural tendency of the current to flow at the outer edges of the PCB winding. Based on the simulation results, an AC to DC resistance ratio of ≈1.42 at $f_{sw} = 300\,\text{kHz}$ can be expected.

In order to quantify the cooling performances of different numbers of thermal interfaces, the peak temperatures $T_{W,max}$ for $N_T = 2, ..., 4$ in the core design of **Fig. 24** have been calculated. Hence for total conduction losses of $P_{W,max} = 18\,\text{W}$ and the specifications and parameters of **Tab. III**, the following peak temperatures can be found according to (12):

$$T_{W,max}(N_T = 2) = 202\,°\text{C}$$
$$T_{W,max}(N_T = 3) = 154\,°\text{C}$$
$$T_{W,max}(N_T = 4) = 132\,°\text{C}.$$

Hence, all four thermal interfaces are required in order to be able to keep the worst case inductor temperature below the thermal limit of 150 °C.

In order to verify the calculated peak temperature of the winding, the inductor has been mounted on an aluminum base plate with a temperature of $T_A = 25\,°\text{C}$. The winding was excited by an equivalent DC current of 22.5 A (considering the HF losses as well), resulting in the worst case conduction losses of 18 W. The maximum measured temperature of the winding was $T_{W,max} = 80.1\,°\text{C}$, which yields a temperature difference from the hot spot to the heat sink of $\Delta T(18\,\text{W}) = 55.1\,°\text{C}$. Hence, assuming a maximum heat sink temperature of $T_A = 80\,°\text{C}$ (cf. **Tab. III**), the hot spot temperature within the winding would be $T_{W,max} = 135.1\,°\text{C}$ in the final system, which is in good agreement with the estimated maximum temperature.

Based on this measurement, the maximum allowable AC to DC resistance ratio can be calculated

$$\frac{R_{AC}}{R_{DC}} \propto \frac{I^2_{RMS,DC}(P_W = 18W)}{I^2_{RMS,AC}(P_W = 18W)} = \frac{22.5^2}{17.9^2} = 1.58. \qquad (18)$$

Using an impedance analyzer, the actual AC to DC resistance ratio of the PCB winding can be measured, while for 300 kHz where the maximum RMS currents will occur, an AC to DC resistance ratio of 1.49 has been found, which yields a safety margin of 6 % before the maximum calculated PCB temperature is reached. As the inductor current for higher switching frequencies is significantly lower, only the AC to DC resistance ratio at 300 kHz needs to be considered here. However, in other applications, the losses over the full switching frequency range should be calculated, in order to find the absolute worst case inductor losses. If the measured AC to DC resistance ratio should be higher than the one found in (18), a larger number of air gaps could be used in order to improve the magnetic field compensation and therefore reducing the AC to DC resistance ratio of the winding. Alternatively, more and/or wider thermal interfaces could be used in order to decrease the thermal resistance of the PCB winding.

Consequently, these measurements show the applicability and feasibility of the proposed PCB winding inductor concept.

However, in practical implementations of this concept, some mechanical challenges are arising, especially if the inductors are employed in a harsh operating environment, as e.g. in automotive applications, where sensitivity to vibration is a serious issue. Thus, even though the manufacturing of large quantities of the different core parts is not very difficult, as the same forming and sintering processes as for conventional ferrite cores can be applied, it is essential to end up with a stable assembly of the total inductor by fixing the individual parts of the core sturdily. This can be achieved by potting the core using a thermally conductive epoxy resin, which then guarantees a stable mechanical connection among the individual core parts, as well as between the core and the PCB winding. Alternatively, a plastic core holder as shown in **Fig. 26** can be used, which is glued to the individual ferrite pieces and ensures both, a homogeneous air gap length along the circular air gaps, as well as the optimal distance between the winding and the air gap. The two resulting core halves can then be treated as conventional E or EQ cores and can be

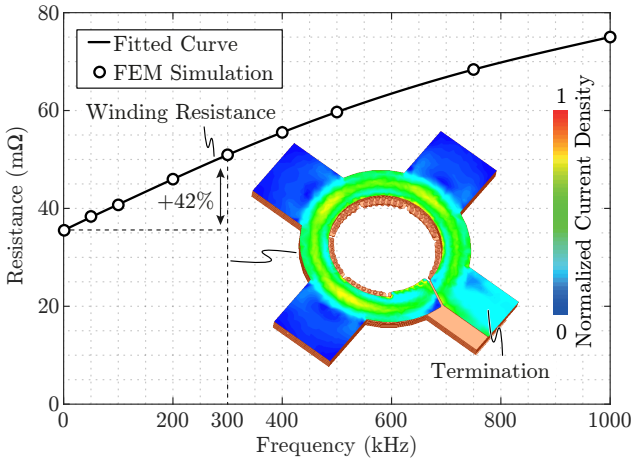

Fig. 25. FEM-simulated winding resistance of the PCB-winding inductor shown in **Fig. 24** and the corresponding normalized current density distribution at 300 kHz.

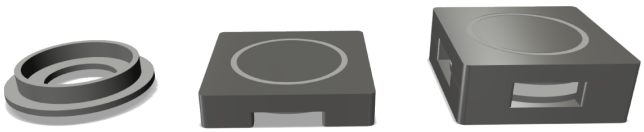

Fig. 26. Plastic core holder which is used to fix the individual core pieces.

attached to the PCB by means of clamps.

Another issue, which needs to be addressed in a practical application, is the isolation between the winding and the inductor core. Even though the required clearance between the edges of the PCB and the most outer PCB track (which is given by the PCB manufacturer ($\approx 200\,\mu\mathrm{m}$)) is usually sufficient to guarantee full galvanic isolation between the core and the winding, a more elaborate isolation method might be required in high voltage applications. In order to ensure a certain required isolation, Kapton tape can be wrapped around the inner and the outer core limbs to separate the PCB from the ferrite core, or, more production-friendly, the complete core could simply be coated. Thus, the proposed inductor design concept can even be used in high voltage applications.

VII. Conclusion

In this paper, a novel design strategy for PCB winding inductors has been proposed, which utilizes the fringing field around a single air gap or multiple air gaps to compensate the parasitic skin and proximity fields within the winding and accordingly is denominated as compensating fringing field concept (CFFC). Consequently, compared to state-of-the-art PCB-winding inductors, significantly lower AC conduction losses can be achieved, as has been shown by means of various experimental measurements.

The proposed loss model of the PCB winding allows for an accurate prediction of the occurring conduction losses and therefore can directly be used in simple design optimization algorithms. Furthermore, an accurate thermal model of the PCB winding has been introduced, which allows to accurately estimate the temperatures within the PCB winding for a given amount of conduction losses. It has been shown, that a utilization of multiple thermal interfaces allows for operating the inductor with very high current densities, whereby highly power-dense inductor designs can be achieved. However, even though the proposed field compensation concept results in low AC to DC resistance ratios and therefore a good copper utilization even for very high frequencies, the limited available copper in a PCB impedes the design of PCB winding inductors which are highly efficient and power-dense at the same time. Hence, compared to solid wire inductors, the winding filling factor of inductors with a PCB winding will always be lower and thus the efficiency often as well. Nevertheless, as proven in this paper by multiple experimental hardware prototypes, the extremely high allowable current densities in PCB windings outweigh the lower winding filling factor, whereby highly power-dense and cost-effective inductors can be built.

Appendix A
Derivation of the Design Equations for the Inductor Core

Based on the required magnetic core cross-section A_C of the inductor, the radius r_C of the center leg of the ferrite core can directly be calculated according to

$$r_\mathrm{C} = \sqrt{\frac{A_\mathrm{C}}{\pi}}. \tag{19}$$

If the flux density in the outer core limbs should be the same as in the center leg, the total core cross-section of the outer core limbs needs to be equal to A_C. Thus, each outer core limb needs a minimum cross-section A_o of

$$A_\mathrm{o} = \frac{A_\mathrm{C}}{4} = \frac{r_\mathrm{C}^2\pi}{4}. \tag{20}$$

However, the area A_o depends on various design parameters as e.g. the outer core radius r_out, the width of the thermal interfaces b_th as well as the total side length l_C of the core (cf. **Fig. 22**). The width b_th can easily be calculated based on the thermal model of the winding and the maximum allowable thermal resistance of one thermal interface $R_\mathrm{th,T}$ (cf. (5)) according to

$$b_\mathrm{th} = \frac{l_\mathrm{w}}{\lambda_\mathrm{eff} \cdot h_\mathrm{PCB} \cdot R_\mathrm{th,T}}. \tag{21}$$

Furthermore, the outer radius r_out is given as

$$r_\mathrm{out} = r_\mathrm{C} + 2d_\mathrm{clr} + b_\mathrm{w}, \tag{22}$$

where $d_\mathrm{clr} \approx 1\,\mathrm{mm}$ denotes the required clearance between the ferrite core and the PCB winding. As the area of one outer core limb A_o is defined as

$$A_\mathrm{o} = l_\mathrm{C}^2 - r_\mathrm{out}^2\pi + b_\mathrm{th}k - 2l_\mathrm{C}b_\mathrm{th} + 4r_\mathrm{out}\tan^{-1}\left(\frac{b_\mathrm{th}}{k}\right), \tag{23}$$

with

$$k = \sqrt{4r_\mathrm{out} - b_\mathrm{th}^2}, \tag{24}$$

the total width l_C of the inductor core can be calculated according to

$$l_\mathrm{C} = b_\mathrm{th} + \sqrt{b_\mathrm{th}^2 + A_\mathrm{o} + r_\mathrm{out}^2\pi - b_\mathrm{th}k - 4r_\mathrm{out}\tan^{-1}\left(\frac{b_\mathrm{th}}{k}\right)}. \tag{25}$$

Hence, all required geometrical dimensions have been found and the core can be designed accordingly.

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Jannik Schäfer (SM'16) received the B.Sc. and M.Sc. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2014 and 2016, respectively. In June 2016, he joined the Power Electronic Systems Laboratory (PES) of ETH Zurich as a Ph.D. candidate. In his research, he is currently focusing on highly compact combined electric vehicle chargers, with a special emphasis on PCB-integrated magnetic components.

Dominik Bortis (M'08) received the M.Sc. and Ph.D. degree in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Switzerland, in 2005 and 2008, respectively. In May 2005, he joined the Power Electronic Systems Laboratory (PES), ETH Zurich, as a Ph.D. student. From 2008 to 2011, he has been a Postdoctoral Fellow and from 2011 to 2016 a Research Associate with PES, co-supervising Ph.D. students and leading industry research projects. Since January 2016 Dr. Bortis is heading the research group Advanced Mechatronic Systems at PES, which concentrates on ultra-high speed motors, magnetic bearings and bearingless drives, new linear-rotary actuator and machine concepts with integrated power electronics. In this context, multi-objective optimizations concerning weight/volume/efficiency/costs, the analysis of interactions of power electronics and electric machines, and EMI are given special attention. Targeted applications include advanced industry automation and manufacturing, e.g. highly dynamic and precise positioning systems, medical and pharmaceutical systems, e.g. ultra-high purity and blood pumps, and future mobility concepts, including motors and actuators for hybrid and electric vehicles, more electric aircraft and satellites. Dr. Bortis has published more than 90 scientific papers in international journals and conference proceedings. He has filed 32 patents and has received 6 IEEE Conference Prize Paper Awards.

Johann W. Kolar (F'10) received the M.Sc. and Ph.D. degree (summa cum laude / promotio sub auspiciis praesidentis rei publicae) from the University of Technology Vienna, Austria, in 1997 and 1999, respectively. Since 1984, he has been working as an independent researcher and international consultant in close collaboration with the University of Technology Vienna, in the fields of power electronics, industrial electronics and high performance drive systems. He has proposed numerous novel PWM converter topologies, modulation and control concepts and has supervised 70+ Ph.D. students. He has published 880+ scientific papers in international journals and conference proceedings, 4 book chapters, and has filed 190+ patents. The focus of his current research is on ultra-compact and ultra-efficient SiC and GaN converter systems, wireless power transfer, solid-state transformers, power supplies on chip, and ultra-high speed and bearingless motors. Dr. Kolar has received 28 IEEE Transactions and Conference Prize Paper Awards, the 2014 IEEE Middlebrook Award, the 2016 IEEE William E. Newell Power Electronics Award, the 2016 IEEE PEMC Council Award and two ETH Zurich Golden Owl Awards for excellence in teaching. He initiated and/or is the founder of four ETH Spin-off companies. He is a member of the steering committees of several leading international conferences in the field and has served from 2001 through 2013 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.