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Comparative Evaluation of Harmonic Injection Techniques for a Phase-Modular Three-Phase Six-Switch Buck-Boost Y-Inverter

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***Abstract*—Phase-modular buck-boost dc/ac inverters extend the voltage conversion range of conventional buck-type inverter topologies, and accordingly offer significant advantages for variable-speed motor drives powered from dc sources with wide-voltage-ranges like fuel cells or batteries. In this Letter, two new modulation schemes are applied to the Six-Switch Buck-Boost Y-Inverter (6YI) topology, with an analysis of the efficiency improvement for the proposed Third Harmonic Injection PWM (TPWM) and Discontinuous PWM (DPWM) schemes relative to conventional Sinusoidal Pulse Width Modulation (SPWM). TPWM substantially reduces conduction losses and DPWM extends this gain by eliminating high-frequency switching for 1/3 of the fundamental period. These gains are validated on a $1\,\mathrm{kW}$ hardware demonstrator across a dc input voltage from $80\,\mathrm{V}$ to $240\,\mathrm{V}$, with DPWM reducing total converter losses by $31\,\%$ over SPWM for a peak efficiency at nominal load of $95.6\,\%$ with a power density of $62.3\,\mathrm{W/in^3}$.**

***Index Terms*—Three-Phase Buck-Boost Inverter, Y-Inverter, Wide Input and Output Voltage Range, Harmonic Injection**

I. Introduction

The power supply of electric motors from batteries, Fuel Cells (FCs) or renewable sources introduces the requirement of a wide-dc-voltage range during normal operation - for example, the dc output voltage of an FC to drive an electric motor is dependent on the power and may vary by 3x or more across a normal drive cycle [1]. Similarly, the output of a solar cell in a standalone field application under maximum power point tracking will vary substantially across luminescence [2]. Accordingly, the three-phase dc/ac converters needed for these application areas, must provide both buck and boost capabilities simultaneously.

Phase-modular three-phase buck-boost dc/ac converters have, accordingly, gained interest in these critical applications [1]–[5]. With the buck-boost capability in a single stage, the need for an additional buck or boost dc/dc converter is obviated, and the phase-modular approach realizes a simple control approach (and the potential for fault tolerance in certain applications). The Twelve-Switch Buck-Boost Y-Inverter (12YI) topology [1] utilizes four switches per phase with dedicated buck- and boost-half-bridges, and was shown to reach a peak efficiency of $98.3\,\%$ with a power density of $108\,\mathrm{W/in^3}$ for a wide-dc-input-voltage application [6]. The disadvantage of a total of 12 switches, however, is clear and a two-switch realization of the buck-boost converter modules, the Six-Switch Buck-Boost Y-Inverter (6YI) [3]–[5] is an alternative with lower component count and therefore much lower complexity. The main power circuit of the 6YI is shown in **Fig. 1** (module a is highlighted in light gray) for an FC-powered motor drive.

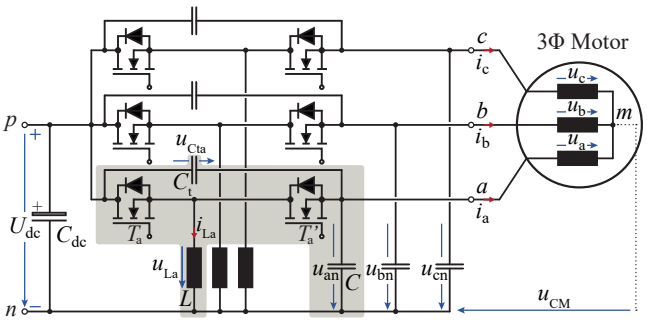

Fig. 1. Six-Switch Buck-Boost Y-Inverter (6YI) to power an electrified auxiliary system (e.g. a pump, fan, or compressor) from a battery or Fuel Cell (FC) power source. Wide dc-input-voltage ranges are a characteristic of these batteries and FCs employed in electric transportation, requiring buck-boost three-phase power conversion. The 6YI topology results in strictly-negative output capacitor voltages and sinusoidal motor voltages and currents.

Table I
6YI Specifications

Parameter	Value
System power P_{nom}	$1\,\mathrm{kW}$
DC input voltage U_{dc}	$80\,\mathrm{V}$ to $240\,\mathrm{V}$
AC pk. voltage $\hat{U}_{\mathrm{ac,nom}}$	$80\,\mathrm{V_{pk}}$
AC frequency $f_{\mathrm{ac,nom}}$	$50\,\mathrm{Hz}$
Nominal efficiency η_{nom}	$>95\,\%$
Power density ρ	$>3\,\mathrm{kW/dm^3}$ ($>50\,\mathrm{W/in^3}$)

The detailed operation principle of the 6YI was described and verified in [5], where a dc input voltage U_{dc} is converted into strictly-negative output capacitor voltages u_{an},u_{bn},u_{cn} of arbitrary amplitude. Because the offset voltage u_{CM} is present in all three output capacitors, it doesn't result in a current in the open-star-point motor windings and sinusoidal output voltages u_{a},u_{b},u_{c} (with amplitude $\hat{U}_{\mathrm{ac}}$) and currents i_{a},i_{b},i_{c} (with amplitude $\hat{I}_{\mathrm{ac}}$) are realized. These continuous ac output voltages reduce the high-frequency motor losses [7], a further benefit of the 6YI topology.

Despite the clear advantages in complexity and reduced component count, though, no performance metrics for the 6YI exist in literature. Further, although advanced modulation techniques were explored for the 12YI phase-modular converter in [1] (namely, the conventional Sinusoidal Pulse Width Modulation (SPWM), Third Harmonic Injection PWM (TPWM), and Discontinuous PWM (DPWM)), these have not been explored for the 6YI beyond a cursory mention (without a performance evaluation or hardware validation) in [4]. TPWM is known to increase the utilization of the dc-link voltage in buck-type systems [1], but because the 6YI is a

buck-boost system, the ac output voltage is not constrained by the dc input voltage and TPWM can realize benefits through lowering component voltage and current stresses. Similarly, DPWM is known to decrease switching losses [1] but has not been analyzed for the 6YI topology.

Our goal here, then, is to analyze and evaluate whether the low-complexity, high-reliability, and low-component 6YI structure can, with advanced modulation techniques, meet industry-standard requirements for a $1\,\mathrm{kW}$ FC-powered auxiliary motor drive with a 1:3 input voltage range of $U_\mathrm{dc} = 80\,\mathrm{V}$ to $U_\mathrm{dc} = 240\,\mathrm{V}$. With $1\,\mathrm{kW}$ motor efficiencies in the $81\,\%$-$87\,\%$ range [8], the 6YI efficiency need only exceed $95\,\%$, but the power density for these next-generation applications must exceed $50\,\mathrm{W/in^3}$ [9]. Further specifications are detailed in **Table I**.

In this Letter, indeed, we demonstrate the important benefits of harmonic injection for the 6YI, with reductions in semiconductor blocking voltage, semiconductor switching losses, inductor peak and RMS currents, and inductor and semiconductor conduction losses. In **Sec. II**, we summarize the conventional SPWM principle and introduce the two potential harmonic injection techniques, Third Harmonic Injection PWM (TPWM) and Discontinuous PWM (DPWM). The theoretical performance gains of these techniques are verified on a $1\,\mathrm{kW}$ hardware demonstrator in **Sec. III**, where we measure up to $2\,\%$ efficiency gains ($30\,\%$ lower losses) with the proposed 6YI modulation techniques and meet or exceed the auxiliary motor drive specifications. **Sec. IV** summarizes the vital improvement in ac/dc power conversion and discusses the tradeoffs between the 6YI and 12YI approaches for buck-boost applications.

II. 6YI Modulation Strategy

We briefly detail the fundamentals of 6YI operation before moving to introduce the proposed harmonic injection techniques. With detailed converter operation for the 6YI derived and verified previously [5], we only summarize the basics required to understand the advantages of harmonic injection.

A. 6YI Fundamentals

With the phase-modular approach of the 6YI topology, a single phase is sufficient to understand operation, and we use module a with references from **Fig. 1**.

The blocking voltage for the active semiconductor devices is defined by the commutation capacitor voltage u_Cta and depends on the time-varying output capacitor voltage u_an as:

$$u_\mathrm{Cta}(t) = U_\mathrm{dc} - u_\mathrm{an}(t) \geq U_\mathrm{dc}. \tag{1}$$

In the buck-boost topology, the inductor current does not flow continuously towards the output. A balanced voltage-time area for the inductor L yields the duty cycle:

$$d_\mathrm{a}(t) = \frac{|u_\mathrm{an}(t)|}{U_\mathrm{dc} + |u_\mathrm{an}(t)|}, \tag{2}$$

and, assuming the current into the output filter capacitor C can be neglected in steady-state, the low-frequency inductor current $\langle i_\mathrm{La}\rangle$ is defined by the phase output current i_a and the duty cycle d_a as:

$$\langle i_\mathrm{La}\rangle(t) = \frac{-i_\mathrm{a}(t)}{1-d_\mathrm{a}(t)}, \quad |\langle i_\mathrm{La}\rangle| \geq |i_\mathrm{a}(t)|, \tag{3}$$

with the high-frequency inductor current ripple $\Delta i_\mathrm{La,pp}$:

$$\Delta i_\mathrm{La,pp}(t) = \frac{U_\mathrm{dc}\cdot d_\mathrm{a}(t)}{f_\mathrm{s}\cdot L}. \tag{4}$$

We see that inductor stress, as expected, increases with increased boosting effort; that is, for a given U_dc (and i_a), both $|\langle i_\mathrm{La}\rangle|$ and $\Delta i_\mathrm{La,pp}$ increase monotonically with increasing $|u_\mathrm{an}|$ (higher $d_\mathrm{a}(t)$).

B. Harmonic Injection

The proposed harmonic injection for the 6YI is enabled by the fact that the Common Mode (CM) offset voltage u_CM remains a degree-of-freedom for the modulation, with only the constraint of the buck-boost topology that the output capacitor voltages u_an,u_bn,u_cn remain strictly negative. The CM voltage is defined as:

$$u_\mathrm{CM}(t) = \frac{1}{3}(u_\mathrm{an}(t) + u_\mathrm{bn}(t) + u_\mathrm{cn}(t)). \tag{5}$$

The duty cycle waveform d_a is dependent on the output capacitor voltage (see (2)), which can be defined in terms of the CM voltage as $u_\mathrm{an} = u_\mathrm{a} + u_\mathrm{CM}$, and the duty cycle therefore depends on the CM voltage. We see, further, that harmonic injection, utilizing a proper $u_\mathrm{CM}(t)$, also affects the *(a)* semiconductor blocking voltage u_Cta, through (1), *(b)* the low-frequency inductor current $\langle i_\mathrm{La}\rangle$, through (3), and *(c)* the high-frequency inductor current ripple $\Delta i_\mathrm{La,pp}$, through (4). With switching losses directly determined by blocking voltage, conduction losses (in the semiconductors and inductors) affected by the low-frequency and high-frequency currents, and core losses determined by high-frequency current ripple, we see that intelligent harmonic injection schemes could meaningfully reduce converter losses.

1) Sinusoidal Pulse Width Modulation (SPWM): The conventional SPWM scheme (employed in [5]) selects a constant offset voltage u_CM, with the minimum constant offset limited by the peak output voltage, $\hat{U}_\mathrm{ac}$, and selected as this minimum to reduce component stress as:

$$u_\mathrm{CM,S} = -\hat{U}_\mathrm{ac} \tag{6}$$

Note that a margin, of, e.g. $5\,\%$ ($u_\mathrm{CM} = 1.05\cdot u_\mathrm{CM,S}$) may be included in practical realizations for controllability and to avoid unintended turn-on of semiconductor body diodes. The voltage, duty cycle, and current waveforms for SPWM are given in **Fig. 2a**.

2) Third Harmonic Injection PWM (TPWM): The TPWM approach of [1] injects a third-harmonic component into u_CM to reduce the dc value of u_CM relative to SPWM:

$$u_\mathrm{CM,T}(t) = -\frac{\sqrt{3}}{2}\hat{U}_\mathrm{ac} + \frac{1}{6}\hat{U}_\mathrm{ac}\sin\left(3\cdot(2\pi f_\mathrm{ac})\cdot t\right). \tag{7}$$

The voltage, duty cycle, and current waveforms for TPWM are given in **Fig. 2b**. With lower output capacitor voltages than under SPWM operation, the semiconductors incur lower switching losses and the inductor current stresses (and loss) are reduced. We note here that a time-varying voltage u_CM may cause CM currents in the parasitic capacitance of the motor star-point to ground; these CM currents due to the harmonic injection, however, are rather small in amplitude, especially when compared to a standard motor drive system,

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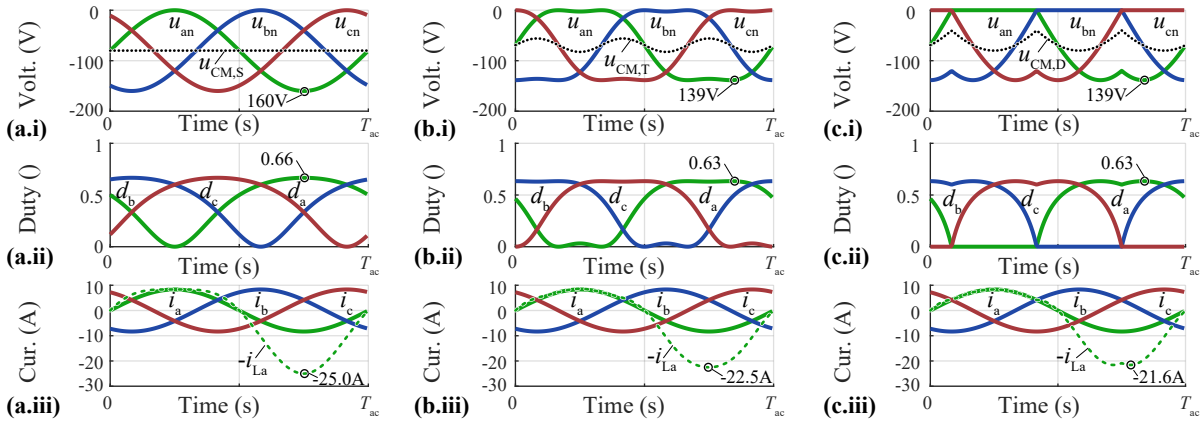

Fig. 2. Key converter waveforms for $U_{\mathrm{dc}} = 80\,\mathrm{V}$ and the proposed modulation approaches (**(a)** SPWM, **(b)** TPWM, and **(c)** DPWM), with the output capacitor voltages u_{an},u_{bn},u_{cn} (and the CM voltage u_{CM}), duty cycles d_{a},d_{b},d_{c}, and output currents i_{a},i_{b},i_{c} (and the negative inductor current $-i_{\mathrm{La}}$ of phase a) shown. The respective extreme values of phase a are highlighted by a scatter point.

TABLE II
6YI ANALYTIC LOW-FREQUENCY COMPONENT STRESS EXPRESSIONS

	SPWM	**TPWM**	**DPWM**
$u_{\mathrm{Cta,max}}$	$U_{\mathrm{dc}}(M+1)$	$U_{\mathrm{dc}}(1+M\frac{\sqrt{3}}{2})$	$U_{\mathrm{dc}}(1+M\frac{\sqrt{3}}{2})$
$I_{\mathrm{La,rms}}/I_{\mathrm{ac,rms}}$	$\frac{1}{4}\sqrt{7M^2+16M+16}$	$\frac{1}{24}\sqrt{206M^2+288M+576}$	$\frac{1}{8\sqrt{\pi}}\sqrt{(20\pi+3\sqrt{3})M^2+96\sqrt{3}M+64\pi}$
$I_{\mathrm{Ta,rms}}/I_{\mathrm{ac,rms}}$	$\frac{1}{4}\sqrt{M}\sqrt{7M+8}$	$\frac{1}{24}\sqrt{2M}\sqrt{103M+72\sqrt{3}}$	$\frac{1}{8\sqrt{\pi}}\sqrt{M}\sqrt{(20\pi+3\sqrt{3})M+48\sqrt{3}}$
$I_{\mathrm{Ta',rms}}/I_{\mathrm{ac,rms}}$	$\frac{\sqrt{M+2}}{\sqrt{2}}$	$\frac{\sqrt{M\sqrt{3}+4}}{2}$	$\frac{\sqrt{3M\sqrt{3}+4\pi}}{2\sqrt{\pi}}$
$\lvert i_{\mathrm{La}}(t=\frac{3}{4}T_{\mathrm{ac}})\rvert/\hat{I}_{\mathrm{ac}}$	$M+1$	$(\frac{3\sqrt{3}+5}{12})M+1$	$\frac{3}{4}M+1$
$\Delta I_{\mathrm{La,pp,max}}$	$\frac{MU_{\mathrm{dc}}}{(M+1)Lf_{\mathrm{s}}}$	$\frac{\sqrt{3}MU_{\mathrm{dc}}}{(\sqrt{3}M+2)Lf_{\mathrm{s}}}$	$\frac{\sqrt{3}MU_{\mathrm{dc}}}{(\sqrt{3}M+2)Lf_{\mathrm{s}}}$

where a switching-frequency CM voltage drives substantial ground currents [10].

3) Discontinuous PWM (DPWM): In DPWM, u_{CM} is selected such that the phase module with the output capacitor voltage closest to zero is not high-frequency switched (i.e. the respective semiconductor T' is permanently turned on) during one-third of the fundamental period [1]. The CM voltage can be defined as:

$$u_{\mathrm{CM,D}}(t) = -\max(u_{\mathrm{a}}(t), u_{\mathrm{b}}(t), u_{\mathrm{c}}(t)). \tag{8}$$

The voltage, duty cycle, and current waveforms for DPWM are given in **Fig. 2c**, where again the dc component of u_{CM} is reduced compared to SPWM for lower switching losses and inductor currents, but with the added benefit of no high-frequency switching in one-third of the fundamental period.

C. Component Stresses

Apart from the selected modulation strategy, the converter component stresses also depend on the voltage step-up ratio, which can be described by the modulation index M as:

$$M = \frac{2\hat{U}_{\mathrm{ac}}}{U_{\mathrm{dc}}}, \tag{9}$$

with $M = 1$ corresponding to the maximum output voltage of a standard buck-type inverter with SPWM and $M > 1$, therefore, corresponding to boost operation.

In **Fig. 2**, the extreme values of the 6YI low-frequency waveforms are highlighted, and **Table II** provides analytic equations for the operating-point-dependent 6YI low-frequency component stresses within a fundamental ac period.

The maximum blocking voltage ($u_{\mathrm{Cta,max}} = max(u_{\mathrm{Cta}}(t))$, according to (1)) is of particular importance for the selection of the power semiconductors. For all modulation schemes, the worst case value of $u_{\mathrm{Ct,max}}$ results for $U_{\mathrm{dc}} = 240\,\mathrm{V}$ and $M = 2/3$ (i.e., nominal output voltage $\hat{U}_{\mathrm{ac}} = 80\,\mathrm{V_{pk}}$) and can be reduced from $400\,\mathrm{V}$ for SPWM to $379\,\mathrm{V}$ for TPWM and DPWM due to the reduced output capacitor voltages. It is important to highlight that the 6YI semiconductors are exposed to the sum of input *and* output capacitor voltage. In contrast, the 12YI buck- and boost-stage semiconductors only block the dc voltage U_{dc} and the output capacitor voltage u_{an}, respectively [6]. Hence, switches with higher voltage rating and worse figure-of-merit [11] are required for the 6YI, which limits the performance relative to a 12YI with given dc and ac converter voltage operating ranges.

Table II also highlights the low-frequency RMS current stresses of the inductor and both the high-side T_{a} and low-side semiconductor T'_{a} within a fundamental ac period, all normalized by the ac output current. There, the worst-case stresses result for the maximum step-up ratio with $U_{\mathrm{dc}} = 80\,\mathrm{V}$ and $M = 2$ (i.e., nominal output voltage $\hat{U}_{\mathrm{ac}} = 80\,\mathrm{V_{pk}}$). Harmonic injection reduces the low-frequency inductor RMS current stresses from $12.8\,\mathrm{A_{rms}}$ with SPWM to $12.0\,\mathrm{A_{rms}}$ ($-6\,\%$), and $11.8\,\mathrm{A_{rms}}$ ($-8\,\%$), corresponding to a conduction loss decrease of $-12\,\%$ and $-16\,\%$ for TPWM and DPWM, respectively. The maximum absolute value of the low-frequency inductor current according to (3) can be

approximated with $max(|i_{\mathrm{La}}(t)|) \approx |i_{\mathrm{La}}(t = \frac{3}{4}T_{\mathrm{ac}})|$, where harmonic injection again reduces this critical metric to the design of the power inductor (to avoid saturation). Overall, the 6YI is subject to elevated RMS and peak low-frequency current stresses compared to the 12YI [6] due to the fact that the 6YI inductor current is strictly larger than the ac output current (cf., (3)), even for buck operation with $M \leq 1$.

Lastly, we highlight that the switching-frequency inductor current impacts both the converter conduction stresses and the current-dependent hard- and soft-switching losses in the semiconductors. In **Table II**, only the maximum inductor current high-frequency ripple ($\Delta I_{\mathrm{La,pp,max}} = max(\Delta i_{\mathrm{La,pp}}(t))$, according to (4)) is provided, as the analytic expressions for the overall high-frequency RMS current stresses are excessively complex. Accordingly, the resulting switched inductor current waveforms were calculated numerically for the converter design and loss distribution calculation presented in **Sec. III**.

III. Hardware Validation

A. Test Setup

To compare the performance of the three modulation strategies, a 1 kW 6YI hardware demonstrator is constructed (shown in **Fig. 3a**). This demonstrator is operated with a switching frequency $f_{\mathrm{s}} = 300\,\mathrm{kHz}$, for small filter components and high power density, into a resistive three-phase load of $R = 9.6\,\Omega$ at $f_{\mathrm{ac}} = 50\,\mathrm{Hz}$ (for unity power factor operation, the typical operating condition for a synchronous permanent magnet machine [6]). A volume breakdown of the hardware prototype is given in **Fig. 3b**, with the power inductors still constituting nearly one quarter of the total volume, even with the high selected switching frequency. Because of the low inductor value needed to achieve high power density, the converter operates in complete or partial soft-switching for a major of the period, and a direct measurement comparison of the proposed modulation techniques is more accurate and direct than a difficult analytical approach to loss estimation.

The output current control implementation deserves a special explanation, as the high switching frequency f_{s} may result in a high and/or expensive computational burden. Instead of the traditional three cascaded PI controllers *per phase*, a simple control structure is implemented here (summarized visually in **Fig. 4**). The current flowing into the output capacitor C is neglected, and the phase current reference i_{a}^{*} is directly translated into a corresponding inductor current reference i_{La}^{*}. A PI controller then tracks this inductor current reference by adjusting the duty cycle d_{a}, which is subsequently processed by a PWM block into the mutually-exclusive switching signals T_{a} and T_{a}'. With a single PI controller per phase, this control technique can be implemented with a low-cost DSP instead of an FPGA.

B. Experimental Waveforms

The measured converter waveforms for the three considered modulation strategies are given in **Fig. 5** for a nominal output power of 1 kW and an input voltage of $U_{\mathrm{dc}} = 80\,\mathrm{V}$ (and with a 5 % margin on the dc component of the CM voltage in SPWM and TPWM to avoid an unintended polarity

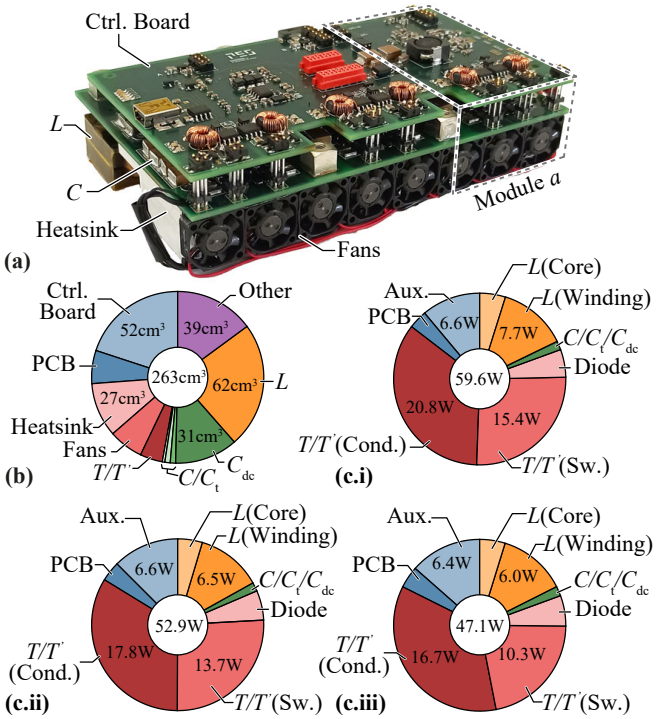

Fig. 3. (a) 1 kW 6YI hardware prototype for an FC-powered auxiliary motor drive with dimensions 120 mm x 80 mm x 27.4 mm for a power density of $62.3\,\mathrm{W/in^3}$. Power semiconductors are 2x IFX GaN IGLD60R070D1 (600 V, 70 mΩ) switched at 300 kHz and controlled by the *TMS320F28335* DSP. Power inductors ($L = 9.3\,\mu\mathrm{H}$) are implemented with a TDK ELP 32 ferrite core (N87) with a 1.0 mm air gap and 8 turns of 420 x 71 µm litz wire. The capacitor values are $C = 2\,\mu\mathrm{F}$ and $C_{\mathrm{t}} = 2.2\,\mu\mathrm{F}$. Further prototype specifications are given in **Table I**. **(b)** Converter volume distribution, with the control board and power inductors together comprising 43 % of total volume. **(c)** Calculated loss distribution under **(c.i)** SPWM, **(c.ii)** TPWM, and **(c.iii)** DPWM operation for $U_{\mathrm{dc}} = 80\,\mathrm{V}$ and $P_{\mathrm{nom}} = 1\,\mathrm{kW}$. The losses of the power semiconductors (conduction and switching) dominate the total converter losses (> 57 % of total losses), even with the loss reduction of DPWM.

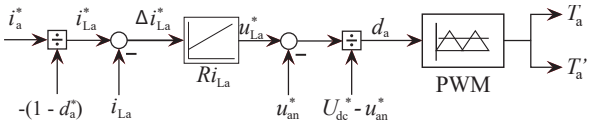

Fig. 4. Output current control diagram of the 6YI module a.

reversal). As predicted, the low-frequency inductor current $-\langle i_{\mathrm{La}} \rangle$ peak value is reduced by 8 % under TPWM and 14 % under DPWM relative to SPWM, an important result that is highlighted with the dotted line of the maximum magnitude of $-\langle i_{\mathrm{La}} \rangle = 24.4\,\mathrm{A}$ under SPWM. DPWM exhibits the lack of high-frequency switching during 1/3 of the fundamental period, as expected. Finally, because of the relatively low inductance value ($L = 9.3\,\mu\mathrm{H}$), the converter is soft-switched during a relatively large portion of the period (anywhere, to first order, with a polarity reversal of i_{La}).

The measured ratio of $i_{\mathrm{La,rms}}/I_{\mathrm{ac,rms}}$ at $P = 1\,\mathrm{kW}$ for different values of U_{dc} is summarized in **Table III**, and reduces from 2.44 (SPWM) to 2.06 (DPWM) at $U_{\mathrm{dc}} = 80\,\mathrm{V}$ and from 1.93 (SPWM) to 1.67 (DPWM) at $U_{\mathrm{dc}} = 240\,\mathrm{V}$. This underscores that while harmonic injection and DPWM are valuable at any input voltage, the proposed techniques are especially impactful at high step-up ratios (i.e. low dc

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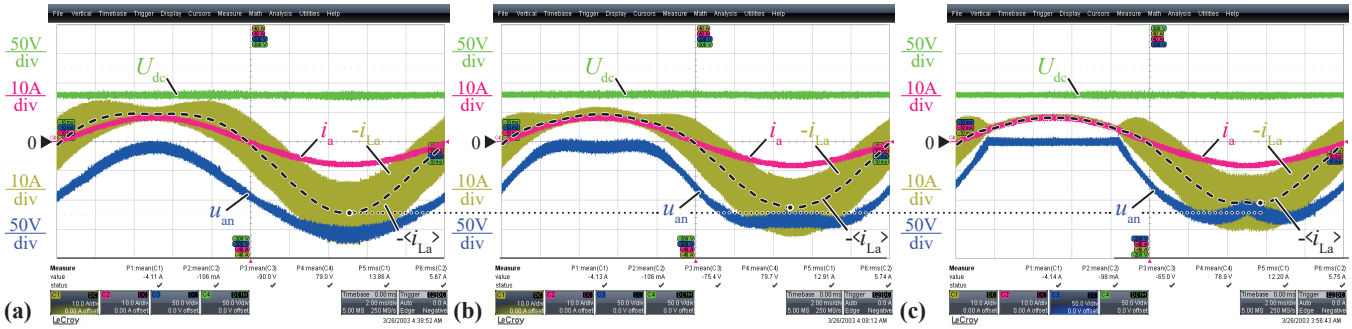

Fig. 5. 6YI experimental voltage (module a output capacitor voltage u_{an}) and current (output current i_a and negative inductor current $-i_{La}$) waveforms for modulation with **(a)** SPWM, **(b)** TPWM, **(c)** DPWM at dc input voltage U_{dc}=80 V. The negative low-frequency inductor current $-\langle i_{La} \rangle$ was extracted from the exported oscilloscope waveforms and added manually for illustration purposes, with maximum magnitude values of 24.4 A for SPWM, 22.6 A (-8 %) for TPWM, and 21.0 A (-14 %) for DPWM.

TABLE III
RELATIVE INDUCTOR CURRENT STRESS AND THD AT $P = 1\,\mathrm{kW}$ FOR DIFFERENT MODULATION STRATEGIES

U_{dc}	80 V	160 V	240 V
$I_{La,rms}/I_{ac,rms}$ (p.u.)			
SPWM	2.44	1.96	1.93
TPWM	2.24	1.84	1.81
DPWM	2.06	1.70	1.67
Total Harmonic Distortion (THD) (%)			
SPWM	3.3	3.4	1.3
TPWM	2.9	2.8	1.1
DPWM	3.7	4.0	2.7

input voltage). **Table III** also provides the measured Total Harmonic Distortion (THD). The maximum THD values result for the minimum value $U_{dc} = 80\,\mathrm{V}$, i.e., for the maximum step-up ratio. This can be explained by the simple control scheme depicted in **Fig. 4**, which does not consider the reactive current flow into the output capacitor, C. Further, the THD values are higher for TPWM and DPWM compared to SPWM, which can be explained by the additional frequency components in the output voltage waveforms (cf., **Fig. 2**). However, even for DPWM, the maximum THD value remains $< 5\,\%$.

With the expected converter waveforms validated, the input voltage U_{dc} and output power are swept to measure the efficiency improvement of the proposed harmonic injection schemes.

C. Efficiency Measurements

The converter power losses are measured with a Yokogawa WT1804E power analyzer and reported in **Fig. 6** for dc input voltages of 80 V and 240 V. At low-power levels, the losses for SPWM and TPWM are nearly identical, with the advantages of TPWM increasing with higher output powers up to a loss decrease of 13 % for $U_{dc} = 80\,\mathrm{V}$. This power-dependent comparison occurs because, although the switched voltage is slightly reduced in TPWM over SPWM, the main improvement is in the smaller conduction losses from reduced low- and high-frequency currents in TPWM.

DPWM reaches the maximum measured efficiency of 95.6 % for $U_{dc} = 240\,\mathrm{V}$, with substantial conduction *and*

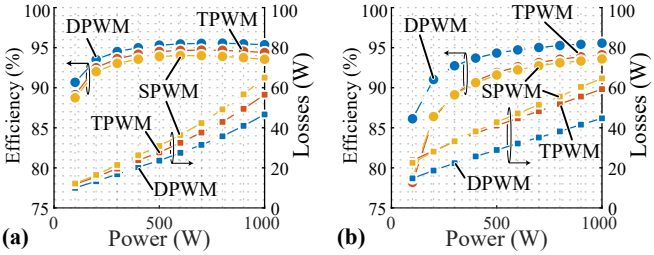

Fig. 6. Measured converter efficiency (round scatter symbols) and power losses (square scatter symbols) over output power for **(a)** $U_{dc} = 80\,\mathrm{V}$ and **(b)** $U_{dc} = 240\,\mathrm{V}$ for the considered modulation techniques. Auxiliary circuits were externally supplied, with measured auxiliary powers of $P_{aux} = 6.6\,\mathrm{W}$ for SPWM and TPWM and $P_{aux,D} = 6.4\,\mathrm{W}$ for DPWM (due to reduced gate drive power). The auxiliary power consumption is included in the reported efficiencies.

switching loss decreases relative to SPWM and TPWM. A loss breakdown for DPWM operation at $U_{dc} = 80\,\mathrm{V}$ is given in **Fig. 3c.iii**, where the semiconductor losses comprise nearly 60 % of total converter losses – even with the reductions in both switching and conduction losses of DPWM. The switching loss decrease, in particular, is especially valuable at lower output powers, where DPWM achieves a multi-point efficiency improvement relative to SPWM and TPWM at all input voltages at $P = 100\,\mathrm{W}$ (especially pronounced at high U_{dc} operating points, which have the highest switching losses). The loss decrease of DPWM over SPWM reaches 31 % for $U_{dc} = 240\,\mathrm{V}$ and $P = 1\,\mathrm{kW}$, with an associated efficiency increase of a full 2 %.

IV. CONCLUSION

In this Letter, we propose two harmonic injection schemes for the Six-Switch Buck-Boost Y-Inverter (6YI), a low complexity phase-modular buck-boost three-phase inverter. These new modulation techniques improve both conduction (through reduced low- and high-frequency currents) and switching (through reduced blocking voltages and, for DPWM, no high-frequency switching during 1/3 of the fundamental period). The advantages of the novel modulation strategies are validated on a 1 kW hardware prototype that achieves the auxiliary motor drive targets of 95 % efficiency and $50\,\mathrm{W/in^3}$ power density, with the efficiency metric only achievable with the loss reductions of TPWM and DPWM of up to 31 % relative to the conventional SPWM (at nominal power).

With these modulation schemes, the Six-Switch Buck-Boost Y-Inverter (6YI) topology becomes more attractive in applications requiring buck-boost capabilities, although the consequence of simplicity and a low component count remain: even with the advanced modulation schemes, the Six-Switch Buck-Boost Y-Inverter (6YI) incurs a simultaneous penalty of a $2\times$ reduction in power density and a $2\times$ increase in losses relative to the Twelve-Switch Buck-Boost Y-Inverter (12YI) [6]. The selection of topology for a phase-modular, single-stage, buck-boost inverter will, therefore, be dependent on the particular application weights to complexity, efficiency, size, and cost.

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