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***Abstract*— In solid-state-transformer technology, the isolation and power transfer between low voltage and medium voltage side is performed by a high power DC/DC converter. This DC/DC converter provides a defined ratio between input and output voltages, whereby, in order to reduce switching losses, zero-current-switching modulation schemes are often mandatory. The series-resonant-converter operated in half-cycle discontinuous-conduction-mode possesses all the aforementioned features, thus making it highly attractive for solid-state-transformer applications. For this reason, a comprehensive analytical model of the converter's static and dynamic behavior is provided in this paper. In addition, a method to model the switching losses under ZCS conditions, which is based on the behavior of the stored charge in the semiconductors, is presented. This enables an efficiency/power density (η-ρ) Pareto optimization of the aforementioned converter system.**

I. Introduction

Solid-state transformers (SST) are envisioned as one of the key enabling technologies for future highly compact traction power conversion systems [1]–[3], renewable energy generation [4], [5], and smart grid implementations [6], [7]. SSTs are utilizing a high-power DC/DC converter to provide the required isolation and to link the medium voltage (MV) system to the low voltage (LV) side DC/AC converter [6]. Moreover, this DC/DC converter can be utilized to regulate the output voltage. In SST applications however, voltage regulation is not mandatory, whereby the DC/DC converter can be used to provide a fixed ratio between the MV and LV DC levels relying on the MV AC/DC and/or LV DC/AC converters to perform output voltage regulation. Because semiconductor devices with high voltage blocking capability are required on the MV side, IGBTs are often considered. In order to operate these semiconductors in the medium frequency (MF) range, zero-current-switching (ZCS) modulation schemes are highly desirable and very often mandatory in order to reduce the switching losses.

The half-cycle discontinuous-conduction-mode (DCM) series-resonant-converter (HC-DCM-SRC) comprises all the aforementioned desired features of DC/DC converters within SSTs: 1) isolation, 2) fixed LV to MV DC voltage transfer ratio and 3) ZCS of all semiconductor devices. This type of resonant converter has been analyzed in [8]–[10] for full-cycle DCM, i. e. with a full resonant-cycle flowing during one half of a switching cycle, and in [11], [12] for half-cycle DCM operation, whereby an analytical description of the static and dynamic behavior in this operating mode has been presented in [13], [14] already in the early 90ies. Therefore, the HC-DCM-SRC is a well-known concept that now is regaining attention for high-power applications such as discussed here, but also for low-power applications, which benefit from isolation and fixed voltage transfer ratio in open-loop operation, as for example described in [15].

The main aforementioned publications are comprehensively summarized in this paper in order to provide models that accurately describe the operating principles of the HC-DCM-SRC. With these models, all currents and voltages in the converter can be analytically described, which, together with efforts focused on the ZCS behavior of power semiconductors [2], [3], [16] and specifically the analysis presented in [17] for ZCS-loss mechanisms in IGBTs, allows the HC-DCM-SRC to be thoroughly modeled, providing a base to perform a power density/efficiency (η-ρ) Pareto optimization [18] of this converter.

II. Operating Principle

In this section, the fundamental operating principle of the HC-DCM-SRC is described, illustrating its terminal behavior as a "DC transformer" and the influence of the converter losses on the input/output voltage transfer ratio.

Ideally, the HC-DCM-SRC (Fig. 1(a)) is operated such that the switching event occurs at the zero-crossing of the resonant tank current in order to achieve low switching losses. Thus, the sign of the resonant current, i_r, determines the states of the switches:

$$\begin{aligned} i_\mathrm{r} > 0: &\ \mathrm{S}_1 \text{ and } \mathrm{S}_4 \text{ are turned on,} \\ i_\mathrm{r} < 0: &\ \mathrm{S}_2 \text{ and } \mathrm{S}_3 \text{ are turned on,} \end{aligned} \tag{1}$$

where the presented analysis confines to power transfer from MV side to LV side; operation for the opposite power flow direction yields similar results. As a consequence, a self-sustained oscillation close to the resonance frequency, $f_0 = \left(2\pi\sqrt{L_\mathrm{r}C_\mathrm{r}}\right)^{-1}$, of the resonant tank is achieved (Fig. 1(b)), since a practical converter design features a comparably low ohmic voltage drop.

The resulting steady state output voltage, V_LV, is close to V_MV/n, however, a small difference $V_\mathrm{MV}/n - V_\mathrm{LV}$ remains

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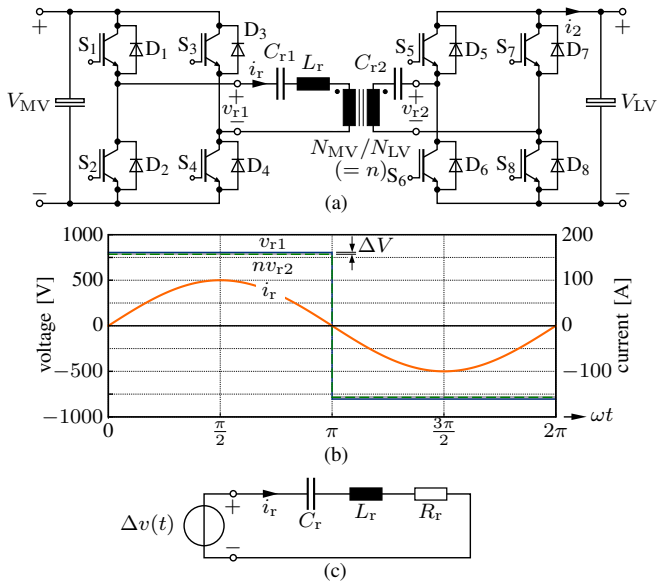

Fig. 1. (a) HC-DCM-SRC topology; (b) simulated current and voltage waveforms for $L_r = 16\,\mu H$, $C_r = 25\,\mu F$, $R_r = 130\,m\Omega$, $V_{MV} = 800\,V$ and $P_{out} = 50\,kW$; (c) simplified and primary side referred converter model [13].

due to converter losses. In the following, an analytical model introduced in [13] will be used to determine the influence of the load power and the losses on this voltage difference, on which the model is based. It employs the simplified converter circuit depicted in Fig. 1(c), which neglects all parasitic components of the transformer and refers all currents and voltages to the primary side. There, R_r summarizes the resistive components of the circuit and $\Delta v(t)$ is the effective voltage applied to L_r, C_r and R_r;

$$\Delta v(t) = [V_{MV} - 2V_{f,IGBT} - n(V_{LV} + 2V_{f,diode})] \cdot \text{sign}\,(i_r(t)) = \Delta V \cdot \text{sign}\,(i_r(t)) \quad (2)$$

and

$$R_r = R_{L+C+tr} + 2(R_{d,IGBT} + n^2 R_{d,diode}), \quad (3)$$

where R_{L+C+tr} is the sum of the series resistances of L_r, C_r and the transformer; $V_{f,IGBT}$ and $V_{f,diode}$ are the (approximately) constant forward voltage drops of IGBTs and diodes; and $R_{d,IGBT}$ and $R_{d,diode}$ are the IGBTs' and diodes' differential resistances.[1]

The steady state operating point is calculated by means of fundamental frequency analysis [13], which features an accurate description of the processes in the resonant tank due to the reasons given below:

1) The amplitude of each odd n-th harmonic component of the rectangular voltage $\Delta v(t)$, $\Delta V_{(n),pk}$, is given with $\Delta V_{(n),pk} = \Delta V_{(1),pk}/n$. Thus, the impact of $\Delta V_{(n),pk}$ on the waveform of i_r decreases with increasing n.
2) The frequency of the fundamental component of $\Delta v(t)$ is very close to f_0. The resonant tank represents a low pass filter for $f > f_0$ and effectively reduces harmonic current components with $n > 1$ (cf. Fig. 2).

Laplace transform is used to analyze the initial excitation

[1]Assuming identical diodes $D_1 \ldots D_8$ and identical IGBTs $S_1 \ldots S_8$.

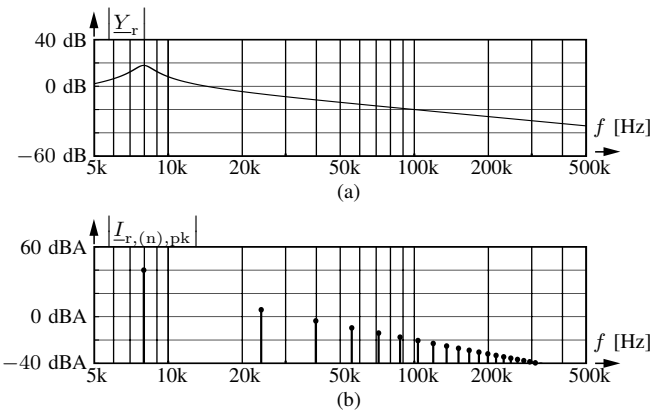

Fig. 2. (a) Admittance of the resonant tank ($L_r = 16\,\mu H$, $C_r = 25\,\mu F$, $R_r = 130\,m\Omega$); (b) calculated spectrum of i_r: $I_{r,(1),pk}$ is 34 dB higher than $I_{r,(3),pk}$. The spectrum of Fig. 2(b) corresponds to the current depicted in Fig. 1(b), which is almost sinusoidal.

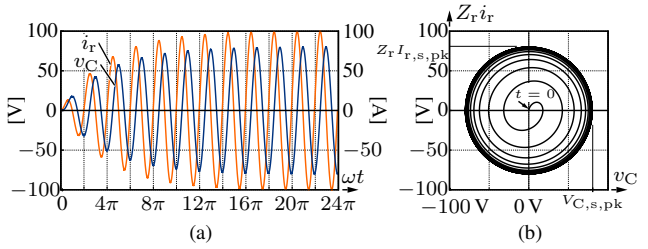

Fig. 3. (a) Response of the resonant tank of Fig. 1 to a sinusoidal excitation; (b) corresponding phase diagram.

of the resonant tank with

$$\Delta v_{(1)}(t) = \frac{4}{\pi}\Delta V \sin(\omega_0 t) \text{ where } \omega_0 = \frac{1}{\sqrt{L_r C_r}}. \quad (4)$$

This yields the response shown in Fig. 3, which illustrates how steady state operation is reached after a few oscillations. The steady state operating point is calculated with conventional circuit theory,

$$\Delta \underline{V}_{(1),pk} = \frac{4}{\pi}\Delta V e^{j\omega_0 t}, \quad \underline{I}_{r,(1),pk} = \frac{\Delta \underline{V}_{(1),pk}}{R_r},$$
$$\underline{V}_{C,(1),pk} = -jZ_0 \underline{I}_{r,(1),pk} \text{ with } Z_0 = \sqrt{\frac{L_r}{C_r}}, \quad (5)$$

and the resulting amplitudes of the capacitor voltage, v_C, and the inductor current, i_r, are:

$$V_{C,(1),pk} = \frac{4\Delta V}{\pi}\frac{Z_0}{R_r}, \quad I_{r,(1),pk} = \frac{4\Delta V}{\pi}\frac{1}{R_r}. \quad (6)$$

The capacitor connected to the output side rectifier impresses a constant voltage, V_{LV}, and thus the output power is proportional to the square of the average resonant tank current. Accordingly, (6) enables the calculation of ΔV as a function of the transferred power,

$$P_{out} = \left(\frac{2}{\pi} I_{r,(1),pk}\right)^2 n^2 R_{load} = \left(\frac{8}{\pi^2}\frac{\Delta V}{R_r}\right)^2 n^2 R_{load}$$
$$\Rightarrow \Delta V(P_{out}) = R_r \frac{\pi^2}{8}\sqrt{\frac{P_{out}}{n^2 R_{load}}} = R_r \frac{\pi^2}{8}\frac{P_{out}}{nV_{LV}}, \quad (7)$$

where $R_{load} = V_{LV}^2/P_{out}$ has been used for the last step. From that, V_{LV} can be obtained as

$$V_{LV} = [V_{MV} - \Delta V(P_{out}) - 2V_{f,IGBT}]/n - 2V_{f,diode}, \quad (8)$$

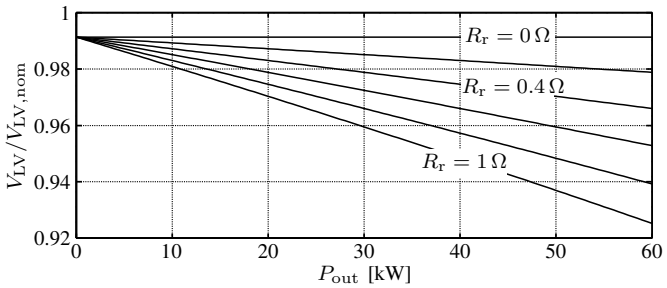

Fig. 4. Dependence of the LV side output voltage on the transferred power and the resistor R_{r}.

and by substituting $\Delta V(P_{\mathrm{out}})$ by (7), the relation between transferred power and resulting deviation from the ideal voltage transfer ratio can be found as

$$V_{\mathrm{LV}} = \frac{1}{2}V_0 + \frac{1}{2}\sqrt{V_0^2 - \frac{\pi^2}{2n^2}R_{\mathrm{r}}P_{\mathrm{out}}}, \tag{9}$$

$$\text{where } V_0 = \frac{1}{n}V_{\mathrm{MV}} - 2\left(\frac{1}{n}V_{\mathrm{f,IGBT}} + V_{\mathrm{f,diode}}\right).$$

This equation and its visualization in Fig. 4 show clearly that the system losses, here considered only by the semiconductor voltage drops and the resistor R_{r} for reasons of clarity, cause a load-dependent variation of the input/output DC voltage ratio. Switching losses and core losses can be regarded as an increase of the effective load power. In order to achieve a tight coupling between input and output DC voltages that is (nearly) independent from the transferred power, it is thus mandatory to minimize the converter losses.

Additionally, the fundamental frequency model enables the derivation of a small signal model (cf. Fig. 5(a)) [13], which employs transformed component values

$$L_{\mathrm{r,eq}} = \frac{\pi^2}{4}L_{\mathrm{r}},\ R_{\mathrm{r,eq}} = \frac{\pi^2}{8}R_{\mathrm{r}}. \tag{10}$$

The model can be used to accurately predict the dynamic response of the average output current and output voltage (cf. Fig. 5(b)). This makes it possible to model the DC/DC stage as a very simple "black box" within the complex model of a complete SST system.

So far it has been assumed that the switching frequency, f_{s}, equals the resonance frequency. However, in a real system $f_0 > f_{\mathrm{s}}$ has to be chosen in order to account for the finite switching speed and the interlock delay time requirements. In addition, the resulting zero current interval between the end of the resonant half cycle and the switching transition (cf. Fig. 8(a)) can be used to reduce ZCS switching losses as will be shown later. Assuming piecewise sinusoidal currents, the transferred power for the case $f_0 > f_{\mathrm{s}}$ and the topology shown in Fig. 7 is given by

$$P = \frac{2}{T_{\mathrm{s}}}\int_0^{\frac{T_0}{2}} \frac{V_{\mathrm{MV,dc}}}{2} I_{\mathrm{r,pk}} \sin(2\pi f_0 t)\, dt = \frac{V_{\mathrm{MV,dc}} I_{\mathrm{r,pk}} f_{\mathrm{s}}}{\pi f_0}, \tag{11}$$

where $T_{\mathrm{s}} = 1/f_{\mathrm{s}}$ and $T_0 = 1/f_0$. Neglecting losses, the peak currents on both sides of the transformer can be calculated as

$$\hat{I}_{\mathrm{r,MV}} = \frac{P\pi f_0}{V_{\mathrm{MV,dc}} f_{\mathrm{s}}} \text{ and } \hat{I}_{\mathrm{r,LV}} = \frac{P\pi f_0}{2V_{\mathrm{LV,dc}} f_{\mathrm{s}}}. \tag{12}$$

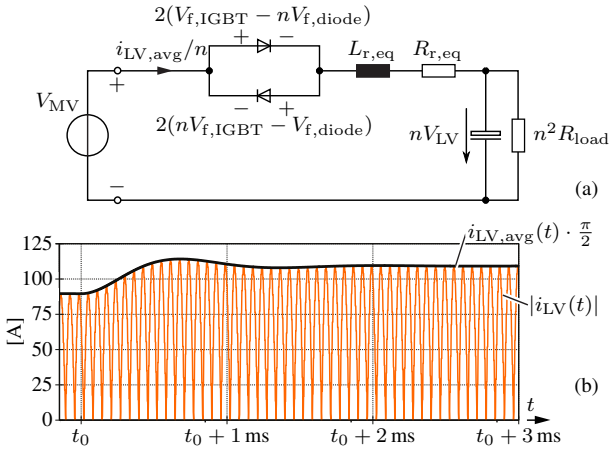

Fig. 5. (a) Small signal model of the HC-DCM-SRC; (b) simulated response to a load step (45 kW → 55 kW) at t_0: the peak values of the oscillating current, obtained from a simulation of the circuit shown in Fig. 1, are in good agreement with the envelope (thick line), which is obtained by scaling the average current, $i_{\mathrm{LV,avg}}$, of Fig. 5(b) with a factor of $2/\pi$. Component values: $L_{\mathrm{r,eq}} = 39.5\,\mu\mathrm{H}$, $R_{\mathrm{r,eq}} = 160\,\mathrm{m}\Omega$.

The positive semi-cycle of the AC link current on the MV side can therefore be described as

$$i_{\mathrm{r,MV}}(t) = \begin{cases} \hat{I}_{\mathrm{r,MV}} \sin(2\pi f_0 t) & 0 \le t < T_0/2 \\ 0 & T_0/2 \le t \le T_{\mathrm{s}}/2 \end{cases}; \tag{13}$$

the negative semi-cycle follows from symmetry considerations.

III. MV Side Topologies

For operation in the MV and MF range, IGBTs with 1.7 kV blocking voltage offer a feasible compromise between switching losses and the required number of semiconductors. The choice is further justified by cost considerations in comparison to IGBTs of higher blocking capability. Because the converter to be considered for the η-ρ optimization uses a DC link voltage of 2.2 kV, three-level topologies must be considered for the MV side. In addition to the standard neutral-point-clamped (NPC) topology shown in Fig. 7 and used later in the Pareto optimization, Fig. 6 shows two alternative realization options for the MV side bridge. In both variants, additional capacitors are employed instead of clamping diodes.

Fig. 6(a) is a flying capacitor topology where the capacitor C_3 is charged to half the DC link voltage and thus ensures voltage limitation for the switches [19]. The output current, i_{r}, flows through the flying capacitor during the freewheeling state. Since in the HC-DCM-SRC the freewheeling interval is very short and only the magnetizing current is flowing during that time, C_3 can be made small. By proper choice of the freewheeling states, natural balancing of its voltage can be achieved because of the dependence of the magnetizing current on the applied voltage. However, there is still a need to pre-charge that capacitor.

The third topology [20] is shown in Fig. 6(b). Since the DC link midpoint is connected between S_2 and S_3, the switch voltage stress is limited to half the DC link voltage. The resonant capacitor, C_{r}, carries a DC offset of $V_{\mathrm{DC}}/2$, which enables again to apply three voltage levels to the transformer. However, C_{r} is subject to high DC voltage and simultaneously

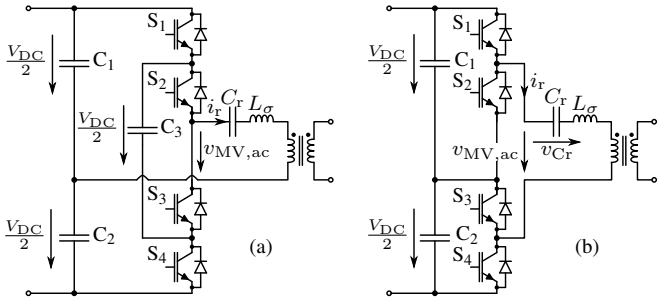

Fig. 6. Other realization options for the MV side bridge that allow for using 1.7 kV IGBTs for $V_{\mathrm{DC}} = 2.2\,\mathrm{kV}$; (a) adds a flying capacitor while (b) uses a DC offset of $V_{\mathrm{DC}}/2$ on the resonant capacitor [20].

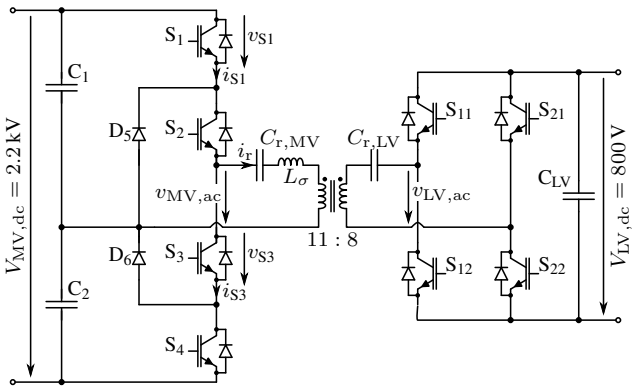

Fig. 7. HC-DCM-SRC topology considered for the η-ρ Pareto analysis.

high current stress and/or AC voltage ripple, which is the main drawback of this topology.

Accordingly, all further considerations are for the NPC three-level topology depicted in Fig. 7.

IV. System Modeling

Performing an η-ρ Pareto optimization [18] for a converter is a suitable way of identifying designs that result in low overall losses and thus in a tight coupling of the DC voltages and on the other hand ensure a reasonably high power density. To do so, it is required to estimate the losses generated in the main components (semiconductors, transformer, resonant capacitors, DC link capacitors) as well as the component volumes for a given design. There exist a variety of models of these component losses, except for the switching losses under the conditions found in the HC-DCM-SRC. Therefore, the modeling of the other components is only briefly discussed, whereas more room is dedicated to the semiconductor switching loss modeling. Fig. 7 shows the converter topology considered for the Pareto optimization and Table I gives an overview on the system specifications.

A. Semiconductors

Even though the switching instants are such that ZCS is obtained, significant switching losses are generated because of the dynamic behavior of the charge in the N-base layer of the IGBTs [17], [21]. A suitable model that allows estimation of the semiconductor losses under these conditions is presented in the following.

TABLE I
DC/DC Converter Specifications.

P	52.5 kW
Power flow direction	MV $\rightarrow$ LV
$V_{\mathrm{MV,dc}}$	2.2 kV
$V_{\mathrm{LV,dc}}$	800 V
Max. DC voltage ripple	0.5 %
Max. junction temp. T_{j}	125 °C
Ambient temperature T_{a}	50 °C
Switching frequency range	5 kHz to 15 kHz
Transformer volume range.	1 L to 30 L
Current zero interval duration	0 to $0.5T_{\mathrm{S}}/2$

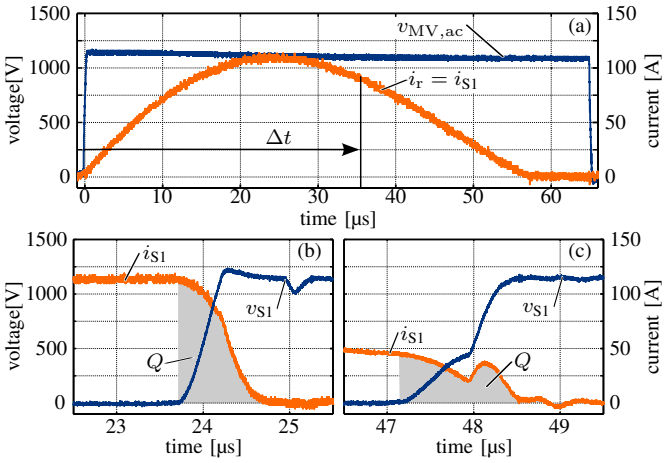

Fig. 8. (a) Positive current pulse where the current through S_1 equals the current i_{r} for $L_\sigma = 7.6\,\mu\mathrm{H}$ and $C_{\mathrm{r}} = 43\,\mu\mathrm{F}$, resulting in $f_0 \approx 8.8\,\mathrm{kHz}$. The turn-off time is defined by Δt and varied to measure the extracted charge at different points of the current waveform. Definition of the charge extracted from S_1 for (b) $\Delta t = 24\,\mu\mathrm{s}$ and (c) $\Delta t = 48\,\mu\mathrm{s}$.

1) Stored Charge Behavior: This phenomenon has been analyzed in [21] and an analytical model for the stored charge, $Q(t)$, has been derived in [17] as

$$\frac{dQ(t)}{dt} = -\frac{Q(t)}{\tau} + k_{\mathrm{s}} \cdot i_{\mathrm{s}}(t), \tag{14}$$

where τ and k_{s} are device parameters and $i_{\mathrm{s}}(t)$ is the current through the device. This model enables the calculation of the amount of charge, Q_{off}, that needs to be evacuated when the device is turned off, therefore providing information about the dissipated energy during the switching transient.

The model parameters τ and k_{s} are construction parameters of the semiconductors, which are generally not public, and therefore must be determined by curve fitting to experimental data as has been done in [17] for triangular current waveforms. The experiment is repeated here for the sinusoidal current of the HC-DCM-SRC shown in Fig. 8(a) for the positive semi-cycle. The duration, Δt, of the applied voltage pulse is reduced in steps in order to measure the amount of charge extracted from S_1 at different points within the current waveform. Fig. 8(b) and Fig. 8(c) illustrate how this charge is measured during the turn-off switching transition of S_1.

Fig. 9 shows the measured charge, $Q(t)$, as well as the charge calculated with the the parameters k_{s} and τ obtained from fitting (14) to the measurement data (cf. Table II for

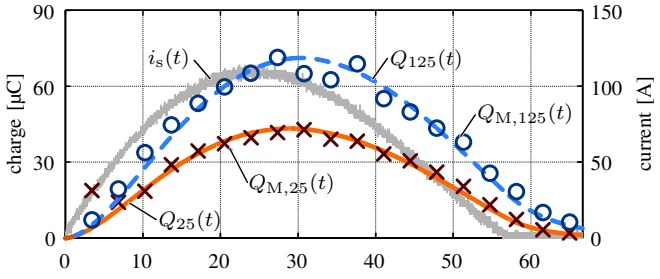

Fig. 9. Behavior of the stored charge for the FF150R17KE4 IGBT at $T_j = 25\,°C$ and $T_j = 125\,°C$. $Q_{M,25}(t)$, $Q_{M,125}(t)$ are measurements and $Q_{25}(t)$, $Q_{125}(t)$ are obtained with (14) and k_s, τ as given in Table II.

TABLE II
EXTRACTED PARAMETERS FOR THE FF150R17KE4 IGBT.

Temperature T_j	τ	k_s
25 °C	4.45 µs	0.092
125 °C	6.04 µs	0.115

parameter values). As can be seen, the model enables accurate prediction of the behavior of the stored charge in the IGBT.

2) Switching Loss Reduction: When the switch current reaches zero, the charge carriers in the N-base layer recombine and thus the amount of stored charge in S_1 decays exponentially. During the subsequent transition from positive active state to freewheeling, first S_1 turns off, but since the current is already zero, v_{S1} stays low until the complementary switch S_3 turns on when the interlock delay time is over. If the turn-on of S_3, which ultimately forces v_{S1} to rise, occurs before the recombination process in S_1 is completed, the remaining charge in S_1 has to be evacuated through both of these switches and the resulting current spike generates turn-off losses in S_1 and turn-on losses in S_3, even though zero current switching is used (cf. Fig. 11(a)). However, there are several possibilities to reduce these switching losses as discussed in the following.

a) Zero Current Interval Duration: During the time when the AC current is zero, the amount of stored charge decays because of recombination. Therefore, by increasing the duration of the zero-current interval, Q_{off} can effectively be reduced [3], [16]. However, from (12) it follows that $I_{r,pk} \propto f_0/f_s$ for $P = const.$, which clearly shows that a longer zero current interval (corresponding to higher f_0), while reducing switching losses, increases the peak current for the same amount of transferred power. This causes higher conduction losses in the semiconductors and also higher losses in passive components due to higher rms current. However, as illustrated by Fig. 10, there is an optimum duration of the zero current interval resulting in lowest overall losses. The results in Fig. 10 consider only semiconductor losses for the sake of clarity, while later in the η-ρ Pareto optimization all affected losses are included.

b) Magnetizing Current: The magnetizing current, which is still flowing after the resonant current has already decayed to zero, helps to extract the charge from S_1 during the interlock delay time between the turn-off of S_1 and the turn-on of S_3 as described in [2], [16]. If the magnetizing current is high enough, ZVS turn-on for S_3 can be achieved. On the other

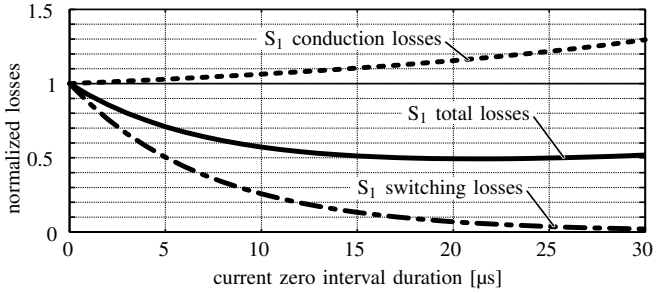

Fig. 10. Influence of the zero current interval duration on the semiconductor losses for $f_s = 7.5\,kHz$ and $T_j = 125\,°C$. Note that the optimum is shifted to the left and upwards if other losses related to rms current are included.

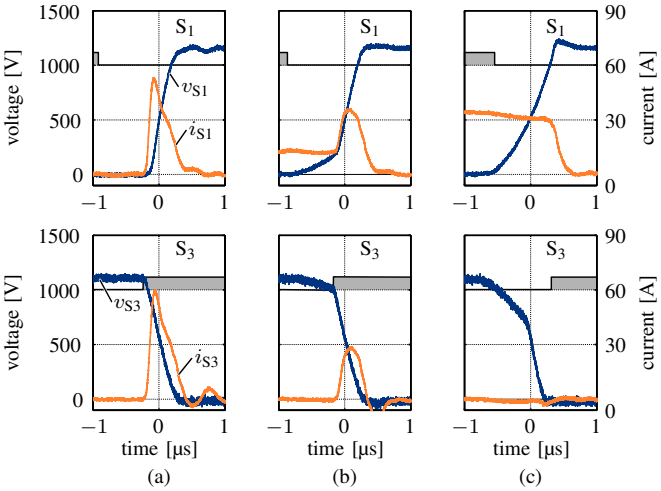

Fig. 11. The commutation process changes with increasing magnetizing current from (a) pure ZCS via (b) a mixed form to (c) soft-switching. The measurements were taken with a zero current interval of about 2 µs and an effective interlock time of about 0.8 µs; the gate signals are indicated qualitatively.

hand, the turn-off losses in S_1 increase because the magnetizing current influences the charge profile and is switched off actively. Fig. 11 shows the switching transitions for S_1 and S_3 for three different magnetizing current peak values. These results were obtained by connecting different external inductors in parallel to the MV transformer winding in order to emulate different magnetizing inductances [2]. Fig. 12 shows the measured turn-off losses of S_1 and turn-on losses of S_3 for two different junction temperatures as a function of the peak magnetizing current. It can clearly be seen that there is an optimum regarding the overall switching losses, which occurs for the lowest magnetizing current peak value that is sufficient

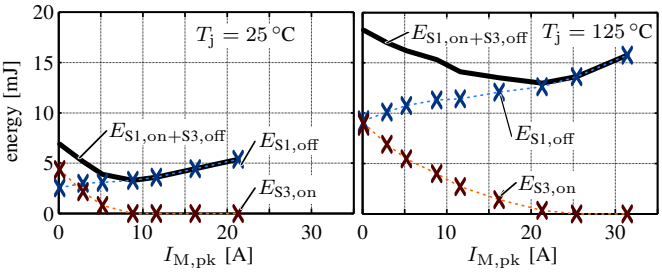

Fig. 12. Influence of the magnetizing current peak value, $I_{M,pk}$, on the turn-off losses in S_1 and the turn-on losses in the complementary switch S_3.

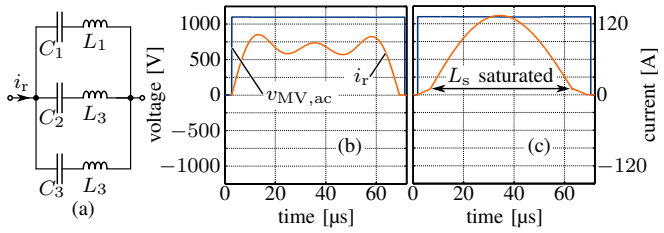

Fig. 13. (a) Extended resonant tank where branch 1 is tuned to $f_0 = 7500\,\text{kHz}$, branch 2 to $3f_0$ and branch 3 to $5f_0$ and (b) resulting current waveform. (c) shows the current shape when a saturable inductor is connected in series to the normal LC resonant tank instead.

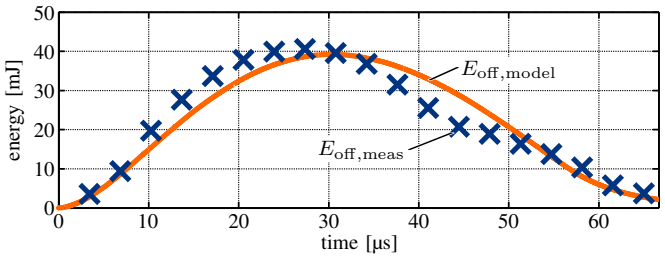

Fig. 14. Measurement and estimate of the turn-off losses in S_1 at $T_j = 125\,°C$. The Δt values used for the measurements are the same as in Fig. 9.

to achieve ZVS turn-on for S_3. The required peak magnetizing current can be estimated from $I_{M,pk} = Q_{off}/\Delta t_{il}$ under the assumption of constant magnetizing current during the interlock delay time Δt_{il}. Q_{off} is the remaining charge in S_1 at its turn-off instant.

To increase the accuracy, recombination of the charge according to (14) during Δt_{il} must be considered as well as the influence of a given magnetizing current peak value on the switch current waveform (hence on losses in all components carrying the magnetizing current) and the resulting charge profile in S_1, which has to be done in an iterative way. In the η-ρ Pareto optimization, the influence of the magnetizing current on conduction and passive component losses is included.

c) Current Pulse Shaping: The stored charge in the IGBT at a given point in time depends on the shape of the current up to that point. By shaping the current with an appropriate extension of the resonant tank, as e. g. described in [22] and [23] for thyristor commutation circuits, the stored charge and/or the switching losses could be influenced, and/or shaping the current to a rectangular block with lower rms value for a given power would allow to reduce rms losses in the system. Such a current shape could be created by connecting several series resonant circuits in parallel as shown in Fig. 13(a). As an example, let one resonant tank be tuned to f_0, the second to $3f_0$ and the third to $5f_0$. Fig. 13(b) shows the resulting shape of the resonant current. The rms value is reduced to 93 % when compared with the rms value of a pure sinusoidal current for the same transferred power. This corresponds to a reduction of all I^2-losses to 86.5 %.

In order to complete the picture, it has to be pointed out that it is not sufficient anymore to consider only the steady state forward characteristics when estimating conduction losses if the current shows a high di/dt at the beginning of the pulse. Instead, the dynamic behavior of the IGBT (S_1) forward voltage after turn-on [21] would have to be considered. A corresponding extension to the semiconductor modeling approach presented here is subject to future work by the authors.

Regarding the adverse effect of high di/dt at the beginning of the current pulse, another option of shaping the current consists of connecting a saturable inductor, L_s, in series to the standard LC resonant tank. This saturable inductor represents a high inductance for low currents, i. e. at the beginning and at the end of the pulse, and almost no inductance as soon as the current crosses the saturation threshold. Fig. 13(c) shows a resulting current waveform, which shows low di/dt at the beginning and at the end, where the latter is beneficial regarding Q_{off}, similar to an increase of the zero current interval duration.

3) Semiconductor Loss Modeling: The charge that would have to be removed for the current described by (13) can be calculated with (14). As indicated above, an iterative procedure is then used to determine the required magnetizing current to achieve ZVS turn-on for the complementary switch in order to obtain lowest overall switching losses. From that, Q_{off} of the turning-off switch can be determined and the turn-off energy can be estimated according to

$$E_{off} = \frac{1}{2} Q_{off} \frac{V_{MV,dc}}{2}. \tag{15}$$

This approach is based on the assumption that the turn-off energy corresponds to the energy in a capacitance with charge Q_{off} at the blocking voltage of the device. Fig. 14 illustrates that the assumption does agree well with measurements for pure ZCS (ca. $\Delta t \geq 55\,\mu s$) as well as for pure soft-switching (ca. $\Delta t \leq 40\,\mu s$). Especially for the mixed form (cf. Fig. 11(b)), future work will be required to unveil a more appropriate method of relating Q_{off} to the turn-off energy. However, all in all it becomes possible also with the models presented here to calculate semiconductor losses under ZCS conditions, which is a cornerstone of any comprehensive optimization of the HC-DCM-SRC.

These losses occur four times (in all four MV side switches) per switching period and consequently the switching losses are given by

$$P_{off} = 4 f_s E_{off}. \tag{16}$$

The switching losses of the diodes on the LV side are estimated accordingly. Conduction losses of both bridges are modeled following the procedure described in [24] using datasheet forward characteristics.

B. Heat Sinks

The losses generated in the semiconductors need to be removed in order to keep the maximum junction temperature below a certain value (typ. 125 °C). With the semiconductor loss estimates and datasheet values for the thermal resistances from junction to heat sink, the maximum allowable heat sink temperature can be calculated:

$$T_{HS,max} = T_{j,max} - (P_{switch} + P_{cond}) R_{th,J\text{-}H} \tag{17}$$

Using the Cooling System Performance Index (CSPI) introduced in [25], it is possible to estimate the size of an air cooled heat sink for given power dissipation, ambient temperature and

required maximum heat sink temperature as

$$V_{\mathrm{HS}} = \frac{1}{CSPI \cdot R_{\mathrm{th,HS,max}}}, \tag{18}$$

where $R_{\mathrm{th,HS,max}} = (T_{\mathrm{HS,max}} - T_{\mathrm{a}})/P_{\mathrm{loss}}$. A CSPI value of 5 W/KL is used, which corresponds to a standard forced air cooled heat sink [25].

C. DC Link Capacitors

When constant DC input and output currents, $I_{\mathrm{MV,dc}} = P/V_{\mathrm{MV,dc}}$ and $I_{\mathrm{LV,dc}} = P/V_{\mathrm{LV,dc}}$, are assumed, the total current flowing through the DC link capacitors can directly be calculated using the total AC link current from (13), where the magnetizing current has to be added for the active bridge (i. e. the MV bridge in the case at hand). Integration of the current waveform gives the charge ripple and from that the capacitance needed to fulfill the voltage ripple requirement can be calculated. The capacitor volume is estimated assuming a constant volume per capacitance for a given technology and voltage range, which is found to be $0.41\,\mathrm{cm^3/\mu F}$ from averaging the values for 1.3 kV film capacitors from different manufacturers. DC link capacitor losses are calculated from the rms current and the ESR of the capacitors.

D. Transformer

The MF transformer is a core component of an isolated DC/DC converter. An existing optimization tool was used to optimize transformers for a given boxed volume. This tool considers different core materials, winding arrangements, etc. It would exceed the scope of this paper to fully describe the transformer optimization procedure, however, it will be matter of further publications.

For the transformer cooling, a heat transfer coefficient of $\alpha = 15\,\mathrm{W/m^2K}$ for free convection cooling is assumed [26] and designs that result in losses that could not be removed through the transformer surface for a maximum permissible surface temperature of 100 °C at 50 °C ambient temperature are dismissed.

E. Resonant Capacitors

The transformer stray inductance, L_σ, is one of the output parameters of the transformer optimization loop. Together with the desired resonance frequency f_0, and neglecting the influence of the DC link capacitors, this defines the required series capacitance value as

$$C_{\mathrm{r}} = \frac{1}{4\pi^2 f_0^2 L_\sigma}. \tag{19}$$

Realization of C_{r} by capacitors of proper capacitance on both sides of the transformer as shown in Fig. 7 is considered in order to prevent a DC magnetization of the transformer. The losses and the required volume are estimated in the same way as described above for the DC link capacitors.

V. η-ρ Pareto Optimization

The possibility of modeling the behavior of the stored charge in the IGBT enables estimating switching losses also for the conditions found in the HC-DCM-SRC. This is a requirement for performing a comprehensive η-ρ Pareto optimization [18] of the HC-DCM-SRC, which is described in this section.

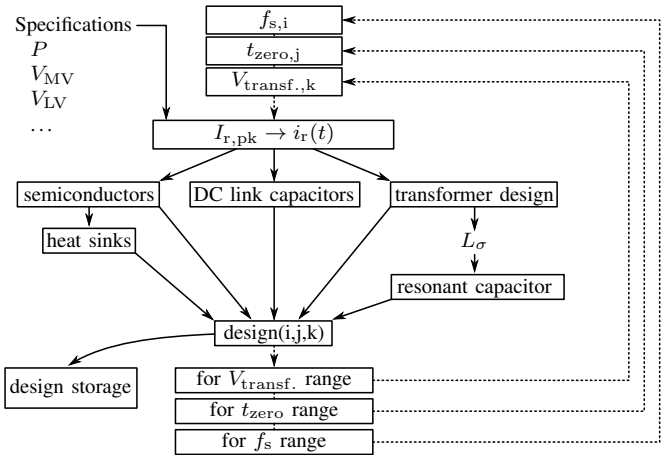

Fig. 15. Visualization of the procedure that calculates the design points used to find the Pareto front shown in Fig. 16.

Using the modeling approach described above, a set of designs can be obtained by sweeping switching frequency, current zero interval duration and admissible transformer volume. The procedure is illustrated by Fig. 15. Each combination of these three parameters results in a specific design. The total losses of a design are given by the sum of individual component losses and the total component volume is given by the sum of the individual component volumes. In [18] it is suggested to account for form factor mismatches between components and inevitable empty spaces within a real converter with a coefficient $C_{\mathrm{P}} = 0.5 \ldots 0.7$ that relates the total volume, V_{t}, to the sum V_{c} of component volumes as $V_{\mathrm{t}} = V_{\mathrm{c}}/C_{\mathrm{P}}$.

From the volume and the power loss, the efficiency $\eta = 1 - P_{\mathrm{loss}}/P$ and the power density $\rho = PC_{\mathrm{P}}/V_{\mathrm{c}}$ can be calculated directly and thus each design corresponds to a point in the $\eta\rho$-plane as shown in Fig. 16, where colors are used to indicate the designs' switching frequencies. An immediate conclusion from Fig. 16 is that switching frequencies higher than about 10 kHz do not contribute anymore to volume reduction because the required heat sink size as a result of increasing switching losses does outweigh the reduction in size of passive components.

The achievable power density depends on the cooling concept. It would for example be possible to include a local optimization of a forced-air cooled heat sink into the overall optimization loop, which would result in a higher CSPI value and consequently shift the design points to the right, i. e. would increase the power density for a required efficiency. Also, considering a more advanced thermal management for the transformer (corresponding to an increase of α) would influence the specific position of the design points in the $\eta\rho$-plane.

It is in general also possible to calculate a Pareto front for a more specific design, where for example the arrangement of the components with respect to each other, various other constraints as well as additional variables such as costs could be considered. Furthermore, more detailed models for the individual components could be employed, however, at the cost of increased computation time.

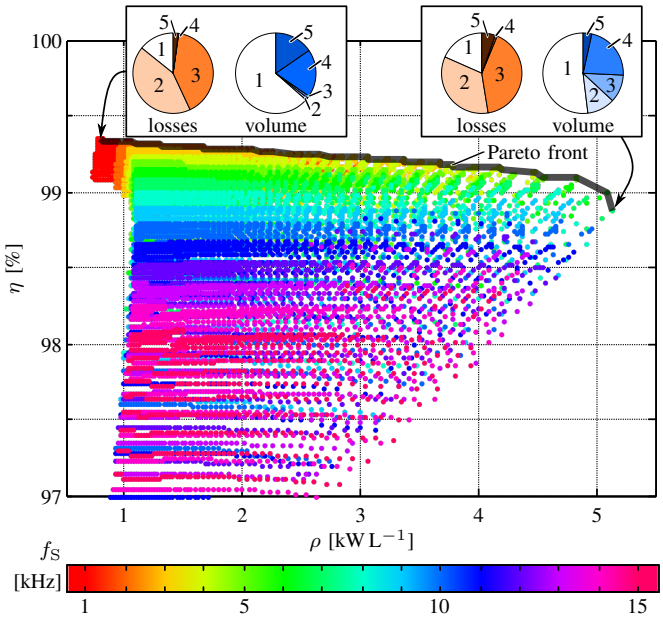

Fig. 16. Resulting designs in the $\eta\rho$-plane with $C_{\mathrm{P}} = 0.7$; the Pareto front is highlighted and relative loss and volume distribution for the two extreme points of the Pareto front are shown: 1) transformer, 2) LV semiconductors, 3) MV semiconductors, 4) DC links, 5) resonant capacitors.

A Pareto optimization is thus a very suitable tool for investigating the performance limits of a given converter topology, operating mode and components' technology [18] as well as for finding a feasible tradeoff between efficiency, power density and possibly other performance indices when designing a specific system.

VI. Conclusion

The HC-DCM-SRC ideally behaves as a "DC transformer" with respect to its input and output DC terminals by providing isolation and fixed voltage transfer ratio, which makes it a very interesting converter for high-power as well as low-power applications. In addition, very low switching losses can be achieved because ZCS for all switches is possible.

However, converter losses introduce a slight load dependence of the input/output DC voltage ratio. A small-signal model that represents this steady-state behavior of the HC-DCM-SRC as well as its dynamic behavior has been described. It represents a suitable way to include the DC/DC stage in a larger model of a complete SST system.

A detailed model for the behavior of the stored charge in the semiconductors has been verified for the conditions found in the HC-DCM-SRC. This allows for estimating switching losses and evaluating several methods to reduce these losses. Furthermore, it facilitates a comprehensive efficiency versus power density trade-off analysis resulting in the η-ρ Pareto front of the HC-DCM-SRC.

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