A 120 °C Ambient Temperature Forced Air-Cooled Normally-off SiC JFET Automotive Inverter System

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***Abstract*—The degree of integration of power electronic converters in current hybrid electric vehicles can be increased by mitigation of special requirements of these converters, especially those regarding ambient air and cooling fluid temperature levels. Today, converters have their own cooling circuit or are placed far away from hot spots caused by the internal combustion engine and its peripheral components.**

In this paper, it is shown, how the use of SiC power semiconductors and active control electronics cooling employing a Peltier cooler can help to build an air-cooled inverter system for 120 °C ambient temperature. First, a detailed analysis shows, how the optimum junction of this high temperature system can be calculated. Then, the operating temperature ranges of power semiconductors, thermal interface materials, capacitors and control electronics are investigated, leading to a comprehensive analysis of mechanical concepts for the inverter system in order to show new ways to solve electrical and thermal trade-offs. In particular, the operation of the signal electronics and the gate driver for power semiconductors with a junction temperature of 250 °C within the specified operating temperature range is ensured by appropriate placement and cooling methods while taking the electrical requirements for limits on the wiring inductances and symmetry requirements into account. The analysis includes an accurate thermal model of the converter and an optimized active cooling of the signal electronics using a Peltier cooler.

Finally, a hardware prototype with discrete power semiconductor devices and thus with a junction temperature limit of 175 °C driving high speed electrical machines is shown to validate the theoretical considerations in a custom designed high temperature test environment.

***Index Terms*—Automotive applications, automotive electronics, electronics cooling, high-temperature techniques, inverters, JFET switches, silicon carbide**

I. Introduction

Power electronic converters are used in Hybrid Electric Vehicles (HEVs) to drive the electrical machine in the vehicle's drive train or to supply electrical energy to loads on different voltage levels from a high voltage traction battery. Today's converters for HEVs feature silicon (Si) power semiconductors which corresponds to the state of the art of power electronics in the vast majority of application areas. Si though has a high intrinsic charge carrier concentration which increases further with temperature due to random thermal motion of Si atoms leading to broken interatomic bonds such that intrinsic conduction begins at a certain threshold temperature (which depends on the blocking voltage rating of the device). Thus, the junction temperature of high voltage Si semiconductors is typically subjected to an upper temperature limit between 150 °C and 175 °C [1].

In order to effectively remove the heat dissipated by the power semiconductor switches, a sufficiently large temperature difference between the semiconductor junction, where the switching and conduction losses of the switches occur, and the coolant has to be maintained. That is, the temperature of the coolant for the power electronic converter based on Si semiconductors has to be well below the temperature level of the cooling circuit of the internal combustion engine (ICE) and thus today two separate water-ethylene-glycol circuits are needed. The temperature of this low temperature cooling circuit is typically around 65 °C [2]. The hybrid models of the Volkswagen Touareg (model year 2010), Porsche Cayenne (model year 2010) and Panamera (model year 2011) [3], [4] as well as previous and actual generations of the Toyota Hybrid Synergy Drive (*cf.* Fig. 1) used for most of the Toyota and Lexus HEVs [5]–[8] can be given as industrial examples of this concept.

With silicon carbide (SiC), a group IV compound semiconductor material, a new option has become available, that can be used for power semiconductor switches [9]. Up to the melting point of Si at 1410 °C, the intrinsic charge carrier concentration of SiC is always lower than the respective value for Si which is mainly due to the larger band-gap of SiC compared to Si. At 995 °C, 4H-SiC reaches the intrinsic charge carrier concentration Si shows at 175 °C. Compared to Si, SiC switches are thus capable of significantly higher operating temperatures of (theoretically) more than 400 °C [10].

Junction temperatures exceeding today's limit of 175 °C of course affect the efficiency of the converter due to rising losses with increasing temperate as will be shown in Section II and require significant advancements in the packaging of power semiconductors. Novel joining and bonding technologies such as low temperature sintered silver die attachment and copper bonding instead of aluminium bonding are currently investigated and promise considerably improved reliability for thermal cycling with increased temperature swing [11]–[13].

The benefit of a higher junction temperature of power semiconductors in converters for HEVs is the chance to make the separation of the cooling circuits obsolete as the

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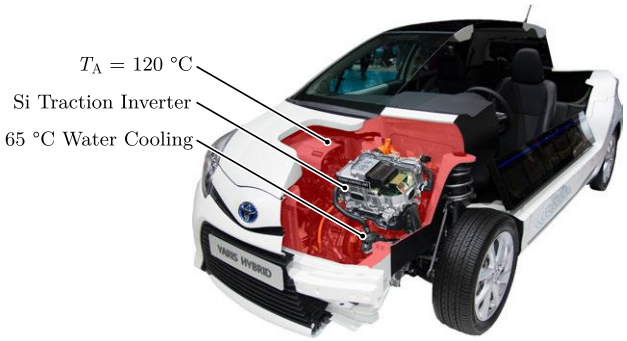


Fig. 1. Toyota Hybrid Synergy Drive in a Yaris Hybrid of the model year 2012: Industrial example of a traction inverter with Si IGBTs which is placed under the engine hood with ambient temperatures up to 120 °C and hence requires a low temperature water cooling circuit. (Photograph taken at the world premiere of the Toyota Yaris Hybrid at the 82nd Geneva International Motor Show in March 2012.)

junction temperature can be increased beyond 175 °C and thus a significant temperature difference to the ICE coolant at 120 °C can be established which is increasingly highlighted by car manufacturers such as Toyota [2], [14], [15]. Hence, some high ambient temperature converter concepts with SiC have been presented in the literature [16]–[20] and research centers of car manufacturers work on the production of SiC devices [21], [22].

Furthermore, alternative cooling concepts such as pure air-cooling even in hot environments (the ambient temperature underneath the engine hood can heat up to 120 °C, *cf.* Fig. 1) become feasible. Ambient-air-cooled converter systems can reduce the overall system complexity compared to water cooling as pumps, water pipes, the water-ethylene-glycol fluid itself and heat exchangers are not needed any more. For this reason, other components of the electrical drive train, e.g. the traction battery, are already air-cooled. This can significantly increase the flexibility in arranging the converters within the vehicle, helping both, to turn conventional models into HEVs and to develop novel car concepts [23], [24].

Accordingly, air-cooled power electronic converters can already be found in current HEVs, e.g. in the 2006 Honda Civic Hybrid model. As these drive inverters still feature Si power semiconductors, the ambient air used for cooling needs to be of low temperature. Hence, the gain in arrangement flexibility is not as high as with SiC because they cannot be placed, for example, in the engine compartment: For the Honda Civic, the drive inverter is placed behind the rear seat to ensure a low ambient air temperature level [25], [26] — in contrast to many other HEVs, such as the Toyota or Lexus hybrid models, where the low-temperature-water-cooled converter is placed in the engine compartment. Additionally, placing the drive inverter close to the electrical machine (which means for many of today's HEVs in the engine compartment) is favorable in terms of electromagnetic interference (EMI) issues as the switched high voltages do not need to be transmitted for a long distance within the car.

For automotive components, weight and volume are further key performance indicators. Especially for vehicles that are offered as both conventional and hybrid electrical vehicles, the additional volume and weight introduced by the components of the electrical part of the drive train should not affect the vehicle characteristics or performance such that the advantages of having two propulsion systems turn into a disadvantage at the end of the day when customers compare the hybrid model to its direct conventional counterpart. As with today's technology the traction battery needed for the hybrid alternative adds a significant portion of weight and volume compared to conventional vehicles, it is even more important for the other main components of the hybrid type such as the power electronics (and the electrical machine) to be as lightweight and small as possible for a given output power.

To reduce weight and volume of the electrical machine, a trend towards electrical machines for HEVs with higher rotational speeds and a reduction gear can be observed [27]. A high speed electrical machine requires the dc-ac inverter to drive the machine with an ac current having a frequency f_o that at least equals the rotational speed n_m of the machine. With a higher number of pole pairs, the required output frequency f_o rises accordingly. A high converter output frequency f_o makes a high switching frequency of the power semiconductors necessary for a sinusoidal output current which is desired to reduce the losses in the machine caused by the harmonic content of the current fed into the machine [28].

Hence, in this paper, a compact three-phase dc-ac inverter system for HEVs using SiC semiconductors is investigated in detail that is directly cooled with ambient air of up to 120 °C and thus offers a significantly increased flexibility regarding its mounting location without the need for a complex and costly water cooling circuit. The switching frequency of 50 kHz of the converter system covers a wide speed range for electrical machines employed in HEVs and keeps the volume and weight of passive filter components, such as common mode inductances, low. It also allows to extend the potential area of application to other industrial sectors where high speed drives are employed.

Besides the SiC power semiconductors, further critical components needed for the realization of the high temperature converter system as shown in Fig. 2 are identified in this paper: The specific temperature ranges as well as functional requirements of dc-link capacitors, current, voltage and temperature measurement, control electronics, auxiliary power supplies and heat sinks with fans to cool the power semiconductors. The main challenge in designing the inverter system for an ambient temperature of 120 °C and a maximum junction temperature of 250 °C, addressed in this paper, is to make sure that the individual devices are operated within their specified temperature ranges by placing and, if necessary, active cooling of the components [29]. The specifications of the converter system are summarized in Table I.

In Section II, basic considerations on the optimum junction temperature for SiC devices are shown and lead to the choice of a maximum design junction temperature of 250 °C for the investigated inverter system. After a short overview over the allowed operating temperatures of the different components in Section III, the inverter system is designed in Section IV and possible placing solutions of the power semiconductors, the heat sinks, the fans, the control electronics and the DC-

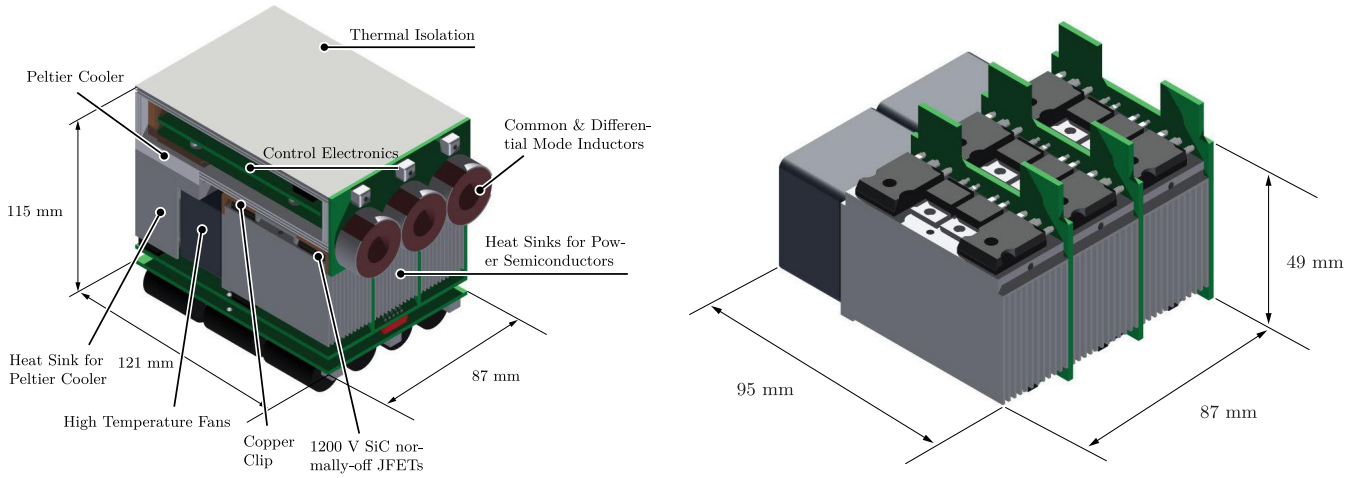


Fig. 2. (a) CAD representation of the complete investigated inverter. The overall volume including dc-link capacitors and active control electronics cooling is 1.2 l. (b) CAD representation of power part of the inverter system with a volume of 0.4 l (including the fans).

link capacitors are analyzed with respect to power density and modularity. It is shown that in any case an active cooling of the control electronics is needed. The optimization of the design of the Peltier cooling with respect to volume and power consumption is shown in Section V using a detailed thermal equivalent circuit diagram. In Section VI, the theoretical considerations are verified in a custom developed test environment by a demonstrator system with discrete power semiconductor devices and thus with a junction temperature limit of 175 °C.

II. Maximum Junction Temperature of SiC Power Semiconductor Devices

As outlined in Section I, the maximum junction temperature limit for today's high voltage power semiconductor devices made of Si is around 175 °C. In the design process of a power electronic converter, typically the loss-relevant converter specifications, e.g. switched current and voltage as well as switching frequency, lead together with the Si junction temperature limit to the selection of the employed power semiconductors and the design of a cooling system.

Not considering semiconductor device packaging related issues for the following analysis, the significantly higher allowable junction temperatures of SiC devices raises the question, how the additional degree of freedom can be taken into account for a safe and optimum (in terms of utilization of semiconductor area) converter design. With the help of Fig. 3, it is shown in this section, that there is a temperature limit for semiconductor devices, that is not mainly given by material parameters like the intrinsic charge carrier concentration, but by the loss behaviour of the device and the cooling system of the converter. Measured on-state and switching losses of four paralleled 1200 V normally-off SiC JFETs [30] and the following system specifications for an 2-level 3-phase inverter form the basis of Fig. 3:

- The ambient temperature T_A is around 120 °C for power electronic converters placed under the engine hood of hybrid electric vehicle if they are cooled by ambient air or by the cooling circuit of the internal combustion engine (*cf.* Section I).
- A high dc-link voltage V_dc on the one hand helps to minimize the current for a certain power level so that the ohmic losses — which are proportional to the square of the current rms value — in the switches, supply lines and the electrical machine can be decreased. On the other hand, a high dc-link voltage adds to the problem of capacitively coupled bearing currents which can reduce the lifetime of the bearings. The choice of V_dc also depends on the maximum voltage that can be applied to the electrical machine. Accounting also for potential partial discharge issues in the machine, V_dc is chosen to 700 V for this inverter system.
- The switching frequency f_S is specified depending on requirements regarding EMI filtering, harmonic losses in the electrical machine and the desired rotational speed of the electrical machine. Here, f_S is chosen to 50 kHz.
- The thermal resistance $R_\mathrm{th,JA}$ from the power semiconductor junction to the ambience is determined by the particular package configuration. Furthermore, it will not stay constant for different die sizes A_d as the heat spreading of several small dies is better than that of a single larger die. Hence, a correlation between $R_\mathrm{th,JA}$ and the die area A_d is required for precise results. This

TABLE I
Overview over dc-ac converter system specifications.

Compact High Temperature / Output Frequency Automotive Inverter	
Maximum Inverter Output Power	10 kW
Maximum Ambient Temperature	120 °C
Maximum Power Semiconductor Junction Temp. (for first prototype with discrete devices)	175 °C
Maximum Power Semiconductor Junction Temp. (for design process)	250 °C
DC-Link Voltage	700 V
Blocking Voltage of SiC Power Semiconductors (normally-off JFETs and diodes)	1200 V
Switching Frequency	50 kHz

can be obtained by measuring or simulating the package configuration with different die sizes. A curve fitting algorithm using the correlation

$$R_{\mathrm{th,JA}}(A_{\mathrm{d}}) = \frac{a_{R\mathrm{th}}}{A_{\mathrm{d}}^{b_{R\mathrm{th}}}} \tag{1}$$

usually gives good fitting results because for very small die sizes, the thermal resistance approaches infinity, and for die sizes close to the maximum (i.e. a size equal to the area of the surface where the dies are soldered onto and that is feeding the heat into the cooling system) $R_{\mathrm{th,JA}}$ reaches its minimum. The constants $a_{R\mathrm{th}}$ and $b_{R\mathrm{th}}$ are positive real values. For the exemplary calculations using the 1200 V SemiSouth normally-off SiC JFET, 4 dies are connected in parallel for each switch leading to an estimate of $R_{\mathrm{th,JA}} = 1\,\mathrm{K/W}$.

The solid black straight line in Fig. 3(a) is the characteristic of the cooling system. It cannot dissipate any power, if the junction temperature T_{J} equals the ambient temperature T_{A}. With increasing temperature difference between the power semiconductor junction and the ambience, the power that can be dissipated increases linearly with $1/R_{\mathrm{th,JA}}$. (Actually, a constant $R_{\mathrm{th,JA}}$ is only an approximation as it is not completely temperature independent due to temperature dependent material properties, e.g. the thermal conductivity or the density of the cooling fluid.)

The solid red lines represent the losses in one of the six inverter switches (in this example each made of four paralleled 1200 V normally-off SiC JFETs, in contrast to the inverter design shown in Section IV-A where two dies are paralleled in one single package for each of the six inverter switches) for the specifications mentioned in terms of V_{dc} and f_{S} and for two different drain current levels, $I_{\mathrm{D,max,n\text{-}off}}$ and $I_{\mathrm{D,submax,n\text{-}off}}$. The intersections between the cooling system characteristic and the temperature dependence of the loss characteristic for a given drain current define steady-state operating points. The first intersection at $T_{\mathrm{J,submax,n\text{-}off}} = 230\,^{\circ}\mathrm{C}$ for $I_{\mathrm{D,submax,n\text{-}off}}$ is the only thermally stable operating point for this current level.

For disturbances like, e.g. a short deviation in the current level or ambient temperature, the operating point will always return to this intersection: If the junction temperature decreases due to such a short disturbance, the power loss is higher than the power that can be dissipated by the cooling system. This difference in power flow will heat up the power semiconductor junction. If the junction temperature is higher than $T_{\mathrm{J,submax,n\text{-}off}}$ due to a disturbance, the power loss is lower than the heat transferred by the cooling system, and hence, the junction cools down back to $T_{\mathrm{J,submax,n\text{-}off}}$.

With the same reasoning, it can be shown, that the second intersection of the cooling system characteristic and the curve for $I_{\mathrm{D,submax,n\text{-}off}}$ at $T_{\mathrm{J}} = 640\,^{\circ}\mathrm{C}$ is inherently unstable. A small disturbance causing a lower junction temperature will lead to a continuously decreasing temperature until $T_{\mathrm{J,submax,n\text{-}off}}$ is reached, a disturbance leading to a higher junction temperature will heat up the semiconductor until it is thermally destroyed ("thermal runaway") because the loss curve and the cooling system curve do not have another intersection. (After thermal breakdown, it conducts zero drain current and has no more power loss corresponding to an intersection with the cooling system characteristic and an "operating" point at $T_{\mathrm{J}} = T_{\mathrm{A}} = 120\,^{\circ}\mathrm{C}$.)

The dark gray curve in Fig. 3(a) for $I_{\mathrm{D,max,n\text{-}off}}$ corresponds to the maximum rms drain current that the device is able to conduct in steady state operation without thermal runaway: For higher currents, there would be no intersection with the cooling system characteristic. Accordingly, a thermal runaway could occur. Therefore, the drain current level must always remain below this level. Fig. 3(b) illustrates this fact by plotting directly the rms drain current over the junction temperature, one curve for the mentioned normally-off SiC JFET and for a normally-on SiC JFET to show the influence of the switch characteristic on the drain current temperature behaviour.

This leads directly to the conclusion, that all stable operating points lie between $T_{\mathrm{J}} = T_{\mathrm{A}}$ and $T_{\mathrm{J}} = T_{\mathrm{J,max,n\text{-}off}}$ and hence $T_{\mathrm{J,max,n\text{-}off}}$ constitutes the operating junction temperature limit [31], [32]. A reduction of only 10% from the maximum drain current $I_{\mathrm{D,max,n\text{-}off}}$ to $I_{\mathrm{D,submax,n\text{-}off}}$ furthermore brings a large reduction in junction temperature, which significantly improves the reliability and the efficiency. (With Si, the considerations are exactly the same. However, for typical converter designs, the 175 °C material temperature limit is below the temperature limit for thermal runaway.)

Hence, the inverter system investigated in this paper is designed for a maximum junction temperature of 250 °C.

III. Operating Temperature Ranges of Inverter Components

To consider different inverter designs and possible options for placing the components, it has to be analyzed first, for which temperature levels the components needed are available. Fig. 4 gives an overview over the operating temperature ranges. Often, there are devices for specialized industries such as military, downhole or aerospace applications available that have partially significantly extended operating temperature ranges at the expense of reduced performance or functionality. The high temperature power FET technology by Honeywell can exemplify this: The n-channel FET is fabricated using a SOI process in order to reduce the leakage currents at high temperatures. The device is rated up to 225 °C, i.e. the device shows a significantly higher upper temperature limit than conventional Si power semiconductors [33]. Disadvantageous are the higher component costs and the derated performance of the device, e.g. in terms of the die area specific on-resistance, which is with $43\,\mathrm{m\Omega cm^2}$ in the same range as the specific on-resistance of conventional Si power semiconductors, that have an order of magnitude higher blocking voltage (55 V compared to 650 V) [34]. Against the background of industrial practicability, therefore, no special components with derated performance will be chosen for this inverter system.

IV. Inverter Design with Active Electronics Cooling

The first prototype of the inverter system is designed for and built with discrete power semiconductor devices with an

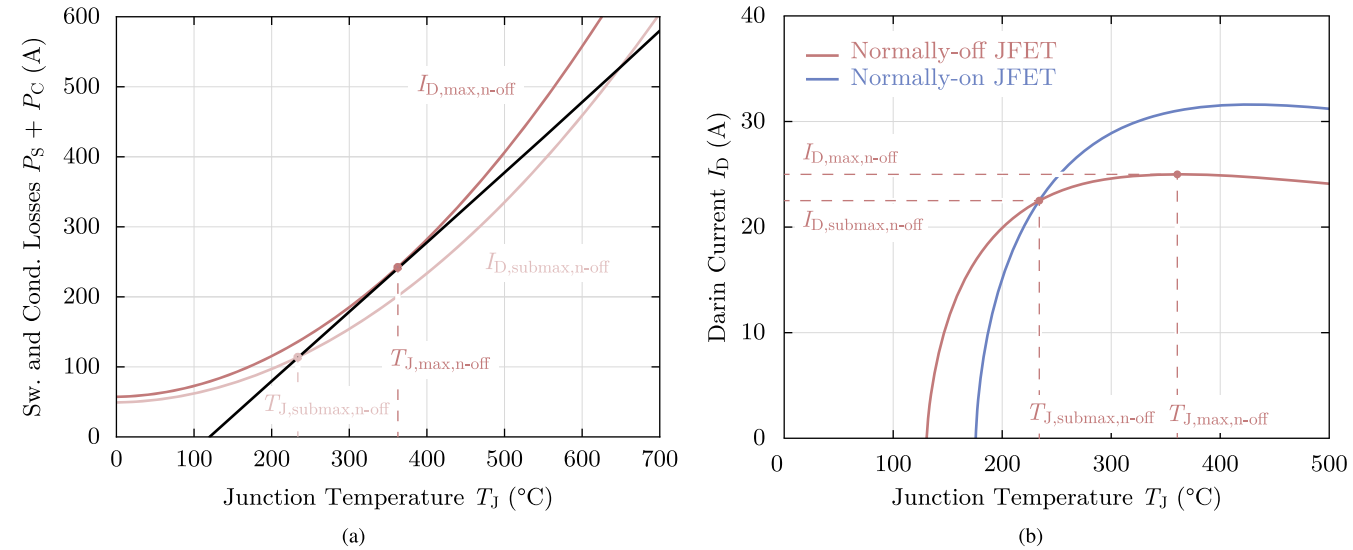


Fig. 3. Illustration of the "thermal runaway" phenomenon setting a junction temperature limit to the operation of SiC power semiconductor devices: (a) The actual junction temperature depends on the drain current in steady state operation and can be found as intersection between the cooling system characteristic (straight black line) and the loss characteristics of a semiconductor switch for different drain currents (red lines). All thermally stable operating points are located below $T_{J,max,n\text{-}off}$ on the characteristic of the cooling system. The same information is shown in (b) where the drain current of one of six switches of the inverter is shown. The drain current that the switch can carry reaches its maximum at $T_{J,max,n\text{-}off}$ and decreases with higher junction temperatures.

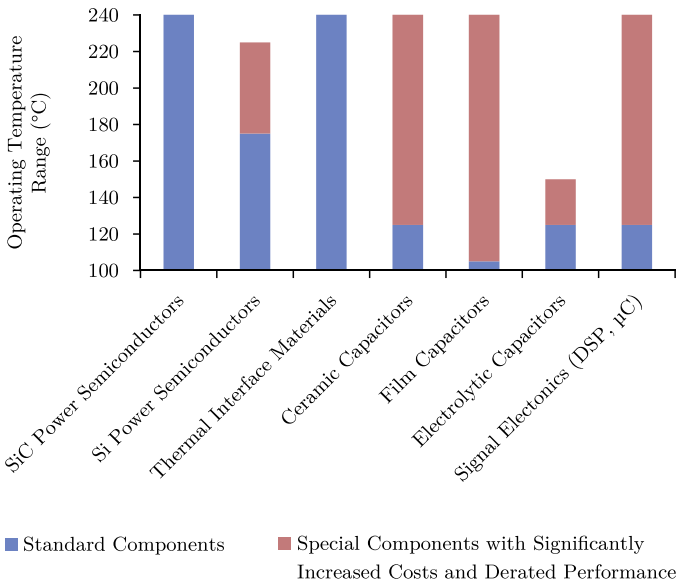


Fig. 4. Overview over operating temperature ranges of the main components of the investigated inverter system. The significantly derated performance of special components refers to the much higher on-resistance of silicon-on-insulator-type Si power semiconductors, the much lower energy density of high temperature capacitors or the limited signal processing capability of high temperature DSPs.

upper junction temperature limit of 175 °C in Section IV-A. Therefore, the system will be operated either at the nominal ambient temperature of 120 °C with reduced output power or at the nominal power level of 10 kW at reduced ambient temperature. The power level is chosen to 10 kW as this allows laboratory testing on the one hand and scaling the power up to larger values using the same generic concepts on the other hand. The arrangement of the main components and the thermal design of the encapsulation of the control and gate drive electronics is conducted for power semiconductors with junction temperatures up to 250 °C, as will be shown in Section IV-C. This makes it possible to replace the discrete power semiconductors with a customized power semiconductor module having a junction temperature limit of 250 °C while maintaining the concepts developed in this paper.

A. *Power Semiconductors*

The instantaneous value of the output phase current i_{ph} is either carried by the high-side or the low-side switch (instantaneous current i_D, *cf.* Fig. 5). During steady state converter operation, the rms current values of the high- and low-side switches are the same for symmetric modulation schemes. Apart from currents charging the parasitic capacitances of the switches during the switching transients, the switches do not conduct currents at the same time and hence

$$I_D = \frac{I_{ph}}{\sqrt{2}} \tag{2}$$

applies for the rms values.

The correlation between the real output power P_o of the 3-phase inverter and I_{ph} is

$$P_o = 3 \cdot V_{ph} I_{ph} \cos \Phi, \tag{3}$$

where V_{ph} denotes the rms value of the output phase voltage and $\cos \Phi$ the phase shift between V_{ph} and I_{ph}.

PWM modulation with third harmonic injection or space vector modulation leads to a maximum modulation index of $m_{max} = 2/\sqrt{3}$ without overmodulation and thus, the maximum amplitude $\hat{V}_{ph}$ of the phase voltage fundamental is

$$\hat{V}_{ph} = m_{max} \cdot \frac{V_{dc}}{2} = \frac{2}{\sqrt{3}} \frac{V_{dc}}{2} \tag{4}$$

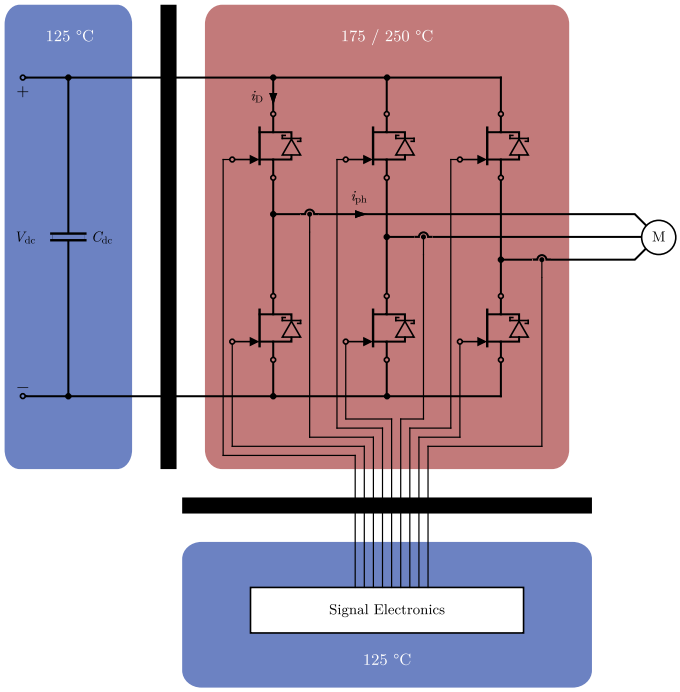


Fig. 5. Concept of thermal design of high temperature inverter system: The dc-link capacitors with an upper temperature limit of 125 °C are thermally isolated from the hot power semiconductors (junction temperature up to 250 °C) by placing them below the heat sinks (distance: 45 mm). The control electronics need to be very close to the gate connections of the switches to allow fast switching and low switching losses. Thus, a special thermally isolating material is used to isolate the control electronics from the hot switches. Additionally, the signal electronics are actively cooled by a Peltier cooler.

with V_{dc} being the dc-link voltage of the voltage source inverter. In order to supply the output power P_{o} at this voltage, a phase current I_{ph} according to

$$I_{\mathrm{ph}} = \frac{P_{\mathrm{o}}}{\sqrt{3}\frac{V_{\mathrm{dc}}}{\sqrt{2}}\cos\Phi} \tag{5}$$

(*cf.* (3)) has to be impressed. With (2), this results in a rms current of each switch of

$$I_{\mathrm{D}} = \frac{P_{\mathrm{o}}}{\sqrt{3}V_{\mathrm{dc}}\cos\Phi} = 10.3\,\mathrm{A} \tag{6}$$

with an assumed displacement power factor of $\cos\Phi = 0.8$ for a high-speed permanent magnet synchronous machine as employed on the test bench in Section VI.

The normally-off JFET is available in a TO-247 discrete package with either a single $4.5\,\mathrm{mm}^2$ die having a nominal on-resistance of $100\,\mathrm{m\Omega}$ at 25 °C or two dies of the same size in parallel cutting also the on-resistance in half [35], [36]. For this design, the $50\,\mathrm{m\Omega}$ switch is chosen as this promises increased efficiency while keeping the package and thus volume constant.

The switches are operated at their specified maximum junction temperature of 175 °C. For a drain current of 10 A, the measured drain-source on-resistance of a switch with $37\,\mathrm{m\Omega}$ at 25 °C and a gate current of 25 mA increases at 175 °C to $113\,\mathrm{m\Omega}$ despite a gate current of 100 mA. As the maximum specified on-resistance of these switches is with $50\,\mathrm{m\Omega}$ at room temperature 35% higher than for the measured switch, this additional margin has to be considered for the conduction loss calculation in order to make sure, that this calculation covers the highest possible on-resistance of the switch leading to $R_{\mathrm{DS,on}} = 153\,\mathrm{m\Omega}$. Hence, the conduction losses for one of the six switches in the inverter under full-load condition at 175 °C can be calculated to

$$P_{\mathrm{C}} = I_{\mathrm{D}}^2 \cdot R_{\mathrm{DS,on}} = 16\,\mathrm{W}. \tag{7}$$

The total switching energy E_{S} for a switch in a half-bridge setup with an inductive load is measured for different junction temperatures, dc-link voltages, and load currents. As the output phase current and hence also the current switched by one of the six switches varies sinusoidally, the switching losses for one switch can be calculated by integrating the switching losses of a single pulse period over one half-wave of the output current,

$$\begin{aligned} P_{\mathrm{S}} &= \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\Phi}^{\frac{\pi}{2}+\Phi} E_{\mathrm{S}}(i_{\mathrm{D}}, T_{\mathrm{J}}) f_{\mathrm{S}}\,\mathrm{d}\varphi \\ &= h_E(T_{\mathrm{J}}) f_{\mathrm{S}} \left(\frac{1}{2}a_E + \frac{1}{\pi}\hat{I}_{\mathrm{ph}} b_E + \frac{1}{4}\hat{I}_{\mathrm{ph}}^2 c_E\right) = 14\,\mathrm{W}, \end{aligned} \tag{8}$$

where h_E is a second-order-polynomial representing the dependency of the switching energies on the junction temperature, and a_E, b_E, and c_E are the constant zeroth, first and second order coefficients of the second-order-polynomial representing the dependency of the switching energies on the drain current level.

B. DC-link Capacitor

Important characteristics of the dc-link capacitor for this inverter system include the dc voltage, current ripple and maximum allowable ambient and/or operating temperature as well as the capacitance needed.

A comprehensive study of the available capacitors (foil, ceramic and electrolytic capacitors) for 120 °C ambient temperature reveals, that film capacitors suffer from significant voltage derating (between 4 V/K and 8 V/K) as soon as the temperature rises above 85 °C. If the operating voltage at high ambient temperature is half of the nominal voltage, four capacitors would be needed to achieve the same capacitance as the capacitance is cut in half by a series connection of two capacitors. Ceramic capacitors suffer from a decreasing capacitance at high ambient temperatures and at high dc voltages. Furthermore, they have a low capacitance per device, leading to a high number of devices needed while the reliability of the devices is questioned due to cracks potentially occurring at the caps. With respect to electrolytic capacitors, reduced lifetime especially at elevated temperatures is often seen as disadvantageous. This is particularly the case for many power electronic applications with specified lifetimes of significantly more than 10'000 h [37]. For automotive requirements, the lifetime of properly designed electrolytic capacitors is sufficient. Therefore, electrolytic capacitors are considered for this inverter system.

The required dc voltage rating is given by the dc-link voltage of the inverter system (700 V) and the ambient temperature

of 120 °C defines the operating temperature in a first step. The capacitance is given by the allowed dc-link voltage variation depending on capacitor current and switching frequency, by the duration of a supply failure that has to be compensated as well as the dynamic response of the supply to load variations and is chosen to 50 μF. The most essential parameter for choosing the right electrolytic capacitor is the rms value I_C of the capacitor current, that can be calculated by

$$I_C = \frac{P_o}{\sqrt{3}\frac{V_{dc}}{\sqrt{2}}\cos\Phi}\sqrt{2m\frac{\sqrt{3}}{4\pi}+\cos^2\Phi\left(\frac{\sqrt{3}}{\pi}-\frac{9}{116}m\right)} = 8.4\,\mathrm{A} \tag{9}$$

for $\cos\Phi = 0.8$ and $m = 0.68$, which is the value where the maximum current ripple occurs for $\cos\Phi = 0.8$ [38]. The electrolytic capacitor Epcos B43693A2476 with a capacitance of 47 μF, a rated dc voltage of 250 V and a ripple current capability of 3.38 A at 125 °C is chosen [39]: Three capacitors are connected in series and 4 in parallel, leading to an overall capacitance of 63 μF and 13.5 A rms current carrying capability. The volume consumed by the 12 capacitors is 0.19 l.

C. Arrangement of Main Components

The arrangement of the main components of the inverter system is subject to certain, partially conflicting, electrical and thermal constraints.

First, the setup is required to be symmetrical (identical for each phase) with respect to the gate drive inductances of the three half-bridge legs in order to facilitate equal switching times and hence equal switching losses. The air flow for cooling the power semiconductors has also to be symmetrical to make sure that the thermal resistance of the power semiconductor switches and diodes, respectively, is equal.

Second, the connections between the power semiconductors and the control electronics including the gate driver as well as between the power semiconductors and the dc-link capacitors have to be of very low inductance in order to allow fast switching without excessive gate ringing and to avoid oscillations of the dc-link voltage.

Third, the main components operate at significantly different temperature levels, as can be seen from Fig. 4. The SiC power semiconductor switches and diodes have to be operated at junction temperatures up to 250 °C under full load condition in order to fully utilize them at ambient temperatures of 120 °C (*cf.* Section II). The temperature of the power semiconductor package surfaces that are not attached to the heat sink (i.e. the top side and shoulders of the package) is very close to the junction temperature of the semiconductor as the thermal resistance from this surface to the surrounding air is significantly higher than from the junction to the surface. The upper temperature limit of the control electronics and dc-link capacitors that are available as standard components is 125 °C. Hence, it has to be made sure, that the required temperature drop of 250 °C − 125 °C = 125 K from the power semiconductors to the control electronics and dc-link capacitors is maintained.

Fig. 6 shows two of the considered setups. In Fig. 6(a) the power semiconductors are mounted horizontally on heat sinks with vertical fins, whereas in Fig. 6(b) the switches and diodes are mounted vertically on heat sinks with horizontal fins. The dimensions of both concepts are determined by the footprint of the power semiconductor packages and the height of the cooling fans. The semiconductors of a bridge leg are assembled adjacent to each other in a row, determining the length of the heat sink. The two fans placed in front of the heat sinks match with a width of 80 mm the width of the three bridge legs in Fig. 6.

The PCBs for the control electronics and the dc-link capacitors are mounted on top and underneath the power semiconductors, heat sinks and fans. It is also possible to place both together either on top or underneath the heat sinks. If they are placed at the sides of the heat sinks in parallel to the fins, a symmetrical connection to the three half-bridge legs will not be possible.

In the concept shown in Fig. 6(b), the power semiconductor packages with surface temperatures close to 250 °C are not placed directly underneath the control electronics PCB compared to Fig. 6(a). Furthermore, the air flow generated by the fans makes sure, that the surface of the packages as well as the pins are cooled so that only a negligible amount of heat is fed into the connecting PCB and thus to the gate drivers and dc-link capacitors. Hence, the dissipated power is not directly induced into the control electronics PCB while the gate driver and dc-link parasitic inductances are the same for both concepts.

Finally, Fig. 6(a) is chosen for this inverter system because of the 10% lower thermal resistance of this arrangement for equal overall volume. As can easily be seen, the length of the fins has to be decreased for the version shown in Fig. 6(b) and the baseplate area of the heat sinks is not fully utilized as it is larger (60 mm · 44 mm) than the area consumed by the power semiconductor packages (two TO-247 packages containing each two 4.5 mm² SiC JFET dies and two TO-220 packages containing each a 8 mm² SiC Schottky diode die). Accordingly, the outer fins of the heat sink do not contribute significantly to the cooling. Furthermore, in concept Fig. 6(b), the packages of the power semiconductors including their pins are located directly in the air-flow leading to an increased risk of breakdown caused by small dust particles that might be contained in the air-flow.

In the final concept of Fig. 6(a), the dc-link capacitor board is placed underneath the heat sinks. The bottom end of the heat sinks has a temperature of + 10 K to + 20 K (depending on whether the junction temperature is 175 °C or 250 °C) above ambient temperature level. PCBs with broad (60 mm) and close (distance between a pair of tracks only 0.5 mm) tracks make sure, that the connection has a low parasitic inductance. The thermal management of the control electronics is described in Section V.

D. Design of Power Semiconductor Heat Sinks

An optimum fin geometry can be calculated for the physical dimensions of the heat sink derived in Section IV-C and the fluid dynamic performance of the fan [40]. The results of this optimization for an aluminium heat sink with a width of 80 mm

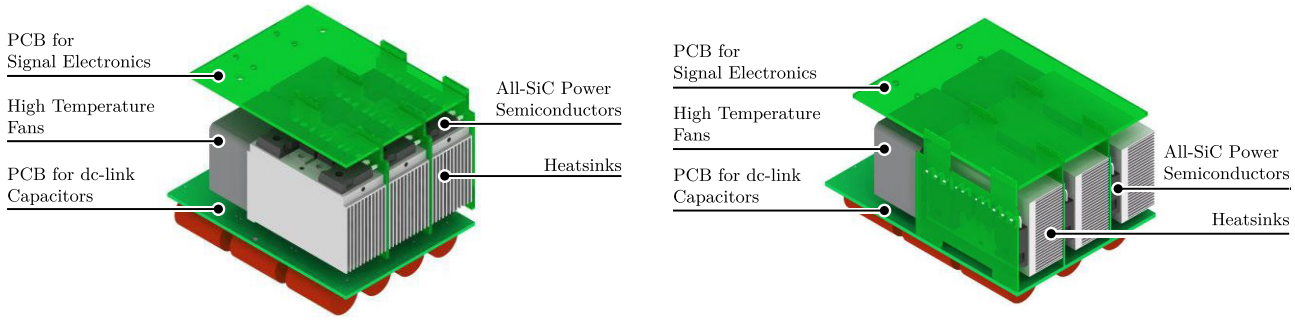


Fig. 6. Considered arrangement of SiC power semiconductors, heat sinks, fans, control and dc-link capacitor PCBs. For the (b) vertical arrangement, the hot power semiconductors are not placed close to the signal electronics in contrast to the (a) horizontal concept. The disadvantage of (b) compared to (a) is the 10% higher thermal resistance for the same overall volume. Hence, the setup according to (a) is chosen for this inverter system.

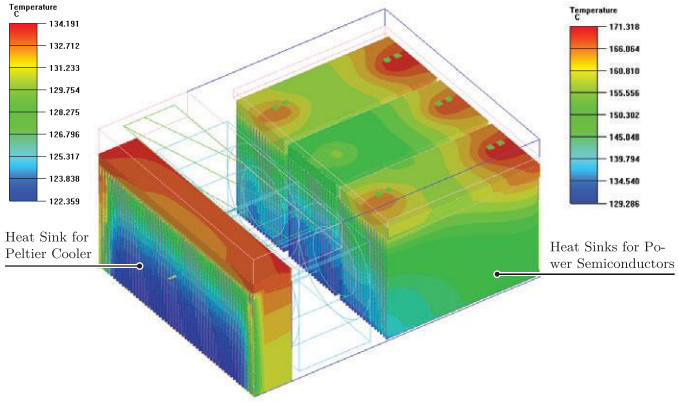


Fig. 7. Thermal simulations of the cooling of the power semiconductors and the Peltier cooler. The ambient temperature is 120 °C, the junction temperature of the power semiconductors is set to 250 °C (relevant operating point for the design of the electronics cooling) and the power dissipated by the Peltier device is 50 W.

(thus matching the cross-section of two fans) and a length of 83 mm (62 mm for the heat sink of the power semiconductors and 21 mm for the heat sink of the Peltier cooler) are as follows: A minimum thermal resistance of 0.14 K/W can be achieved for 46 fins with a thickness of 0.52 mm. Such thin fins can be manufactured by wire eroding. In the case at hand, the heat sinks are milled and thus the thickness is subject to a limit of 0.9 mm to avoid destruction of the fins during machining. The spacing is limited to values larger than 1.6 mm due to the availability of saw blades with a thickness of 1.6 mm and a diameter of more than 40 mm. This leads to 30 fins and a thermal resistance for this heat sink of 0.15 K/W. Due to a rather flat optimum of the thermal resistance, the thermal resistance increases only by 10% even though the number of fins is reduced by a factor of more than 1.5. The thermal resistance of each of the three heat sinks for the power semiconductors depicted in Fig. 6 is then calculated to $3 \cdot \frac{83\,\mathrm{mm}}{62\,\mathrm{mm}} \cdot 0.15\,\mathrm{K/W} = 0.6\,\mathrm{K/W}$. The resulting temperature distribution for the heat sink of the Peltier cooler and the power semiconductor heat sinks is simulated with Icepak and shown in Fig. 7.

V. Signal Electronics Cooling

A. Concept of Signal Electronics Box

For the control electronics with an upper temperature limit of 125 °C, which according to Fig. 6(a) are placed directly above the hot power semiconductors and heat sink baseplate, a thermal isolation and cooling concept is developed. The key ideas are shown in Fig. 8. The hot surface of the power semiconductors as well as their gate and source connections cause a heat input into the control board. Additionally, heat is dissipated by the control electronics (e.g. by the DSP and the gate drivers delivering 100 mA at a voltage level of 3 V to each switch during its on-state). At the same time, it has to be assumed as a worst case scenario in the later arrangement within the HEV, that the converter is encapsulated such that the control electronics experience a very high thermal resistance to the 120 °C ambience. Therefore, the allowed temperature drop is only 5 K, the power that could be conducted to the ambience would be very limited compared to the heat input. Therefore, an active cooling of the control electronics is needed. For this purpose, the control electronics are encapsulated in a thermally isolating box and are cooled to a temperature level of 120 °C by a Peltier cooler. The power extracted from the electronics box and the heat dissipated by the Peltier device is fed into a heat sink. Ambient air (120 °C) is sucked through this heat sink by the fan located in between the heat sinks for the Peltier cooler and the power semiconductors, respectively. Then, the air slightly heated up by the Peltier device heat sink is blown through the heat sinks of the power semiconductors.

To limit the electrical power that has to be fed into the Peltier cooler, the heat induced into the control board has to be minimized. For a detailed analysis of the different heat sources, an equivalent circuit model is shown in Fig. 9. A significant temperature reduction of the top sides of the power semiconductor packages can be achieved by means of copper clips mounted on the packages and attached to the heat sink baseplate (*cf.* Fig. 2(a)). These clips (thickness: 2 mm) cover the top sides and a poor contact area to the packages (e.g. by a rough copper surface or isolating film in between) together with a connection of low thermal impedance to the heat sink makes sure the temperature of the clips is comparable to the temperature of the heat sink baseplate. The clips are

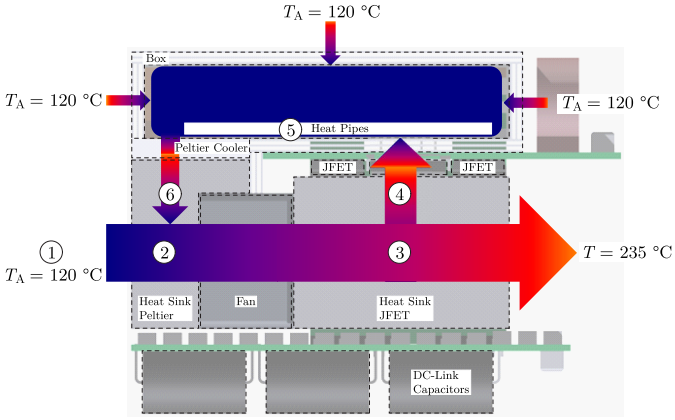


Fig. 8. Illustration of heat flow within the inverter system: Ambient air (120 °C) ① is sucked through the heat sink ② for the Peltier cooler by the fans located in between the heat sinks for the Peltier device and the power semiconductors. Then, the air slightly heated up by the Peltier cooler heat sink is blown through the heat sinks ③ of the power semiconductors. The hot surface of the power semiconductors as well as their gate and source connections cause a heat input into the control electronics box ④; the heat is transferred within the box by horizontal heat pipes ⑤ to the Peltier device ⑥.

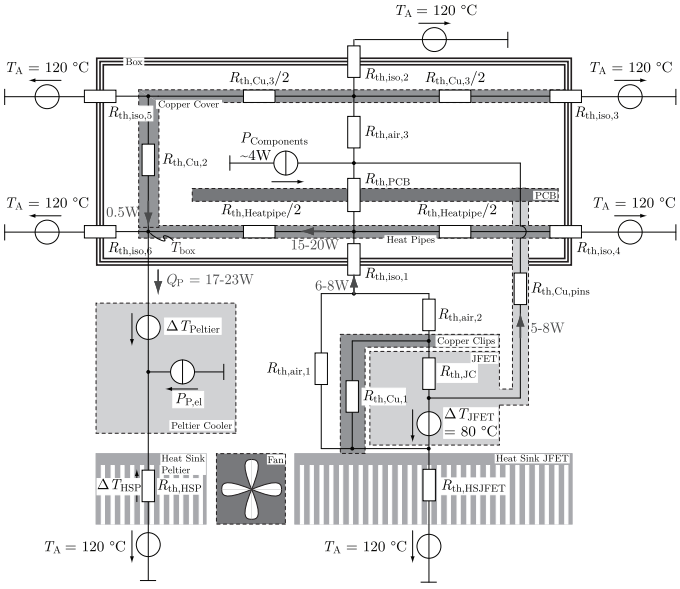


Fig. 9. Equivalent circuit model to calculate the heat induced into the control electronics box (20 W) and to derive a model for the Peltier cooling.

represented in Fig. 9 by $R_{\mathrm{th,cu},1}$.

Furthermore, a thermal isolation material is mounted between the clips and the control electronics PCB (*cf.* Fig. 2(a)). Frenzelit novaplan 02980 sheets with a thermal conductivity of 0.1 W/mK, a temperature limit of more than 1000 °C and a thickness of 0.8 mm [41] are glued together with a distance of 0.8 mm to make use of the good thermal isolation capabilities of air (thermal conductivity: 0.026 W/mK). Loctite 5399 glue with a thermal conductivity of less than 0.3 W/mK and a maximum specified temperature of 275 °C is used [42]. This sandwich construction (total thickness of 4 mm) is also used for the faces of the electronics box. The resulting thermal resistances of the isolation are denoted in Fig. 9 by $R_{\mathrm{th,iso},i}, 1 \leq i \leq 6, i \in \mathbf{N}$.

The heat fed into the electronics box by the pins can be significantly reduced by only feeding the required gate and source connections of the switches into the electronics box with 10 mil narrow, 35 μm thick and 10 mm long tracks ($R_{\mathrm{th,cu,pins}}$ in Fig. 9). This leads to an increase of the thermal resistance of each connection by a factor of 10 (27 K/W for each TO-247 pin compared to 300 K/W for each PCB track). Additionally, the drain and diode pins are interconnected on the vertical PCBs in between the heat sinks (*cf.* Fig. 2) so that only 6 times 1 gate and source connection, 3 times 2 tracks for the current measurement signal and 1 times 2 tracks for the voltage measurement signal (20 in total) need to be fed into the control electronics box. Overall, a total amount of 20 W needs to be pumped out of the electronics box. Including a safety margin, the Peltier cooler is designed in Section V-B for a removal of 30 W out of the electronics box.

As can be seen from Fig. 8 and Fig. 9, the largest portion of heat is fed into the box in the region above the power semiconductors (right hand side). On the left hand side, the Peltier cooler pumps the heat out of the box. To enable an even temperature distribution in the box, heat pipes are soldered on the bottom layer of the PCB in order to thermally short the PCB to the Peltier device. Furthermore, an L-shaped copper cover is soldered to the upper control electronics PCB in order to provide a thermal shielding and a low thermal resistance path to the Peltier cooler.

B. Design of Peltier Cooler for Optimum Cooling

By feeding electrical power P_{el} into the Peltier cooler, heat Q is transported from the cold side of the Peltier cooler to the hot side. At the hot side, the sum $P_{\mathrm{el}} + Q$ has to be fed to a heat sink.

The characteristics of a Peltier cooler are shown in Fig. 10 (solid lines) and include the maximum cooling power (only available at zero temperature difference $\Delta T_{\mathrm{Peltier}}$ between hot and cold side) and the maximum temperature difference ΔT_{max} between the cold and hot side. At a constant supply current, the cooling power decreases with increasing $\Delta T_{\mathrm{Peltier}}$ linearly and is zero at ΔT_{max}. The electrical power P_{el} fed into the cooler is proportional to its supply voltage. With the supply current decreasing, the load line is shifted towards lower cooling power and P_{el} decreases. This can lead to a higher efficiency. Hence, the cooling system is not necessarily smallest at a maximum supply current I_{max}.

With increasing $\Delta T_{\mathrm{Peltier}}$ the cooling power and efficiency of the Peltier cooler decrease. To be able to use a small Peltier cooler, $\Delta T_{\mathrm{Peltier}}$ should be kept at a low level. This makes a small thermal resistance $R_{\mathrm{th,HSP}}$ of the heat sink necessary and thus leads to a bulky heat sink.

On the other hand, with a large $\Delta T_{\mathrm{Peltier}}$, a higher thermal resistance and thus a smaller heat sink is feasible, on the expense of a larger area Peltier cooler. The resulting optimum with respect to the volume of the heat sink can be calculated using a "temperature loop" in Fig. 9,

$$\Delta T_{\mathrm{Peltier}} = T_{\mathrm{box}} - T_{\mathrm{A}} + \Delta T_{\mathrm{HSP}}, \qquad (10)$$

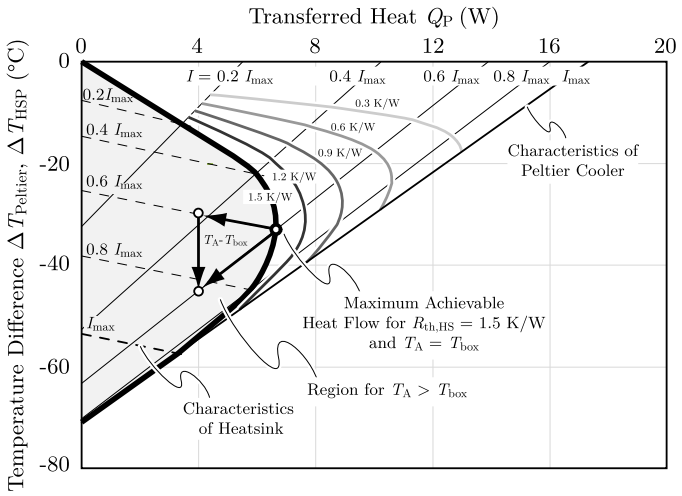


Fig. 10. Characteristic curves of Peltier cooler (solid lines) and heat sink for the Peltier cooler (dashed lines). Intersections (thick solid line) mark the possible operating points where the temperature inside the box is at the same level as the ambient temperature. This front is shifted for different heat sink sizes. The most right point on each front designates the maximum achievable heat flow with a certain heat sink.

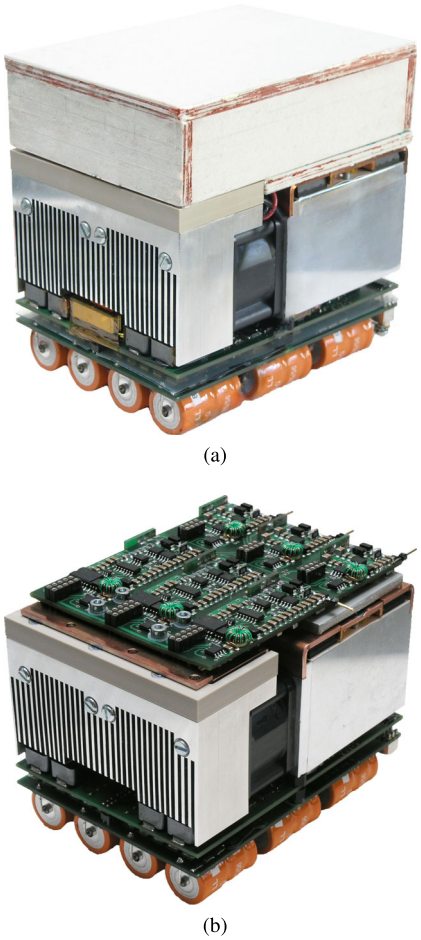
as $T_{box} = T_A = 120\,°C$. P_{el} and Q depend on the chosen Peltier cooler. As similar Peltier devices have comparable characteristics, the calculation is conducted with the single-stage Peltier cooler QC-31-1.4-8.5M manufactured by Quick-cool. The following calculation leads to the total area needed for the Peltier devices. This area can be filled by several smaller Peltier coolers or a single one having the required size.

$R_{th,HSP}$ depends on the fan, the volume of the heat sink and choice of fin geometry. The width and height of the heat sink is given by the choice of power semiconductors and fans (*cf.* Section IV-A). To calculate the power that can be dissipated by the Peltier cooler, the thermal resistance $R_{th,HSP} = 1.5\,\mathrm{K/W}$ of a heat sink having the same size as the Peltier device is determined like for the heat sinks of the power semiconductors (*cf.* Section IV-D). In addition to the characteristic curves depicted in Fig. 10, the characteristic curves of the heat sink (shown as dashed lines in Fig. 10) can be calculated according to

$$\Delta T_{HSP} = R_{th,HSP}\,(Q + P_{el})\,. \tag{11}$$

For this inverter system, T_{box} equals T_A, leading to $\Delta T_{Peltier} = \Delta T_{HSP}$. This corresponds to the intersections of the Peltier and heat sink characteristic curves (thick solid lines in Fig. 10). This front is shifted for different thermal resistances and thus volumes of the Peltier heat sink. Here, the maximum heat flow of 7.5 W can be achieved for approximately $0.6 I_{max}$. With the required total heat flow of 30 W (*cf.* Section V-A), four $20\,\mathrm{mm} \cdot 20\,\mathrm{mm}$ coolers or one $40\,\mathrm{mm} \cdot 40\,\mathrm{mm}$ sized Peltier cooler is needed.

Here, the current of $0.6 I_{max}$ is a fixed value. If the pumped heat is lower (e.g. 4 W instead of 7.5 W for each Peltier cooler), the operating point of the Peltier cooler is shifted away from the intersections line. The smaller amount of heat leads to a smaller temperature drop across the heat sink, but to a larger temperature drop $\Delta T_{Peltier}$ across the Peltier device.



(a)

(b)

Fig. 11. Hardware prototype of the 120 °C ambient temperature forced air-cooled normally-off SiC JFET automotive inverter system (a) with and (b) without the box that thermally isolates the actively cooled control and gate drive electronics from the ambience. The key specifications can be found in Table I.

This causes a temperature difference between the ambient air T_A and the box T_{box} such that the temperature level inside the box is lower. If the pumped heat Q increases to values larger than 7.5 W, the temperature in the box will be higher than the ambient air temperature.

VI. Realization and Experimental Analysis of Inverter System

Fig. 11 shows the hardware prototype of the investigated inverter system. A comprehensive thermal and electrical test environment is built in order to operate the inverter system at 120 °C ambient temperature and to drive electrical machines, both permanent magnet synchronous and induction machines, with the rated inverter power of 10 kW.

The design of the high temperature test environment includes the following considerations and challenges: On the one hand, the high temperature inverter system has to be placed in the thermal test chamber such that the ambient air around the signal electronics as well as the the air which the inverter takes to cool its power semiconductors is heated up to precisely 120 °C before it is blown through the heat sinks by the fans of the inverter. On the other hand, the test environment

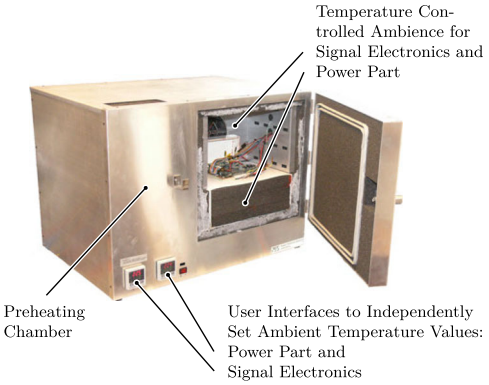


Fig. 12. Photograph of the complete thermal chamber which is used to test the inverter system at 120 °C ambient temperature.

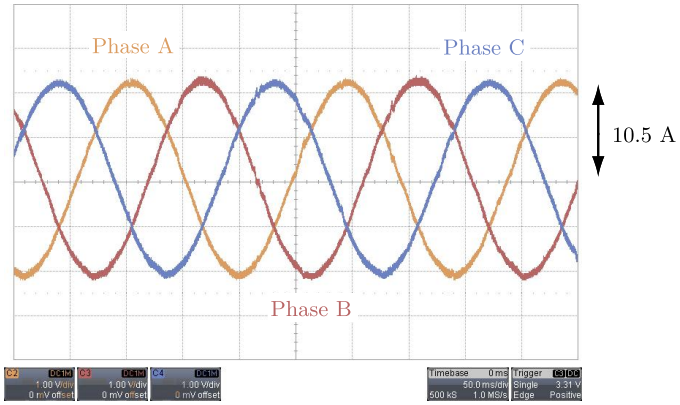


Fig. 14. 3-phase currents of the inverter driving the PMSM. The currents are almost sinusoidal with very low harmonic distortion due to the high inverter switching frequency of 50 kHz.

should at the same time not influence the performance of the inverter system by e.g. introducing an additional pressure drop for the cooling system of the inverter. Furthermore, separating the temperature controls for the ambient air around the signal electronics in the upper part of the converter (*cf.* Fig. 2 and Fig. 11) and the temperature around the power semiconductor heat sinks is helpful for testing purposes.

Fig. 12 shows a photograph of the developed thermal chamber. The inverter is placed in the chamber, and the isolation box covering the signal electronics is removed. The main compartment that can be seen surrounds the signal electronics. The left part of the chamber is used to preheat the air used for cooling the power electronics. The air is heated up and blown into the preheating chamber where the air temperature is monitored; the heater is automatically controlled to maintain the desired air temperature. The operating point of the fan blowing the air into the preheating box is calculated such that it compensates the additional pressure drop caused by the preheating box making sure that the influence of the test chamber on the cooling system performance of the inverter system is minimized. This air is then guided through a channel to the lower part of the inverter system. The temperature level for the ambient air around the signal electronics and for the power electronics can be set independently.

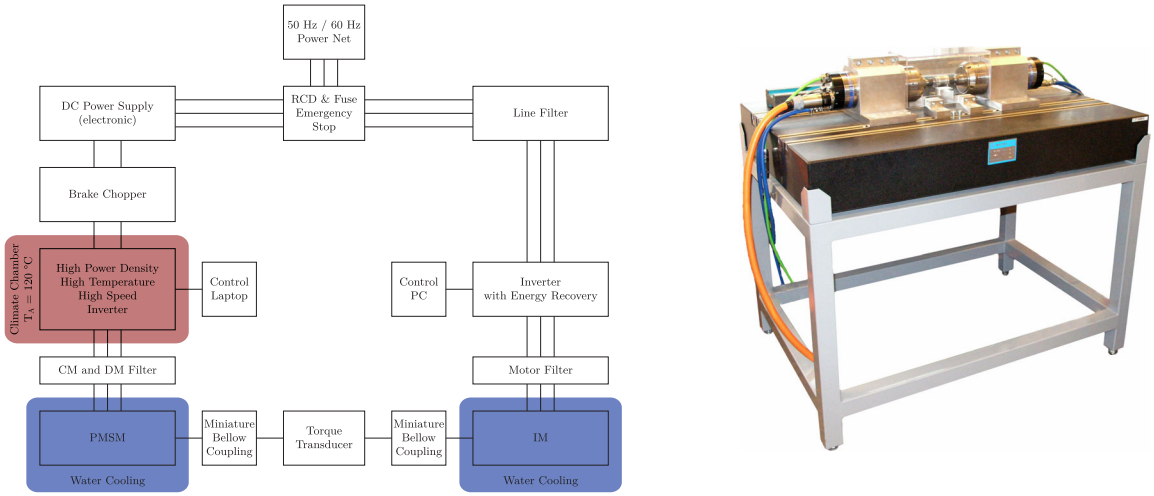
Temperature measurements are conducted in the developed thermal test chamber using IC temperature sensors on the signal electronics PCB as well as thermocouples inside and outside of the signal electronics box. At a power level of only 30 W of the Peltier cooler, the temperature inside the box ranges from 5 K below ambient temperature (temperature at the outside of the signal electronics box) measured by the PCB sensor close to the Peltier device to 3 K above ambient temperature (outside of the box) measured by a thermocouple placed in "free air" inside the box. These results support the thermal concept of actively cooling the signal electronics (*cf.* Section V) in order to meet their operating conditions with respect to their allowed temperature level.

Electrical tests of the inverter system are conducted using a high speed drives test bench with a permanent magnet synchronous machine (PMSM) and an induction machine (IM), each with a rated power of 10 kW, four poles and a maximum rotational speed of 30'000 min^{-1} in order to meet the trend towards higher rotational speeds in HEVs (*cf.* Section I). Fig. 13(a) shows the block diagram of the complete test setup and Fig. 13(b) a picture of the machines on the test bench. The inverter system is the device under test, which is supplied by a dc power supply and drives either the PMSM or the IM. The shafts of these water-cooled machines are mechanically coupled with a precisely balanced miniature bellow coupling. A torque transducer can be placed in between the machines to be able to measure the mechanical power. A commercial inverter feeds the energy of the load machine back to the dc supply of the device under test. This energy flow can also be reversed. Fig. 14 shows the 3-phase currents of the inverter driving the PMSM. The currents are almost sinusoidal with very low harmonic distortion due to the high switching frequency of 50 kHz.

VII. Conclusion

The design of a 120 °C ambient temperature forced air-cooled automotive inverter with a switching frequency of 50 kHz is shown. It employs 1200 V SiC normally-off JFETs with anti-parallel Schottky diodes and allows the use of power semiconductors with junction temperatures up to 250 °C. To operate other inverter components such as the signal electronics and the dc-link capacitors within their specified temperature range a heat management concept is developed that includes active cooling with the help of a Peltier cooler. This is possible only at the expense of a significantly higher complexity and a reduced efficiency and power density of the overall converter. The volume needed for the active cooling of the signal electronics accounts for 20% of the overall converter volume. Further research in the area of high-temperature fans and high temperature current measurement can be found in [43], [44].

Compact converters with high ambient temperature and output frequency rating are also requested in other application areas than the automotive industry, e.g. in the aerospace industry: Possible astronautical applications include the exploration of the surface or atmosphere of other planets with more hostile environmental conditions [45]. The aviation industry is currently working towards a More Electric Aircraft in order



(a) (b)

Fig. 13. (a) Setup of the high temperature inverter system test bench. The PMSM and IM have a rated power of 10 kW, four poles, and a maximum rotational speed of 30'000 min^{-1}. (b) Photograph of the test bench equipped with a PMSM and an IM, a miniature bellow coupling, a transparent safety hood covering all rotating parts, a marble ruler as an adjustment fixture, and a marble machine base.

to substitute the heavy and inflexible hydraulic infrastructure. As the energy in an aircraft is converted by a combustion process of fossil fuels, the ambient temperatures for power electronic converters are likely to be in a comparable range like for automotive or also military applications [46]. Downhole applications in the oil and gas industry also have to deal with harsh environmental conditions such as high pressure and high ambient temperature [47], [48].

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