Comparison and Implementation of a 3-Level NPC Voltage Link Back-to-Back Converter with SiC and Si Diodes

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***Abstract*—This paper presents a high efficiency 10 kVA high-frequency input and output Si IGBT and SiC Schottky diode 3-level neutral point clamped voltage dc-link back-to-back converter (3LNPC-VLBBC). A switching frequency of 48 kHz makes the converter suitable for driving high-speed and low-inductive machines. A detailed loss analysis reveals that only four of the six diodes in a 3-level bridge-leg have to be replaced by SiC diodes to enable high efficiency operation if an appropriate modulation scheme is used. A comparison with an All-Si 3-level converter shows a reduction of the semiconductor losses by 10% at the nominal operating point. In addition, a semiconductor chip area based comparison is presented, showing the chip area partitioning of the individual semiconductor types and the corresponding costs for different implementations. The payback time for the additional costs resulting from replacing the Si diodes in the 3-level converter by SiC diodes due to energy savings is estimated. Finally, experimental results of the prototype are provided.**

I. Introduction

In many current power electronic applications 3-phase voltages with high frequency and quality are required. In aircraft applications, the on-board mains grid voltage has a frequency of 400 Hz to 800 Hz, and the EMI requirements are very stringent. In high-speed drives rotational speeds of up to 60'000 rpm are common, which demand typically electrical inverter output frequencies in the range of 1 kHz. These machines are mostly low-inductive and consequently the current and torque ripple would be unacceptably high if standard (2-level) inverters with e.g. 8 kHz switching frequency were used [1]. In order to generate these fundamental frequencies and to minimize the current ripple, a high switching frequency above 25 kHz is necessary.

Unfortunately, the semiconductor losses increase with increasing switching frequencies, which reduces the overall drive efficiency and asks for a bulkier cooling system. Teichmann showed in [2] that a 3-level NPC converter, built with 600 V TrenchGate IGBTs, has lower losses than a 2-level converter built with 1200 V TrenchGate IGBTs if the switching frequency is high enough ($f_s > 10\,\mathrm{kHz}$). This is due to the reduced switching and conduction losses of the low-voltage devices which overcompensates the increased conduction losses caused by the higher number of series connected devices in the current path. Additionally, the 3-level converter generates a better voltage and current spectrum compared to the 2-level converter. This has the ability to reduce the additional PWM losses in electrical motors [3].

The silicon carbide (SiC) semiconductor technology allows utilizing SiC Schottky barrier diodes with virtually no reverse recovery effect. The implementation of SiC diodes has a positive effect on the IGBT turn-on losses, since a large fraction of typically 35% is actually caused by the reverse recovery charge of the commutating diode [4].

A detailed loss analysis in section II shows that replacing the appropriate Si diodes with SiC Schottky diodes enables an increase of the 3-level NPC converter efficiency. Since SiC Schottky diodes are expensive compared to the conventional Si diodes their use is not always justified. In section IV the required semiconductor area is investigated and the payback time for the additional costs is calculated. In section V the 10 kVA prototype for a 3LNPC-VLBBC is presented. The power circuit is built with six custom 3-level bridge-leg modules. This prototype allows for experimentally investigating the impact of utilizing SiC diodes in a 3-level converter topology (rectifier and inverter) by replacing the standard all-Si 3-level phase leg modules with pin compatible custom modules with SiC diodes.

II. Comparison of 3-level converter losses with Si and SiC schottky diodes

The calculation of the device losses in a 3-level inverter stage requires some more effort than for the well-known 2-level inverter. In previous publications the losses have been calculated approximatively for sinusoidal, carrier based PWM [5] or directly determined from time-domain simulation. In order to identify accurately the influence of different module configurations with Si and SiC diodes an appropriate method for the loss calculation with space vector modulation has been utilized. This method inherently allows for the consideration

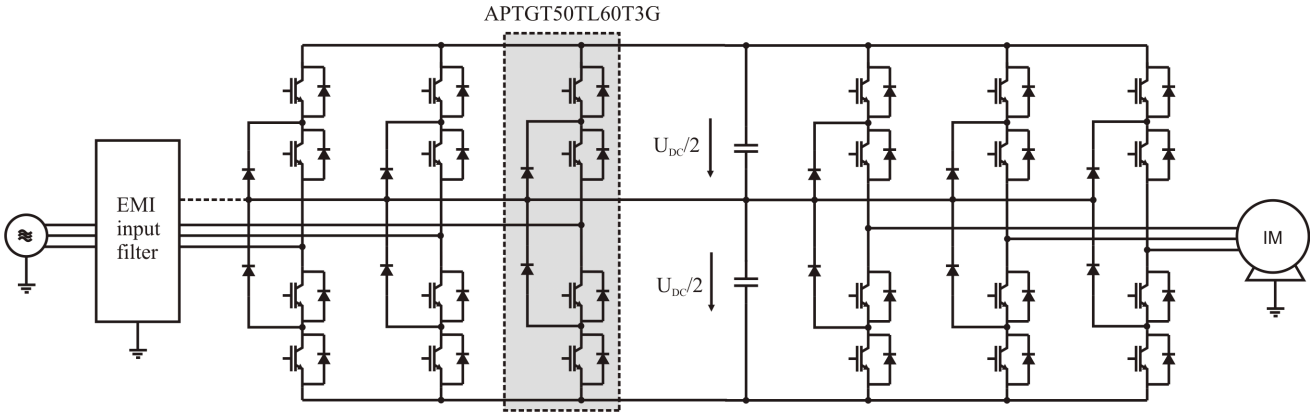
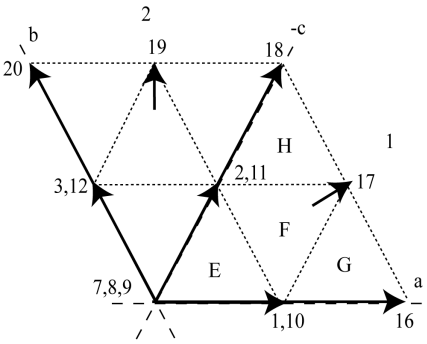


Fig. 1. Topology of the 3LNPC-VLBBC.



SV_x	S_{xa}	S_{xb}	S_{xc}
1	1	0	0
2	1	1	0
3	0	1	0
7	0	0	0
8	1	1	1
9	-1	-1	-1
10	0	-1	-1
11	0	0	-1
12	-1	0	-1
16	1	-1	-1
17	1	0	-1
18	1	1	-1
19	0	1	-1
20	-1	1	-1

Fig. 2. Voltage vectors in the 3-level NPC topology.

of phase clamping strategies as it incorporates the modulation strategy in the calculation.

Several modulation strategies exist for the 3-level NPC topology. For the converter presented in this paper a space vector modulation scheme, as described in [6], is implemented. The output voltage vector is always formed with the three nearest discrete voltage space vectors. Since the 3-level topology offers redundant space vectors (three equivalent zero vectors and always two equivalent vectors on the inner hexagon, cf. Fig. 2), it is possible to implement an optimal clamping strategy in order to reduce the switching losses. This is done by selecting an appropriate redundant vector and an appropriate vector sequence. The selection of the redundant vector plays also an important role in the balancing of the dc-link capacitor voltages which is discussed in chapter III.

A. Direct loss calculation with space vector modulation

In order to determine the losses, the space vector modulation scheme is repeated analytically for the rectifier and the inverter stage. Each voltage space vector defines if an output phase (a,b,c) is connected to the positive (1), neutral point (0) or the negative dc-link rail (-1). Together with the sign of the actual phase current and the vector sequence it is well-defined in which elements of the 3-level bridge leg the losses occur.

The conduction losses are approximated linearly for each device (IGBT, Si- or SiC-diode, c.f. Fig 3) depending on the device characteristics. It is possible to define a matrix giving the conduction losses of all devices in the rectifier (or inverter) stage depending on the current vector $\vec{I} = [i_a\ i_b\ i_c]$ and the actually applied discrete switching state space vector $\overrightarrow{SV} = [S_a\ S_b\ S_c]$.

$$P_{cond}(\overrightarrow{SV}, \overrightarrow{I}) = \begin{pmatrix} P_{c,T1a} & P_{c,D1a} & \cdots & P_{c,D5a} & P_{c,D6a} \\ P_{c,T1b} & P_{c,D1b} & \cdots & P_{c,D5b} & P_{c,D6b} \\ P_{c,T1c} & P_{c,D1c} & \cdots & P_{c,D5c} & P_{c,D6c} \end{pmatrix} \tag{1}$$

Each element of the matrix is defined as a piecewise function depending on the switching state and the output current sign. The first two elements can be written as:

$$P_{c,T1a} = \begin{cases} V_{f,T} \cdot i_a + r_{on,T} \cdot i_a^2 & i_a \geq 0\ \&\ S_a = 1 \\ 0 & \text{otherwise} \end{cases} \tag{2}$$

$$P_{c,D1a} = \begin{cases} V_{f,D} \cdot (\text{-}i_a) + r_{on,D} \cdot (\text{-}i_a)^2 & i_a < 0\ \&\ S_a = 1 \\ 0 & \text{otherwise} \end{cases} \tag{3}$$

With the modulation strategy, which defines the relative on-times of the discrete voltage space vectors, the averaged conduction losses over one switching period can be calculated. As an example, in sector 1E of the space vector diagram (cf. Fig. 2) the output voltage can be formed with $\overrightarrow{SV_1}$, $\overrightarrow{SV_2}$ and $\overrightarrow{SV_8}$ with the corresponding on-times d_1, d_2 and d_8.

$$\begin{aligned} P_{cond,avg}(\overrightarrow{U}, \overrightarrow{I}) = & d_1 \cdot P_{cond}(\overrightarrow{SV_1}, \overrightarrow{I}) + d_2 \cdot P_{cond}(\overrightarrow{SV_2}, \overrightarrow{I}) \\ & + d_8 \cdot P_{cond}(\overrightarrow{SV_8}, \overrightarrow{I}) \end{aligned} \tag{4}$$

It should be noted that these relative on-times are functions of the output voltage vector $\overrightarrow{U}$ and are calculated differently for each subsector E, F, G and H in Fig 2. They need to be described also as piecewise functions.

For the calculation of the switching losses, a similar approach is possible. The switching loss energy, occuring in each

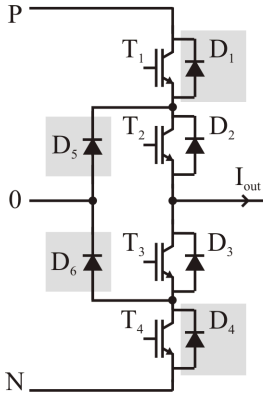


Fig. 3. 3-level bridge leg showing the placement of the SiC Schottky diodes (colored gray).

TABLE I
SWITCHING LOSS ENERGIES

Switching Transition	Generated switching loss energies
$I_{out} \geq 0$	
$1 \rightarrow -1$	E_{T1off}, E_{T2off}, E_{D3on}, E_{D4on}
$1 \rightarrow 0$	E_{T1off}, E_{D5on}
$-1 \rightarrow 1$	E_{T1on}, E_{T2on}, E_{D3off}, E_{D4off}
$-1 \rightarrow 0$	E_{T2on}, E_{D4off}, E_{D5on}
$0 \rightarrow 1$	E_{T1on}, E_{D5off}
$0 \rightarrow -1$	E_{T2off}, E_{D3on}, E_{D4on}
$I_{out} < 0$	
$1 \rightarrow -1$	E_{D1off}, E_{D2off}, E_{T3on}, E_{T4on}
$1 \rightarrow 0$	E_{D1off}, E_{T3on}
$-1 \rightarrow 1$	E_{D1on}, E_{D2on}, E_{T3off}, E_{T4off}
$-1 \rightarrow 0$	E_{T4off}, E_{D6on}
$0 \rightarrow 1$	E_{D1on}, E_{T3off}
$0 \rightarrow -1$	E_{T4on}, E_{D6off}

device in the 3-level bridge leg, is defined by the phase current and the voltage space vector transition. As an approximation, the switching energy is scaled linearly with the device current according to (5). This is not very accurate but is suitable for the comparison of two module configurations.

$$E_s(i) = E_N \cdot \frac{U_{DC}/2}{U_N} \cdot \frac{i}{I_N} \tag{5}$$

At first sight it is not clear in which devices of a 3-level bridge leg switching losses occur. With measurements on a test setup it was determined for each switch transition which devices actually exhibit losses. Table I summarizes the switching energies occurring in one inverter leg depending on the switching transition. It can be noticed that only for direct transitions between positive (1) and negative (-1) dc-link voltage rail (or from -1 to 1) turn-off losses in the inner diodes D_2 and D_3 occur.

Now it is possible to define a switching energy matrix giving the actual losses of all inverter devices depending on the output current space vector and the transition from the old voltage space vector $\overrightarrow{SV_o}$ to the new vector $\overrightarrow{SV_n}$:

$$E_{sw}(\overrightarrow{SV_o}, \overrightarrow{SV_n}, \overrightarrow{I}) = \begin{pmatrix} E_{s,T1a} & E_{s,D1a} & \cdots & E_{s,D5a} & E_{s,D6a} \\ E_{s,T1b} & E_{s,D1b} & \cdots & E_{s,D5b} & E_{s,D6b} \\ E_{s,T1c} & E_{s,D1c} & \cdots & E_{s,D5c} & E_{s,D6c} \end{pmatrix} \tag{6}$$

Again each element of this matrix is a piecewise function returning the switching loss energies depending on the switching transition and the output current signs. The first two elements of the matrix are:

$$E_{s,T1a} = \begin{cases} E_{T1off}(i_a) & S_{a,o} = 1 \,\&\, S_{a,n} = -1 \,\&\, i_a \geq 0 \\ E_{T1off}(i_a) & S_{a,o} = 1 \,\&\, S_{a,n} = 0 \,\&\, i_a \geq 0 \\ E_{T1on}(i_a) & S_{a,o} = -1 \,\&\, S_{a,n} = 1 \,\&\, i_a \geq 0 \\ E_{T1on}(i_a) & S_{a,o} = 0 \,\&\, S_{a,n} = 1 \,\&\, i_a \geq 0 \\ 0 & \text{otherwise} \end{cases} \tag{7}$$

$$E_{s,D1a} = \begin{cases} E_{D1off}(\text{-}i_a) & S_{a,o} = 1 \,\&\, S_{a,n} = -1 \,\&\, i_a < 0 \\ E_{D1off}(\text{-}i_a) & S_{a,o} = 1 \,\&\, S_{a,n} = 0 \,\&\, i_a < 0 \\ 0 & \text{otherwise} \end{cases} \tag{8}$$

The turn-on energy of the diodes is very small and has been neglected. The space vector sequence defined by the modulation scheme allows for calculating the average switching loss over one switching period. For a symmetric space vector sequence 1-2-8-2-1 in sector 1E the average switching losses for one switching period are:

$$\begin{aligned} P_{sw,avg}(\overrightarrow{U}, \overrightarrow{I}) = & \frac{1}{T_s} \cdot (E_{sw}(\overrightarrow{SV_1}, \overrightarrow{SV_2}, \overrightarrow{I}) + \\ & E_{sw}(\overrightarrow{SV_2}, \overrightarrow{SV_8}, \overrightarrow{I}) + E_{sw}(\overrightarrow{SV_8}, \overrightarrow{SV_2}, \overrightarrow{I}) + \\ & E_{sw}(\overrightarrow{SV_2}, \overrightarrow{SV_1}, \overrightarrow{I})) \end{aligned} \tag{9}$$

Finally the average conduction and switching loss matrices contain the losses for each device in the 3-level inverter depending on the output voltage, the output current and the modulation strategy. Now the modulation in terms of the vector sequence and the relative on-times depending on the output voltage vector $\vec{U}$ has to be defined. It is sufficient to do that for the first electrical 120° because of the inherent 3-phase symmetry. With some effort this is possible with a modern mathematics software like Mathematica.

The resulting loss curves of one inverter stage bridge-leg for a switching frequency of 48 kHz are depicted in Fig. 4. An optimal clamping strategy is used so that the output phase with the highest instantaneous current value is not switched during an electric output angle of 60°. However for voltage link balancing the rectifier stage cannot do an optimal clamping scheme so that its losses will be increased slightly.

As a result of the above calculation the conduction and the switching losses averaged over a switching period are available. The mean losses over a fundamental period in each device can be obtained by integrating the corresponding

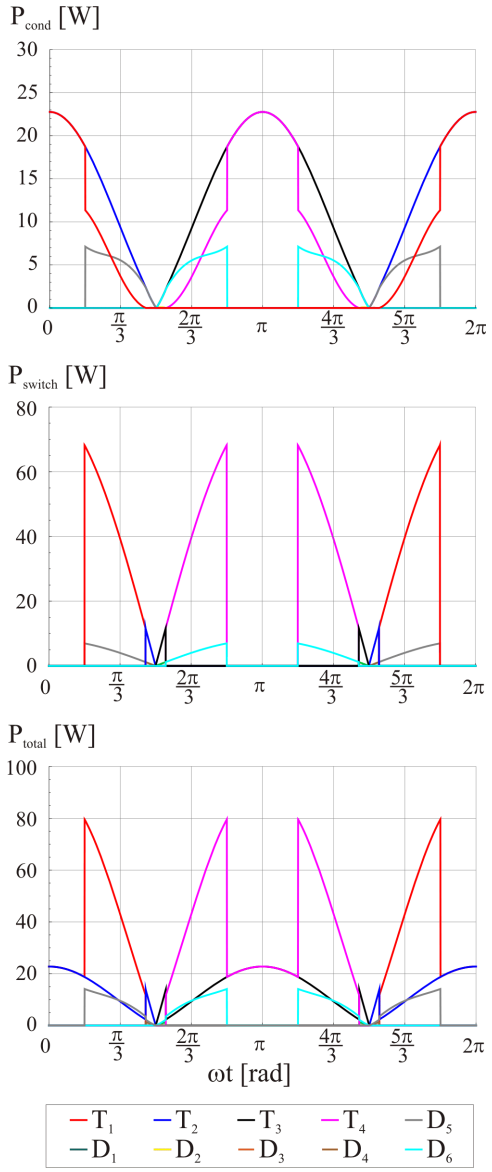


Fig. 4. 3-level inverter stage a) conduction, b) switching and c) total losses over electric output angle ($\tilde{U}_2 = 325\,\mathrm{V}$, $\tilde{I}_2 = 20.5\,\mathrm{A}$, $\varphi_2 = 0\,^\circ$).

expressions over the full electric output angle of 360°.

$$\overline{P_{cond}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} P_{cond,avg} \cdot d\alpha \tag{10}$$

$$\overline{P_{sw}} = \frac{1}{2\pi} \cdot \int_0^{2\pi} P_{sw,avg} \cdot d\alpha \tag{11}$$

The mean losses of the devices in the rectifier and in the inverter stage are depicted in Fig. 5a and Fig. 5c. It can be observed that the inner diodes D_2 and D_3 exhibit no switching losses. This is due the implemented modulation strategy which clamps the output phase with the highest current symmetrically around $-30^\circ \ldots +30^\circ$ (for a phase displacement of 0° between voltage and current space vector which is true for the rectifier stage and the inverter stage for low-inductive loads). As an example the vector sequences for the subsector E are given here.

(100) - (110) - (111) - (110) - (100) for $0 \leq \alpha < 30^\circ$
(00-1) - (0-1-1) - (-1-1-1) - (0-1-1) - (00-1) for $30^\circ \leq \alpha < 60^\circ$

If one has a closer look at the single switch commutations it can be recognized that no direct commutations from the positive to the negative dc-link rail or vice versa occur (1 to -1 or -1 to 1). There exist similar sequences for all subsectors E, F, G and H and for all other main sectors ($\alpha > 60^\circ$) which exhibit only commutations from or to the neutral (0) rail [6].

As mentioned above, if for all commutations a step over the neutral dc-link rail occurs, the diodes D_2 and D_3 do not have any switching losses. Depending on the operation mode (inverter or rectifier / motor or generator operation) the semiconductors are loaded differently. For rectifier operation the diodes D_1-D_4 (cf. Fig. 5) are mainly conducting. With the increased forward voltage drop of SiC diodes compared to Si diodes, the rectifier efficiency therefore would be reduced if all Si diodes would be replaced by SiC devices. With this facts in mind, for increasing the converter efficiency a custom SiC module for the 3-level topology replacing the diodes D_1, D_4, D_5 and D_6 with SiC counterparts has been tested and employed in the 3LNPC-VLBBC. The inner diodes D_2 and D_3 remain in conventional Si technology. SiC Schottky diodes with equivalent current rating (30 A / 600 V, 3x10A SiC dies in parallel per diode) have been used for the custom module.

B. Converter efficiency with Si- and SiC module configuration

The results of the comparison between the custom SiC module with a standard Si module are depicted in Fig. 5 representatively for one rectifier and inverter bridge-leg. The calculation is based on semiconductor datasheet values for the conduction losses and on switching loss energies determined with a test setup for both the standard and the custom SiC module. The losses are averaged over one electrical period for nominal operation. It can be noticed that the diodes D_1, D_4, D_5 and D_6 exhibit nearly zero switching losses in the SiC configuration. The IGBT switching losses are also reduced. This is due to the smaller turn-on energy if the commutating diode has no reverse recovery effect as is the case with SiC devices. On the contrary, the conduction losses of the SiC diodes are slightly increased comparing to the Si version. In the inverter stage mainly the IGBTs exhibit conduction losses so that the increased conduction losses of the SiC diodes only occur in the clamping diodes D_5 and D_6.

If we compare the total converter efficiency curves (cf. Fig. 6, pure semiconductor efficiency) a considerable increase in efficiency with the custom SiC module can be achieved. The intersection point at which the common Si module exhibits smaller losses (because of the lower conduction losses) than its SiC counterpart is below 5 kHz. At the nominal switching frequency of 48 kHz and at nominal output power of 10 kVA the losses could be reduced by 10%. The converter built with the SiC module reaches a pure semiconductor efficiency of 97.0% compared to 96.6% of the standard Si version.

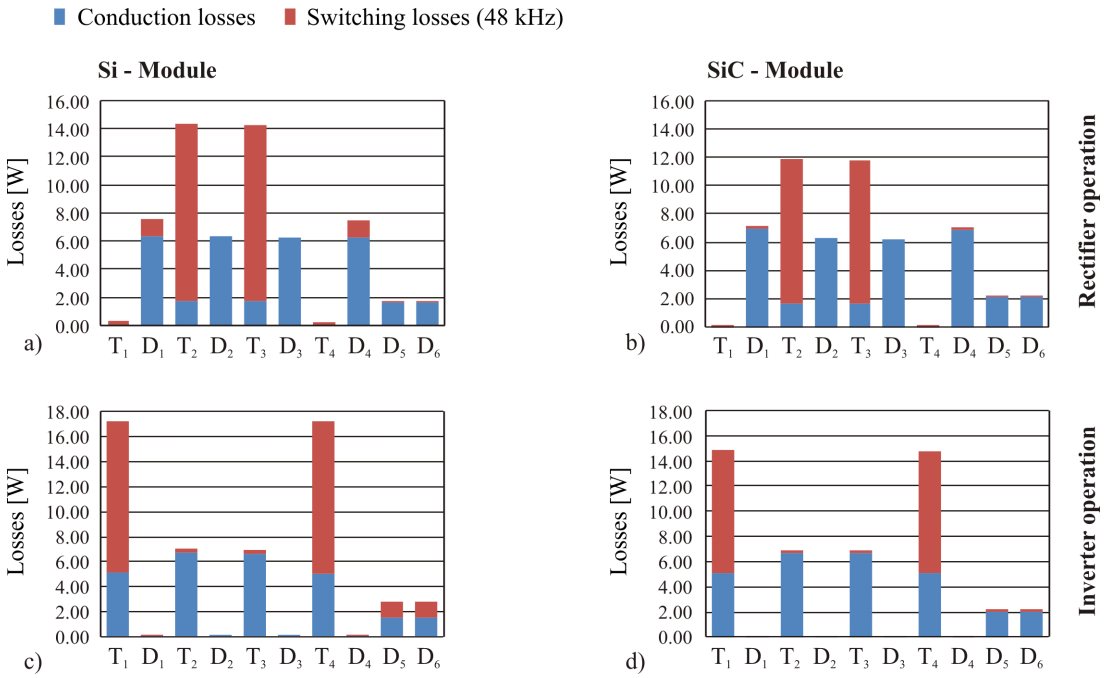


Fig. 5. Comparison of the total losses in a bridge-leg for the rectifier and inverter stage (rectifier operating point: $\hat{U}_1 = 325\,\mathrm{V}$, $\hat{I}_1 = 21.3\,\mathrm{A}$, $\varphi_1 = 0\,°$ inverter operating point: $\hat{U}_2 = 325\,\mathrm{V}$, $\hat{I}_2 = 20.5\,\mathrm{A}$, $\varphi_2 = 0\,°$).

Compared to an equivalent 2-level converter with 1200 V IGBTs of the same generation, the reduction of the losses is 42%.

Interesting is also the very flat dependency of the efficiency on the switching frequency. This opens an additional degree of freedom for optimizing the converter. A very compact system with small filtering components because of the higher switching frequency and a low volume cooling system due to the small losses could be realized.

It should be noted that in the real implementation additional loss sources as forced-air cooling fans (15W), digital control and gate drive power (15W) and also losses in the boost inductors (30W) are present. These will sum up to additional 60W and reduce the efficiency of the SiC 3LNPC-VLBBC to approximately 96.4%.

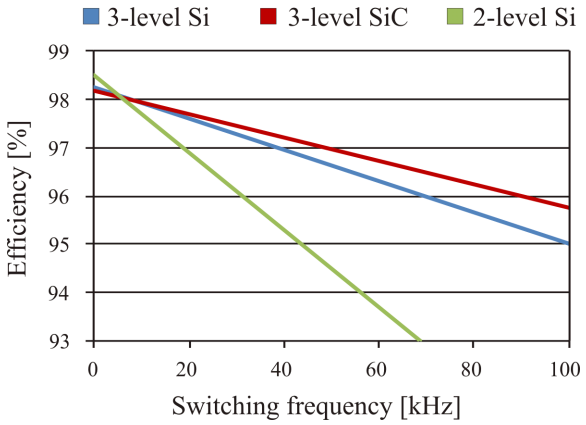


Fig. 6. Comparison of total converter efficiency.

III. Clamping and DC-link balancing

In the previous section the loss calculation has been carried out neglecting the dc-link balancing. If the described clamping scheme is applied the dc-link capacitors are loaded differently depending in which sector and subsector of the space vector diagram the reference voltage vector and the current vector are located [7]. If the displacement angle between voltage and current vector is small (as is the case for the rectifier stage or the inverter stage with low inductive loads) a symmetric clamping around $\pm 30°$ results in minimum switching losses.

If the dc-link capacitors are big enough as is the case with electrolytic capacitors this is no problem for the converter because the capacitor loading balances out over the fundamental period. However, since electrolytic capacitors are prone to early aging and have been the source for reliability issues in the past, they have been omitted in the design of the 3LNPC-VLBBC prototype. Instead a reduced dc-link capacitance has been realized with foil capacitors. If the converter is designed with a low dc-link capacitance, the balancing of the capacitors is more difficult and the modulation should be coupled between rectifier and inverter stage.

The dc-link balancing can be achieved with the rectifier stage changing the vector sequence depending on the capacitor unbalance. In sector E the vector sequence (100) - (110) - (111) - (110) - (100) solely loads the high-side capacitor while the alternative sequence (00-1) - (0-1-1) - (-1-1-1) - (0-1-1) - (00-1) solely loads the low-side capacitor. As for the nominal operating voltage of $230\,\mathrm{V_{rms}}$ at the rectifier side subsector E is never crossed, the reference voltage vector is located always

in the subsectors F, G and H. Using an appropriate sequence in these sectors also allows for balancing the dc-link. However, in these subsectors always both capacitors are loaded, but one slightly more than the other depending on the used sequence. The clamping of the phase with the highest current amplitude is not anymore possible, and thus the switching losses of the rectifier stage are increased.

It has to be noted that the mean capacitor loading over one switching period is solely due to active power, reactive power at the output power will not additionally unbalance the capacitors. It can be seen that the worst combination for the dc-link balancing solely with the rectifier stage is a small inverter stage voltage vector located in the inner hexagon (subsector E) and optimal clamping. This leads to an alternating loading of the upper and lower capacitor every electric 60° of the output period. As a solution the inverter stage should adopt in subsector E a changing to an alternative sequence (0-1-1)-(00-1)-(000)-(00-1)-(0-1-1). In this case optimal clamping of the phase with the highest current amplitude can still be maintained.

If dc-link balancing is done with different sequences, special care should be given on the sequence change, because this can happen frequently depending on the maximum allowed link unbalance. An intermediate sequence has to be introduced to prevent an increase of the net switching frequency due to the sequence change. Also a switching directly from positive to negative dc-link rail or in the opposite direction should be avoided during the sequence change so that the benefits of the special SiC module configuration are utilized.

IV. Semiconductor Area Usage and Cost Comparison

Power semiconductors in SiC technology are more expensive than devices in conventional Si technology. Therfore, it is important to know if the excess expenditure will pay back with the saved energy in a reasonable time period. First, one has to know the specific partition of Si to SiC semiconductor area. In Fig. 7 the semiconductor partitioning of the conventional Si module and the custom SiC module is depicted. One can see a small increase of 18.8% in total semiconductor area for the custom module.

Considering the costs for the two modules, the custom SiC module is roughly 6.5 times more expensive than the conventional module. The converter costs accordingly will increase by roughly 300$. With a loss reduction of 10% = 32 W the energy payback time with an energy price of 0.1$/kWh [8] will be 93'700 hours, what is equivalent to 10.5 years of uninterrupted operation at nominal power. At a switching frequency of 120 kHz the payback time reduces to 3.2 years of uninterrupted operation. This is quite a long operating time and restricts the application of the SiC 3-level converter to niche areas where exceptional high switching frequencies and efficiencies is required. This is the case e.g. in aircraft applications where weight and efficiency are of major interest.

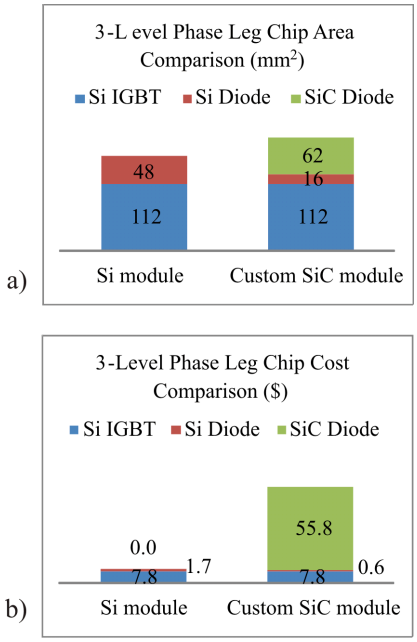


Fig. 7. Semiconductor a) area and b) cost comparison.

P_N	10 kVA
U_N	230 V_{rms}
f_N	50 Hz / 800 Hz
f_s	48 kHz
U_{DC}	700 V
C_{DC}	2 x 66 μF in series
L_{Boost}	3 x 300 μH
ρ	2.9 kW/dm^3 (47.5 W/in^3)
γ	2 kW/kg
η_N	96.5%
Weight	5 kg
EMI filter	CISPR Class A

TABLE II
Key Performance Data of the 3-Level Converter

V. 10 kVA/ 48 kHz 3-Level SiC Converter Prototype

The 3LNPC-VLBBC is designed for a modular assembly (cf. Fig. 8). A gate-drive board populated with 26 isolated gate drive circuits and 5 current sensors for the input and output current is directly mounted on the 3-level modules. In order to investigate the impact of the proposed SiC configuration the custom 3-level bridge-leg module is pin compatible to an existing module from Microsemi (APTGT50TL60T3G).

A digital signal processing board with a TI DSP and a Lattice FPGA as well as filtering and amplification circuitry is mounted on top of the gate-drive board.

Three boost inductors with an inductance value of 300 μH have been employed. They limit the unfiltered current ripple at the rectifier stage to 4 A_{pp}. A minimum dc-link capacitance of 33 μF has been calculated, limiting the voltage overshoot in case of a sudden load drop from nominal power to zero to an acceptable value of 10%. Foil capacitors have been used for a reliable solution without electrolytic capacitors.

The topmost board is a compact EMI filter board which

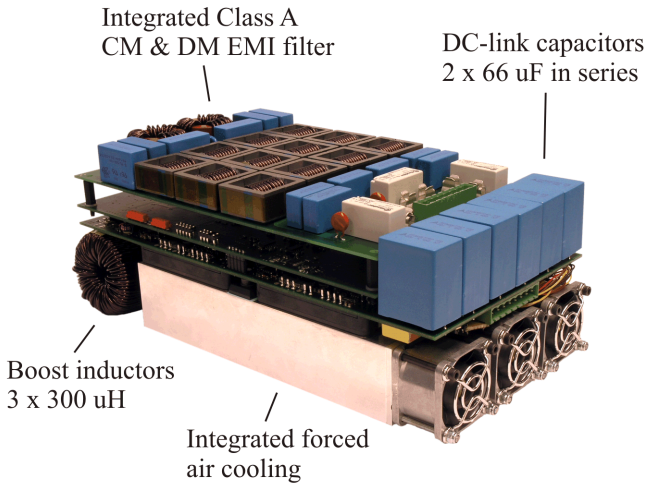


Fig. 8. Compact 10 kVA, 3LNPC-VLBBC prototype with 48 kHz switching frequency.

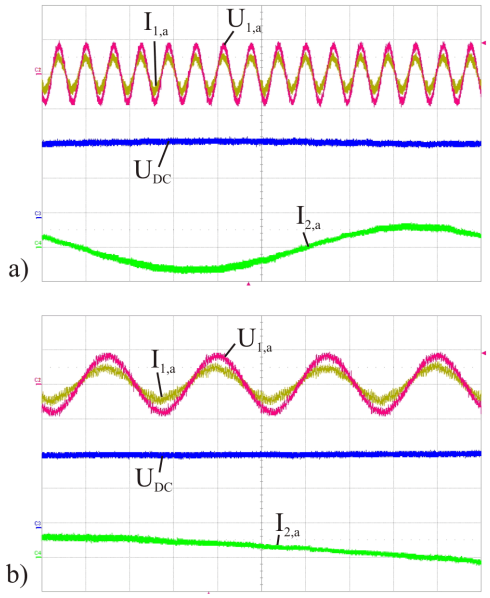


Fig. 9. Initial 3-level converter measurements operating at $f_1 = 800\,\mathrm{Hz}$, $U_1 = 115\,\mathrm{V_{rms}}$, $U_{DC} = 400\,\mathrm{V}$, $f_2 = 50\,\mathrm{Hz}$, $P = 1.5\,\mathrm{kW}$ ($U_1 = 200\,\mathrm{V/div}$, $I_1 = 10\,\mathrm{A/div}$, $I_2 = 10\,\mathrm{A/div}$, $U_{dc} = 200\,\mathrm{V/div}$, timescale a) $2\,\mathrm{ms/div}$ b) $500\,\mu\mathrm{s/div}$).

allows for an easy exchange so that both 50/60 Hz grid and 400 Hz aircraft on board grid frequency can be tested. A forced air cooling system and an optimized heatsink have been dimensioned for a maximum junction temperature of $T_j = 125\,^{\circ}\mathrm{C}$. The power density of the total converter including cooling system and EMI filter is $2.9\,\mathrm{kW/dm^3}$. The key properties of the converter are summarized in Tab. II. The target system efficiency is 96.5% including the losses in the EMI input filter, the losses caused by the fans and the digital signal processing board.

Initial measurements at an input voltage of $115\,\mathrm{V_{rms}}$ and a dc-link voltage of 400 V show the basic functionality. To demonstrate the system performance measurements at 800 Hz fundamental input frequency and 50 Hz fundamental output frequency are provided in Fig. 9. A sinusoidal input current with unity power factor has been achieved. The dc-link voltage is regulated to a stable value.

VI. Conclusion

In this paper a 3-level topology with the anti-parallel diodes partially replaced SiC Schottky diodes is presented. This approach allows for reducing the converter losses for switching frequencies above 5 kHz and thus makes the converter suitable for driving high-speed and low-inductive machines. A loss analysis revealed that only four of the six diodes in a 3-level bridge-leg have to be replaced by SiC diodes to enable high efficiency operation. The losses have been reduced by 10% at nominal operating point.

It has been shown that with an appropriate dc-link balancing method the converter is able to operate also with a reduced link capacitance, avoiding the use of electrolytic capacitors which are sensitive to aging. A simple cost comparison showed that the additional costs for the SiC diodes are considerable.

Initial measurements at the prototype have been performed, showing the operation with unity power factor at a high fundamental input frequency of 800 Hz. The currents are sinusoidal and the dc-link voltage is stable.

References

[1] K. Jalili, D. Krug, S. Bernet, M. Malinowski, and B. J. C. Filho, "Design and characteristics of a rotor flux controlled high speed induction motor drive applying two-level and three-level npc voltage source converters," in *Proc. of 36th IEEE Power Electronics Specialists Conference PESC '05*, pp. 1820–1826, 16 June 2005.

[2] R. Teichmann and S. Bernet, "A comparison of three-level converters versus two-level converters for low-voltage drives, traction, and utility applications," *IEEE Trans. Ind. Appl.*, vol. 41, pp. 855–865, May–June 2005.

[3] A. Boglietti, A. Cavagnino, A. M. Knight, and Y. Zhan, "Factors affecting losses in induction motors with non-sinusoidal supply," in *Proc. of 42nd IEEE IAS Annual Meeting*, pp. 1193–1199, 23–27 Sept. 2007.

[4] A. Elasser, M. H. Kheraluwala, M. Ghezzo, R. L. Steigerwald, N. A. Evers, J. Kretchmer, and T. P. Chow, "A comparative evaluation of new silicon carbide diodes and state-of-the-art silicon diodes for power electronic applications," *IEEE Trans. Ind. Appl.*, vol. 39, pp. 915–921, July–Aug. 2003.

[5] D. Krug, S. Bernet, and S. Dieckerhoff, "Comparison of state-of-the-art voltage source converter topologies for medium voltage applications," in *Proc. of 38th IEEE IAS Annual Meeting*, vol. 1, pp. 168–175, 12–16 Oct. 2003.

[6] B. Kaku, I. Miyashita, and S. Sone, "Switching loss minimised space vector pwm method for igbt three-level inverter," *IEE Proceedings - Electric Power Applications*, vol. 144, pp. 182–190, May 1997.

[7] N. Celanovic and D. Boroyevich, "A comprehensive study of neutral-point voltage balancing problem in three-level neutral-point-clamped voltage source pwm inverters," *IEEE Trans. Power Electron.*, vol. 15, pp. 242–249, March 2000.

[8] "Average Retail Price of Electricity to Ultimate Customers." http://www.eia.doe.gov/, Nov. 13, 2009.