Design and Performance of a 200-kHz All-SiC JFET Current DC-Link Back-to-Back Converter

Thomas Friedli, *Student Member, IEEE*, Simon D. Round, *Senior Member, IEEE*, Dominik Hassler, and Johann W. Kolar, *Senior Member, IEEE*

***Abstract*—Silicon carbide (SiC) switching devices have been widely discussed in power electronics due to their desirable properties and are believed to set new standards in efficiency, switching behavior, and power density for state-of-the-art converter systems. In this paper, the design, construction, and performance of a 3-kVA All-SiC current-source converter (CSC), also known as current dc-link back-to-back converter (CLBBC), is presented. CSC topologies have been successfully used for many years for high-power applications. However, for low-power-range converter systems, they could not compete with voltage-source-converter topologies with capacitors in the dc-link, since the link inductor has always been a physically large and heavy component due to the comparatively low switching frequencies of conventional high-blocking-voltage silicon devices. New SiC switches such as the JFET, which are providing simultaneously high-voltage blocking, low switching losses, and low on-state resistance (three times lower compared with Si MOSFET with similar V–I rating), offer new possibilities and enable the implementation of a high switching frequency CLBBC and, thus, reducing size and weight of the dc-link inductor. The prototype CLBBC has been designed specifically for the latest generation 1200-V 6-A SiC JFETs and a target switching frequency of 200 kHz.**

***Index Terms*—All-silicon carbide, current-source converter (CSC), JFET, normally on.**

I. Introduction

BIDIRECTIONAL ac–ac power converters with an active front end are capable of providing simultaneous amplitude and frequency transformation of three-phase voltages, sinusoidal input currents, and unity power factor at the converter input. They are typically applied in electrical drives and frequency changers. These power converters can be divided into two basic categories: those that have an energy-storage element in the interconnecting dc-link and those which have no energy-storage elements, such as the matrix converter (MC) [1]–[3].

Paper 2008 IPCC-141, presented at the 2008 Industry Applications Society Annual Meeting, Edmonton, AB, Canada, October 5–9, and approved for publication in the IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS by the Industrial Power Converter Committee of the IEEE Industry Applications Society. Manuscript submitted for review November 7, 2008 and released for publication April 6, 2009. First published July 14, 2009; current version published September 18, 2009.

T. Friedli, D. Hassler, and J. W. Kolar are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland (e-mail: thomas.friedli@alumni.ethz.ch; hassler@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

S. D. Round was with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland. He is now with ABB Switzerland, Traction Converters/ATTD, 5300 Turgi, Switzerland (e-mail: simon.round@ieee.org).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TIA.2009.2027538

For the converters with dc energy storage, the component can be either a capacitor, as is in the case of the commonly used voltage dc-link back-to-back converter (VLBBC), or an inductor, as in the case of a current dc-link back-to-back converter (CLBBC) shown in Fig. 1. The CLBBC is a three-phase ac–ac bidirectional power-flow converter with a current dc-link, interconnecting the converter input and output stage with an inductor [4]–[7]. Traditionally, the VLBBC is the preferred converter type since the per volume energy-storage density is much higher in a capacitor than in an equivalent inductor. In the CLBBC, the inductive storage element typically has had a high inductance value and, consequently, has been physically large, mainly due to a comparatively low switching frequency of conventional high-blocking-voltage silicon devices [e.g., 1200-V RB-insulated-gate bipolar transistor (RB-IGBTs)]. Furthermore, the VLBBC has a higher efficiency compared with the CLBBC, as it has no additional series diodes in the individual bridge legs. However, a significant advantage of the CLBBC, inherently given by its topology, is that the output voltage is sinusoidal, rather than pulsed, as for a VLBBC without additional output filter. Furthermore, thermal aging of a dc-link inductor is significantly lower compared with a dc-link capacitor.

New wide bandgap power devices, such as SiC JFETs, are offering the possibility of a high blocking voltage, low ON-state resistance, and a high-switching-frequency capability. Due to the normally on characteristic of the considered SiC JFET, the device conducts the current when zero voltage (or a slightly positive voltage) is applied to the gate. In order to turn off the devices, a negative gate–source voltage is required. The question that arises out of the SiC JFETs' properties is on whether and how they can be best applied to bidirectional ac–ac converter systems, or even better, to find a topology which favors the SiC JFET properties. The motivation for this paper is not to simply replace conventional Si devices by SiC but to advantageously match the device properties with the converter topology. This paper firstly presents in Section II the available SiC semiconductor devices that determine the power specifications of the CLBBC (see Table I), followed by the design and the physical construction of the overall converter system. In Section III, the performance of the SiC JFET CLBBC, operating at a switching frequency of 200 kHz, is demonstrated, including characteristic input and output waveforms, total harmonic distortion (THD), achievable efficiency, and electromagnetic interference (EMI) performance. A brief performance comparison between the All-SiC JFET CLBBC and an All-SiC JFET indirect MC (IMC), both operating at

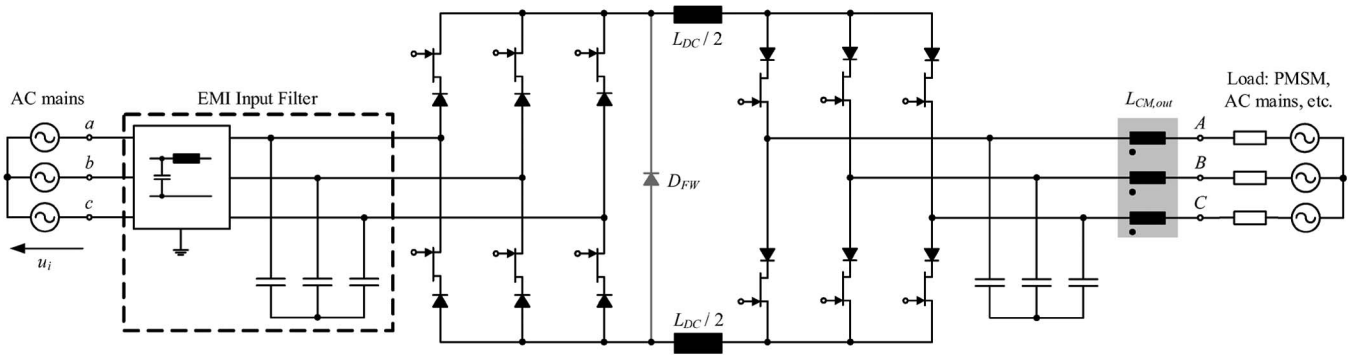

Fig. 1. Schematic of the All-SiC JFET CLBBC. If only unidirectional power-flow operation is required, the additional freewheeling diode D_{FW} can be implemented in order to reduce conduction losses.

TABLE I
ALL-SiC JFET CLBBC SPECIFICATION SUMMARY

Quantity	***Value***
3∼AC Input	
Nominal RMS line-to-line voltages	$3 \times 400\,\mathrm{V}$, $50\,\mathrm{Hz}$
Current displacement angle	$\Phi_1 = 0°, 180°$
3∼AC Output	
Maximal RMS line-to-line voltages	$3 \times 382\,\mathrm{V}$, $0 \ldots 300\,\mathrm{Hz}$
Current displacement angle	$\Phi_2 = 0 \ldots 360°$
Maximum (nominal) output power (at nominal input voltages)	$2.8\,\mathrm{kVA}$ $(2.5\,\mathrm{kVA})$
Switching frequency	$200\,\mathrm{kHz}$
Power switches	SiCED SiC VJFET $1200\,\mathrm{V}$, $6\,\mathrm{A}$
Power diodes	CREE SiC Schottky diode C2D10120, $1200\,\mathrm{V}$, $10\,\mathrm{A}$
Overall outer dimensions	$230\,\mathrm{mm} \times 80\,\mathrm{mm} \times 65\,\mathrm{mm}$
Boxed volume	$1200\,\mathrm{cm}^3 = 1.2\,\mathrm{litre} = 73\,\mathrm{in}^3$
Power density	$2.4\,\mathrm{kVA/litre} = 40\,\mathrm{W/in}^3$
Weight	$1.1\,\mathrm{kg}$

200 kHz is described in Section IV. Finally, the conclusions are given in Section V.

II. DESIGN AND CONSTRUCTION OF THE CLBBC

A. Suitability of CLBBC Topology for SiC JFETs

The topology evaluation and analysis has shown that the best match between power semiconductor and converter topology can be achieved with a current-source-type converter, in this case a CLBBC, as it naturally favors the normally on characteristic of the SiC JFETs. These devices are particularly advantageous for the CLBBC in terms of simplicity of implementation, fault tolerance, and general ruggedness. Under fault conditions such as, for example, gate-driver supply-power loss, a natural freewheeling path is provided for the dc-link inductor current as the JFETs become conducting. An additional advantage is that a phase-leg short circuit cannot occur, such as in the case of an MC or a voltage-source converter (VSC). An equivalent 3-kVA SiC JFET VLBBC, optimized for a low dc-link capacitance of 20 μF and a nominal dc-link voltage of 700 V, has a stored link energy of 4.9 J, which is sufficient to thermally destroy the SiC JFETs in case of a phase-leg shoot through.

Similar to the MC and VLBBC, a proper start-up procedure for the CLBBC must be followed in order to avoid an excessively high dc-link current, when the power circuit is connected to the mains before the JFETs are blocking. When input power is first applied, relays in line with the input EMI filter prevent the voltage from being instantaneously applied to the power switches. Once the auxiliary power supply is running and the controller verifies the correct gate-driver operation, then the relays can be energized and the CLBBC operated. The application of SiC power-semiconductor devices generally broadens the overall converter-system application area in terms of switching frequency, blocking voltage, and junction temperature, as shown in Fig. 2. For the CLBBC, the normally on characteristic of the SiC JFET provides an additional benefit in terms of system-failure behavior and pinpoints the importance of matching semiconductor properties to the converter topology.

B. Power-Semiconductors Selection

In order to analyze the in-system performance of SiC semiconductors, the aim is to develop a CLBBC made entirely of SiC power semiconductors, including both the power switches and the blocking diodes, despite their increased forward voltage drop compared with Si diodes. The possible power devices are limited by their availability. The switching device selected for this design is the SiC JFET produced, in sample quantities, by SiCED and packed in a standard TO-220 package. The JFET is rated for 1200 V with a breakdown voltage typically exceeding the 1300-V level. The dc-current-handling capability is limited to 6 A mainly by the die size of 2.4 mm $\times$ 2.4 mm and the thermal properties of the package. The essential SiC power-semiconductor parameters are summarized in Table II.

In the CLBBC topology, the series diodes significantly contribute to the overall converter-conduction losses as always, four diodes are conducting the dc-link current. The device of choice is a 1200-V 10-A SiC Schottky barrier diode C2D10120 from CREE. As the SiC Schottky diode is a majority carrier device, there is virtually no reverse-recovery charge, which is desirable for high switching-frequency operation. Basically, there are two diodes available from CREE with similar current rating and the same package as the SiC JFET: a 5-A and a 10-A device. In order to minimize the overall converter losses, the diode is selected to be loss optimal and not optimal in terms of semiconductor die usage. By selecting the 10-A SiC diode with a forward voltage drop of $U_F = 1.6$ V (at $I_F = 6$ A, $T_J = 125\ °\mathrm{C}$) instead of the 5-A device with $U_F = 2.4$ V, the forward voltage drop is lowered by 0.8 V, which leads to a reduction of the total conduction losses of 33%.

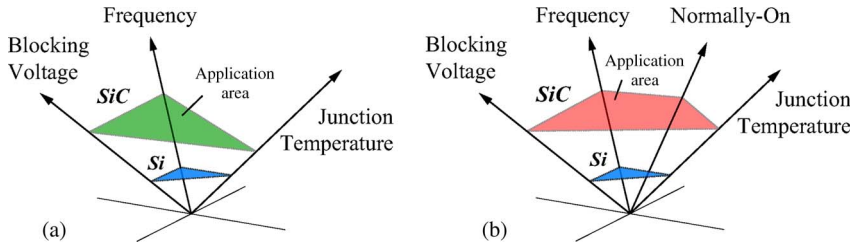

Fig. 2. Benefits of utilizing SiC instead of Si power devices: (a) in general and (b) specifically for the All-SiC JFET CLBBC.

TABLE II
SiC POWER-DEVICE PARAMETERS

SiC JFET Parameters				
C_{GS} at $V_{DS} = 40\,\mathrm{V}$, $V_{GS} = V_{\mathrm{pinchoff}}$				$\approx 0.5\,\mathrm{nF}$
C_{GS} parallel C_{GD} at $V_{DS} = 0\,\mathrm{V}$, $V_{GS} = V_{\mathrm{pinchoff}}$				$\approx 1.0\,\mathrm{nF}$
$r_{DS,on}$ at $I_{DS} = 6\,\mathrm{A}$, $T_J = 125°\mathrm{C}$				$0.55\,\Omega$
Switching loss parameters at $I_{DS} = 6\,\mathrm{A}$, $T_J = 125°\mathrm{C}$				
	K_1 [μJ/V^3]	K_2 [μJ/V^2]	K_3 [μJ/V]	K_4 [μJ]
T_{off-on}	$-7.97 \cdot 10^{-7}$	$9.59 \cdot 10^{-4}$	$5.67 \cdot 10^{-3}$	2.42
T_{on-off}	$-2.06 \cdot 10^{-7}$	$1.70 \cdot 10^{-4}$	$1.15 \cdot 10^{-2}$	0.47
SiC Schottky Diode Parameters				
Diode forward voltage drop $U_F = U_{D0} + r_{FD} \cdot I_F$ $U_{D0} = 0.8\,\mathrm{V}$, $r_{FD} = 0.13\,\Omega$ at $I_F = 6\,\mathrm{A}$, $T_J = 125\,°\mathrm{C}$				1.6 V
Total capacitive charge (reverse recovery)				61 nC
Switching loss parameters at $I_F = 6\,\mathrm{A}$, $T_J = 125°\mathrm{C}$				
	K_1 [μJ/V^3]	K_2 [μJ/V^2]	K_3 [μJ/V]	K_4 [μJ]
D_{on-off}	$-6.23 \cdot 10^{-8}$	$8.85 \cdot 10^{-5}$	$3.99 \cdot 10^{-3}$	0.22

Voltage drop, resistance, and capacitance values are based on sample measuremant data.

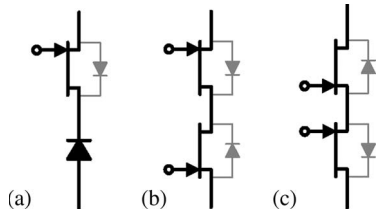

Fig. 3. Replacement of the (a) bridge-leg series diode with a (b) common-drain or (c) common-source SiC JFET configuration.

Optionally, the series diode could be replaced by a SiC JFET, leading, for example, to a common-drain configuration of two discrete JFETs, as shown in Fig. 3. The selection of the common-drain configuration has the advantage that ten isolated gate-driver power supplies are required compared with 12 for the common-source configuration. Depending on the SiC power-device parameters, replacing the series diode by a JFET allows further reduction of the conduction losses. The disadvantage of this approach is that instead of 12 gate-driver circuits, 24 are required and that the minimal number of isolated gate-driver supplies is increased from eight (with series diode) to ten (common-drain). The conduction losses evaluated for a dc current of 6 A and a junction temperature of 125 °C for both the series connection of JFET and diode (1) and the common-drain configuration of two JFETs (2) shows that for the given semiconductor parameters (Table II), the series-diode configuration produces less losses and, therefore, is selected for implementation

$$P_{L,\mathrm{JFET,Diode}} = 0.55\,\Omega \cdot 6^2\,\mathrm{A}^2 + 1.6\,\mathrm{V} \cdot 6\,\mathrm{A} = 29.4\,\mathrm{W} \quad (1)$$

$$P_{L,\mathrm{JFET,JFET}} = 0.55\,\Omega \cdot 6^2\,\mathrm{A}^2 + 2.8\,\mathrm{V} \cdot 6\,\mathrm{A} = 36.6\,\mathrm{W}. \quad (2)$$

C. CLBBC Specifications

The CLBBC power specifications are determined by the rating of the available SiC JFETs. In order to provide a wide switching-frequency range for optimization purposes and to be able to investigate the EMI performance of ac–ac converters, the nominal switching frequency above the start of the Special International Committee on Radio Interference (CISPR 11) EMI norm of 150 kHz is selected to be 200 kHz. The overall design requirements can be summarized as follows.

1) Exclusively, SiC power semiconductors must be implemented.
2) The electromechanical construction aims for a compact design to enable converter-motor embedding. The input EMI filter, an additional common-mode (CM) output filter, and an auxiliary power supply should be integrated into the converter system.
3) Only ceramic capacitors are allowed to be used in the power circuit in order to investigate their suitability and performance in ac–ac converter applications and to enable a compact design.

D. Modulation Scheme

When considering space vectors, there are six active current vectors and three different zero vectors available for CSC topologies. Thus, there is one more zero vector compared with the standard two-level VSCs.

In the literature, a wide variety of different modulation schemes for current-source-type converters can be found [8], [9]. Basically, in all these modulation strategies, typically, two active current vectors and one or two zero vectors are used per modulation cycle. The main differences between the modulation methods are the number of switches involved in one modulation cycle, the different dependences between losses and voltage-to-current displacement angle, and on where the vector sequence starts and ends.

As previously stated, the intended load for the prototype CLBBC is either a permanent-magnet synchronous machine or an RL-type load if it is used as a utility interface between two three-phase mains systems. Both of these applications have in common that the stationary output stage-current displacement angle Φ_2 is close to 0° or 180°. Obviously, the CSC topology can also be operated at power factors other than one. Assuming a constant dc-link current, the advantage of the CSC is that the conduction losses are independent of the power factor and the modulation scheme, as the dc-link current continuously flows through four switches and four diodes. The switching losses, on the contrary, vary with the power factor

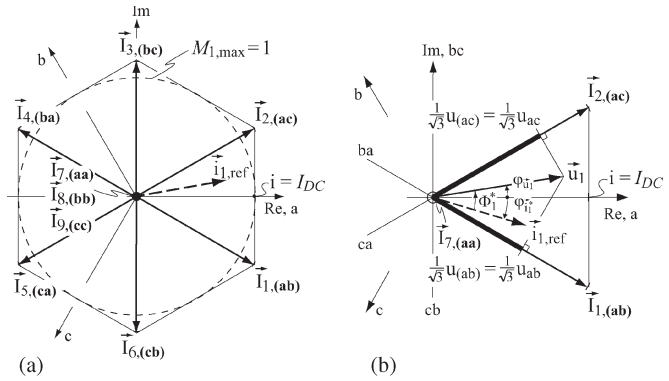

Fig. 4. (a) Space vectors for CSCs, shown for (a, b, c) input stage on mains. (b) Weighting of the vectors for a given reference $\vec{i}_{1,\mathrm{ref}}$.

for a given modulation scheme [8]. Therefore, the modulation scheme should be selected depending on the required power-factor range in order to maximize the converter efficiency. Due to the unity-power-factor requirement at the converter input, the phase-displacement angle Φ_1 is also close to 0° or 180° apart from a small offset for the stationary input EMI filter current-to-voltage displacement compensation. This means that the CLBBC modulation scheme has to result in low losses exactly for this operating condition and should naturally also be advantageous in terms of EMI.

A space-vector modulation scheme, which fulfils the aforementioned requirements, has been selected for implementation. It uses the two neighboring active vectors, i.e., $\vec{I}_1$ and $\vec{I}_2$, with $t_{1,\mathrm{on}} > t_{2,\mathrm{on}}$ of the actual current reference vector $\vec{i}_{1,\mathrm{ref}}$ and the corresponding switching loss-optimal zero vector $\vec{I}_7$, as shown in Fig. 4. The applied current-vector sequence of one modulation cycle, for example, in sector I is: $\vec{I}_7-\vec{I}_1-\vec{I}_2-\vec{I}_2-\vec{I}_1-\vec{I}_7$. For EMI purposes, the vector leading to the smaller line-to-line voltage switched to the dc-link of the two neighboring vectors is switched first. Consequently, this minimizes the voltage change per switching action in the dc-link.

E. Control

Due to the integration of the input and output filters into the CLBBC, the current measurement sensors can be placed beneficially in terms of converter control. Two current sensors are used to measure the output phase currents (after the CM filter) and one sensor for the dc-link current. At the same time, through observation of the actual output-stage switching state, the currents flowing into the output-stage capacitors can also be derived based on the dc-link current measurement. This means that, with only three current sensors, all relevant output currents can either be measured or calculated. The following signals are measured and used for modulation and control: three input and three output voltages, the dc-link current, and two output phase currents.

The basic idea for designing an appropriate control scheme is the consideration of the apparent system dynamics.

1) The switching frequency of 200 kHz provides a theoretically maximum-control bandwidth of approximately 15 kHz to 20 kHz.
2) The determined dc-link inductance allows a minimum magnetization time from 0 A to nominal dc-link current of 6 A within a switching period of 5 μs.
3) The load time constants (inductance of permanent-magnet synchronous motor or coupling inductors for mains application) are in the millisecond range.

This allows the application of the same decoupling principle of individual control loops as used for cascaded control systems, where the inner (fast) control loops can be designed independently of the outer (slow) control loops. Compared with the decoupling approach for cascaded control loops, for the CLBBC system, decoupling does not only occur on control level but also on the system level, due to the difference in time constants. For simplicity, Fig. 5 shows the implemented control scheme for operation on an RL-type load. The quantities to be controlled are the dc-link current and the converter output voltage. The aforementioned concept enables decoupling the dc-link current control from the output voltage control. The dc-link current control loop is the fast loop, while the output voltage is the slow loop. For the best possible load-current response time, the dc-link current is always controlled to be at its nominal level of 6 A, taking into account that the losses are increased. From a control point of view, the CLBBC is a series connection of a buck-type current-source rectifier and boost-type current-source inverter. For the present control scheme, the CLBBC is restricted to buck-type operation.

The selected strategy for the RL-type load is to control the desired CLBBC output voltage and frequency by the output stage and the dc-link current by the input stage. The overall control scheme is digitally implemented in a DSP and optimized for processing speed. The achieved control-cycle speed is 100 kHz, leading to an average system delay time of 10 μs in the control loop. The dc-link current is controlled with a standard proportional–integral (PI) controller. The closed-loop current-control bandwidth is limited by the DSP control cycle speed of 100 kHz and is tuned for 7 kHz to provide enough resolution. The output-stage control consists of a PI voltage controller that generates the required output-current reference vector. The closed-loop voltage-control bandwidth is adjusted for 200 Hz based on the load requirements. The input-current reference is then calculated by feedforward (precontrol) of the estimated output power and the difference of the measured link current and its reference value.

For operation with a permanent-magnet synchronous machine, the control scheme needs simply to be extended with the dq reference-frame machine model and the output-stage filtering capacitors as suggested in [4]. The switching-frequency-related decoupling principle is still valid. An alternative control method for operation is presented in [10].

F. Losses

With the modulation and control scheme defined, the semiconductor losses and, consequently, the overall converter losses can be analytically calculated [11], [12]. The losses are modeled and evaluated for unity input and output power factor, a constant dc-link current of 6 A, a device junction temperature of 125 °C, and an input and output modulation index of 95%. This

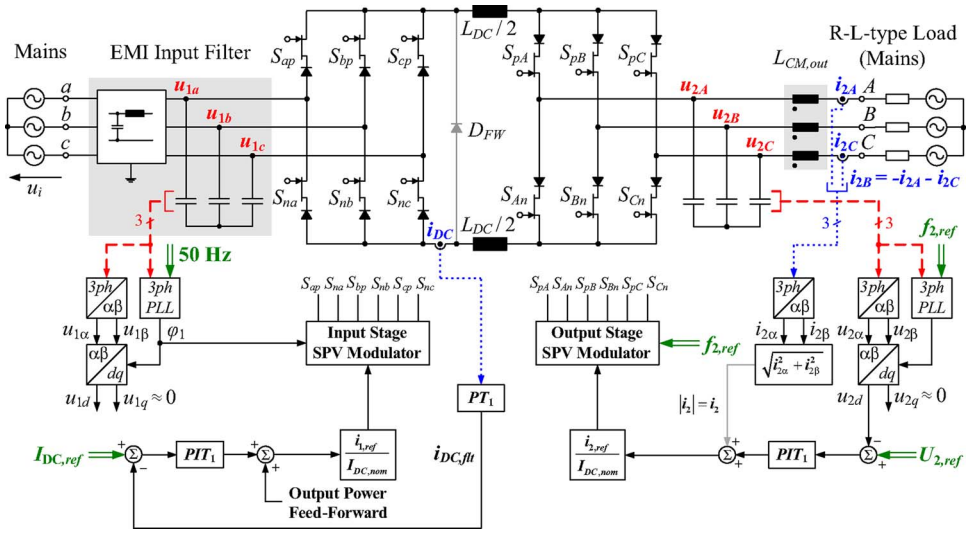

Fig. 5. Simplified dynamic feedback control system, shown for an RL load. Dashed (red): voltage measurement, dotted (blue): current measurement, and double line (green): input/feedforward quantities. (Saturation and antiwindup elements are not shown.)

corresponds to the operating-point settings for nominal output power P_2 of 2.5 kW.

The conduction losses for the input stage $P_{C,\mathrm{Inp}}$ and output stage $P_{C,\mathrm{Out}}$ can be determined by calculating the average current I_{avg} and the rms current I_{rms} through the devices and applying them to (3). U_F is the diode forward voltage drop, r_{FD} is its differential resistance, and $r_{\mathrm{DS,on}}$ is the ON-resistance of the JFET

$$\begin{aligned} P_{C,\mathrm{Inp}} &= P_{C,\mathrm{Out}} \\ &= 6 \cdot \left(U_{D0} \cdot I_{\mathrm{avg}} + (r_{\mathrm{FD}} + r_{\mathrm{DS,on}}) \cdot I_{\mathrm{rms}}^2\right) \\ &= 59\ \mathrm{W} \end{aligned} \tag{3}$$

$$I_{\mathrm{avg}} = \frac{I_{\mathrm{DC}}}{3} = 2\ \mathrm{A}$$

$$I_{\mathrm{rms}} = \frac{I_{\mathrm{DC}}}{\sqrt{3}} = 3.46\ \mathrm{A}. \tag{4}$$

The equations for calculating the switching losses are derived based on the implemented modulation scheme and parameterized with switching-loss measurement data (cf., Fig. 13). For that purpose, the switching-loss energy is represented with a voltage- and current-dependent loss-energy polynomial $w(u, i)$ according to (5). The coefficients K_1 to K_4 are summarized in Table II for a nominal switched dc-link current of 6 A and a junction temperature of 125 °C. For the series connection of JFET and diode, four different switching actions can be identified: JFET and diode turn-on and turn-off for a positive and a negative commutation voltage. The resulting switching losses are JFET turn-on and turn-off losses and diode turn-off (reverse-recovery) losses. For comparison, the JFET turn-on energy is 103 μJ, the turn-off energy is 19 μJ, and the diode turn-off energy is 12 μJ, for a switched voltage of 400 V and a current of 6 A. The diode turn-on losses are negligible

$$w(u, i = I_{\mathrm{DC}}) = w(u) = K_1 \cdot u^3 + K_2 \cdot u^2 + K_3 \cdot u + K_4. \tag{5}$$

The loss polynomial is then evaluated for the JFETs and diodes of the input and output stage by averaging the applied device voltage and current during switching over one input- and output-stage period. The procedure to calculate the input- and output-stage switching losses is identical and is given for the output stage, as an example, considering the high-side switch S_{pB} and the high-side diode D_{pB}. The switching losses for the JFET or the diode can be calculated according to

$$P_{S,\mathrm{Out,J/D}} = \frac{1}{2\pi} \cdot f_S \int_0^{2\pi} w(u_\mu)\, d\varphi \tag{6}$$

$$u_\mu = \hat{U}_2 \cdot \cos(\varphi + \Phi_2). \tag{7}$$

u_μ represents the commutation voltage across the JFET and the diode. $\hat{U}_2$ is the output-stage voltage and Φ_2 the displacement factor. Turn-on and turn-off switching losses occur in the JFET S_{pB} for $u_\mu > 0$. The diode turn-off losses in D_{pB} are generated for $u_\mu < 0$. The total output-stage switching losses can then be calculated by evaluating (6) for the selected modulation scheme and for $\Phi_2 = 0$, which leads to

$$\begin{aligned} P_{S,\mathrm{Out}} &= 6 \cdot \frac{1}{2\pi} \cdot f_S \cdot \left(\int_{\pi/6}^{\pi/3} w(u_\mu)\, d\varphi + \int_{\pi/3}^{\pi/2} w(u_\mu)\, d\varphi \right) \\ &= 29\ \mathrm{W} \end{aligned}$$

$$k_i = k_{i,\mathrm{JFET,on}} + k_{i,\mathrm{JFET,off}} + k_{i,\mathrm{Diode,off}}. \tag{8}$$

The total input-stage switching losses $P_{S,\mathrm{Inp}}$ are determined identically to the output-stage switching losses and equal to 33 W. The total CLBBC losses, including the additional 25 W for auxiliary supply, filtering component, and dc-link inductor losses for the considered operating point, are 205 W. This results in a predicted converter efficiency of 92.4%. The outcomes of the loss calculation are summarized in Fig. 6. A similar procedure for calculating the converter efficiency based on experimental loss-measurement data is given for MCs in [13].

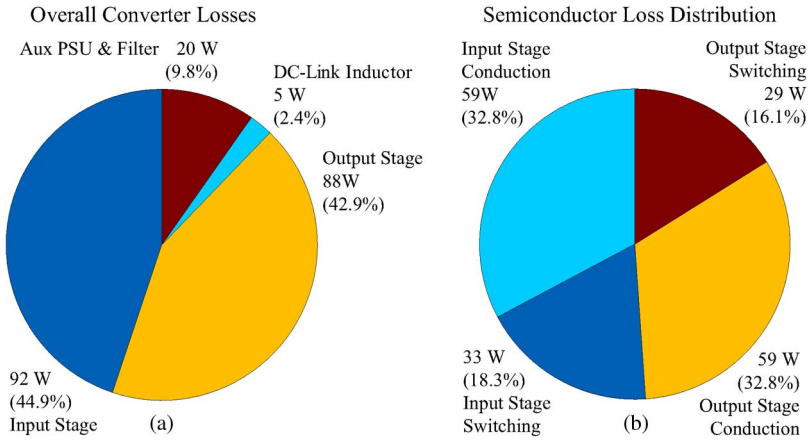

Fig. 6. (a) Overall converter losses. (b) Semiconductor-loss distribution for nominal output power at $T_J = 125\ ^\circ$C.

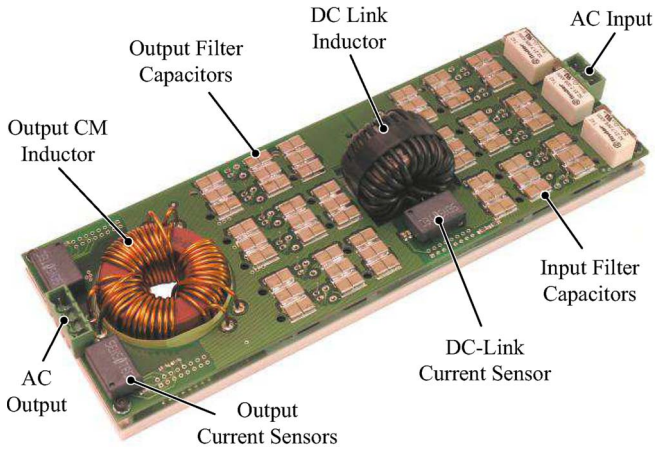

Fig. 7. Power board, showing the essential components.

If the 200-kHz CLBBC, for comparison, would be implemented with Si-MOSFETs with similar V/I ratings (IXYS IXFR16N120, 1200 V, 9 A, $r_{\mathrm{DS,on}} = 1.9\ \Omega$ at $T_J = 125\ ^\circ$C) and the same SiC diode, the estimated efficiency would be 87% compared with 92.4% for the All-SiC implementation. This is mainly due to the difference between the ON-resistance of the Si MOSFET and the SiC JFET. Si IGBTs do not have favorable characteristics when operated at 200 kHz.

G. Construction Concept

The physical construction of the CLBBC consists of a planar arrangement in which a stack is assembled from individual printed circuit boards (PCBs). The stack is designed such that power flows in through the EMI input filter and then directly through the input stage, dc-link, and output stage of the power board. The PCBs in the stack, starting at the bottom, are the power board, gate-driver board, DSP control and measurement board, and EMI board (Fig. 7). A base plate is used as a thermal interface to a variety of cooling systems for testing purposes and has the same volume as a high-performance water-cooled heat sink. The resulting outer dimensions of the CLBBC are 230 mm $\times$ 80 mm $\times$ 65 mm, corresponding to a boxed volume of 1.2 L (73 in^3). This results in a power density of 2.4 kVA/L (40 W/in^3). The actual power density for the given CLBBC is mainly limited by the current rating of the SiC JFETs and could easily be doubled by paralleling two JFET dies.

H. Power Circuit

The power board, shown in Fig. 7, contains the interconnections for the three-phase input from the EMI filter and the three-phase output to the load, the input and output capacitors, the dc-link connection to the inductor, and the three low-profile magnetoresistive current sensors (Sensitec CDS4006). These sensors have a typical bandwidth of 150 kHz.

The four-layer PCB separates the input rectifier stage and the output inverter stage with the high-frequency link inductor. The ac filter capacitors are soldered directly on the power board above the JFET switches in order to provide a degree of overvoltage protection, a low-impedance connection, and improved filtering.

I. Gate Drives

To turn off the SiC JFET, a negative-bias voltage less than the pinchoff voltage is required. The gate resistor R_1 equals 10 Ω and is selected to provide a compromise between switching speed and overshoot for the given layout. Due to the present processing variations in the SiC JFET's pinchoff voltage (-15 to -23 V) and gate–source breakdown voltage, a gate-driver concept has been developed that includes a dc blocking capacitor C_1 as shown in Fig. 8 [14]. This capacitor blocks and protects the gate junction from any dc current caused by the applied turn-off voltage (-25 V) exceeding the gate–source breakdown voltage. The capacitor is sized to be 47 nF to ensure a correct time constant with R_1 for operation at 200 kHz. R_3 is set to 12 kΩ to provide high-ohmic discharging of C_1, and the diode D_1 (PMEG40) prevents positive gate voltages. The additional turn-off impedance path (D_2, R_2) is implemented to optionally balance turn-on and turn-off speeds due to component variation. In the experimental implementation, D_2 and R_2 are not populated. To ensure a low delay time in the switching signals, which is required for high-frequency operation, a magnetic isolator (ADuM1100) is used followed by a 4-A gate-drive IC (IXDN404). The total signal propagation time is only 30 ns. An isolated -25-V supply is implemented for each gate driver by a full-bridge

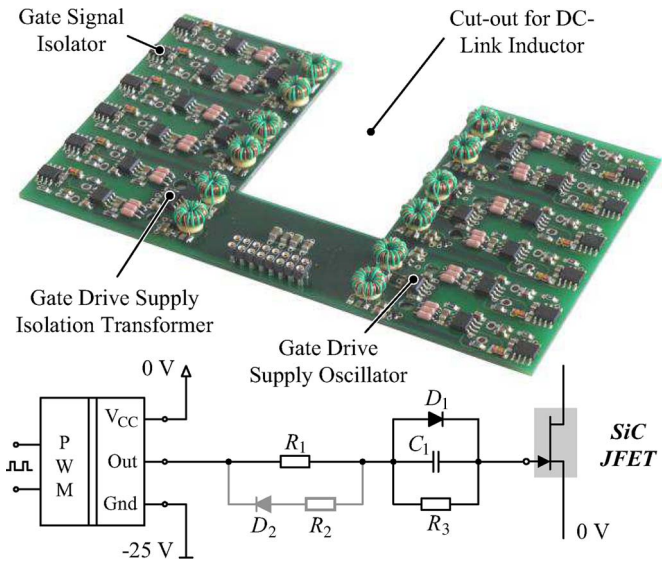

Fig. 8. Gate-driver board with schematic of the gate-drive circuit.

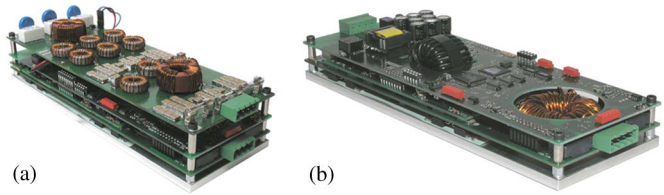

Fig. 9. Hardware prototype of the All-SiC JFET CLBBC. (a) Complete CLBBC, dimensions 230 mm × 80 mm × 65 mm. (b) CLBBC without EMI input filter board, showing the DSP/Field-programmable gate array control and measurement board with wide input-voltage-range auxiliary power supply.

IC (MAX256) and a small toroidal transformer followed by a rectifier circuit.

J. DC-Link Inductor

The main advantage of increasing the switching frequency is to reduce the size and weight of the passive components. The dc-link inductor is the most significant passive component of the All-SiC JFET CLBBC (see Fig. 9). Volume, weight, and losses are the key criteria for its design.

In a first step, the required inductance value has to be calculated. The approach is to limit the dc-link current ripple $\Delta I_{L,\mathrm{DC}}$ to 15% of the nominal dc-link current of 6 A, which leads to $\Delta I_{L,\mathrm{DC}} \approx 1$ A. This is a reasonable value in terms of dynamic performance [15] and typical ac core losses. The apparent dc-link ripple can be derived based on the equations for the modulation scheme as a function of the dc-link inductance L_{DC}, the input and output stage modulation indexes M_1, M_2, the switching frequency f_S, the input and output voltages $\hat{U}_1$, $\hat{U}_2$, and the input- and output-stage current reference angles $\varphi_{I1,\mathrm{ref}}$, $\varphi_{I2,\mathrm{ref}}$ according to

$$\Delta I_{L,\mathrm{DC}}(M_1, \hat{U}_1, \varphi_{I1,\mathrm{ref}}, M_2, \hat{U}_2, \varphi_{I2,\mathrm{ref}}, f_S)|_{\max}. \quad (9)$$

Equation (9), evaluated for L_{DC} leads to

$$L_{\mathrm{DC}} = \frac{3 \cdot (2 - \sqrt{3}) \cdot \hat{U}_1}{4 \cdot \Delta I_{L,\mathrm{DC}} \cdot f_S} = 327\ \mu\mathrm{H}. \quad (10)$$

Core	2 stacked Magnetics MPP 55071-A2
Winding	57 turns
Wire	Multi-stranded copper wire (0.8 mm^2)
Inductance	400 µH at 0 A, 200 kHz
	320 µH at 6 A, 200 kHz
Losses	5.1 W
Weight	120 g
Volume	40 cm^3 = 2.4 in^3

Fig. 10. Implemented dc-link inductor with construction data.

Different magnetic materials and inductor-construction principles such as planar E and SMD ferrite cores, toroidal and E powder cores, and tape-wound C-cores have been analyzed regarding losses, size, fringing flux, and cooling performance. Toroidal powder-core materials (with distributed air gap) provide the best compromise between losses, cooling, and size due to the dc bias.

The power-board layout allows splitting the dc-link inductance into two equal inductors for CM EMI purposes (one for the positive link and one for the negative link, Fig. 1) or using just a single-link inductor. Fig. 10 shows the implemented single link inductor and key data. There are two reason for selecting a single link inductor: First, it can be constructed more compactly as only one winding is required, and, second, in view of the required CM attenuation, the splitting of the dc-link inductor would only provide an additional CM inductance of $L_{\mathrm{CM,DC}} = L_{\mathrm{DC}}/4 = 100\ \mu$H, compared with 7.2 mH at 200 kHz in the total CM path. Therefore, the additional CM attenuation provided by splitting the dc-link inductor is negligible.

K. Integrated EMI Input and Output Filters

An EMI input and an output filters are required to meet CISPR Class A-conducted emission (CE) levels. The filter-design procedure is a combination of a time and frequency domain analysis using analytical calculations and simulations. It is based on differential-mode (DM) and CM equivalent circuits of the CLBBC system shown in Fig. 11(a) and (b). Several simplifications are assumed in order to reduce the calculation effort: The switching waveforms do not account for the influence of inner converter nonidealities, the circuits are considered to be symmetric with respect to the three phases, and the parasitics of the passive components are not considered

$$u_{\mathrm{CM}} = \frac{u_{a,\mathrm{PE}} + u_{b,\mathrm{PE}} + u_{c,\mathrm{PE}}}{3} - \frac{u_{A,\mathrm{PE}} + u_{B,\mathrm{PE}} + u_{C,\mathrm{PE}}}{3}. \quad (11)$$

A volume-minimized design procedure is used, which minimizes the value of the DM inductive components. This can be achieved by increasing the amount of DM capacitance, as the capacitance per volume ratio is much higher than the inductance per volume ratio if ceramic capacitors are used [16, Figs. 25–27]. The maximum amount of capacitance per phase is selected such that at nominal output power, the voltage-to-current lag at the filter input is equal to or less than 5°, leading to approximately 6 μF per phase. The key point of the filter design is the determination of the DM and CM frequency spectrum of the converter, represented by the DM current and CM voltage sources. These noise sources are then Fourier transformed and injected into equivalent circuits to calculate the required filter attenuation by determining the difference between the Line

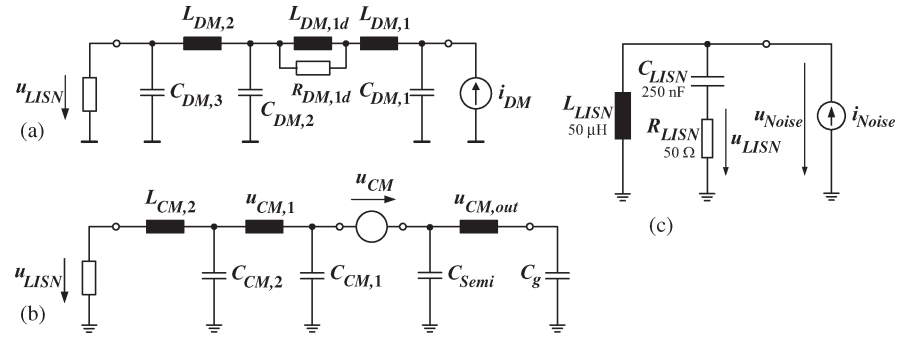

Fig. 11. (a) CLBBC DM equivalent circuit. (b) CLBBC CM equivalent circuit. (c) LISN equivalent circuit.

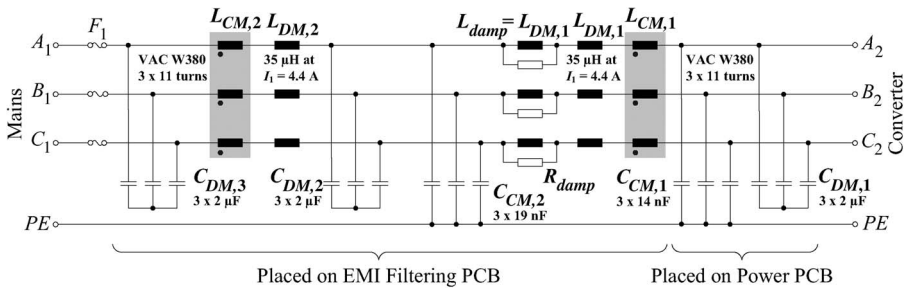

Fig. 12. Schematic of the implemented input EMI filter.

Impedance Stabilization Networks (LISN) voltage $u_{\rm LISN}$ and the CISPR A quasi-peak limit (79 dBμV from 150 to 500 kHz and 73 dBμV from 500 to 30 MHz). In order to model the LISN, the most widespread $50\ \Omega/50\ \mu$H LISN configuration, shown in Fig. 11(c), is implemented, which is defined in EMC standards, specifically in CISPR 16. The filter is designed for nominal operation and an output power factor of $\Phi = 1$.

For the DM filter model, only one phase needs to be considered as symmetrical mains are assumed. The DM source $i_{\rm DM}$ equals the unfiltered CLBBC input current as the converter features a current-impressed input (e.g., $i_{\rm DM} = i_a$). The actual DM source is generated by numerical simulation of the input phase current. The CM equivalent circuit uses the CM voltage $u_{\rm CM}$ as noise source and accounts for the dominant components in the CM path. $u_{\rm CM}$ is calculated based on simulation results as the difference between the unfiltered converter input to output CM voltage as shown in (11), and $u_{i,\rm PE}$ and $u_{I,\rm PE}$ correspond to the converter input and output voltage referenced to protective earth (PE). $C_{\rm Semi} = 250$ pF models the output-stage power semiconductor capacitance to PE. The measured parasitic capacitance of a TO-220 package to the heat sink (PE potential) is approximately 20 pF. The parasitic capacitance of the input-stage semiconductors is included in the capacitance $C_{\rm CM1}$. C_g represents the resulting capacitance to PE of the load machine. The capacitance of C_g has been determined through measurements of the target permanent-magnet synchronous load machine (Lust LST-127) and is set to 5 nF. The requirement for the CM output inductor is to provide enough impedance to keep the resulting CM rms voltage for the switching frequency and its harmonics across C_g lower than 15 V. This allows limiting the motor-bearing currents to a harmless level [16].

For both equivalent models, the LISN voltage $u_{\rm LISN}$ is processed similar to an EMC test receiver to find the worst case noise peak value [17]. The filtering components are then designed such that the DM and CM spectra fulfill CISPR class A norm. For the DM filter, a margin of 5 to 6 dB is used; for the CM filter, a margin of approximately 10 dB is used. Fig. 12 shows the resulting input EMI filter with its parameters. For the output CM inductor, a VAC 424 core with 3×18 turns is implemented.

III. Experimental Performance at 200 kHz

A. Characteristic Waveforms and THD

The following measurements demonstrate the switching behavior of the SiC JFETs and the operation of the CLBBC for a gate resistance of $R_1 = 10\ \Omega$ and a dc blocking capacitance of $C_1 = 47$ nF.

Fig. 13 presents the drain–source voltage and the drain–current waveforms for inductive switching of a low-side output-stage JFET generated with a double-pulse test. A turn-on and turn-off time of approximately 30 ns is achieved. The load has an inductance of 160 μH with a parallel capacitance of 40 pF. From these measurements, the switching-loss data in Table II is generated.

The CLBBC input and output voltage and current waveforms at nominal output power for an RL load (50 Ω, 1.5 mH) are shown in Fig. 14. The input frequency is 50 Hz; the output frequency is 40 Hz. As can be seen, the input and output phase currents are of sinusoidal shape, which proves proper operation of the implemented modulation scheme. The semitriangular voltage-waveform shape is caused by the voltage (E-field)-dependent variation of the selected ceramic ac filtering capacitors. The input current is slightly leading the input voltage in consequence of the capacitive behavior of the CLBBC input filter, as the stationary active filter current to voltage lead compensator is deactivated.

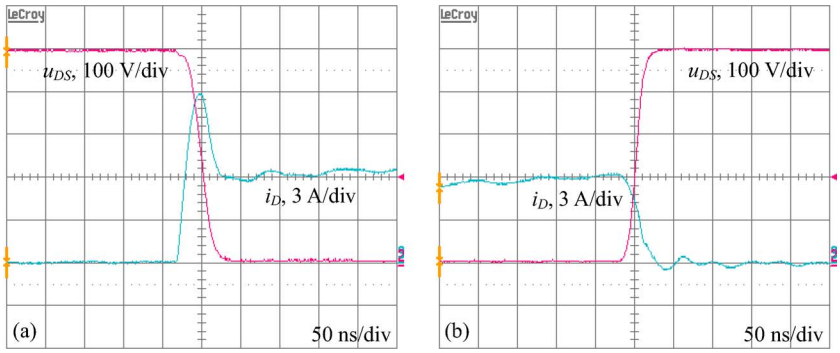

Fig. 13. SiC JFET double-pulse test for a switched voltage of 500 V and a switched current of 6 A at $T_J = 125\,^{\circ}\mathrm{C}$. (a) SiC JFET turn-on. (b) Turn-off switching waveforms, showing the drain–source voltage u_{DS} and the drain–current i_D.

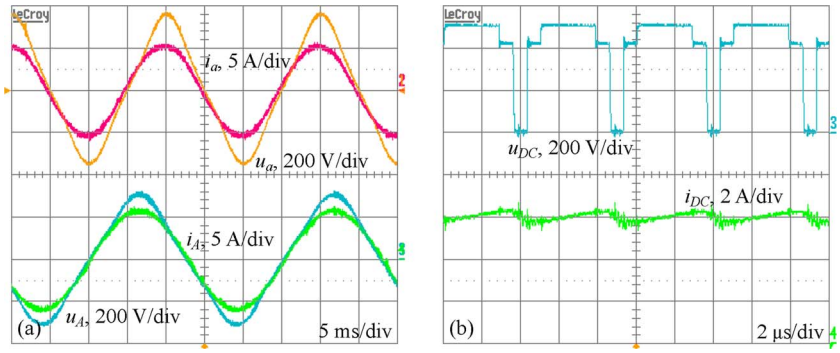

Fig. 14. Nominal operation with RL load (50 Ω, 1.5 mH). (a) CLBBC input and output voltage and current waveforms. (b) DC-link voltage and current waveforms.

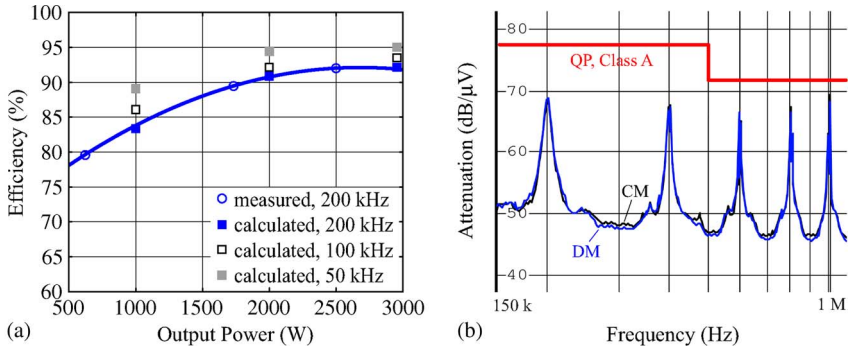

Fig. 15. (a) Measured efficiency versus output power on RL load. (b) Quasi-peak CE EMI measurement result up to 1 MHz: blue, DM; black, CM.

The measured THD for nominal operation is 5%. The comparatively high THD value can be explained with the aforementioned nonlinear behavior of the filtering capacitors and the resulting distortion of the capacitor-voltage waveform. By replacing the implemented X7R ceramic capacitors by C0G ceramic capacitors, the THD can be improved considerably, as C0G dielectric material is virtually insensitive to voltage, frequency, and temperature variation. Unfortunately, the capacitance per volume ratio of C0G ceramic capacitors typically is lower by a factor of five compared with X7R.

B. Efficiency

The overall converter efficiency is measured for different output power levels for an RL load (50 Ω, 1.5 mH), a converter input frequency of 50 Hz, and an output frequency of 40 Hz. The fitted efficiency curve is plotted in Fig. 15(a). The maximum efficiency is 92% and matches well with the analytically predicted values. Using the analytical model, the efficiency for discrete values of switching frequency and output power is also shown in Fig. 15(a). As can be seen, if the switching frequency is decreased to 50 kHz, the maximum efficiency increases to 95.5% at nominal output power due to the reduction of switching losses. To maintain the same current ripple in the dc-link inductor, the inductance needs to be increased by a factor of four. Therefore, there is a tradeoff between reduced losses and increased passive-component volume. In order to determine a volume-optimal switching frequency, a full analysis needs to be performed taking into account both the thermal and electromagnetical component properties as proposed in [16], [18].

C. CE EMI Measurements

The prototype All-SiC CLBBC (Fig. 1) has not yet been constructed with an appropriate enclosure. Therefore, CISPR 11 Class A CE levels obviously cannot be fulfilled over the full

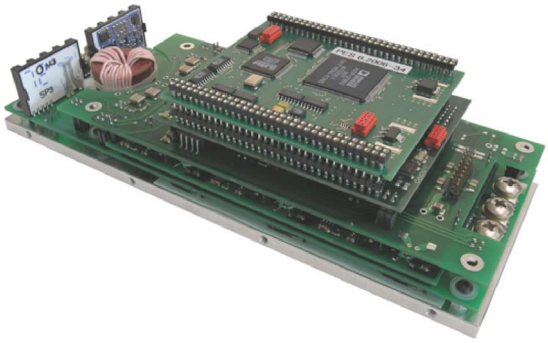

Fig. 16. 200-kHz 2.5-kVA All-SiC JFET IMC, shown without EMI input filter. Base area: 220 mm × 80 mm.

frequency range from 150 to 30 MHz, as the PE interconnection of the individual PCBs has too high impedance. For that reason, Fig. 15(b) presents the CE measurement results only in the frequency range of 150 kHz to 1 MHz, which seems to be representative for the given electromechanical construction. As can be clearly seen, the low-frequency performance below 1 MHz meets the CE Class A requirements, and at 200 kHz (switching frequency), there is a 9-dB margin as desired from the design. Above 1 MHz, the CLBBC CE levels exceed the Class A limits and therefore shows that a suitable enclosure with good PE bonding is required to avoid direct coupling between the power circuit and the mains input.

IV. Comparison With SiC IMC

Prior to the CLBBC, a 200-kHz All-SiC JFET IMC had been developed, as shown in Fig. 16 [18]. The IMC utilizes 18 SiC JFETs as power semiconductors and has an output power of 2.5 kVA. Compared with the CLBBC, the IMC input-current-waveform quality is similar, since the input stages of both converters are current impressed. In the case of the IMC, the current is impressed by the load inductance and in the case of the CLBBC, from the dc-link inductor. This accounts for their topology-based relationship and why they are appropriate for comparison.

On the load side, the IMC has a switched voltage output compared with the sinusoidal voltage of the CLBBC. This is an advantage for the CLBBC, since an additional voluminous output filter is not required. A three-phase sine-type output filter for the IMC would basically need three times the dc-link inductor of the CLBBC with a similar amount of output-filtering capacitance. From this perspective, the CLBBC allows a more compact higher power-density implementation compared with the IMC if a sine-type output is required. The disadvantage of the CLBBC compared with the IMC is the lower efficiency: 92% for the CLBBC and 94% for the IMC, both operating at a switching frequency of 200 kHz. In terms of conduction losses, this is mainly due to the absence of the series diode in the IMC output stage. Furthermore, the input stage of the IMC can be switched at zero current, enabling almost lossless switching apart from the parasitic effects.

V. Conclusion

In this paper, the design, construction, and operation of a fully digitally controlled All-SiC JFET CLBBC has been presented. The CLBBC can be operated at the desired switching frequency of 200 kHz and at nominal output power of 2.8 kVA. Given inherently by its topology, the CLBBC features an integrated sine-type output filter, which has been further enhanced by adding a CM stage to the converter output. The EMI requirements are achieved in the low-frequency range and could be met in the high-frequency range by using an appropriate converter enclosure.

Design and construction of a proper enclosure, providing low-impedance connection to PE, is subject to ongoing research and will hopefully provide a better understanding about the high-frequency suitability of the described filter-design procedure. Further work will also focus on the boost operation of the CLBBC. It is unlikely that the CLBBC will replace the well-known and well-established VLBBC. Nevertheless, for applications where mains-bridging capability or ultimate control performance (which requires sufficiently high converter internal energy storage) is of secondary importance, the SiC JFET CLBBC is a serious alternative. A further point in favor of the CLBBC is that due the absence of a link capacitor with thermally sensitive aging, the CLBBC could also be operated at elevated temperatures compared with a VLBBC. This would also match well with the advantageous temperature properties of SiC devices.

To conclude, the perceived undesirable normally on characteristic of the SiC JFET can be beneficially used in an appropriate topology such as the CLBBC and pinpoints the importance of matching semiconductor properties to the converter-topology requirements.

References

[1] P. W. Wheeler, J. Rodriguez, J. C. Clare, L. Empringham, and A. Weinstein, "Matrix converters: A technology review," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 276–288, Apr. 2002.

[2] C. Klumpner, P. Nielsen, I. Boldea, and F. Blaabjerg, "A new matrix converter motor (MCM) for industry applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 2, pp. 325–335, Apr. 2002.

[3] J. W. Kolar, F. Schafmeister, S. D. Round, and H. Ertl, "Novel three-phase AC–AC sparse matrix converters," *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1649–1661, Jul. 2007.

[4] K. Kuusela, M. Salo, and H. Tuusa, "A current source PWM inverter fed permanent magnet synchronous motor drive," in *Proc. PCIM*, Nuremberg, Germany, Jun. 22–24, 1999, pp. 315–320.

[5] M. Kazerani, "A direct AC/AC converter based on current-source converter modules," *IEEE Trans. Power Electron.*, vol. 18, no. 5, pp. 1168–1175, Sep. 2003.

[6] A. Kloenne and F. W. Fuchs, "High dynamic performance of a PWM current source converter induction machine drive," in *Proc. 10th EPE*, Toulouse, France, Sep. 2–4, 2003, pp. 1–10.

[7] M. Salo and H. Tuusa, "A vector-controlled PWM current-source-inverter-fed induction motor drive with a new stator current control method," *IEEE Trans. Ind. Electron*, vol. 52, no. 2, pp. 523–531, Apr. 2005.

[8] T. Halkosaari and H. Tuusa, "Optimal vector modulation of a PWM current source converter according to minimal switching losses," in *Proc. 31st Annu. IEEE PESC*, Galway, Ireland, Jun. 18–23, 2000, vol. 1, pp. 127–132.

[9] M. H. Bierhoff and F. W. Fuchs, "Loss minimized pulse width modulation of IGBT current source converters," in *Proc. 32nd Annu. IEEE IECON*, Paris, France, Nov. 7–10, 2006, pp. 1739–1744.

[10] M. Salo and H. Tuusa, "A new control system with a control delay compensation for a current-source active power filter," *IEEE Trans. Ind. Electron.*, vol. 52, no. 6, pp. 1616–1624, Dec. 2005.

[11] M. H. Bierhoff and F. W. Fuchs, "Semiconductor losses in voltage source and current source IGBT converters based on analytical derivation," in *Proc. 35th Annu. IEEE PESC*, Aachen, Germany, Jun. 20–25, 2004, vol. 4, pp. 2836–2842.

[12] C. J. Cass, R. Burgos, F. Wang, and D. Boroyevic, "Three-phase AC buck rectifier using normally-on SiC JFETs at 150 kHz switching frequency," in *Proc. 38th Annu. IEEE PESC*, Orlando, FL, Jun. 17–21, 2007, pp. 2162–2167.
[13] T. Friedli, L. Heldwein, F. Giezendanner, and J. W. Kolar, "A high efficiency indirect matrix converter utilizing RB-IGBTs," in *Proc. 37th IEEE PESC*, Jeju, South Korea, Jun. 18–22, 2006, pp. 1–7.
[14] S. Round, M. Heldwein, J. Kolar, I. Hofsajer, and P. Friedrichs, "A SiC JFET driver for a 5 kW, 150 kHz three-phase PWM converter," in *Conf. Rec. 40th IEEE IAS Annu. Meeting*, Oct. 2–6, 2005, vol. 1, pp. 410–416.
[15] F. W. Fuchs and A. Kloenne, "DC link and dynamic performance features of PWM IGBT current source converter induction machine drives with respect to industrial requirements," in *Proc. 4th IPEMC*, Xi'an, China, Aug. 14–16, 2004, vol. 3, pp. 1393–1398.
[16] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM converter power density barriers," in *Proc. PCC*, Nagoya, Japan, Apr. 2–5, 2007, pp. 9–29.
[17] M. L. Heldwein, T. Nussbaumer, and J. W. Kolar, "Differential mode EMC input filter design for three-phase AC-DC-AC sparse matrix PWM converters," in *Proc. 35th Annu. IEEE PESC*, 2004, vol. 1, pp. 284–291.
[18] T. Friedli, S. D. Round, and J. W. Kolar, "A 100 kHz SiC sparse matrix converter," in *Proc. 38th Annu. IEEE PESC*, Orlando, FL, Jun. 17–21, 2007, pp. 2148–2154.

Thomas Friedli (S'06) received the M.Sc. degree (with distinction) in electrical engineering from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in 2005. During his M.Sc. studies he focused on power electronics, control engineering, signal processing, and hardware development. His thesis research involved the design and implementation of a modular three-phase PFC input stage (Delta-Rectifier). He has been working toward the Ph.D. degree in the Power Electronic Systems Laboratory, ETH Zurich, since 2005.

From 2003 to 2004, he was a Student Trainee with the R&D Center for telecom power supplies, Power One. His research activities deal with the further development of current-source and matrix-converter topologies using silicon carbide power semiconductors and a comparative assessment of different ac–ac converter topologies.

Simon D. Round (SM'01) received the B.E. (Hons.) and Ph.D. degrees from the University of Canterbury, Christchurch, New Zealand, in 1989 and 1993, respectively.

From 1992 to 1995, he was a Research Associate in the Department of Electrical Engineering, University of Minnesota, and a Research Fellow at the Norwegian Institute of Technology, Trondheim, Norway. From 1995 to 2003, he was a Lecturer/Senior Lecturer in the Department of Electrical and Electronic Engineering, University of Canterbury, where he performed research on power-quality compensators, electric-vehicle electronics, and cryogenic power electronics. He was also a Power Electronic Consultant for Vectek Electronics, where he developed a "state-of-the-art" digital controller for high-power inverter systems. From 2004 to 2008, he was with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, as a Senior Researcher. Since October 2008, he has been with ABB Switzerland, Turgi, Switzerland, as the Control Platform Manager for the Power Electronics and Medium Voltage Drives Business Unit. His current research interests are in the areas of ultracompact power converters, applications of silicon carbide power devices, and three-phase ac–ac converters. He has over 100 publications in journals and international conference proceedings.

Dr. Round has been actively involved in the IEEE New Zealand South Section, where he was Vice-Chair and Chairman from 2001 to 2004. He was the recipient of the University of Canterbury Teaching Award in 2001.

Dominik Hassler received the M.Sc. degree from the Swiss Federal Institute of Technology (ETH) Zurich, Zurich, Switzerland, in May 2007. During his studies, he focused on power electronics, high-voltage technology, and embedded systems.

Since then, he has been with the Power Electronic Systems Laboratory, ETH Zurich, as a Research Associate, with main focus on hardware development and software engineering.

Johann W. Kolar (M'89–SM'04) received the Ph.D. degree (*summa cum laude/promotio sub auspiciis praesidentis rei publicae*) from the University of Technology Vienna, Austria.

Since 1984, he has been an Independent International Consultant in close collaboration with the Vienna University of Technology, in the fields of power electronics, industrial electronics, and high-performance drives. On February 1, 2001, he was appointed as a Professor and Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), Zürich, Switzerland. He has proposed numerous novel PWM converter topologies, and modulation and control concepts, e.g., the VIENNA rectifier and the three-phase ac–ac sparse matrix converter. He has published over 300 scientific papers in international journals and conference proceedings. He is the holder of 75 patents. His current research is on ac–ac and ac–dc converter topologies with low effects on the mains, e.g., for power supply of telecommunication systems, more electric aircraft, and distributed power systems in connection with fuel cells. His other main areas of research include the realization of ultracompact intelligent converter modules employing latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multidomain/multiscale modeling and simulation, pulsed power, bearingless motors, and power MEMS.

Dr. Kolar is a member of the Institute of Electrical Engineers of Japan (IEEJ) and the technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 to 2000, he served as an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS, and since 2001, as an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2002, he has been an Associate Editor for the *Journal of Power Electronics* of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the *IEEJ Transactions on Electrical and Electronic Engineering*. He was the recipient of the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005 and an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003. In 2006, the European Power Supplies Manufacturers Association awarded the Power Electronics Systems Laboratory of ETH Zürich as the leading academic research institution in Europe.