# Analysis of High Efficiency Three-Phase Two- and Three-level Unidirectional Hybrid Rectifiers

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***Abstract*— This paper presents highly efficient 3-phase high power factor hybrid rectifiers assembled by the parallel connection of a 3-phase diode bridge rectifier and series dc-dc boost converter with a 2- or 3-level unidirectional PWM rectifier. The idea is to obtain a rectifier that is robust, high efficient and simple as a diode based rectifier and also able to benefit from the PWM rectifier capability to reduce the line current harmonic content. Exemplary, 3-phase unidirectional hybrid systems built with a 2-level delta-switch rectifier and 3-level T-type or VIENNA 6-switch rectifiers are suggested. Additionally, control schemes appropriate for safeguarding the high power factor operation while improving the power sharing rating of the hybrid paralleled rectifier units and able to handle a phase loss without changing the controller structure, are proposed. In order to evaluate the studied hybrid rectifiers, first an efficiency comparison between 2- and 3-level hybrid systems with conventional PWM rectifiers is performed. After that, the loss calculations are extended to a variable chip area to allow a fair comparison between these rectifiers. Interestingly, it is shown that the presented hybrid systems can achieve not only higher efficiency but also require less silicon area than the single PWM rectifiers they are based on. Finally, experimental results obtained with an assembled unidirectional hybrid delta-switch rectifier prototype are presented in order to demonstrate the performance and advantages of this solution.**

***Index Terms*— 2- and 3-level converters, feedback control strategy, rectifier systems.**

## I. Introduction

In general, 3-phase ac-to-dc power converters can be classified into line- and self-commuted rectifiers [1]. The first, also known as passive rectifiers, employ diode and/or thyristor based switches, which switch at the zero crossing of the ac side currents. The former concept, also known as active or PWM rectifiers, uses semiconductor technologies, such as, IGBTs, MOSFETs, GTOs, IGCTs, and so forth, which are capable of actively controlling the ac side currents.

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Passive rectifiers are commonly inexpensive, very reliable and highly efficient. On the other hand, they usually inject significant current harmonics into the power grid and additional filtering concepts are necessary to attain unity power factor operation. Consequently, passive rectifiers do not meet IEC 61000-3-2/61000-3-4 guidelines [2].

From the power quality point of view, the active rectifiers are the most promising concept as they can operate at low current THD and high power factor. Nevertheless, they are more expensive, less reliable and display lower efficiency than passive rectifiers [3].

Regarding medium and high power applications, the pursuit for unity power factor rectifier topologies, which combine robustness, simplicity, low cost, and high power density with light weight, has lead the research in this area to a new class of ac-to-dc converters, the hybrid rectifiers [1]-[13]. The term “hybrid rectifier” denotes the parallel connection of a line- and a self-commuted converter [7]. Fig. 1 presents five hybrid rectifiers suitable for shaping the line currents, and also to control the dc-link voltage, $U_{DC}$. The bidirectional switches shown in Fig. 1(a)-1(d) can be implemented with many basic switch types as shown in Fig. 1(f) [13].

Hybrid rectifiers aim to embrace the best features of a passive rectifier and the advantages of active rectifiers. In general, the line-commuted based converter is set to operate with low frequency, processing the highest power rating, while the active system is adjusted to work at higher frequencies and lower power rating [1]. Therefore, a highly efficient rectifier system, capable of providing close to sinusoidal shaped line current can be assembled. When compared to rectifier systems based simply on connection of active rectifiers, the hybrid systems are usually cheaper, more robust and more efficient [7].

In this work the hybrid rectifier concept is distinguished from an ordinary parallel association of rectifiers. For instance, in an ac-to-dc system assembled by a parallel connection of two unity power factor rectifiers, the input current in each unit is ideally sinusoidal. Additionally, each rectifier part is normally set to operate at the same switching frequency and to equally share the total load power. On the other hand, the rectifier units of the hybrid arrangements can operate with different power ratings at different frequencies. In these systems the line currents with sinusoidal shape are obtained by the combination of the currents drained by each rectifier unit, which individually don’t necessarily display high power factor. Finally, hybrid rectifiers cannot be classified as active filters due to the fact that the self-commuted rectifier, in this case, processes high amounts of

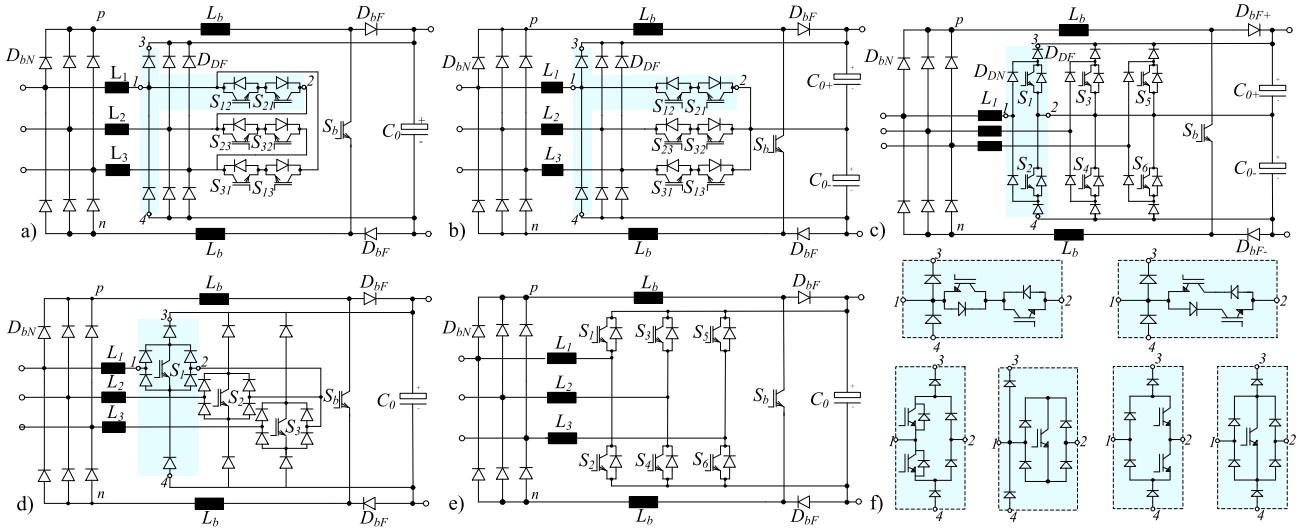



Fig. 1. Hybrid rectifier systems based on: (a) 2-level unidirectional delta-switch rectifier; (b) 3-level unidirectional T-type rectifier; (c) 3-level unidirectional VIENNA 6-switch rectifier (d) 2-level unidirectional wye-switch rectifier; and (e) 2-level bidirectional rectifier. (f) Alternative bidirectional (current) and bipolar (voltage) switches.

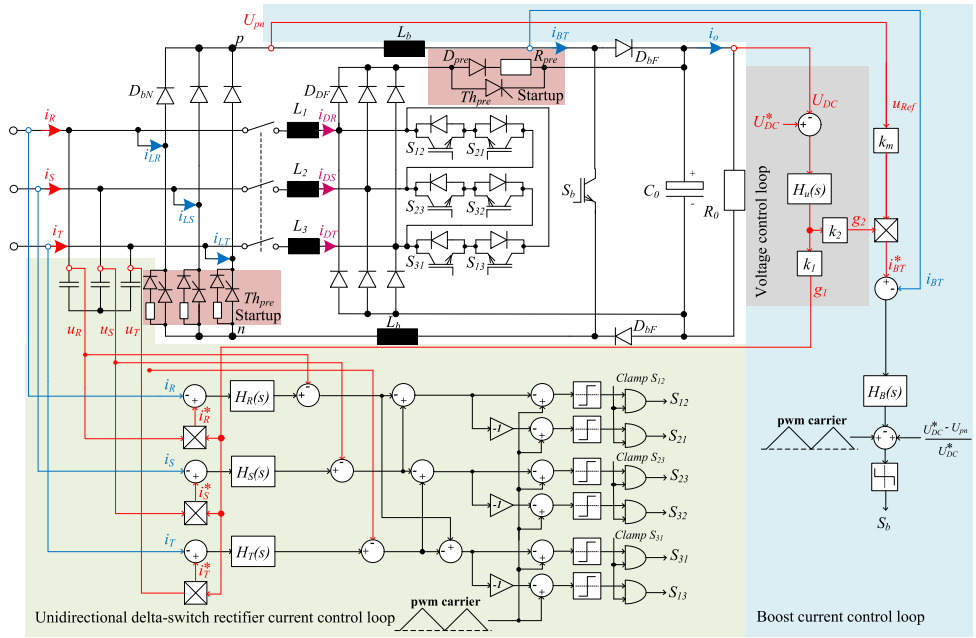



Fig. 2. Structure of the proposed unidirectional hybrid delta-switch rectifier and suitable control scheme. $i^*_{BT}$ is generated by multiplying the sensed rectified voltage, $U_{pn}$, rated by $k_m = 1/3$, with the conductance $g_2$. In order to effectively handle two phase operation the controllers $H_{R,S,T}(s)$ must employ P-regulators.

active power, while active filters are intended to process only reactive power [3].

In this paper, highly efficient 3-phase hybrid rectifiers with controlled dc-link voltage, capable of providing close to sinusoidal shaped line currents are presented. As shown in Fig. 1(a), 1(b) and 1(c), the proposed ac-to-dc systems are formed by the parallel connection of a 3-phase diode bridge rectifier and series dc-dc boost converter with a 3-phase unidirectional 2-level delta-switch rectifier or a 3-level T-type or VIENNA 6-switch rectifiers, respectively. In these hybrid systems, due to the unidirectional power flow limitation of the selected PWM rectifier, the instantaneous input power should present only positive values in order to be able to provide sinusoidal input currents. Therefore, following the idea that the diode bridge based rectifier can be set to operate at higher efficiency than the self-commuted structure, the optimal power sharing ratio between these circuits are typically found in the boundaries of the high power factor operation limit.

This work proposes two control schemes suitable to improve the power sharing ratio of the paralleled rectifier units of the studied hybrid converters, thus these systems can achieve higher efficiency than the control strategy suggested by [1]. Additionally, the control strategies are able to provide continued operation with sinusoidal input current shape during mains phase failure, i.e. interruption or voltage collapse of one mains phase, without changing the controller structure.

This article is organized as follows. Section II presents three unidirectional hybrid rectifier concepts, including their principle of operation. Subsequently, control methods well suitable for hybrid systems are presented in Section III. In

Section IV, for each one of the proposed rectifiers, analytical expressions for calculating the average and *rms* current of the power components are given. In Section V, in order to verify the advantages of the derived unidirectional hybrid rectifiers, a pure semiconductor efficiency comparison between these systems with the conventional PWM rectifier concepts used to assemble them is carried out. The analyses are extended to a variable chip area in order to allow a fair evaluation of these rectifiers. Finally, in Section VI experimental results obtained with a unidirectional hybrid delta-switch rectifier prototype are presented in order to demonstrate the performance and advantages of this solution.

## II. Unidirectional Hybrid Rectifiers

Fig. 1 shows five hybrid rectifiers suitable for shaping the line currents and also for controlling the dc-link voltage of the system. These converter concepts are constructed by the

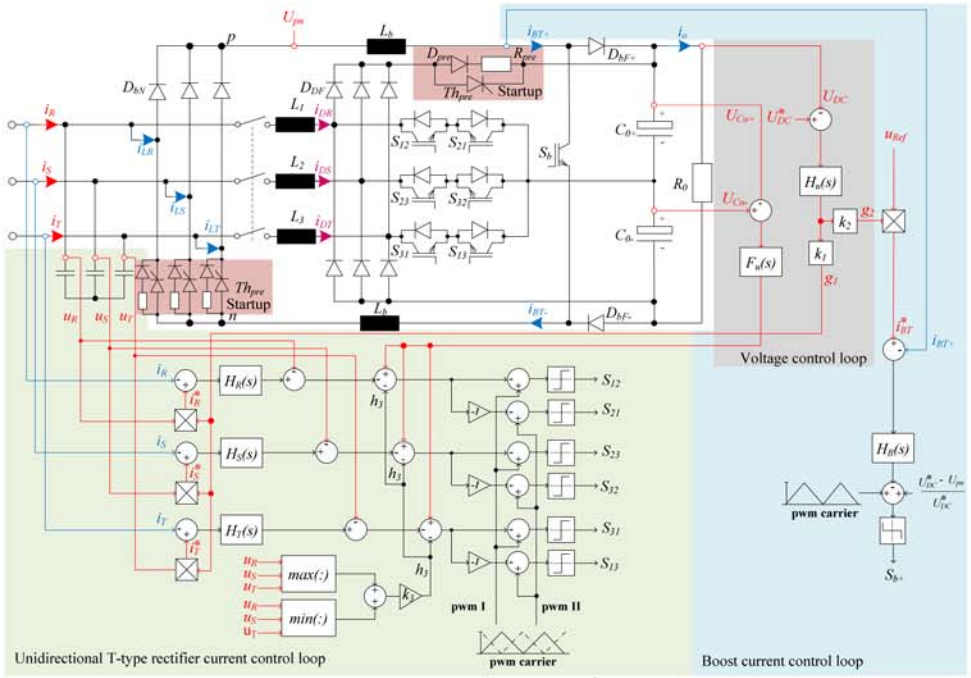



Fig. 3. Structure of the proposed unidirectional T-type rectifier and suitable control scheme. $i^*_{BT}$ is generated by multiplying the signal $u_{Ref}$ by the conductance $g_2$. The signal $u_{Ref}$ is derived from the grid voltages as shown in Fig. 5 or Table II. In order to effectively handle two phase operation the controllers $H_{R,S,T}(s)$ must employ P-regulators.

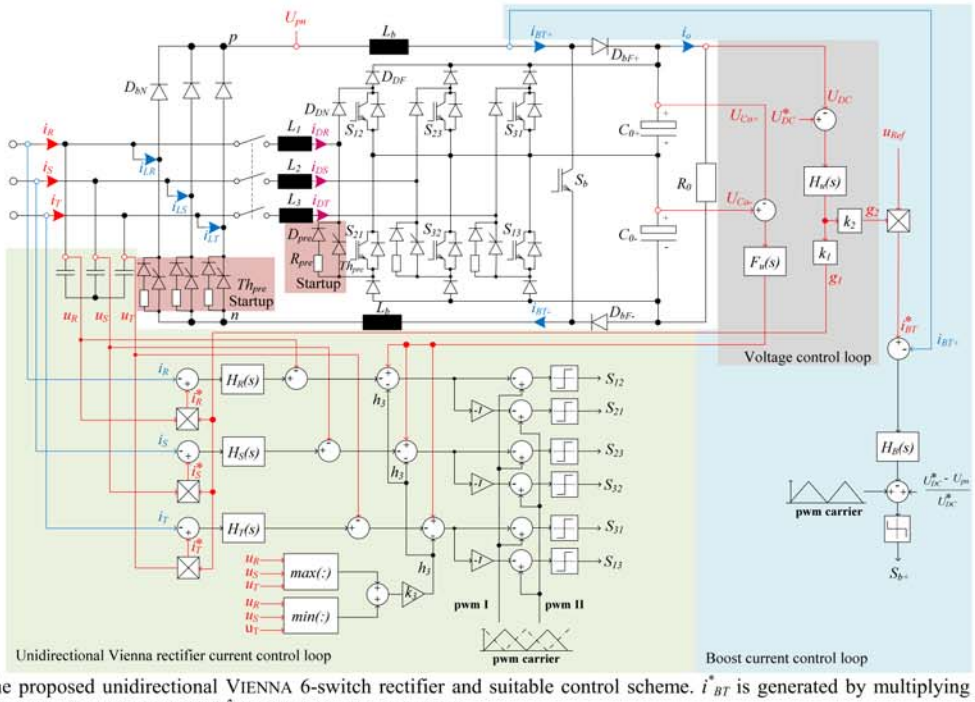



Fig. 4. Structure of the proposed unidirectional Vienna 6-switch rectifier and suitable control scheme. $i^*_{BT}$ is generated by multiplying the constant reference value $u_{Ref}$, given by half input voltage amplitude $\hat{U}_R/2$, with the conductance $g_2$.

parallel connection of a controlled 3-phase diode bridge boost rectifier with a 3-phase unity power factor boost-type rectifier. In Fig. 1(a) the self-commuted system is based on the 2-level unidirectional delta-switch converter technology, which was thoroughly analyzed in [14]. While for the hybrid converters depicted in Fig. 1(b), 1(c), 1(d) and 1(e), the 3-level unidirectional T-type rectifier, 3-level unidirectional VIENNA 6-switch rectifier, the 2-level unidirectional wye-switch topology and the 2-level bidirectional rectifier are employed, respectively. For more details about 3-level PWM rectifiers the reader is referred to [2], [15]-[18].

Due to the fact that the power processed by a hybrid converter is shared between the integrating rectifier units, operation with higher efficiency and robustness can be accomplished when compared to a single self-commuted rectifier solution. For hybrid rectifiers employing a bidirectional (current) self-commuted converter (c.f. Fig. 1(e)), the high power factor operation can theoretically be achieved for any combination of power shared between the compounding rectifiers. For example, if the line-commuted based rectifier is set to process 100% of the output power, $P_o$, the bidirectional system, working as shunt active power filter, will be able to compensate the current harmonics, attaining high power factor operation.

Unidirectional hybrid rectifiers have conditional high power factor operation, which is reliant on the rated active power processed by the self-commuted converter, $P_D = \alpha P_o$. Due to the unidirectional power flow characteristic of this converter, the high line power quality operation can only be achieved if the instantaneous current absolute values of the line-commuted rectifier, $i_{LR,LS,LT}$, are smaller than the absolute values of the line current references, $i_{R,S,T}$.

Fig. 2 shows a suitable circuit implementation of the 2-level unidirectional hybrid delta-switch rectifier, where the sinusoidal shaped line currents, $i_{R,S,T}$, are formed by the sum of the currents of the combined rectifiers, $i_{LR,LS,LT}$ and $i_{DR,DS,DT}$. Correspondingly, the output current, $i_o$, is derived from the sum of the output currents of each paralleled rectifier.

In order to achieve a better line power quality, the controlled dc-dc boost rectifier should operate in Continuous Conduction Mode (CCM). In contrast, the input currents of the delta-switch rectifier, $i_{DR,DS,DT}$, are controlled to allow high power factor operation.

3-phase 3-level unidirectional hybrid systems with similar principle of operation of the hybrid delta-switch rectifier can be seen in Fig. 3 and 4.

It is important to point out that the proposed feedback control strategies shown in Fig. 2 and 3 are especially suitable for unidirectional hybrid rectifiers. There, the current generation schemes presented in Fig. 5 are suggested in order to improve the maximum allowed power rating of the line-commuted topology which preserves the high power factor operation. The control scheme depicted in Fig. 4 was proposed by [1]. More details for these control strategies are given in Section III.

## III. CONTROL STAGE OF THE HYBRID RECTIFIERS

Suitable PWM control schemes for unidirectional hybrid rectifiers are illustrated in Fig. 2, 3 and 4. For these feedback controls, the voltage control loop establishes the DC voltage regulation and the output power sharing between the combined rectifiers of the hybrid system, which is defined mainly by the ratio of the gains $k_1$ and $k_2$.

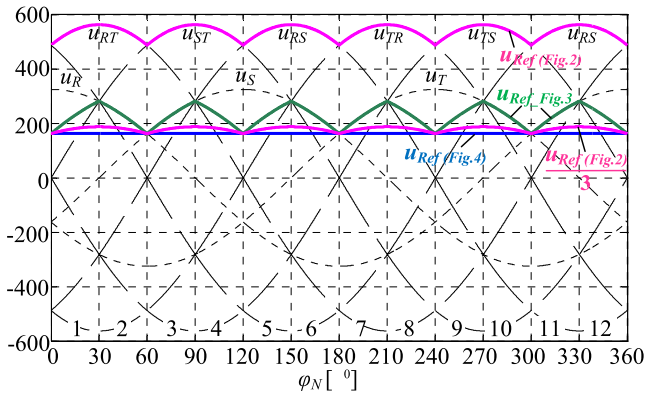



*Fig. 5. Current reference generation for the controlled dc-dc boost rectifier.*

Table. I. Delta-switch PWM modulation with the required clamping actions.

| Sector | $S_{12}$ | $S_{21}$ | $S_{23}$ | $S_{32}$ | $S_{13}$ | $S_{31}$ |
|---|---|---|---|---|---|---|
| 330°-30° | $pwm_{12}$ | 1 | 0 | 0 | $pwm_{13}$ | 1 |
| 30°-90° | 0 | 0 | $pwm_{23}$ | 1 | $pwm_{13}$ | 1 |
| 90°-150° | 1 | $pwm_{21}$ | $pwm_{23}$ | 1 | 0 | 0 |
| 150°-210° | 1 | $pwm_{21}$ | 0 | 0 | 1 | $pwm_{31}$ |
| 210°-270° | 0 | 0 | 1 | $pwm_{32}$ | 1 | $pwm_{31}$ |
| 270°-330° | $pwm_{12}$ | 1 | 1 | $pwm_{32}$ | 0 | 0 |

Table II. Current reference generation (cf. Fig. 5). $\hat{U}_R$ is the amplitude of the input voltage, $u_i$ is the phase voltage and $u_{ij}$ is the line-to-line input voltage.

| Sector | $u_{Ref}$ (Fig.2) | $u_{Ref}$ (Fig.3) | $u_{Ref}$ (Fig.4) | Sector | $u_{Ref}$ (Fig.2) | $u_{Ref}$ (Fig.3) | $u_{Ref}$ (Fig.4) |
|---|---|---|---|---|---|---|---|
| 0°-30° | $u_{RT}$ | $-u_T$ | $\hat{U}_R/2$ | 180°-210° | $u_{TR}$ | $u_T$ | $\hat{U}_R/2$ |
| 30°-60° | $u_{RT}$ | $u_R$ | $\hat{U}_R/2$ | 210°-240° | $u_{TR}$ | $-u_R$ | $\hat{U}_R/2$ |
| 60°-90° | $u_{ST}$ | $u_S$ | $\hat{U}_R/2$ | 240°-270° | $u_{TS}$ | $-u_S$ | $\hat{U}_R/2$ |
| 90°-120° | $u_{ST}$ | $-u_T$ | $\hat{U}_R/2$ | 270°-300° | $u_{TS}$ | $u_T$ | $\hat{U}_R/2$ |
| 120°-150° | $u_{SR}$ | $-u_R$ | $\hat{U}_R/2$ | 300°-330° | $u_{RS}$ | $u_R$ | $\hat{U}_R/2$ |
| 150°-180° | $u_{SR}$ | $u_S$ | $\hat{U}_R/2$ | 330°-360° | $u_{RS}$ | $-u_S$ | $\hat{U}_R/2$ |

Table. III. Unidirectional hybrid rectifier systems specification.

| | |
|---|---|
| Input voltage, $u_{R,S,T}$: | 230 Vrms |
| Input frequency, $f_N$: | 50 Hz |
| Switching frequency, $f_S$: | 50 kHz |
| DC-link voltage, $U_{DC}$: | 800 V |
| Output power, $P_0$: | 10 kW |
| Output capacitor, $C_0$: | 1.47 mF |
| DC inductor, $L_b$: | 1 mH |
| Delta-switch rectifier inductors, $L_{1,2,3}$: | 1 mH |

For the self-commuted rectifier, the line current references, $i^*_{R,S,T}$, are generated by multiplying the sensed mains voltages, $u_{R,S,T}$, by a reference conductance, $g_1$, which is defined by the superimposed output voltage controller, $H_u(s)$, rated by the established power loading sharing factor $k_1$. Together with a mains voltage feed-forward signal, the current controllers, $H_{R,S,T}(s)$, generate the required converter phase voltages. Subsequently, for the 2-level delta-switch system shown in

Fig. 2, these signals are converted into line-to-line voltage quantities. On the other hand, for the 3-level systems shown in Fig. 3 and 4 a feed-forward third harmonic signal is added to the main control loop [16]. Finally, two independent PWM signals are generated to command the active switches.

In order to improve the efficiency of the delta-switch rectifier the PWM signals are guided by clamping signals derived from the mains voltages. The resulting clamping actions, considering all $60^0$ space vector sectors, are shown in Table I. Therein, "1" specifies that the corresponding active switch is turned on, "0" designates the turn-off state, and *pwm* indicates that the transistor is modulated by the current controller. The modulation strategies for the 3-level T-type and VIENNA 6-switch rectifiers naturally incorporate clamping actions during the positive and negative semi-cycles of the mains voltages.

For the single-switch boost converter the current $i_{BT}$ is sensed and compared to the reference current signal, $i^*_{BT}$, which can be derived in three different ways as presented in Fig. 2, 3, 4 and 5 (cf. Table II). The error signal is applied to the current compensator $H_B(s)$ and the PWM modulator, incorporating a feed-forward control loop, generates the gate signal of the boost switch.

In the control strategy shown in Fig. 4, the currents are not optimally shared between both paralleled rectifiers. Therein, the hybrid rectifier, based on unidirectional PWM rectifiers, needs to limit the rating of active power processed by the line-commuted rectifier, $P_B$, into 55.1% of the output power, $P_o$, in order to allow sinusoidal shaped line currents. According to the concept of the hybrid rectifier, it is commonly desired that the fast switched self-commuted rectifiers process the least power possible in order to make the system more efficient. Therefore, the control proposed in Fig. 3 with $u_{Ref}$ derived from the grid voltages as shown in Fig. 5 or Table II, constitutes the optimum choice especially for high power applications (> 100 kW) where the switching frequency of the self-commuted rectifier could be set much higher than the other rectifier unit. Therein, the minimum rated active power processed by the self-commuted rectifier, $P_D$, which allows high power factor operation, is given by $P_D \approx 0.229 P_o$ (or $P_B \approx 0.771 P_o$). In the control proposed in Fig. 2, the minimum rated output power processed by the self-commuted rectifier, which allows imposed sinusoidal line currents, is given by $P_D \approx 0.392 P_o$ (or $P_B \approx 0.608 P_o$). The line current formation at the limit of high power factor operation for phase $R$ in each studied control scheme is shown in Fig. 6.

Note that the maximal rated active power of the line-commuted circuit $P_B = (1-\alpha_{min}) P_o$ (or $P_D = \alpha_{min} P_o$) is defined by the maximum averaged current passing through the inductor $L_b$ ($i_{Lb,avg}$) which guarantees that the instantaneous values of $i_{LR,LS,LT}$ are kept below the absolute value of the line currents, $i_{R,S,T}$. For the control strategies depicted in Fig. 2, 3 and 4 the value of $i_{Lb,avg}$ are given by (1), (2) and (3), respectively. By defining $i_{Lb,avg}$ as equal to the characteristic averaged current value of $L_b$ modeled as a function of the line-commuted structure output power as given by (4), the minimal rated power coefficient ($\alpha_{min}$) of the self-commuted converter can be found. The value of $\alpha_{min}$ for the control strategies shown in Fig. 2, 3 and 4 are given by (5), (6) and (7), respectively.

The simulation results showing the current formation of the proposed hybrid systems with the corresponding control schemes depicted in Fig. 2, 3, and 4, are presented in Fig. 7, 8 and 9, respectively. The converter specification presented in Table III is considered in this performance evaluation. The results display three operation modes defined by the power share rating of the hybrid systems' rectifier units. As can be observed, when the active power processed by the self-commuted converter ($P_D$) is smaller than $P_D < \alpha_{min} P_o$ the unidirectional concepts lose the high power factor operation.

The simulation results of the unidirectional hybrid delta-switch and T-type rectifiers operating with the proposed control strategies under transient conditions are compiled in Fig. 10 and 11, respectively. The results attest the feasibility of the proposed controls as the line currents, $i_{R,S,T}$, can effectively follow the sinusoidal input voltages, $u_{R,S,T}$, even after load steps or during mains phase loss.

$$i_{Lb,avg} = \frac{2\sqrt{3}P_o}{3\pi\hat{U}_R} \tag{1}$$

$$i_{Lb,avg} = \frac{2\left(\sqrt{3}-1\right)P_o}{\pi\hat{U}_R} \tag{2}$$

$$i_{Lb,avg} = \frac{P_o}{3\hat{U}_R} \tag{3}$$

$$i_{Lb,avg} = \frac{\left(1-\alpha_{\min}\right)P_o}{\hat{U}_R}\frac{\pi}{3\sqrt{3}} \tag{4}$$

$$\alpha_{\min} = 1+\frac{6}{\pi^2} \tag{5}$$

$$\alpha_{\min} = 1+\frac{6\sqrt{3}-18}{\pi^2} \tag{6}$$

$$\alpha_{\min} = 1-\frac{\sqrt{3}}{\pi} \tag{7}$$

As can be noticed the main difference between the presented feedback control strategies is found in the reference current generation of the line-commuted rectifier. While keeping the three phase currents of each converter unit symmetric, the suggested controls depicted in Fig. 2 and 3 not only improve the power share rating of the paralleled rectifiers, but also guarantee proper operation of the hybrid rectifiers during a mains phase loss. Therefore, a more robust and efficient operation of the unidirectional hybrid system becomes feasible.

## IV. HYBRID RECTIFIER DESIGN CONSIDERATIONS

In this section some issues regarding the design and the practical realization of the proposed unidirectional hybrid rectifiers will be discussed.

### A. Startup

In order to limit the inrush current at the rectifier startup the pre-charge circuits, as shown in Fig. 2, 3 and 4, are added to the hybrid rectifier units. There, some line-commuted diodes are replaced by thyristors.

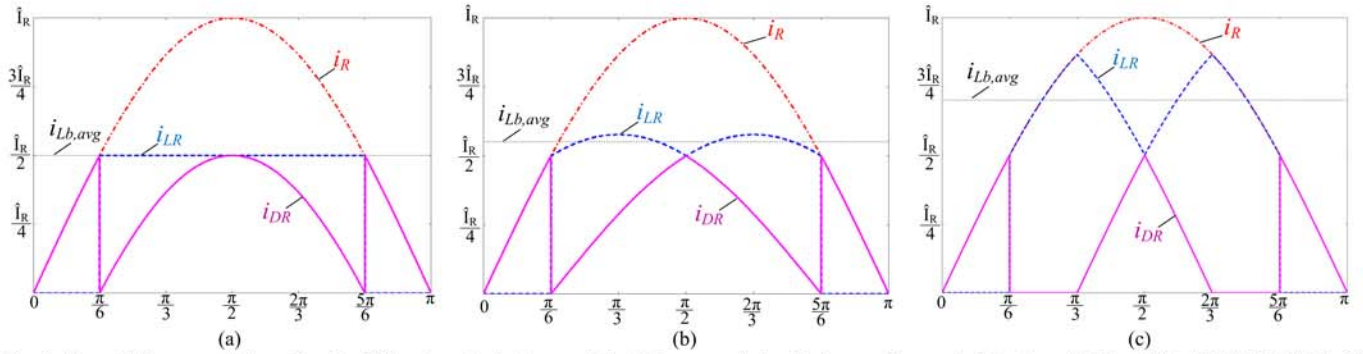



Fig. 6. Phase R line current formation for different control schemes at the high power factor limit operation: control strategy (a) Fig. 4 ($P_D$=0.449$P_o$); (b) Fig. 2 ($P_D$=0.392$P_o$); and (c) Fig. 3($P_D$=0.229$P_o$).

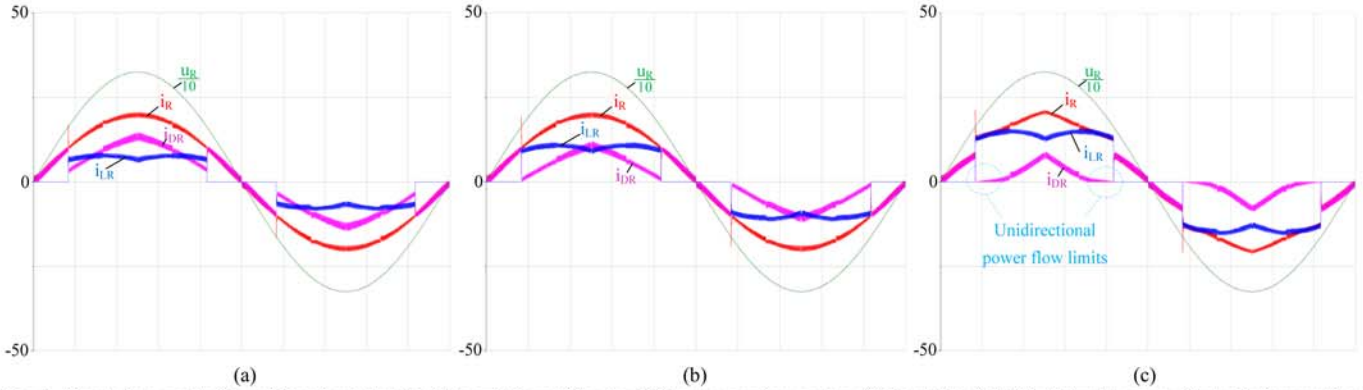



Fig. 7. Simulation results for unidirectional hybrid delta-switch rectifier for different operation modes: (a) ideal $P_D$>0.392$P_o$; (b) unity power factor limit operation $P_D$ ≈0.392$P_o$; and (c) distorted operation $P_D$ <0.392$P_o$.

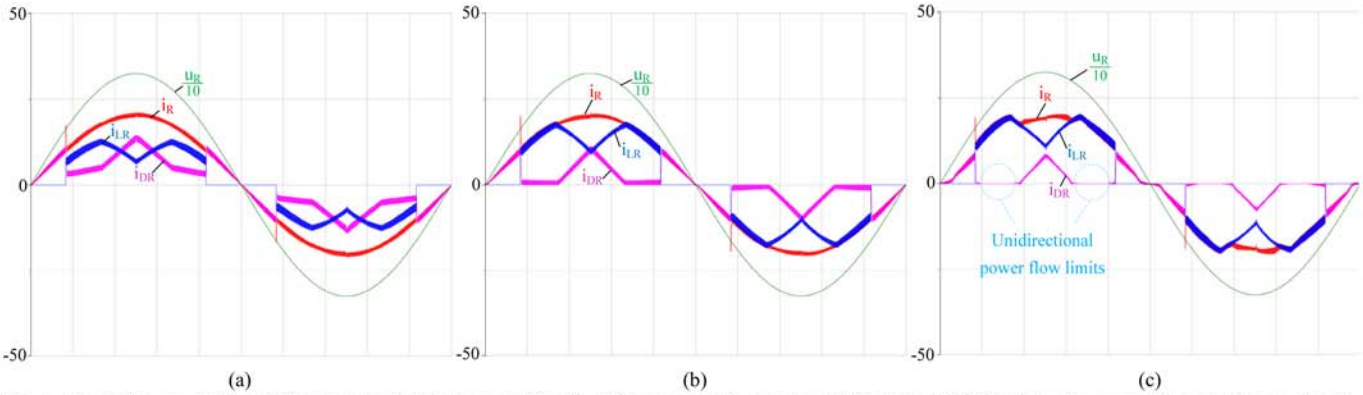



Fig. 8. Simulation results for unidirectional hybrid T-type rectifier for different operation modes: (a) ideal $P_D$>0.229$P_o$; (b) unity power factor limit operation $P_D$ ≈0.229$P_o$; and (c) distorted operation $P_D$ <0.229$P_o$.

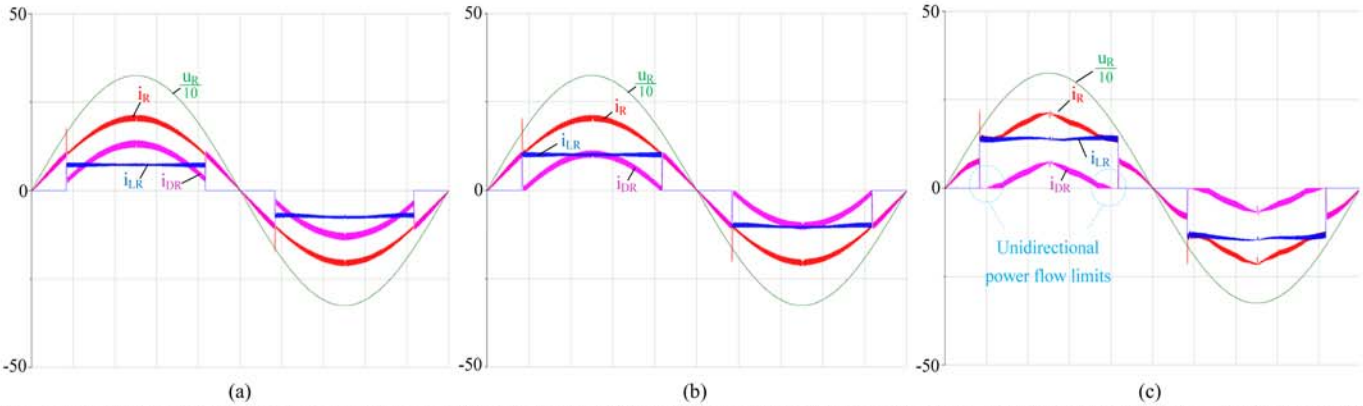



Fig. 9. Simulation results for unidirectional hybrid VIENNA 6-switch rectifier for control scheme proposed by [1], [2] and [5]: (a) ideal $P_D$>0.449$P_o$; (b) unity power factor limit operation $P_D$ ≈0.449$P_o$; and (c) distorted operation $P_D$ <0.449$P_o$.

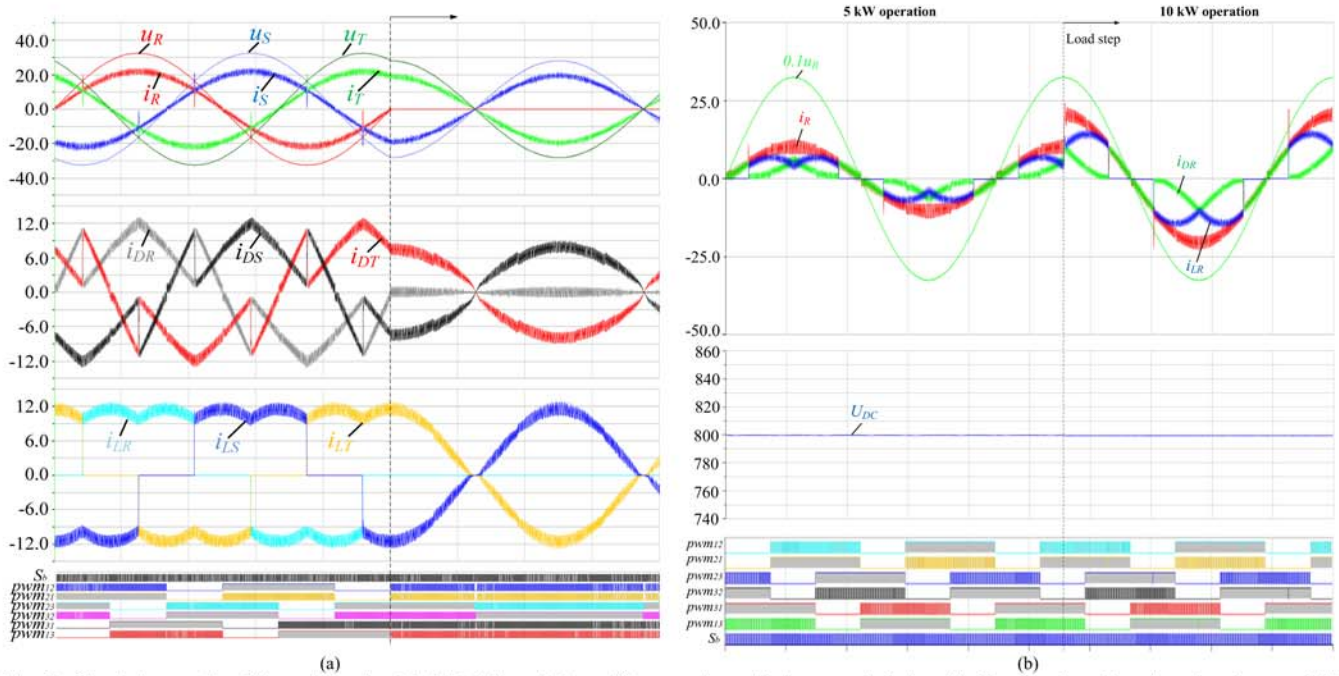



Fig. 10. Simulation results of the unidirectional hybrid delta-switch rectifier operating with the control depicted in Fig. 2 under: (a) mains phase loss; and (b) load variation (from 5kW to 10kW). Note that during the phase loss analysis the output power was deliberately reduced to about 66% of $P_o$ in order to keep the input current at similar amplitude of the nominal operation.

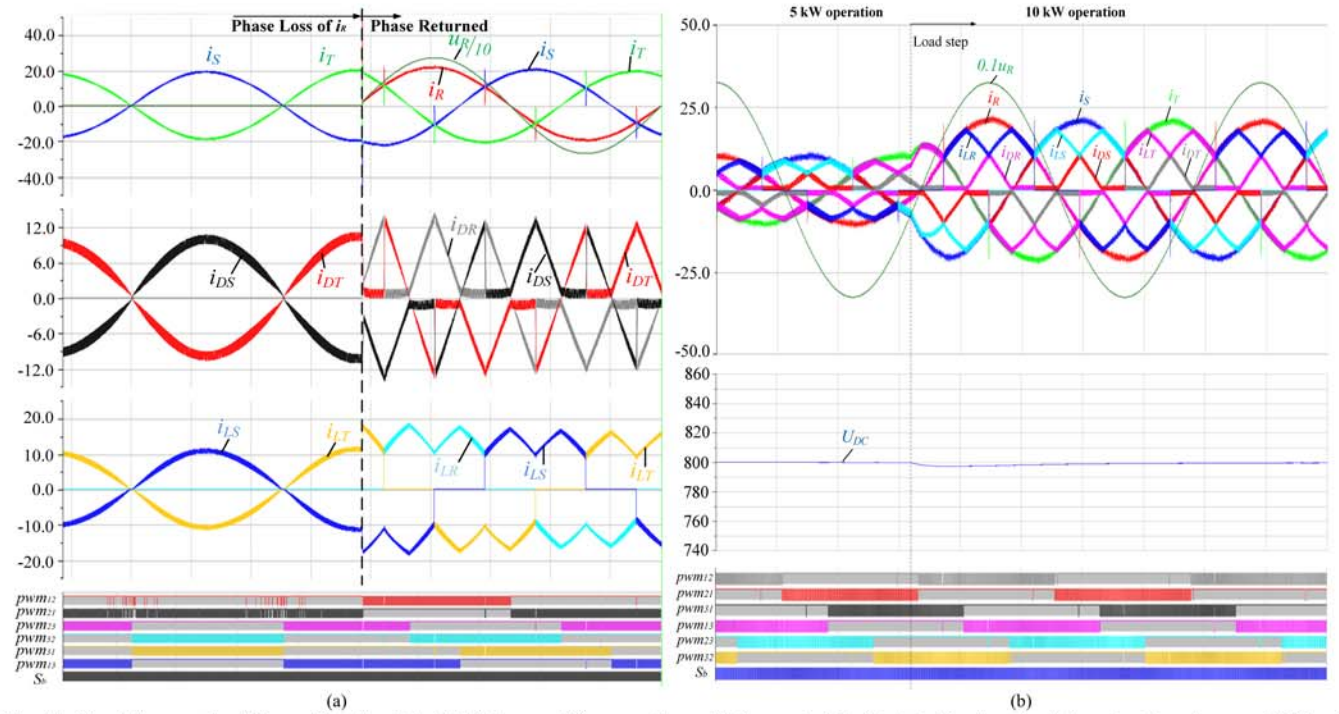



Fig. 11. Simulation results of the unidirectional hybrid T-type rectifier operating with the control depicted in Fig. 3 under: (a) mains phase loss; and (b) load variation (from 5kW to 10kW). Note that during the phase loss analysis the output power was deliberately reduced to about 66% of $P_o$ in order to keep the input current at similar amplitude of the nominal operation.

During the startup all thyristors and transistors are turned off. The inrush current is limited by the pre-charge circuit, which consists of the serial connection of a diode, $D_{pre}$, and a resistor, $R_{pre}$. As soon as the dc-link capacitor $C_o$ is charged to the peak value of the line-to-line voltages all thyristors are turned on and the current controller is finally enabled. Note that the startup can be performed simultaneously by both rectifier units or by a single rectifier structure.

In the hybrid rectifiers based on the 2-level delta-switch and 3-level T-type converters, the pre-charge thyristor, $Th_{pre}$, is located within the commutation path of the self-commuted rectifiers. Consequently, not only the conduction power losses across this device are added to the system, but also the recovery losses of the fast diodes, $D_{DF}$, and turn-on losses of the active switches are increased. A parallel connection of thyristors could be used to reduce the on-resistances.

Table. IV. Summary of the analytical approximations for the average and *rms* current values of the main power components of active rectifiers.

| $M=\frac{\hat{U}_R}{\frac{1}{2}U_{DC}}$ | | 2-LEVEL DELTA SWITCH RECTIFIER | | 3-LEVEL T-TYPE RECTIFIER | | 3-LEVEL VIENNA 6-SWIT. RECT. | |
|---|---|---|---|---|---|---|---|
| | | AVERAGE QUANTITY | RMS QUANTITY | AVERAGE QUANTITY | RMS QUANTITY | AVERAGE QUANTITY | RMS QUANTITY |
| ACTIVE SWITCH | $S_{i,j}$ | $I_{Sij,avg}=\hat{I}_R\left(\frac{1}{2\pi}-\frac{M}{8}\right)$ | $I_{Sij,rms}=\hat{I}_R\sqrt{\left(\frac{1}{6}-\frac{\sqrt{3}}{8\pi}\right)-\frac{M}{4\pi}}$ | $I_{Sij,avg}=\hat{I}_R\left(\frac{1}{\pi}-\frac{M}{4}\right)$ | $I_{Sij,rms}=\hat{I}_R\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$ | $I_{Sij,avg}=\hat{I}_R\left(\frac{1}{\pi}-\frac{M}{4}\right)$ | $I_{Sij,rms}=\hat{I}_R\sqrt{\frac{1}{4}-\frac{2M}{3\pi}}$ |
| DIODE | $D_{DF}$ | $I_{DDF,avg}=\hat{I}_R\frac{M}{4}$ | $I_{DDF,rms}=\hat{I}_R\sqrt{\frac{M(5\sqrt{3}+6)}{24\pi}}$ | $I_{DDF,avg}=\hat{I}_R\frac{M}{4}$ | $I_{DDF,rms}=\hat{I}_R\sqrt{\frac{2M}{3\pi}}$ | $I_{DDF,avg}=\hat{I}_R\frac{M}{4}$ | $I_{DDF,rms}=\hat{I}_R\sqrt{\frac{2M}{3\pi}}$ |
| | $D_{DN}$ | | | | | $I_{DDN,avg}=\frac{1}{\pi}\hat{I}_R$ | $I_{DDN,rms}=\frac{\hat{I}_R}{2}$ |
| MAXIMUM INDUCTOR RIPPLE | $\Delta i_L$ | $\Delta i_{L1,pp,\max}=\frac{U_{DC}}{2L_1f_S}M\left(1-\frac{3M}{4}\right)$ | | $\Delta i_{L1,pp,\max}=\frac{U_{DC}}{L_1f_S}\frac{\sqrt{3}M}{4}\left(1-\frac{\sqrt{3}M}{2}\right)$ | | $\Delta i_{L1,pp,\max}=\frac{U_{DC}}{L_1f_S}\frac{\sqrt{3}M}{4}\left(1-\frac{\sqrt{3}M}{2}\right)$ | |
| CAPACITOR | $C_0$ | $I_{Co,rms}=\hat{I}_R\sqrt{\frac{5\sqrt{3}M}{4\pi}-\frac{9M^2}{16}}$ | | $I_{Co,rms}=\hat{I}_R\sqrt{\frac{5\sqrt{3}M}{4\pi}-\frac{9M^2}{16}}$ | | $I_{Co,rms}=\hat{I}_R\sqrt{\frac{5\sqrt{3}M}{4\pi}-\frac{9M^2}{16}}$ | |

### *B. Power components design expressions*

In Table IV and V equations to determine the average and *rms* values of the current stresses on the power components, as required for the dimensioning of the self-commuted rectifiers and/or the proposed hybrid converters, are specified. The simple analytical expressions are given as functions of the corresponding modulation index, $M$, the output voltage, $U_{DC}$, sinusoidal input current value, $\hat{I}_R$, and the factor of active power processed by the self-commuted rectifier, $\alpha$. There, it is assumed that the rectifiers have: a purely sinusoidal phase current shape; ohmic mains behavior, no low frequency voltage drop across the inductors; and a switching frequency, $f_S$, which is much higher than the mains frequency, $f_N$ ($f_S >> f_N$), and the hybrid systems operates with the current reference generation strategy shown in Fig. 2. Therefore, the expressions are valid for $\alpha > 0.392$, which is a condition that needs to be fulfilled in order to achieve high power factor operation in the PWM control depicted in Fig. 2.

## V. COMPARATIVE EVALUATION OF RECTIFIERS

In order to quantify the advantages of the proposed 2- and 3-level unidirectional hybrid rectifiers, an efficiency comparison between these systems and other concepts shown in Fig. 12, is presented. The converter specifications considered in the analyses are: $P_o$=10 kW, $u_{R,rms}$=230V (50 Hz), and $U_{DC}$= 800 V. The Infineon IGBTs 600V IKW30N60T and 1200V IKW25T120 are selected for the assessment. All the hybrid rectifiers are set to operate with the control strategy illustrated in Fig. 2.

In the analyses each rectifier unit of the hybrid system is designed to cope with fully specified power capability, however the calculations consider the rated active power processed by the self-commuted rectifier to be $\alpha$=0.392. In addition, the 3-phase diode-bridge with single dc-dc boost rectifier is set to operate at 1/5th of the switching frequency of the PWM rectifier unit.

For the specified 800 V dc-link, the T-type rectifier requires 1200V diodes for the top and bottom semiconductors. Since the bidirectional mid-point switches have to block only half of the dc-link voltage, 600V IGBTs and anti-parallel diodes can be used. Therefore, for the analysis of the switching losses, using only the information from the datasheets would not be enough to enable a fair comparison between the studied systems. Due to the mismatch of voltage rated devices, the switching energy of the 600 V IGBTs will be higher if the commutating diode ($D_{DF}$) is 1200 V rated because of the considerably higher reverse recovery charge. In order to accurately determine the loss characteristics of the IGBTs, the single phase T-type bridge-leg test set-up shown in Fig. 13 was built.

In Fig. 14 the pure semiconductor efficiency of the rectifiers under study is presented for operation of the single PWM rectifiers in the switching frequency range of 5 kHz to 50 kHz. According to the results, among the single self-commuted rectifier solutions, the 3-level VIENNA 6-switch constitutes the best solution for a switching frequency above 18 kHz. In fact, this converter is particularly suitable for high switching frequency operation because of the small increase in the switching losses of the employed 600 V devices. In contrast, the 2-level delta-switch rectifier displays very low conduction losses, thus it will only display good performance for low switching frequency operation.

Although the switching losses of the 600V devices of the T-type converter is higher than for the VIENNA rectifier, fortunately there are conduction states where only one semiconductor device per phase-leg conducts current. For the VIENNA rectifier, in all conduction states, there are always two semiconductors in the current path, thus the conduction losses of the T-type rectifier will be lower. These are the reasons that the T-type rectifier can only display better semiconductor efficiency than the VIENNA 6-switch converter for switching frequencies below 18 kHz.

Following the same principles as the 2- and 3-level self-commuted rectifiers, the 3-level hybrid rectifiers constitute the natural choice for high switching frequency operation, while the 2-level hybrid could only be better for very low frequencies.

As expected, the hybrid rectifier topologies can achieve higher efficiency than the single self-commuted rectifier solutions they are based on. Alternatively, for high switching frequencies the loss performance of the hybrid systems could be further improved if the diode-bridge rectifier employed a 2-switch boost dc-dc converter as a replacement for the

Table. V. Summary of the analytical approximations for the average and rms current values of the main power components of hybrid rectifiers. These expressions are only valid for the control strategy depicted in Fig. 2.

| | | | |
|---|---|---|---|
| **THREE-PHASE HYBRID DIODE BRIDGE ACTIVE BOOST RECTIFIER** | | | |
| $M=\frac{\sqrt{3}\hat{U}_R}{U_{DC}}$ | | AVERAGE QUANTITY | RMS QUANTITY |
| ACTIVE SWITCH | $S_b$ | $I_{Sb,avg}=\frac{\pi\hat{I}_R(1-\alpha)}{2\sqrt{3}}\left(1-3\frac{M}{\pi}\right)$ | $I_{Sb,rms}=\frac{\pi\hat{I}_R(1-\alpha)}{2\sqrt{3}}\sqrt{1-3\frac{M}{\pi}}$ |
| DIODE | $D_{bF}$ | $I_{DbF,avg}=\frac{3\hat{I}_R M(1-\alpha)}{2\sqrt{3}}$ | $I_{DbF,rms}=\hat{I}_R(1-\alpha)\sqrt{\frac{\pi M}{4}}$ |
| | $D_{bN}$ | $I_{DbN,avg}=\frac{\pi\hat{I}_R(1-\alpha)}{6\sqrt{3}}$ | $I_{DbN,rms}=\frac{\pi\hat{I}_R(1-\alpha)}{6}$ |
| MAXIMUM INDUCTOR RIPPLE | $\Delta i_{Lb}$ | $\Delta I_{Lb,pp,\max}=\frac{\sqrt{3}\hat{U}_R}{2L_b f_S}(1-M)$ | |
| MAXIMUM CAPACITOR CURRENT | $C_0$ | $I_{Co,rms,\max}=\hat{I}_R\sqrt{\frac{M\pi}{4}\left(1-\frac{3M}{\pi}\right)}$ | |
| **THREE-PHASE 2-LEVEL HYBRID DELTA SWITCH RECTIFIER** | | | |
| $M=\frac{\sqrt{3}\hat{U}_R}{U_{DC}}$ | | AVERAGE QUANTITY | RMS QUANTITY |
| ACTIVE SWITCH | $S_{i,j}$ | $I_{Sij,avg}=\hat{I}_R\left(\frac{6-\pi\sqrt{3}M}{12\pi}+\frac{\sqrt{3}(1-\alpha)(3M-\pi)}{36}\right)$ | $I_{Sij,rms}=\hat{I}_R\sqrt{\frac{4\pi-3\sqrt{3}-4\sqrt{3}M}{24\pi}+\frac{(1-\alpha)(\sqrt{3}M+\pi M+4\sqrt{3}-12)}{24}-\frac{\pi(1-\alpha)^2(3M-\pi)}{72}}$ |
| DIODE | $D_{DF}$ | $I_{DDF,avg}=\frac{M\alpha\hat{I}_R}{2\sqrt{3}}$ | $I_{DDF,rms}=\hat{I}_R\sqrt{\frac{M(2\sqrt{3}+1)}{6\pi}-\frac{M\pi(1-\alpha)(2+\sqrt{3})}{24}+\frac{\pi M(1-\alpha)^2}{12}}$ |
| **THREE-PHASE 3-LEVEL HYBRID T-TYPE RECTIFIER** | | | |
| $M=\frac{\hat{U}_R}{\frac{1}{2}U_{DC}}$ | | AVERAGE QUANTITY | RMS QUANTITY |
| ACTIVE SWITCH | $S_{i,j}$ | $I_{Sij,avg}=\hat{I}_R\left(\frac{4-\pi M}{4\pi}+\frac{(1-\alpha)(9M-2\pi\sqrt{3})}{36}\right)$ | $I_{Sij,rms}=\hat{I}_R\sqrt{\frac{3\pi-8M}{12\pi}+\frac{(1-\alpha)(4\pi\sqrt{3}M+9M-36)}{72}+\frac{\pi(1-\alpha)^2(2\pi-3\sqrt{3}M)}{72}}$ |
| DIODE | $D_{DF}$ | $I_{DDF,avg}=\frac{M\hat{I}_R\alpha}{4}$ | $I_{DDF,rms}=\hat{I}_R\sqrt{\frac{2M}{3\pi}-\frac{M(1-\alpha)(4\pi\sqrt{3}+9)}{72}+\frac{\pi\sqrt{3}M(1-\alpha)^2}{24}}$ |
| **THREE-PHASE 3-LEVEL HYBRID VIENNA 6-SWITCH RECTIFIER** | | | |
| $M=\frac{\hat{U}_R}{\frac{1}{2}U_{DC}}$ | | AVERAGE QUANTITY | RMS QUANTITY |
| ACTIVE SWITCH | $S_{i,j}$ | $I_{Sij,avg}=\hat{I}_R\left(\frac{4-\pi M}{4\pi}+\frac{(1-\alpha)(9M-2\pi\sqrt{3})}{36}\right)$ | $I_{Sij,rms}=\hat{I}_R\sqrt{\frac{3\pi-8M}{12\pi}+\frac{(1-\alpha)(4\pi\sqrt{3}M+9M-36)}{72}+\frac{\pi(1-\alpha)^2(2\pi-3\sqrt{3}M)}{72}}$ |
| DIODE | $D_{DF}$ | $I_{DDF,avg}=\frac{M\hat{I}_R\alpha}{4}$ | $I_{DDF,rms}=\hat{I}_R\sqrt{\frac{2M}{3\pi}-\frac{M(1-\alpha)(4\pi\sqrt{3}+9)}{72}+\frac{\pi\sqrt{3}M(1-\alpha)^2}{24}}$ |
| | $D_{DN}$ | $I_{DDN,avg}=\frac{\hat{I}_R\alpha}{\pi}$ | $I_{DDN,rms}=\frac{\hat{I}_R\alpha}{2}$ |

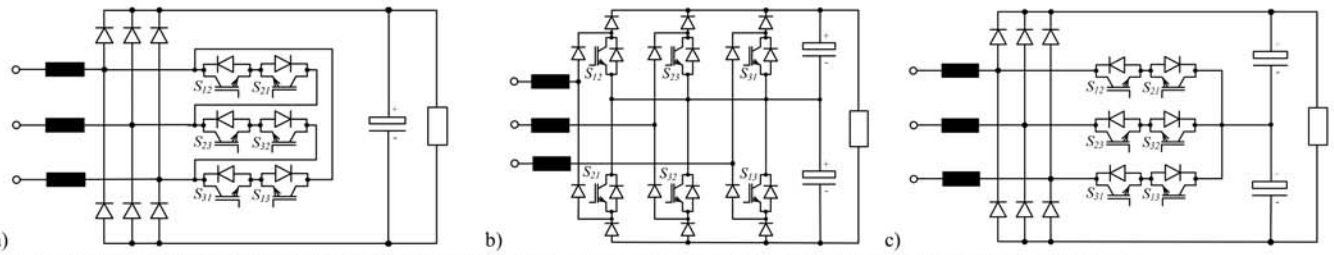



Fig. 12. 3-phase rectifier systems: (a) 2-level delta-switch rectifier; (b) 3-level VIENNA 6-switch rectifier; and (c) 3-level T-type converter.

analyzed single-switch version. Even though this circuit modification would increase conduction losses because of the two IGBT devices in series, when switching losses become dominant, a better efficiency performance could be achieved as semiconductors with better loss characteristics can be employed, e.g. 600 V IGBTs instead of the 1200 V necessary for the single-switch structure [6].

Although the efficiency comparison gives a good overview regarding the expected performance of the analyzed topologies, it can be considered not completely fair. This is particularly true because the selected IGBTs and diodes for each topology are not individually optimized. Therefore, some devices can be found over dimensioned while others can be brought to operate at their limits. For a fair comparison, the semiconductor chip sizes of each rectifier could be adapted for a given operating point such that the maximum or average IGBT and diode junction temperatures, $T_{J,T/D}$, are equal to or less than a predefined maximum value, i.e. $T_{J,max}$=125°C. This strategy not only guarantees optimal chip area partitioning and semiconductor material usage, but also provides a common

basis for comparisons [19]. Additionally, the chip area data enables the semiconductor costs of the different topologies to be determined. This is particularly true as the major costs of a device are related to the silicon chip since the packaging and the bonding account only for 20% of the total costs [19].

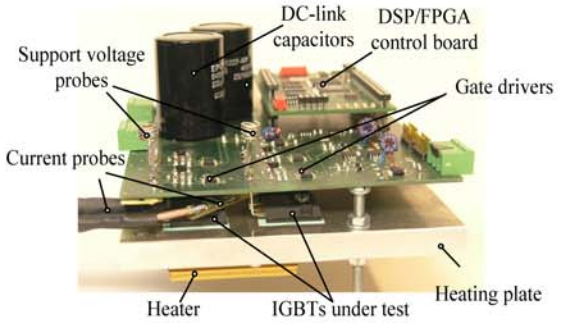



Fig. 13. Switching losses test set-up of a single bridge-leg of the T-type converter.

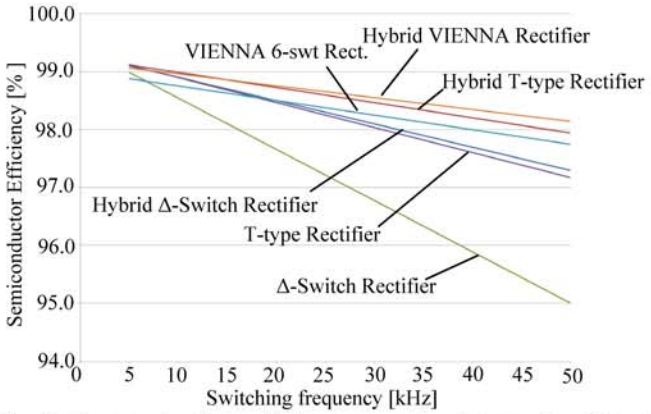



Fig. 14. Pure semiconductor efficiency comparison between the different rectifiers employing commercial components. The converter specifications considered in the analyses are: $P_o$= 10 kW, $u_{R,rms}$ = 230 V (50 Hz), and $U_{DC}$= 800 V.

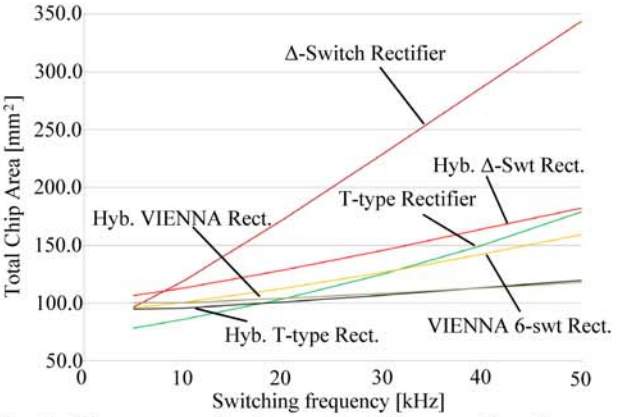



Fig. 15. Chip area comparison between the different rectifiers. The converter specifications considered in the analyses are: $P_o$= 10 kW, $u_{R,rms}$= 230 V (50 Hz), and $U_{DC}$ = 800 V.

Due to their good documentation and data availability, the Infineon Trench and Field Stop 1200V IGBT4 and 600V IGBT3 series have been chosen as the data basis. With a statistical analysis of many commercial devices, datasheets and manufacturer data, the power losses and thermal characteristics of these semiconductor series can be modelled with a chip die size, $A_{S,T/D}$. A thorough description of the employed chip area optimization, including the resulting expressions for the power loss of the IGBTs and diodes and thermal characteristics modelled with a nominal chip area, are given in [19].

In this work, using the derived chip area mathematical expressions, the optimization algorithm calculates the losses of each topology and chip sizes until the average junction temperature of each semiconductor chip reaches $T_J$=125°C, assuming a heat sink temperature of $T_{Sink}$=80°C. By summing up all optimized chip sizes, the total chip area, the semiconductor costs and the total efficiency for a topology and corresponding operation point can be found. Therein, the chip area of each element is limited to a minimum of $A_{Smin}$= 2 mm$^2$. This is due to unconsidered side effects becoming dominant for small chip sizes and the limits in bonding technology.

Fig. 15 shows the chip area optimization results for all analysed rectifier topologies, which have similar specifications and operation conditions to the efficiency comparison employing commercial semiconductors. Therein, the total chip area is calculated depending on the switching frequency.

As can be noticed, the results compiled in Fig. 15 confirm the initial efficiency calculations (cf. Fig. 14). For most of the analysed switching frequency range the hybrid rectifiers require lower semiconductor chip area than the single self-commuted rectifiers used to assemble them. The part count and the count for external circuitry such as isolated gate drivers is increased. However, the total cost of the semiconductors can be expressively lower, especially for high switching frequencies.

Fig. 16- Delta-switch rectifier prototype.

## VI. Experimental Evaluation

Fig. 16 shows a 5 kW / 72 kHz ($U_{DC}$ = 400 V) delta-switch rectifier used to assemble a unidirectional hybrid delta-switch converter. This self-commuted system is air-cooled and has a power to weight ratio of 1.32 kW/kg. The power density of this rectifier is 2.35 kW/dm$^3$. A digital signal processing board with a TI DSP and a Lattice FPGA is used to implement the control strategy shown in Fig. 2. Three inductors with inductance values of 326µH are employed. In total, eighteen 82µF/450V electrolytic capacitors are arranged in parallel.

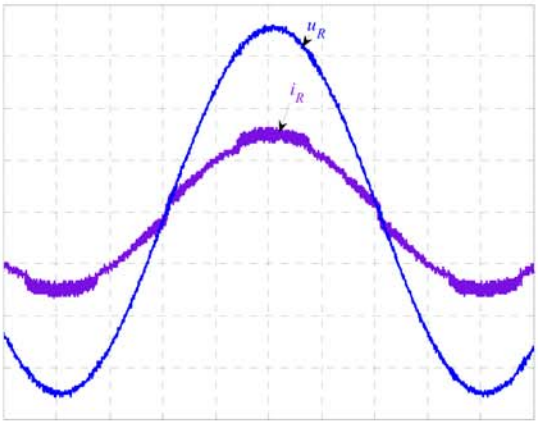
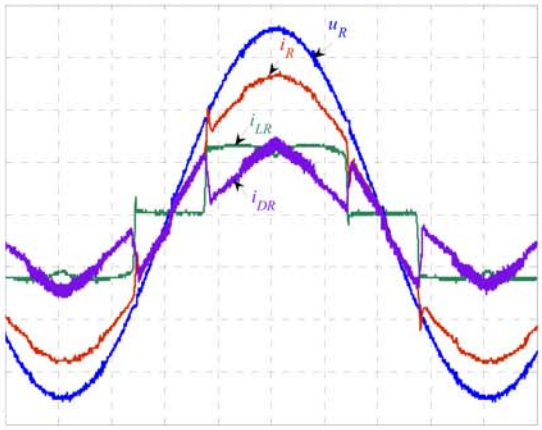
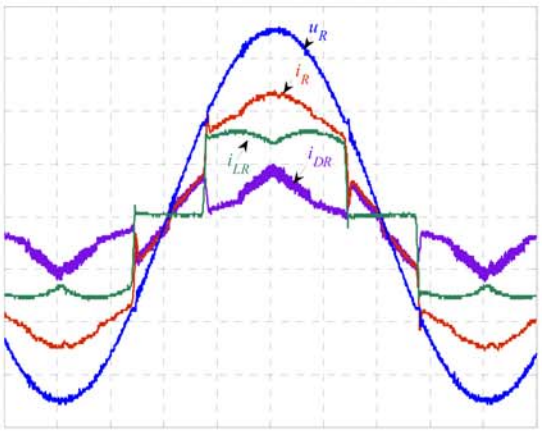



Fig. 17. Delta-switch rectifier experimental result. Ch1: line current ($i_R$: 10A/div) and Ch2: mains voltage ($u_R$: 50V/div).




a)




b)

Fig. 18. Hybrid delta-switch rectifier experimental analysis: (a) high power factor operation; and (b) operation below the unity power factor limit. Ch1: line current ($i_R$: 5A/div), Ch2: mains voltage ($u_R$: 50V/div), Ch3: delta-switch rectifier current ($i_{DR}$: 5A/div), and Ch4: diode bridge + dc-dc boost rectifier current ($i_{LR}$: 5A/div).

The performance of the implemented unidirectional hybrid delta-switch rectifier can be seen in Fig. 17 and 18. Fig. 17 displays the operation condition where the delta-switch rectifier delivers all the active power to the load ($\alpha$ = 100%). Fig. 18(a) shows the main experimental waveforms for high power factor operation of the hybrid system ($\alpha$ = 41%), where an input current THD of 5.1 % and a power factor of $\lambda$ =0.99 have been measured, which attest the feasibility of this converter technology. Fig. 18(b) presents the experimental results when the rated power processed by the delta-switch rectifier is set to be below the unity power factor limit.

The line current THDs measured for different ratio of active power processed by the single delta-switch rectifier are depicted in Fig. 19. As expected, the line currents can become highly distorted for values of $\alpha$ smaller than 39.2%. On the other hand, if the ratio of active power of the paralleled rectifier units respects the high power factor condition ($\alpha$ > 39.2%), the gain in line power quality by increasing $\alpha$ is very small. Therefore, the gain in semiconductor efficiency that can be achieved by distributing the processed active power between the paralleled rectifiers to the high power factor limit ($\alpha = \alpha_{min}$) can be justified as only a small increment on the distortion of the line current occurs.

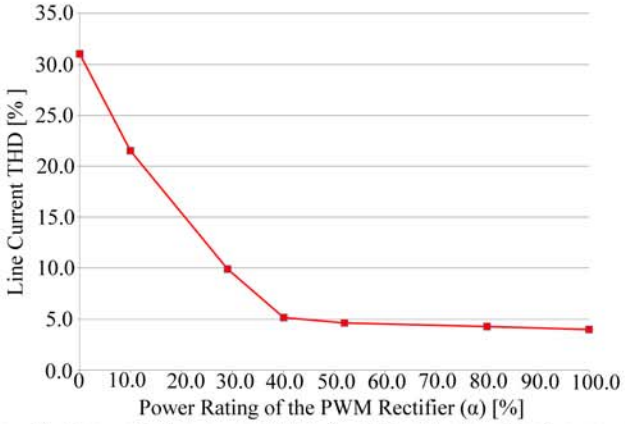



Fig. 19. Measured line current THD for different ratio of active power processed by the single delta-switch rectifier.

## VII. Conclusions

This paper presents 3-phase hybrid rectifiers assembled by the parallel connection of a 3-phase diode bridge active boost rectifier with a 2-level unidirectional delta-switch rectifier or two 3-level VIENNA rectifier technologies. The systems aim to take advantage of the commonly low power losses and high reliability of a diode based boost rectifier and also to benefit from the capability of the delta-rectifier to process reactive power. Therefore, highly efficient and reliable high power factor rectifier systems with controlled dc-link voltage are constructed.

A comparative evaluation between the proposed hybrid rectifiers with the conventional unidirectional PWM rectifiers used to assemble them was carried out and the results have shown that the hybrid systems can achieve much higher efficiency if the switching frequency is high enough. Additionally, a semiconductor area based comparison was used to further evaluate the studied rectifier systems. Surprisingly, at 800 V dc-link voltage the total silicon chip area of the hybrid topologies are already considerably smaller than for their respective self-commuted topology for very low switching frequencies. The part count and the count for external circuitry such as isolated gate drivers is increased, but the total cost of the semiconductors can be expressively lower, especially for high switching frequencies.

Finally, experimental results obtained with a unidirectional hybrid delta-switch rectifier prototype are shown to demonstrate the performance and feasibility of this solution.

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The focus of his current research is on AC-AC and AC-DC converter topologies with low effects on the mains, e.g. for data centers, More-Electric-Aircraft and distributed renewable energy systems, and on Solid-State Transformers for Smart Microgrid Systems. Further main research areas are the realization of ultra-compact and ultra-efficient converter modules employing latest power semiconductor technology (SiC and GaN), micro power electronics and/or Power Supplies on Chip, multi-domain/scale modeling/simulation and multi-objective optimization, physical model-based lifetime prediction, pulsed power, and ultra-high speed and bearingless motors. He has been appointed an IEEE Distinguished Lecturer by the IEEE Power Electronics Society in 2011.

He received the Best Transactions Paper Award of the IEEE Industrial Electronics Society in 2005, the Best Paper Award of the ICPE in 2007, the 1st Prize Paper Award of the IEEE IAS IPCC in 2008, the IEEE IECON Best Paper Award of the IES PETC in 2009, the IEEE PELS Transaction Prize Paper Award 2009, the Best Paper Award of the IEEE/ASME Transactions on Mechatronics 2010, the IEEE PELS Transactions Prize Paper Award 2010, the Best Paper 1st Prize Award at the IEEE ECCE Asia 2011, and the 1st Place IEEE IAS Society Prize Paper Award 2011 and the IEEE IAS EMC Paper Award 2012. Furthermore, he received the ETH Zurich Golden Owl Award 2011 for Excellence in Teaching. He also received an Erskine Fellowship from the University of Canterbury, New Zealand, in 2003.

He initiated and/or is the founder/co-founder of 4 spin-off companies targeting ultra-high speed drives, multi-domain/level simulation, ultra-compact/efficient converter systems and pulsed power/electronic energy processing. In 2006, the European Power Supplies Manufacturers Association (EPSMA) awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Power Electronics in Europe.

Dr. Kolar is a Fellow of the IEEE and a Member of the IEEJ and of International Steering Committees and Technical Program Committees of numerous international conferences in the field (e.g. Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). He is the founding Chairman of the IEEE PELS Austria and Switzerland Chapter and Chairman of the Education Chapter of the EPE Association. From 1997 through 2000 he has been serving as an Associate Editor of the IEEE Transactions on Industrial Electronics and since 2001 as an Associate Editor of the IEEE Transactions on Power Electronics. Since 2002 he also is an Associate Editor of the Journal of Power Electronics of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering.