Design of an 99%-Efficient, 5 kW, Phase-Shift PWM DC-DC Converter for Telecom Applications

U. Badstuebner, J. Biela, and J.W. Kolar
Power Electronic Systems Laboratory, ETH Zurich
Email: badstuebner@lem.ee.ethz.ch; www.pes.ee.ethz.ch

***Abstract*—In the last decade power electronic research focused on the power density maximization mainly to reduce initial systems costs [1]. In the field of data centers and telecom applications, the costs for powering and cooling exceed the purchasing cost in less than 2 years [2]. That causes the changing driving forces in the development of new power supplies to efficiency, while the power density should stay on a high level.**

The commonly used DC-DC converter in the power supply unit (PSU) for data centers and telecom applications are full bridge phase-shift converters since they meet the demands of high power and efficient power conversion, a compact design and the constant operation frequency allows a simple control and EMI design.

The development of the converter with respect to high efficiency has a lot of degrees of freedom. An optimization procedure based on comprehensive analytical models leads to the optimal parameters (e.g. switching frequency, switching devices in parallel and transformer design) for the most efficient design.

In this paper a 5 kW, 400 V - 48..56 V phase-shift PWM converter with LC-output filter is designed for highest efficiency ($\eta \geq$99 %) with a volume limitation and the consideration of the part-load efficiency. The components dependency as well as the optimal design will be explained. The realized prototype design reaches a calculated efficiency of η = 99.2 % under full load condition and a power density of ρ = 36 W/in^3 (2.2 kW/liter).

I. Introduction

Since 1970, the power density of power electronic converters roughly doubles every 10 years, mainly caused by the increasing switching frequency due to the continuous improvements of power switching devices and the decreasing volume of magnetic components [3]. In the area of power supply units (PSU) for data center and telecom applications, this evolution led to the main developing focus on compact design and a capital expenditure (CapEx) measured by the square feet occupied, rather than power consumption [2]. However, the demand for data centers is continuously increasing and the rising energy prices result in powering and cooling costs, which are higher as the purchase cost in less than two years [2]. This causes a change of the driving force in power converter system development towards high efficient power conversion. However, high power density is still required, which leads to multi-objective targets for the system development.

In [4], the prototype of a 5 kW, 400 V to 48..56 V phase-shift PWM DC-DC converter for telecom application is presented, which was optimized with respect to highest achievable power density. There, the design process was based on comprehensive analytical models of the converter system with an automatic optimization procedure, which results in a power density of ρ = 147 W/in^3 and a measured efficiency of η = 94.75 %. These points determine the point of highest power density ρ_{max} in the η-ρ-plane in Fig. 1 a).

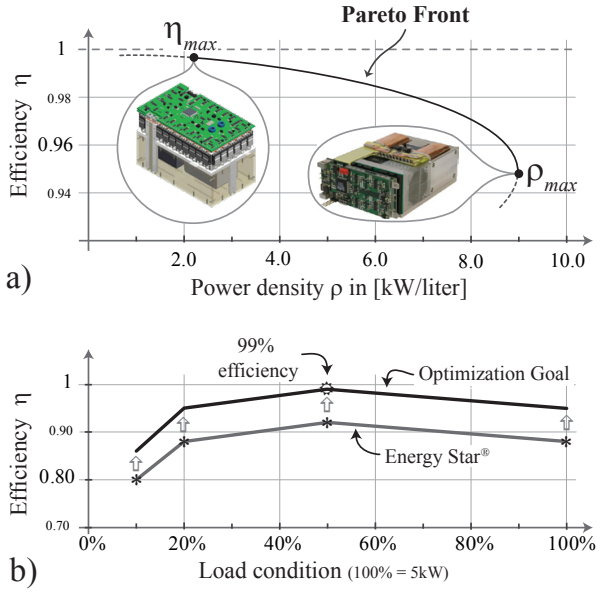

Figure 1. a) Efficiency η vs. power density ρ. The best possible solution of a multi-objective optimization according to the weights w_η for efficiency and w_ρ for power density for a defined topology is presented by the Pareto front. b) Optimization goal the efficiency curve through the point η = 0.99 raised from the values proposed in [5].

In this paper, a design process is presented to reach the point of highest efficiency ($\eta_{max} \geq$99 %) for a phase-shift PWM, 5 kW DC-DC converter with LC output filter as shown in Fig. 2, which is plotted in the diagram Fig. 1 a) as well. The curve between these two optimal points is called Pareto front, which present the optimal points for varying weights w_η of the efficiency and w_ρ of the power density in the optimization procedure. This allows the OEMs a classification of present system and builds the basis for road maps, as well as the identification of unachievable designs.

In the optimization procedure, the part load efficiency of the converter system is considered as well. The reference efficiency curve for the optimization is related to the efficiency points proposed in the Energy Star® requirements of computer serves [5], which have been moved to the point, where the maximum efficiency is 99 %, as shown in Fig. 1 b).

The optimization procedure and the comprehensive analytical electrical and magnetic models are described in **Section II**. After the presentation of the optimization algorithm, the calculation of the topology specific operation point, i.e. all relevant current and voltage waveforms, is described. Within

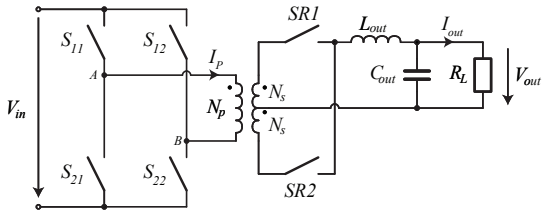

Figure 2. Schematic of the selected phase-shift PWM converter for 99 % efficiency. (V_{in}=400 V, V_{out}=48..54 V, P_{out}=5 kW).

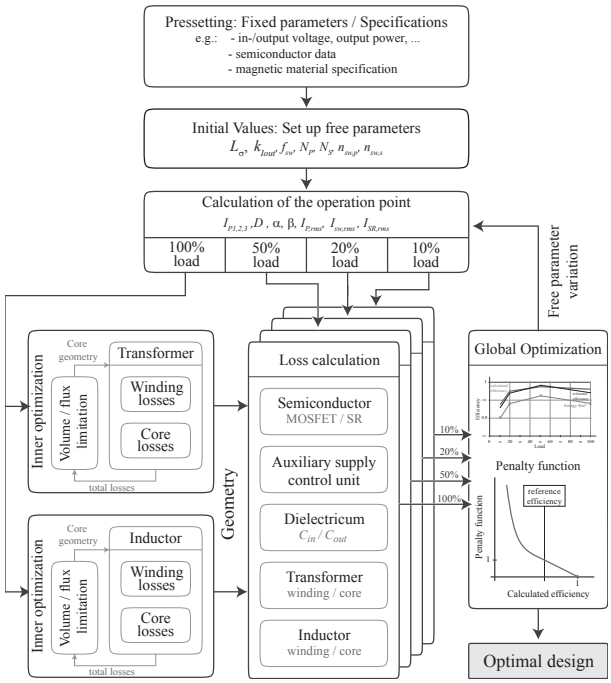

Figure 3. Automatic efficiency optimization procedure for the phase-Shift PWM DC-DC converter considering the part load efficiency.

inner optimization procedures for the transformer and output inductor, the optimal geometry parameters for the cores are determined, considering the core losses and HF-winding losses in the magnetic devices.

The optimization procedure results in the optimal design parameters for the converter given in **Section III**. A prototype design, which reaches a calculated full load efficiency of η = 99.2 % and a power density of ρ = 36 W/in^3 (2.2 kW/liter) is presented in section **Section IV**.

II. Efficiency Optimization

For the design of the selected phase-shift converter and the given specifications, the component values must be chosen so that the efficiency becomes maximal. However, this task is challenging because the components interdepend to some degree from each other. In this section the design process is described based on an optimization procedure, which automatically finds the optimal component values of the converter system. The underlying analytical models are described after the presentation of the procedure in section II-A.

The starting point of the optimization procedure in Fig. 3 are the fixed parameters for the converter design process, i.e. the electrical specifications (e.g. output power P_{out}) and magnetic constraints (e.g. maximum flux density in the transformer or output inductor core, respectively).

With the initial set of the free parameters (the switching frequency f_{sw}, the primary and secondary turns number of the transformer N_p and N_s, the leakage inductance L_σ, the allowed output inductor current ripple characterized by k_{Iout}, as well as the number of parallel primary $n_{sw,p}$ and synchronous $n_{sw,s}$ rectifier MOSFET's) the optimization loop is launched.

The first step in the loop is the calculation of the operation point based on a coupled inductance model of the center tapped transformer. There, the output inductance L_{out} and output capacitance C_{out} are determined for full-load conditions and so, all component values are defined in order to determine all relevant current and voltage waveforms (cf. Fig. 5). In addition, the characteristic waveforms for the part load conditions (cf. [5] and Fig. 1) of the converter have to be calculated as well as explained in section I.

The core of the optimization procedure is the calculation of the losses in the converter system. For the magnetic components, i.e. the center-tapped transformer and the output inductor, the geometry set-up is found in two inner optimization loops. There, the geometry parameters (cf. Fig. 4), are varied systematically, while the volume and flux density stay in the preset limit until the optimum parameter are found, which results in the minimum component losses (considering HF-winding and core loses) under full load condition. The actual loss calculation for the four load conditions (i.e. 10 %, 20 %, 50 %, and 100 %) are running in a for-next loop or in parallel, alternatively. For the given amount of the power switches in parallel, which are optimizided during the optimization process as well, the conduction losses are determined. For the full bridge MOSFETs, the switching losses are considered as well, which is especially important for low load conditions. Besides that, the gate drive losses are added in order to calculate the total semiconductor losses. For magnetic components, the core and winding losses are determined. The HF-losses in the windings are considered for the transformer as well, whereas the HF-losses in the output inductor have only a minor influence. The dielectric losses in the output capacitor are determined with the loss factor. Additional losses in the control unit and auxiliary supply are considered as constant over the whole load range.

The resulting part-load losses, which define the actual efficiency curve η_{act} as depicted in Fig. 1 b) are now compared with the reference efficiency curve η_{ref} (labeled as Optimization goal in Fig. 1 b)). The deviations $\Delta\eta$ between reference and actual efficiency values are the input for a penalty function, which is defined as:

$$penalty(\Delta\eta) = \begin{cases} \dfrac{1}{1-\eta_{ref}} \cdot (1-\eta_{act}), & \text{for } \Delta_\eta < 0 \\ \dfrac{1}{(1-\eta_{ref}+\eta_{act})^{20}}, & \text{for } \Delta_\eta \geq 0. \end{cases} \quad (1)$$

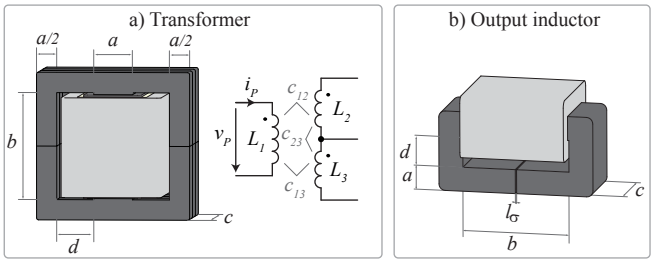

Figure 4. Geometry model of transformer and output inductor. In addition, the coupled inductance model of the transformer is presented.

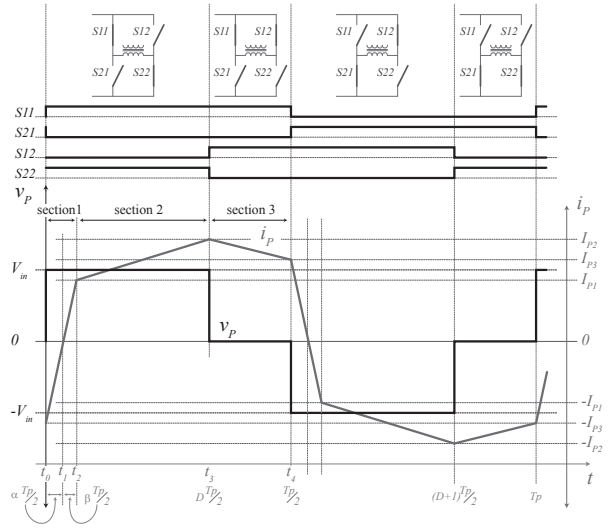

Figure 5. Principle primary side current / voltage waveforms with the characteristic points I_{P1}, I_{P2}, I_{P3} and the switching states.

The sum of the penalty values forms the optimization criteria. The global optimization algorithm changes the free converter parameters systematically, until the minimum penalty value is found. The outputs of the optimization procedure are the converter design parameters which directly enables a prototype assembly.

A. Analytical Models

The analytical models can be divided into 4 parts: First, the formulas for calculating the operation point are explained. After that, the equations for the losses in the power semiconductor devices are derived. In the third subsection, the calculation of the magnetic components is presented and finally the losses in the capacitors are given.

1) Operation point: The models for determining the operation point are based on a coupled inductors equivalent circuit of the center-tapped transformer, as presented in fig:MagGeometry a) on the right hand side. With the set inductance L_1 and the free parameter L_σ, the couple factor c_{12}, the inductance L_2 (which is considered to be equal to L_3) and the transmission ratio ktr can be calculated as:

$$\begin{aligned} c_{12} &= 1 - {}^{L_\sigma}/_{L_1} \\ L_2 &= L_1 \cdot {}^{N_s}/_{N_p} \cdot c_{12} \\ ktr &= \sqrt{{}^{L_1}/_{L_2}} \cdot c_{12}, \end{aligned} \tag{2}$$

whereas N_P is the number of primary turns and N_S the number of one secondary turns.

In Fig. 5, there are three different piecewise linear current sections, whose current slope are determined by the center-tapped transformer (cf. Fig. 4) and the output inductance, as described in the following.

a) Section 1 ($t = t_0..t_2$): The input voltage is applied to the primary side of the transformer and the current slope is limited by the leakage inductance. With the assumption, that the inductances L_2 and L_3 and whose coupling factors in respect to L_1 (c_{12} and c_{13}) are equal, the formula for calculating the current slope in this section is simplified to:

$$\frac{\Delta i_p}{\Delta(t_0..t_2)} = V_{in} \cdot \frac{1 + c_{23}}{L_1 \cdot (1 + c_{23} - 2 \cdot (c_{12})^2)} \tag{3}$$

b) Section 2 ($t = t_2..t_3$): In this section, power is transferred form the input to the output stage. With the applied input voltage V_{in} the resulting output voltage V_{out} and the calculated output inductance L_{out}, the current slope of section 2 is given by:

$$\frac{\Delta i_p}{\Delta(t_2..t_3)} = \frac{V_{in} \cdot (L_{out} + L_2) - c_{12} \cdot \sqrt{L_1} \cdot \sqrt{L_2} \cdot V_{out}}{L_1 \cdot (L_{out} + L_2 \cdot (1 - (c_{12})^2))} \tag{4}$$

The output inductance L_{out} is determined by the allowed output current ripple k_{Iout} and the output current I_{out} under full load condition:

$$L_{out} = \frac{{}^{V_{in}}/_{ktr} - V_{out}}{\frac{P_{out}}{V_{out} \cdot k_{Iout}}} \cdot ktr \cdot {}^{V_{out}}/_{V_{in}} \cdot {}^{Tp}/_{2} \tag{5}$$

c) Section 3 ($t = t_3..t_4$): The converter is in the free-wheeling phase, where the transformer is short circuited by the high-side or low-side MOSFETs, respectively. The current slope is determined by the output side and can be calculated with:

$$\frac{\Delta i_p}{\Delta(t_3..t_4)} = \frac{V_{out} \cdot c_{12} \cdot \sqrt{L_2}}{\sqrt{L_1} \cdot (L_{out} + L_2 \cdot (1 - (c_{12})^2))} \tag{6}$$

With the current slopes, the piecewise linear current sections confer Fig. 5 can be expressed as:

$$\begin{aligned} \frac{\Delta i_p}{\Delta(t_0..t_2)} &= \frac{I_{P1} + I_{P3}}{(\alpha + \beta) \cdot {}^{Tp}/_{2}} \\ \frac{\Delta i_p}{\Delta(t_2..t_3)} &= \frac{I_{P2} - I_{P1}}{(D - \alpha - \beta) \cdot {}^{Tp}/_{2}} \\ \frac{\Delta i_p}{\Delta(t_3..t_4)} &= \frac{I_{P2} - I_{P3}}{(1 - D) \cdot {}^{Tp}/_{2}} \end{aligned} \tag{7}$$

where Tp is the switching period and D is the duty cycle, which is defined as:

$$D = ktr \cdot {}^{V_{out}}/_{V_{in}} + \alpha + \beta \tag{8}$$

By inserting (3)-(6) and (8) in (7) and solving for I_{P1}, I_{P2} and I_{P3}, the result solutions are only depending on α and β.

To eliminate α and β, two additional equations have to be found. The first expression is the periodicity of the primary current:

$$\begin{aligned} 0 = &\frac{\Delta i_p}{\Delta(t_0..t_2)} \cdot \beta \cdot {}^{Tp}/_2 + \frac{\Delta i_p}{\Delta(t_2..t_3)} \cdot (D-\alpha-\beta) \cdot {}^{Tp}/_2 \\ &- \frac{\Delta i_p}{\Delta(t_3..t_4)} \cdot (1-D) \cdot {}^{Tp}/_2 - \frac{\Delta i_p}{\Delta(t_0..t_2)} \cdot \alpha \cdot {}^{Tp}/_2 \end{aligned} \tag{9}$$

The second expression is the equation of the average output power:

$$\begin{aligned} P_{out} = V_{out} \cdot \frac{2}{Tp} \cdot ktr \cdot \Bigg[\quad &\ldots \\ &\int_{\alpha \cdot {}^{Tp}/_2}^{(\alpha+\beta) {}^{Tp}/_2} \frac{\Delta i_p}{\Delta(t_0..t_2)} \cdot (t - \alpha \cdot {}^{Tp}/_2) \cdot dt \\ &+ \int_{(\alpha+\beta) \cdot {}^{Tp}/_2}^{D \cdot {}^{Tp}/_2} I_1 + \frac{\Delta i_p}{\Delta(t_2..t_3)} \cdot (t - (\alpha+\beta) \cdot {}^{Tp}/_2) \cdot dt \\ &+ \int_{D \cdot {}^{Tp}/_2}^{{}^{Tp}/_2} I_2 - \frac{\Delta i_p}{\Delta(t_3..t_4)} \cdot (t - D \cdot {}^{Tp}/_2) \cdot dt \\ &+ \int_{{}^{Tp}/_2}^{(1+\alpha) \cdot {}^{Tp}/_2} I_3 - \frac{\Delta i_p}{\Delta(t_0..t_2)} \cdot (t - {}^{Tp}/_2) \cdot dt \quad \Bigg] \end{aligned} \tag{10}$$

with

$$\begin{aligned} I_1 &= \frac{\Delta i_p}{\Delta(t_0..t_2)} \cdot \alpha \cdot {}^{Tp}/_2 \\ I_2 &= I_1 + \frac{\Delta i_p}{\Delta(t_2..t_3)} \cdot (D - \alpha - \beta) \cdot {}^{Tp}/_2 \\ I_3 &= I_2 - \frac{\Delta i_p}{\Delta(t_3..t_4)} \cdot (1 - D) \cdot {}^{Tp}/_2. \end{aligned} \tag{11}$$

Equations (9) and (10) can be solved for α and β by inserting the characteristic current points from the solutions of (7). (The solutions for I_{P1}, I_{P2} and I_{P3}, as well as for α and β are omitted for the sake of brevity.) The definition of the current and voltage waveforms allows the calculation of the rms-values, the derivations of the rms-values and harmonics for transformer, inductor, capacitor and semiconductor currents for the following loss calculations.

B. Semiconductor Losses

The losses in the full bridge switches are derived with the $R_{DS,on}$, the gate charge Q_G, the energy equivalent output capacitance $C_{oss,eq}$ at 400 V and the energy in the output capacitance $E(V)$ as function of the applied voltage for a preselected MOSFET (cf. section III-A). The conduction losses are calculated with:

$$P_{cond} = \frac{R_{DS,on} \cdot I_{sw,rms}^2}{n_{sw,p}} \tag{12}$$

with the rms-value $I_{sw,rms}$ of the current through the MOSFET and $n_{sw,p}$, the number of parallel connected MOSFETs.

Since the converter topology offers zero voltage switching (ZVS) by inserting an interlock delay between the switching states, switching losses are almost zero in principle. However, especially at part load conditions, the interlock delay might not be sufficient for a complete resonant dis-/charge of the MOSFETs in one bridge leg, i.e. a residual voltage V_{res} is remaining, which has to be discharged by the the MOSFET. The residual voltage is calculated based on a RLC-resonant circuit consisting of the leakage inductance L_σ, the energy equivalent output capacitance $C_{oss,eq}$ and the $R_{DS,on}$ of the parallel connected MOSFETs. With the characteristic energy curve of the used MOSFET, which is described by piecewise polynomial function dependent on the applied residual voltage, the switching losses P_{sw} of one bridge leg can be determined as:

$$P_{sw} = 2 \cdot n_{sw,P} \cdot E(V_{res}) \cdot f_{sw}, \tag{13}$$

where $n_{sw,P}$ is the number of parallel full bridge MOSFETs and f_{sw} is the switching frequency. Since the switch-off current are different for the two bridge legs, the switching losses are calculated separately.

In addition the losses in the gate driver P_{drive} are considered as well and are calculated for each switch with:

$$P_{drive} = n_{sw,P} \cdot (V_{GS,on} \cdot Q_G \cdot f_{sw} + P_{driver}), \tag{14}$$

taking the number of parallel connected MOSFETs $n_{sw,P}$ and losses of the driver P_{driver} into account. Note, that the applied on-gate-source voltage $V_{GS,on}$ has an positive value and the off-gate-source voltage $V_{GS,off}$ is considered to be zero in the assembly and thus omitted in (14).

The conduction and gate drive losses in the synchronous rectifier switches are calculated in the same manner as the full bridge switches with (12) and (14). Since the rectifier MOSFETs are turned-on during the free-wheeling phase, where the voltage is approximately zero over the switches, the switching losses are negligible. Recovery losses in the body diode are avoided because the MOSFETs are turned off at the point, where the current is completely commuted from SR1 to SR2 cf. Fig. 2 or vice versa, respectively.

C. Losses in the Magnetic Components

In the inner optimization procedure, the geometry parameters of the magnetic components cf. Fig. 4 are varied systematically in order to obtain the minimum losses, with the maximum flux density B_{max} and component volume (bounding box) as constraint, since the losses are decreasing continuously for higher volumes as explained in section III-B. For the assembly, foil windings are considered, whose optimal foil thickness can be calculated with [6]:

$$d_{opt} = \frac{1}{\Psi^{\frac{1}{4}}} \cdot \sqrt{\frac{2 \cdot \pi \cdot f_{sw} \cdot I_{rms}}{I'_{rms}}} \cdot \delta_0 \tag{15}$$

with the rms-values of the currents I_{rms} in the windings and whose derivations I'_{rms}, respectively. Ψ is defined as:

$$\Psi = \frac{5 \cdot N^2 - 1}{15}, \tag{16}$$

the skin depth δ_0, the resistivity ρ of copper and the permeability of free space μ_0. The peak-to-peak flux density ΔB in the transformer is approximately defined via:

$$\Delta B = \frac{V_{in} \cdot D \cdot {}^{Tp}/_{2}}{N_P \cdot A_{core}} \tag{17}$$

with number of primary turns N_P and the cores cross section area A_{core}. The maximum flux density B_{max} is half of the peak-to-peak flux density. With the extended Steinmetz formula in [7], the core losses can be determined:

$$P_{co,tr} = \frac{k_i \cdot \Delta B^{(\alpha_S - \beta_S)}}{Tp} \cdot 2 \cdot \left(\frac{V_{in}}{N_P \cdot A_{core}} \cdot D \cdot {}^{Tp}/_{2} \right) \cdot Vol_{co} \tag{18}$$

with the core volume Vol_{co} and

$$k_i = \frac{k_S}{2^{(\beta_S+1)} \cdot \pi^{(\alpha_S-1)} \cdot \left(0.2761 \cdot \frac{1.7061}{\alpha_S + 1.354} \right)}. \tag{19}$$

For the calculation of the winding losses, the HF-losses due to the skin and proximity effect are considered. The underlying model is based on a one-dimensional approach [8]. With the magnitudes of the current harmonics $I_{P,h,n}$ (with $n = 0..n_h$ and n_h the number of calculated harmonics) the primary winding losses due to the skin effect in the windings are:

$$\begin{aligned} P_{skin,P} &= R_{DC,P} \cdot (I_{P,h,0})^2 + \dots \\ &+ \sum_{n=1}^{n_h} R_{DC,P} \cdot \frac{\nu_P}{4} \cdot \frac{\sinh \nu_P + \sin \nu_P}{\cosh \nu_P - \cos \nu_P} \cdot (I_{P,h,n})^2 \end{aligned} \tag{20}$$

with the dc-resistance $R_{DC,P}$ of the primary winding:

$$R_{DC,P} = \frac{l_{w,P} \cdot \rho}{d_{opt,P} \cdot b_{foil}} \tag{21}$$

whereas $l_{w,P}$ is the length of the primary winding, $d_{opt,P}$ is the optimal foil thickness, b_{foil} is the winding width and ν_P is defined as:

$$\nu_p = \frac{d_{opt,P}}{\sqrt{\frac{\rho}{\pi \cdot n \cdot f_{sw} \cdot \mu_0}}} \tag{22}$$

The losses due to the proximity effect in the primary winding are defined as:

$$\begin{aligned} P_{proxP} &= \sum_{n=1}^{n_h} \sum_{m=1}^{N_P} \frac{b_{foil} \cdot \rho}{\sqrt{\frac{\rho}{\pi m f_{sw} \mu_0}}} \cdot \frac{\sinh \nu_P + \sin \nu_P}{\cosh \nu_P - \cos \nu_P} \dots \\ &\cdot \left(\frac{1}{2 \cdot b} \cdot I_{P,h,n} \cdot (2 \cdot m - 1) \right)^2 \cdot l_{w,P} \end{aligned} \tag{23}$$

The winding losses in the secondary windings are calculated with the same approach as for the primary windings, however, since the winding order is: primary - secondary 1 - secondary 2, two cases have to be considered for calculating the proximity effect: Current is flowing in secondary 1 leads only to losses this winding. If the current is flowing in secondary 2, the H-field in secondary 1 is not zero which results in additional losses in secondary 1.

The losses in the output inductor can be calculated with the same approach as for the transformer, however, HF-losses only have minor influence to the winding losses, since the output current has only a small ac-component compared to the dc-component. Because of the negligible ac-component, the foil thickness with (15) would result in large values and thus, its limited to 300 μm. The peak-to-peak flux ΔB_{Lout} can be calculated with:

$$\Delta B_{Lout} = \frac{L_{out} \cdot k_{Iout} \cdot I_{out}}{N_L \cdot A_{core,L}} \tag{24}$$

with the number of output inductor turns N_L and the cross-section area $A_{core,L}$ of the inductor core. The maximum flux density is defined as

$$B_{max,L} = \frac{L_{out} \cdot (I_{out} + {}^{1}/_{2} \cdot k_{Iout} \cdot I_{out})}{N_L \cdot A_{core,L}} \tag{25}$$

D. Dielectric losses in the output capacitor

With the applied output capacitor from muRata [9] (2.2 μF / 100 V / X7R / 1210 housing) and the given loss factor $\tan \delta$ the losses are determined with:

$$P_{Cout} = \frac{I_{Cout,rms}^2 \cdot \tan \delta}{2 \cdot \pi \cdot f_{sw} \cdot C_{out}} \tag{26}$$

with the rms-value of the capacitor ripple current $I_{Cout,rms}$. There, it is assumed, that the output current I_{out} has only a dc-component and the entire ripple current is flowing in the output capacitance. The capacitance can be calculated with the allowed voltage ripple V_{pp} by solving the equation with respect to C_{out}:

$$\begin{aligned} V_{pp} = \frac{1}{C_{out}} \cdot \Bigg[&\int_0^{{}^{1}/_{2} \cdot D \cdot {}^{Tp}/_{2}} \frac{I_{out} \cdot k_{Iout}}{D \cdot {}^{Tp}/_{2}} \cdot t \cdot dt + \dots \\ &+ \int_0^{{}^{1}/_{2} \cdot (1-D) \cdot {}^{Tp}/_{2}} \frac{I_{out} \cdot k_{Iout}}{(1-D) \cdot {}^{Tp}/_{2}} \cdot t \cdot dt \Bigg] \end{aligned} \tag{27}$$

The losses in the auxiliary supply and control unit are considered to be constant over the entire load range and set to 3 W.

III. Optimization Results

In this section the results of the optimization procedure are presented and discussed. The results have been proved with simulations.

A. Optimum Number of Parallel Switches

Before the first start of the optimization procedure, several switches have been compared with respect to the resulting losses. For preselecting the MOSFETs, a figure of merit (FOM) could be defined based on the on-conductance $G_{DS,on}$, which should be high for small conduction losses, and the energy-equivalent output capacitance of the device $C_{oss,eq}$, which should be small in order in order to obtain small/no switching losses over almost the whole power range: $FOM = {}^{G_{DS,on}}/_{C_{oss,eq}}$ [10]. This FOM is usually chosen for hard-switching devices topology and might not result in best choice for soft-switching topologies, as it will be presented.

In Fig. 6 the losses of the full bridge are presented for a fixed operation point in the optimization procedure, which may not result in the optimal design. There, Infineon

CoolMOS^{TM}IPW60R045CP [11] are applied, as an example. It can be seen, that the conduction losses P_{cond} decrease with the increasing number of the parallel switches $1/n_{sw}$, whereas the driver losses P_{drive} increases linearly with n_{sw}. The switching losses P_{sw} are approximately zero until the interlock delay between the switching states is not sufficient for the total charge transfer of the output capacitors of the two MOSFETs in a bridge leg, where the losses are increase drastically. If the number of parallel switches and the respectively capacitance reaches a value, where the capacitors could almost not be dis-/charged and the MOSFETs are completely switched hard off, the switching losses increase linearly with n_{sw}.

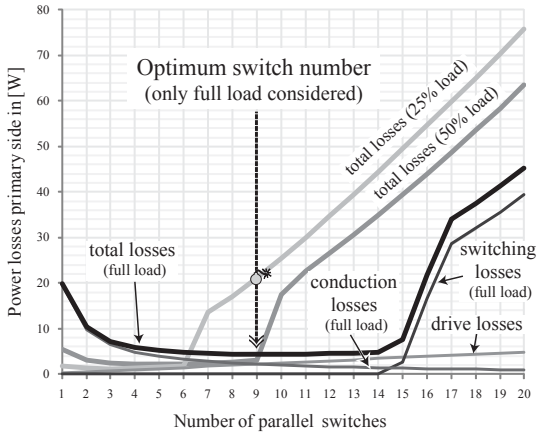

Figure 6. Dependency of parallel H-bridge switches number on device losses. (Infineon CoolMOS^{TM}IPW60R045CP [11] considered.)

If the number of parallel switches would be chosen for full load, the respective optimal point in the example of Fig. 6 would be $n_{sw,P} = 9$ switches in parallel, where the total losses on the primary side are calculated to be 4.4 W. Due to the small losses, the temperature in the devices is small and thus the on-resistance of 25 °C was considered for the comparison of several switching devices. However, at part load (e.g. 25 % output power) the total full-bridge losses increases drastically by an factor of almost 5 to 21.1 W.

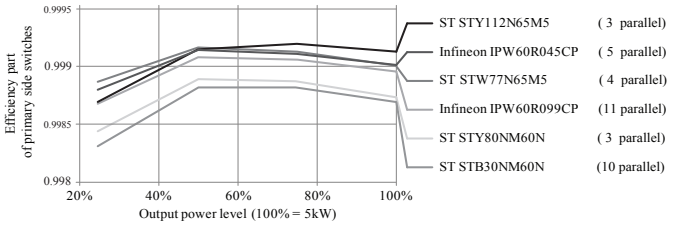

Figure 7. Efficiency contribution of full bridge switches (Examples of the considered MOSFETs). The free-parameters are fixed for the calculation, which may not present the parameters resulting in the optimal design. The curves show the optimum of the semiconductor losses with the respective optimal number of parallel switches.

In Fig. 7 the efficiency contribution of analyzed MOSFETs in the range of 600..700 V is presented. There, the free parameters have been fixed and the respective optimal number of switches which leads to the minimum losses is plotted. For the prototype, the STY112N65M5 from STMicroelectronics [12] has been chosen, since they offer the best conditions in terms of the optimization criteria as described in section II and because of the small $R_{DS,on}$ = 19 mΩ (typ), only 2 MOSFETs are needed for the final prototype design.

The same procedure is performed for the secondary side switches. However, the switching losses are approximately zero over the entire load range since the synchronous rectifiers are turned on with zero voltage condition and the current-capacitance-ratio is high enough to ensure ZVS. The selected MOSFETs for the synchronous rectifiers are IRFP4668PbF from International Rectifier [13] ($R_{DS,on}$ = 8 mΩ (typ.) / 200 V). The optimum number of parallel switches are in this case $n_{sw,s}$=11, which results in 9.3 W total losses in the synchronous rectifier.

B. Losses in the Magnetic Components

In the inner optimization procedure of the magnetic device, the geometry parameters are varied until minimum possible losses result. In Fig. 8, the allowed maximum transformer volume is varied as constraint in the inner optimization procedure with respect to the transformer losses. For each allowed volume, the optimal values for the transformer geometry are chosen so that the overall losses became minimal, considering the maximum allowed flux density in the core. The limited flux density leads to a minimum core area and/or number of primary turns N_P, respectively. The resulting optimized losses are higher because of a higher flux and smaller windings. The more volume allowed, the higher the foil width and/or the smaller the number of primary turns, and thus the smaller are the resulting losses. However, the curve becomes flat, if even a higher volume is used as the constraint in the procedure. There, an increase of the core area would lead to a reduction of the core losses but the skin/proximity losses are increasing due to a larger winding length, which have to be balanced with a larger winding in order to reduce the dc-resistance.

The optimized power losses for the maximum allowed transformer volume are presented in Fig. 8, where the geometry parameters confer Fig. 4 are not limited. It is shown, that the volume in the optimization procedure must be limited in order to obtain realizable geometry parameters and volumes.

C. Optimized Design Parameters

For the practical converter design, the volume point of 18.3 in^3 (0.3 liter) was chosen as limit for both, transformer and output inductor. First runs with the optimization procedure, where the geometry parameters of transformer and output inductor have not been limited, result in geometry parameters for the magnetic components, which are close to available standard cores. These results have been considered in order to limit the geometry parameters a and b (cf. Fig. 4) with respect to the standard core parameters in the inner optimization procedures. The best results have been reached with parameter limits of the EPCOS E70/33/32 E-Core [14] for the transformer and the Metglas AMCC 320 [15] for the inductor, which are presented in the following.

In table I the optimization results of the free parameters are presented. Conferring the described optimization criteria, the

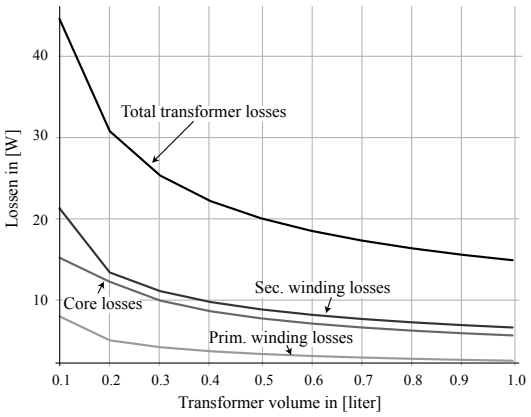

Figure 8. Transformer losses in dependency of transformer volume limit (bounding box). The curves represent the minimal losses resulting from the optimized geometry parameters with the respectively volume limits.

Table I
FREE PARAMETER OPTIMIZATION RESULTS WITH A VOLUME LIMIT OF $18.3\,in^3$ (0.3 LITER). (f_{sw} = SWITCHING FREQUENCY, N_P / N_S / N_L = PRIMARY / SECONDARY / OUTPUT INDUCTOR TURNS NUMBER, L_σ = TRANSFORMER LEAKAGE INDUCTANCE, L_{out} = OUTPUT INDUCTANCE).

f_{sw}	N_P	N_S	N_L	$n_{sw,P}$	$n_{sw,S}$	L_σ [μF]	L_{out} [μF]
16.0 kHz	22	3	5	2	12	2.0	48.8
25.0 kHz	22	3	4	2	11	1.8	43.0
37.5 kHz	15	2	3	2	9	1.0	34.6
50.0 kHz	15	2	3	1	8	1.3	34.0
100.0 kHz	15	2	2	1	6	1.8	23.1
200.0 kHz	7	1	2	1	4	1.8	1.8

optimal design with the best efficiency characteristic can be found at a switching frequency of 25 kHz.

The resulting optimized efficiency values η are given below:

Frequency	$\eta_{10\%}$	$\eta_{20\%}$	$\eta_{50\%}$	$\eta_{100\%}$
Energy star®	80.00 %	88.00 %	92.00 %	88.00 %
Goal	86.09 %	94.70 %	99.00 %	94.70 %
16.0 kHz	96.34 %	98.06 %	98.93 %	98.93 %
25.0 kHz	97.42 %	98.60 %	99.13 %	99.01 %
37.5 kHz	96.98 %	98.39 %	99.09 %	99.07 %
50.0 kHz	97.24 %	98.51 %	99.09 %	98.99 %
100.0 kHz	97.31 %	98.53 %	99.06 %	98.93 %
200.0 kHz	96.52 %	98.12 %	98.88 %	98.82 %

The power losses of the components as function of the switching frequency are presented in Fig. 9. As shown in Fig. 8 and Fig. 9, respectively, the losses in the lower frequency range are mainly determined by the magnetic components because of the volume limitation. At higher switching frequencies, the number of parallel full bridge switches decreases because the switching losses, due to not completely dis-/charge of the drain-source capacitor especially in the low-load condition, increase with the switching frequency. Additionally, the smaller number of parallel MOSETs results in higher conduction losses, as well. The pend in the total losses curve after 37.5 kHz is mainly caused by this effect, since the number of parallel switches in the full bridge changes from two to one.

The most significant impact in the decrease of the total

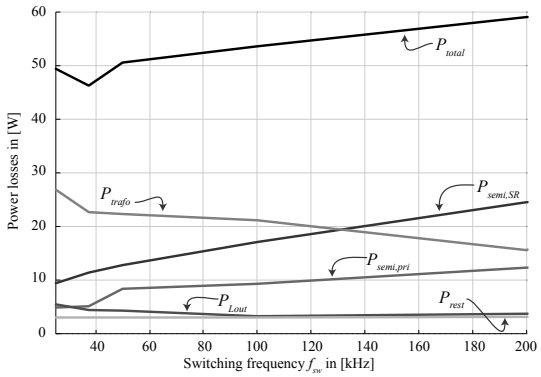

Figure 9. Losses of the optimized Phase-Shift PWM converter as a function of frequency. (P_{total} = total losses, $P_{semi,pri}$ = primary side semiconductor losses, $P_{semi,SR}$ = synchronous rectifier losses, P_{trafo} = transformer losses, P_{Lout} = output inductor losses, P_{rest} = losses in aux. supply, control unit, output capacitors).

power losses with increasing switching frequency have the losses in the synchronous rectifier, which is caused by the continuously decrease of parallel switching devices (cf. table I). Since the synchronous rectifier MOSFETs operate with ZVS, switching losses does not force the optimization procedure to reduce the switches. The decrease is caused by the increasing gate-driver losses with higher switching frequencies, which lead to a significant efficiency drop at lower load-conditions. That is why the number of synchronous rectifier switches is reduced by the optimization algorithm. However, this leads to higher conduction losses at full load.

The transformer losses are higher for lower frequency because of the volume limitation as described before. Due to the flux density limitation, the minimum number of turns rises, which leads to higher winding losses. Because of the decreasing turns numbers and the smaller required cross section areas for higher switching frequencies, the losses in the magnetic components are decreasing as well. For frequencies higher than 200 kHz, the winding losses (due to the proximity and skin effect), as well as the core losses are increasing again. For the output inductor, the losses are mainly caused by the conduction losses, which are decreasing for higher frequency due to the decreasing turns number. However, for higher switching frequencies, HF-losses in the winding and higher core losses are increasing, like for the transformer. (Note, that switching frequencies above 200 kHz have been omitted in this paper, since for higher frequencies, additional losses have especially to be considered in the cores of the magnetic components due to the non-uniform flux distribution. The accuracy of the applied models in the optimization procedure would decrease.)

The residual losses (control unit, auxiliary supply, output capacitors) stay approximately constant over the entire frequency range.

IV. PROTOTYPE

In Fig. 10 the prototype design for the proposed converter is presented. Standard components have been applied:

Transformer	EPCOS E70/33/32, 2 in parallel
Output inductor	Metglas AMCC320 (cut legs)
Full bridge MOSFETs ..	ST STY112N65M5, 2 in parallel
Sync. rectifier MOSFETs	IR IRFP4668PbF, 11 in parallel
Gate driver	IXYS IXDD414
Digital control	TI TMS320F2808

In order to utilize the winding window with a high copper fill factor, Litz wires have been used instead of foil wires (primary winding: 175/0.2 mm; secondary winding: 600/0.2 mm; inductor winding: 1200/0.2 mm) .

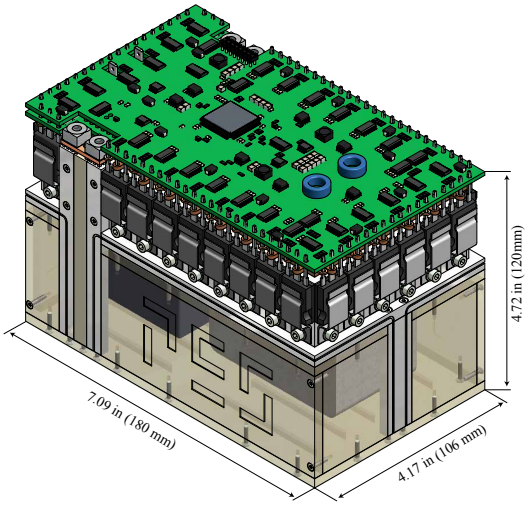

Figure 10. Prototype design of the proposed high efficient DC-DC converter. (η = 99.2 % at full load, ρ = 36 W/in^3 (2.2 kW/liter)).

Because of the selected components, the volumes are higher as the volume limit of 18.3 in^3 (0.3 liter), used in the optimization procedure. For the transformer, the volume results in 29.2 in^3 (0.48 liter) and for the output inductor 23.1 in^3 (0.39 liter). This leads to further improvement for the efficiency as presented below. The total losses decrease to 37.0 W (full load) and the part load efficiency result in:

Load condition	10 %	20 %	50 %	100 %
Efficiency	98.0 %	99.0 %	99.3 %	99.2 %

In Fig. 11 the loss distribution is depicted for full load conditions. The major loss distribution has the transformer together with the output inductor (55 %), followed by the power semiconductor losses (37 %).

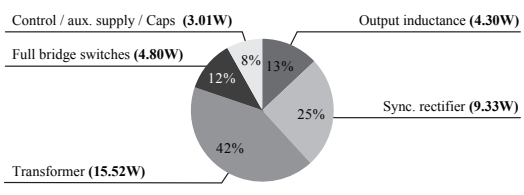

Figure 11. Loss distribution at full load (5 kW) for the prototype design.

The resulting power density of this design is ρ = 36 W/in^3 (2.2 kW/liter). Since the simulations have validated the analytical models and based on the experiences with the power density optimization (e.g. [10] and [4]), the metrological validation with the prototype seems very promising. However, variances could occur mainly because of the not considered contact resistances, which are strongly depended on the design and assembly.

V. Conclusion

In this paper, the design process of an ultra high efficient 400V/48..50V DC-DC converter for data center and telecom application is presented. An optimization procedure based on comprehensive analytical models, considering the part-load efficiency, was applied to find the optimal design. The final prototype design results in a calculated efficiency of η = 99.2 % at full load and offers a flat efficiency curve over the entire load range. At 10 % load, i.e. 500 W, the converter system exhibits still an efficiency of 98.0 %. The power density of the realized prototype is ρ = 36 W/in^3 (2.2 kW/liter).

Acknowledgment

The authors would like to thank Mr. Harder as representative of the European Center for Power Electronics (ECPE) [16] for funding this project. In addition, the authors would like to acknowledge the support of Dr. Kirchenberger and Dr. Rauscher (ST Microelectronics) for providing the full bridge MOSFET samples, Mr. Spring (Rotima AG) for providing the Litz wires and Mr. Rappel (EPCOS AG) for providing E-core samples.

References

[1] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM Converter Power Density Barriers," in *Proceedings of the 4th Power Conversion Conference (PCC'07)*, apr 2007, pp. 9–29.
[2] K. G. Brill, "Moore's law economic meltdown," jun 2008. [Online]. Available: www.forbes.com
[3] J. W. Kolar, J. Biela, and U. Badstubner, "Impact of power density maximization on efficiency of dc-dc converter systems," in *7th Internatonal Conference on Power Electronics (ICPE'07)*, oct 2007, pp. 23–32.
[4] U. Badstuebner, J. Biela, B. Faessler, D. Hoesli, and J. W. Kolar, "An Optimized 5 kW, 147 W/in^3 Telecom Phase-Shift DC-DC Converter with Magnetically Integrated Current Doubler," in *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition (APEC'09)*, vol. 24, feb 2009, pp. 21 – 27.
[5] ENERGY STAR®, "ENERGY STAR® Program Requirements for Computer Servers," aug 2008. [Online]. Available: www.eu-energystar.org/
[6] W. G. Hurley, E. Gath, and J. D. Breslin, "Optimizing the ac resistance of multilayer transformer windings with arbitrary current waveforms," in *IEEE Transaction on Power Electronics*, vol. 15, no. 2, mar 2000, pp. 369–376.
[7] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate Prediction of Ferrite Core Loss with Nonsinusoidal Waveforms Using Only Steinmetz Parameters," in *Proceedings of the 8th IEEE Workshop on Computers in Power Electronics (COMPEL'02)*, jun 2002, pp. 36–41.
[8] J. A. Ferreira, "Improved analytical modeling of conductive losses in magnetic components," in *IEEE Transactions on Power Electronics*, vol. 9, jan 1994, pp. 127–131.
[9] "Homepage of muRata Manufacturing Co., Ltd." [Online]. Available: www.murata.com
[10] J. W. Kolar, J. Biela, and J. Miniboeck, "Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2 % Efficiency vs. 7 kW/dm^3 Power Density," in *14th International Power Electronics and Motion Control Conference (IPEMC'09)*, may 2009.
[11] "Homepage of Infineon." [Online]. Available: www.infineon.com
[12] "Homepage of ST Microelectronics." [Online]. Available: www.st.com
[13] "Homepage of International Rectifier." [Online]. Available: www.irf.com
[14] "Homepage of EPCOS AG." [Online]. Available: www.epcos.com
[15] "Homepage of Metglas Inc." [Online]. Available: www.metglas.com
[16] "Hompage of the European Center for Power Electronics e.V." [Online]. Available: www.ecpe.org