Parallel Connection of Two Three-Phase Three-Switch Buck-Type Unity-Power-Factor Rectifier Systems With DC-Link Current Balancing

Martina Baumann and Johann W. Kolar, *Senior Member, IEEE*

***Abstract*—Connecting three-phase rectifier systems in parallel shows many advantages as compared to a single rectifier system with higher output power, such as higher reliability, smaller current and voltage ripple components, lower filtering effort, or higher system bandwidth. However, current unbalance or circulating currents can occur for modular design. In this paper, the parallel connection of two three-phase three-switch buck-type unity-power-factor pulsewidth-modulation rectifier systems is experimentally investigated for a 10-kW digital-signal-processor-controlled prototype. A space vector modulation scheme is employed showing all the advantages of an interleaved operation. Three control schemes for active dc-link current balancing are described employing an additional free-wheeling state that allows to influence the rate of change of the dc-link currents and can therefore be used for dc-link current balancing. The control schemes differ concerning control action and additional switching losses. Simulation and experimental results confirm the theoretical considerations: The dc-link current-balancing capability of the different control methods is compared, and the influence of the additional free-wheeling state on switching losses and operation behavior is investigated. The most advantageous control method, which employs a hysteresis controller and shows limited switching losses, is selected. The analysis of the mains behavior shows an improvement as compared to a single rectifier operation.**

***Index Terms*—Buck rectifier, circulating current, current balancing, parallel three-phase rectifiers, power factor correction, pulsewidth modulation (PWM).**

I. Introduction

THE PARALLEL connection of three-phase rectifier systems shows many advantages as compared to a single rectifier system with higher output power, such as higher reliability, smaller current and voltage ripple components, lower filtering effort, or higher system bandwidth. However, connecting two (or more) rectifier systems directly in parallel to a common load can cause current differences in the rectifier modules resulting from 1) the current unbalance of the rectifier modules and/or 2) the circulating currents among the phases of different paralleled modules. Therefore, in order to avoid the overloading of one rectifier module, a possibility for balancing the output currents of each rectifier module and for suppressing the circulating current is required. For current balancing, usually, a common reference signal is shared among all rectifier modules [1]. For suppressing the circulating current, there are passive and active methods given in the literature. A passive method is, e.g., to add a three-phase isolation transformer, which is heavy and bulky for high-power applications [2], [3]. Active methods for circulating current suppression are discussed in, e.g., [1] and [4]–[7]. However, most articles treat the parallel connection of three-phase boost-type rectifier systems.

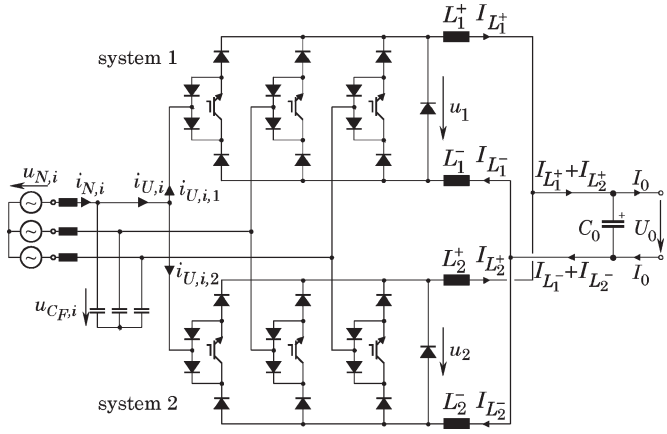

Fig. 1. Power circuit of the parallel connection of two three-phase/switch buck-type unity-power-factor PWM rectifier systems.

In this paper, the parallel connection of two three-phase/switch buck-type unity-power-factor pulsewidth-modulation (PWM) rectifier systems [8], [9] is theoretically and experimentally investigated. At the Vienna University of Technology, a prototype with a rated output power of 10 kW was realized by the parallel connection of two single rectifier systems with integrated boost output stage each having a rated power of 5 kW [10], an input voltage range of (208–480) V_{rms} line-to-line, and 400-V output voltage (cf. Fig. 1). The parallel systems are sharing a common LC input filter and are each operating at $f_P \approx 24$ kHz switching frequency. The parallel operation shows the following advantages over a single system with 10-kW rated power:

- For an interleaved operation, the input current harmonics of the partial systems with switching frequency do cancel each other, i.e., the first high-frequency current harmonic occurring in the input current spectrum is at twice the pulse frequency.
- The input currents show a more continuous shape.

Manuscript received February 28, 2007; revised July 12, 2007.

M. Baumann is with the Institute of Electrical Drives and Machines, Vienna University of Technology, 1040 Vienna, Austria (e-mail: martina.baumann@tuwien.ac.at).

J. W. Kolar is with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, 8092 Zurich, Switzerland (e-mail: kolar@lem.ee.ethz.ch).

Digital Object Identifier 10.1109/TIE.2007.907006

- The cutoff frequency of the input filter can be shifted to higher frequencies, which results in a reduction of the input filter size.
- The cross-over frequency of the output current control can be shifted to higher frequencies, which results in higher control dynamics.
- Higher reliability is obtained. In case one rectifier system fails, a reduced power can still be supplied.

There are different strategies for the parallel connection of three-phase buck-type PWM rectifier systems presented in the literature, where interleaving of the modules is applied to reduce the input current harmonics, ripple components, and size of the input filter. The parallel connection of two three-phase/switch buck-type PWM rectifier systems is treated in [11] and [12]; however, in these papers, no control concept for balancing the dc-link current of the rectifier modules is given. The dc-link current equalization for parallel six-switch buck-type PWM rectifier systems is described in [13], where the dc-link current balancing is realized by the correction of the duration of the free-wheeling and active switching states. Furthermore, the active dc-link current balancing of the parallel buck-type PWM rectifier systems is treated in [14] and [15], where the modeling and control concept are derived from the control concept for the dc-link current equalization of parallel *boost-type* PWM rectifiers, where the mains zero-sequence system is used to detect unequal dc currents. However, an analysis of this concept shows that there is no unique connection between mains zero-sequence system and unbalanced dc currents, i.e., *different* cases of unbalanced dc-link current—which request different controller actions—show the *same* mains zero-sequence systems.

In this paper, a new space-vector-oriented control concept for the parallel connection of n three-phase/switch buck-type PWM rectifier systems is presented considering the appearance of $(2n-1)$ independent dc currents [16]. In Section II, the basic principle of operation is briefly described, and the input current space vectors are analyzed concerning their redundancy of the switching states. An advantageous modulation method is presented in Section III. Furthermore, the connection between the mains zero-sequence system and the dc-link current unbalance is analyzed in Section IV, possibilities for an active dc-link current balancing by redundant switching states are discussed, and a control structure is presented in Section V. In Section VI, the global and local system operating behavior is experimentally investigated, the influence of the additional switching state on the system operating behavior is investigated, and two modified control structures are proposed, which allow to reduce additional switching losses. Moreover, experimental results derived from the modified control structures are compared, and the mains behavior is analyzed.

II. Theoretical Considerations

In this section, a brief outline of the basic principle of operation of the three-phase/switch buck-type unity-power-factor PWM rectifier is given based on a single-system operation. The time behavior of the resulting rectifier input currents and the corresponding rectifier input current space vectors are shown.

In order to obtain a resistive fundamental mains behavior, the phase currents $i_{N,i}$ and/or the fundamentals of the discontinuous rectifier input phase currents $i_{U,i}$, where the subscript $i = R, S, T$, lying in phase with the corresponding mains phase voltages $u_{N,i}, i = R, S, T$, have to be formed (there, the voltage drop across the mains filter inductors L_F is neglected, i.e., $u_{N,i} \approx u_{C_F,i}$ is assumed). This is achieved by proper selection of the on-times of the power transistors S_i, $i = R, S, T$,[1] whereby the output current is sinusoidally distributed to the mains phases [9], where the dc-link current I is assumed to be impressed by the output inductors and shows a constant value.

A. Input Current Space Vectors

The following considerations are limited to a mains interval $u_{N,R} > u_{N,S} > u_{N,T}$, which is denoted as "interval 1" in this paper, with the mains phase voltages being defined as

$$\begin{aligned} u_{N,R} &= \hat{U}_N \cos(\varphi_U) \\ u_{N,S} &= \hat{U}_N \cos(\varphi_U - 2\pi/3) \\ u_{N,T} &= \hat{U}_N \cos(\varphi_U + 2\pi/3) \end{aligned} \tag{1}$$

where φ_U denotes the mains phase angle ($\varphi_U = \omega_N t$). Due to the symmetric structure of the rectifier system and of the symmetry of the feeding ac mains, the considerations can be transferred to the other mains intervals. For a single rectifier system, there can be three active current space vectors and four zero current space vectors [switching states $j = (100), (010), (001)$ or (000)] formed at the input [cf. Fig. 2(a)]. The current in one phase can show three different values, i.e., I, 0, and $-I$; therefore, the system shows a three-level behavior. The time behavior of the mains phase current $i_{N,R}$ in phase R is shown in Fig. 2(b). The current space vectors available at the input of two rectifier systems connected in parallel are obtained by the summation of the current space vectors of each system [cf. Fig. 2(c)]. By projection on the real axis, one obtains five different magnitudes for the current in phase R, i.e., $2I$, I, 0, $-I$, and $-2I$. Therefore, the parallel connection of two rectifier systems shows a five-level behavior [cf. Fig. 2(d)]. Within interval 1, there are five active current space vectors $i_{U,\mathrm{Ak}}$, $k = 1, \ldots, 5$, and the zero vector $i_{U,\mathrm{FW}}$, which can be achieved by the different switching states of the rectifier systems. These redundant vectors are marked with an asterisk $(*)$ in Fig. 2(c).

For example, an input current condition

$$i_{U,R} = +I, \quad i_{U,S} = 0, \quad i_{U,T} = -I \tag{2}$$

is obtained if one system is in an active switching state

$$i_{U,R,1} = +I, \quad i_{U,S,1} = 0, \quad i_{U,T,1} = -I \tag{3}$$

while the other system is in the free-wheeling state

$$i_{U,R,2} = i_{U,S,2} = i_{U,T,2} = 0. \tag{4}$$

[1]For the characterization of a switching state of one system, we use the combination $j = (s_R s_S s_T)$ of the phase switching functions s_i. There, the switching function does define the switching state of the corresponding power transistor, where $s_i = 0$ denotes the OFF-state, and $s_i = 1$ denotes the ON-state.

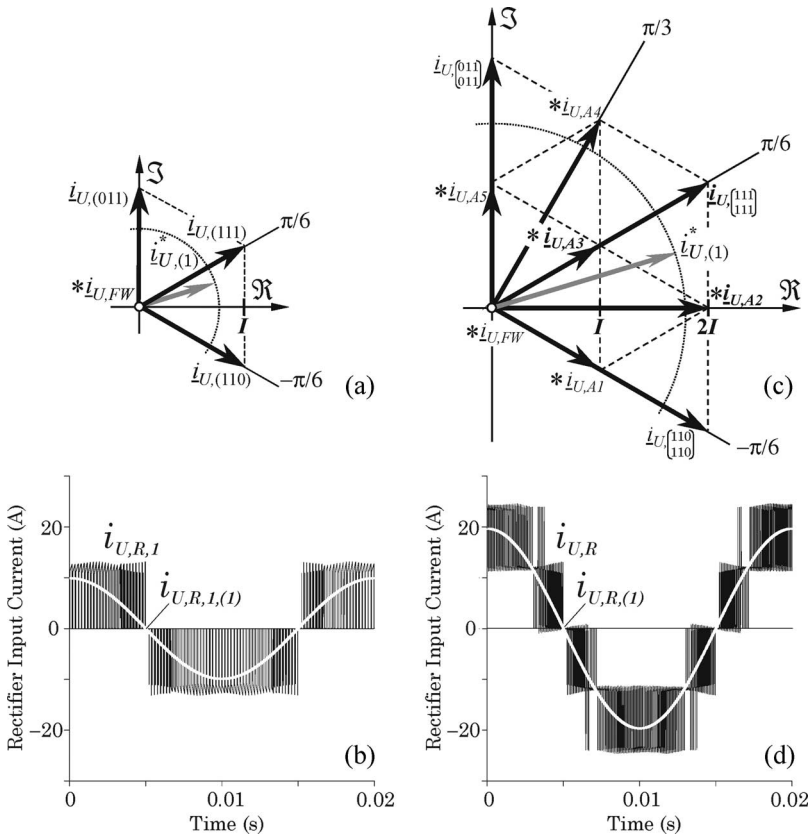

Fig. 2. Current space vectors and time behavior of the discontinuous rectifier input current in phase R for (a) and (b) single-system operation and (c) and (d) parallel operation of two rectifier systems. Furthermore, the current fundamental $\underline{i}_{U,(1)}$ in the complex space vector plane and $i_{U,R,(1)}$ in the time domain, respectively, as well as the projection of the space vectors on the positive real axis, are given. Current space vectors with redundant switching states are marked with an asterisk $(*)$.

The other possibility is switching both systems into an active switching state with, e.g.,

$$i_{U,R,1} = +I, \quad i_{U,S,1} = -I, \quad i_{U,T,1} = 0 \tag{5}$$

$$i_{U,R,2} = 0, \quad i_{U,S,2} = +I, \quad i_{U,T,2} = -I. \tag{6}$$

Both combinations (3) + (4) and (5) + (6) result in the input current condition (2); hence, they are redundant switching states concerning the input current formation. However, both possibilities result in different rates of change di/dt of the currents in the dc-link inductors, whereby the dc-link current time behavior can be influenced.

It is important to note that it is necessary to split the dc-link inductance in two parts to the positive and negative dc-link rails to avoid overcurrents. This is explained by considering switching state $j = \binom{110}{111}$ during interval 1: The desired current paths, which result in the current space vector $i_{U,A2}$ in Fig. 2(c), are shown in Fig. 3(a). If the dc-link inductors are only placed in the positive dc-link rails, the total output current $I_0 = 2I$ flows via phase T of system 2 back to the mains [cf. Fig. 3(b)]. Thereby phase T of system 2 is stressed by an overcurrent, and furthermore, the resulting input current space vector is $i_{U,\binom{111}{111}}$ in Fig. 2(c), which correspond to switching state $j = \binom{111}{111}$. Hence, it would not be possible to achieve the input current space vector $i_{U,A2}$ without splitted dc-link inductors.

III. Modulation Scheme

In [17], a modulation scheme for a high-power current-source gate-turn-off thyristor (GTO) converter is presented, where it is decided prior to each switching action which current space vector with redundant switching states is used to control and balance the dc-link currents. This method is suitable for rectifier systems with low switching frequency. For high switching frequencies, the modulation scheme employed for the parallel connection is advantageously developed based on the modulation scheme of a single rectifier system. This proposed modulation scheme of the three-phase/switch buck-type rectifier system shows the following:

1) minimum switching losses [9];
2) a minimum ripple of the dc-link inductor current [18] and of the input filter capacitor voltages [19];
3) the possibility of active current balancing for two parallel-connected rectifier systems (cf. Section V-C);
4) during a $\pi/3$-wide mains interval, one switch is clamped in the ON-state. [Remark: If the mains current distortions originating from the sliding input filter capacitor voltage intersections should be prevented, the switching state $j = (111)$ must not be used, i.e., no power transistor is clamped in the ON-state during a mains interval [20]. For example, in mains interval 1, the switching state $j = (101)$ is used instead of $j = (111)$].

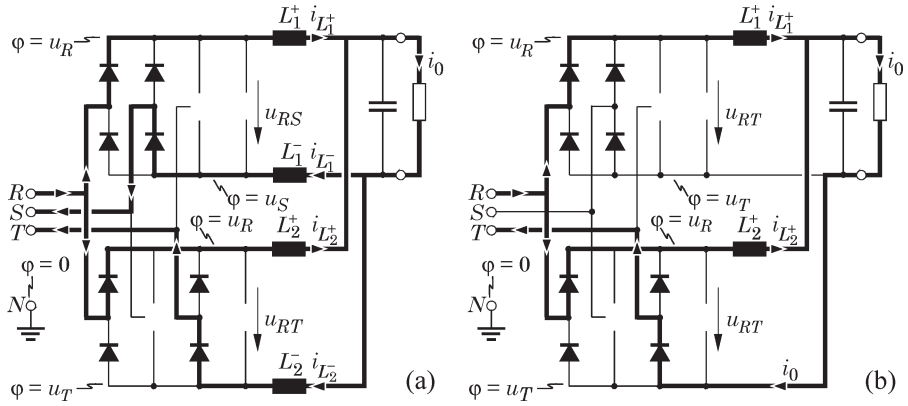

Fig. 3. Necessity for splitting of dc-link inductors to positive and negative dc-link rails for parallel-connected rectifier systems. (a) Splitted dc-link inductors to positive and negative dc-link rails. (b) DC-link inductors placed only in the positive dc-link rails resulting in overloading system 2 and in a different input current formation.

In the proposed modulation scheme, two active switching states and one free-wheeling state are employed within one pulse half period. The free-wheeling state is placed subsequent to the active switching states at the end of the pulse half period. During the free-wheeling state, the power transistor of that phase showing the minimum absolute voltage is kept in the ON-state, whereby the voltage stress on the power semiconductors in the bridge legs is held on a minimum value. In the second pulse half period, the switching states are arranged in reverse order, i.e., symmetrically to the middle of the pulse period

$$|_{t_\mu=0}\,(111)\,(110)\,(010)\,|_{t_\mu=\frac{T_P}{2}}\,(010)\,(110)\,(111)\,|_{t_\mu=T_P}. \tag{7}$$

The modulation scheme for rectifier system 2 is obtained by phase shifting the modulation scheme of rectifier system 1 by one pulse half period $T_P/2$, whereby an interleaved operation is achieved.

IV. Circulating Currents

Paralleling three-phase rectifier systems directly without using a three-phase isolation transformer [2], [3] can result in circulating currents, which are superimposed to the dc-link currents but do not contribute to the output current. The path of the circulating current is closed via the input of the rectifier systems, and the circulating current appears as a zero-sequence current in the rectifier input currents of each module connected in parallel. In dependency on the type of paralleled rectifier systems, there are different possibilities for circulating currents. In the following, the dependency between circulating current and zero-sequence current for parallel *boost-type* and *buck-type* rectifier systems is investigated.

A. Paralleled Boost-Type Rectifier Systems

The interleaved modulation of two boost-type PWM rectifier systems leads to circulating currents [1], [2]–[7], [21]. The pure zero-sequence current is explicitly shown at the cross over between two sectors if both modules are in different free-wheeling states, e.g., the top switches of one module are connected to the positive dc rail, and the bottom switches of the other module are connected to the negative dc rail. The three-phase currents will simultaneously flow from the dc-link capacitor through the top switches of one module, the boost inductors, the bottom switches of the other module, and back to the dc-link capacitor (cf. [1, Fig. 8]). Assuming an equal distribution of the circulating current i_C to all three phases, one receives for the zero-sequence current

$$i_{U,m,0} = \frac{1}{3}[i_{U,1,R} + i_{U,1,S} + i_{U,1,T}], \qquad m = 1, 2 \tag{8}$$

for modules 1 and 2

$$i_{U,1,0} = \frac{1}{3}\left[\frac{-i_C}{3} + \frac{-i_C}{3} + \frac{-i_C}{3}\right] = -\frac{i_C}{3} \tag{9}$$

$$i_{U,2,0} = \frac{1}{3}\left[\frac{i_C}{3} + \frac{i_C}{3} + \frac{i_C}{3}\right] = \frac{i_C}{3}. \tag{10}$$

A second possibility for generating a path of a pure zero-sequence current is given with the three-phase currents opposite in sign, which will now simultaneously flow from the dc-link capacitor through the bottom switches of the first module, the boost inductors, the top switches of the other module, and back to the dc-link capacitor, i.e., the circulating current has changed its direction, and one receives for the zero-sequence currents

$$i_{U,1,0} = \frac{i_C}{3} \tag{11}$$

$$i_{U,2,0} = -\frac{i_C}{3}. \tag{12}$$

Due to a single dc-link energy storage (dc-link capacitor), there is a unique dependence between the zero-sequence current and the circulating current. Therefore, by measuring the three-phase currents, the average value of the circulating current can be controlled in such a manner that it does not accumulate [1].

In [14] and [15], this method is transferred to the parallel connection of two buck-type PWM rectifier systems. Therefore, in the following subsection, the dependency of the zero-sequence current on the circulating current is investigated for paralleled buck-type rectifier systems.

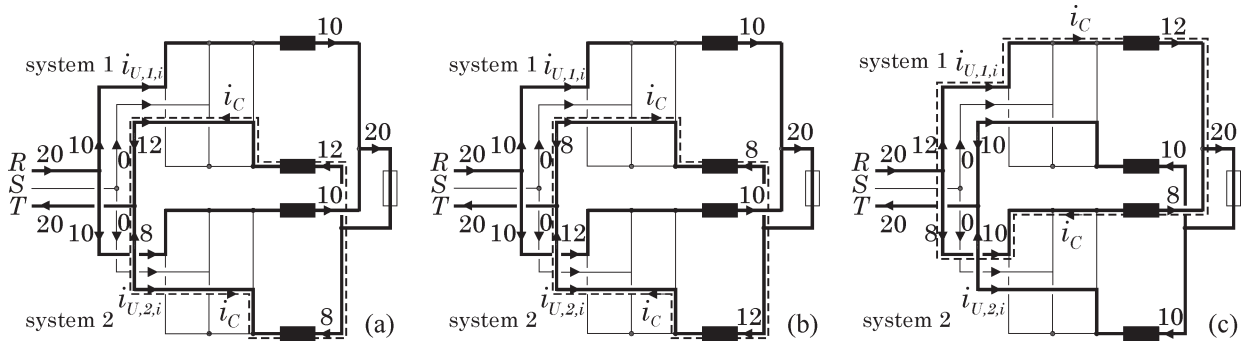

Fig. 4. Circulating currents and zero-sequence currents for paralleled three-phase/switch buck-type rectifier systems for switching state $\binom{111}{111}$. (a) Positive circulating current i_C in the negative dc-link rail of system 1. (b) Negative circulating current in the negative dc-link rail of system 1. (c) Positive circulating current i_C in the positive dc-link rail of system 1. The power semiconductors are not shown explicitly for the sake of clearness, and the numbers stand for current values (in amperes). The current flow of the circulating current i_C shown by bold lines is only valid for $i_C < I_0/2$.

B. Paralleled Buck-Type Rectifier Systems

Due to the higher number of dc energy storage (dc-link inductors), there is a higher number of circulating currents for paralleled buck-type rectifier systems. In Fig. 4, three possibilities for circulating currents are shown, where the output current is assumed to be $I_0 = 20$ A.

Case 1: In Fig. 4(a), the currents in the positive dc-link inductors are assumed to be equal, whereas the currents in the negative dc-link inductors show different values, where $i_{L_1^-} > i_{L_2^-}$. For the circulating current i_C and the zero-sequence currents at the input of modules 1 and 2, one receives with (8)

$$\begin{aligned} i_C &= i_{L_1^-} - \frac{I_0}{2} = 12\text{ A} - 10\text{ A} = 2\text{ A} \\ i_{U,1,0} &= \frac{1}{3}[10\text{ A} + 0\text{ A} - 12\text{ A}] = -\frac{2}{3}\text{ A} \\ i_{U,2,0} &= \frac{1}{3}[10\text{ A} + 0\text{ A} - 8\text{ A}] = +\frac{2}{3}\text{ A}. \end{aligned} \tag{13}$$

Case 2: If the currents in the positive dc-link inductors are assumed to be equal again, and the current $i_{L_1^-}$ is smaller than $i_{L_2^-}$ [cf. Fig. 4(b)], one receives for circulating current and zero-sequence currents

$$\begin{aligned} i_C &= i_{L_1^-} - \frac{I_0}{2} = 8\text{ A} - 10\text{ A} = -2\text{ A} \\ i_{U,1,0} &= \frac{1}{3}[10\text{ A} + 0\text{ A} - 8\text{ A}] = +\frac{2}{3}\text{ A} \\ i_{U,2,0} &= \frac{1}{3}[10\text{ A} + 0\text{ A} - 12\text{ A}] = -\frac{2}{3}\text{ A} \end{aligned} \tag{14}$$

i.e., the currents show opposite signs as compared to case 1.

Case 3: Case 3 is depicted in Fig. 4(c), where the currents in the negative dc-link rails are equal, and the current in the positive dc-link rail of system 1 is higher than the current in the positive dc-link rail of system 2. One receives the following for i_C, $i_{U,1,0}$, and $i_{U,2,0}$:

$$\begin{aligned} i_C &= i_{L_1^+} - \frac{I_0}{2} = 12\text{ A} - 10\text{ A} = 2\text{ A} \\ i_{U,1,0} &= \frac{1}{3}[12\text{ A} + 0\text{ A} - 10\text{ A}] = +\frac{2}{3}\text{ A} \\ i_{U,2,0} &= \frac{1}{3}[8\text{ A} + 0\text{ A} - 10\text{ A}] = -\frac{2}{3}\text{ A} \end{aligned} \tag{15}$$

i.e., the zero-sequence currents in cases 2 and 3 show equal values. Also, in case of, e.g., $i_{L_1^+} = i_{L_2^-} = 11$ A and $i_{L_1^-} = i_{L_2^+} = 9$ A, one receives the same values for the zero-sequence currents. Generally, one can say that a different set of dc-link currents resulting in different circulating currents can result in equal zero-sequence systems. Therefore, there is no unique dependency of circulating currents and zero-sequence system given like it is for boost-type rectifier systems. Hence, causing a zero-sequence system cannot be used for compensating the circulating currents as described in [14] and [15].

An alternative method for balancing the dc-link currents is shown in the following section.

V. DC-Link Current Symmetrization

As mentioned in Section II-A, there are switching states that are redundant concerning the input current space vector but show different current change rates of the currents in the four dc-link inductors. These redundant switching states can be used for balancing the dc-link currents. Based on a dc/dc equivalent circuit of the parallel connection of two rectifier systems, a control concept is designed.

A. Equivalent Circuit

In Fig. 5, a dc/dc equivalent circuit of two parallel-connected buck-type rectifier systems is given, where the buck-stage output voltage reference values u_1^* and u_2^* of systems 1 and 2 are split into two parts

$$u_m^* = \underbrace{u_{pm} + u_0^*/2}_{u_{\mathrm{pos},m}} + \underbrace{u_{nm} + u_0^*/2}_{u_{\mathrm{neg},m}}, \qquad m = 1, 2 \tag{16}$$

where $u_{\mathrm{pos},m}$ denotes the positive component and $u_{\mathrm{neg},m}$ denotes the negative component with reference to a common fictitious point C, where the potential φ_C of point C is equal to the potential of the phase with the power transistor kept in the ON-state during a $\pi/3$-wide mains interval and/or is kept in the ON-state during the free-wheeling state (cf. Fig. 6). The voltage sources $u_0^*/2$ are representing the buck-stage output voltages being necessary for generating the system output voltage u_0, and the additional voltage sources u_{pm} and u_{nm} allow to

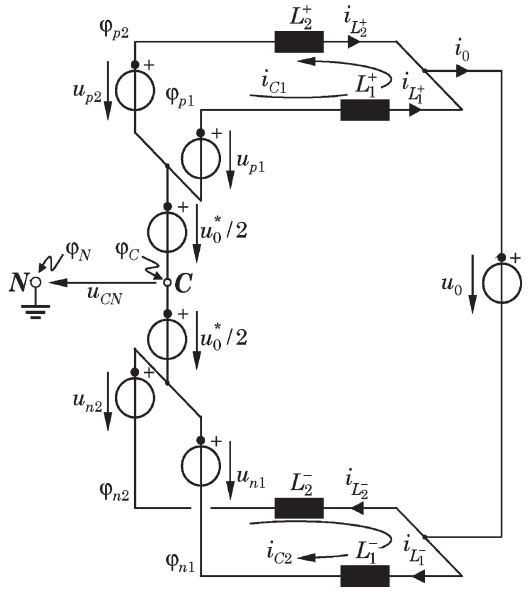

Fig. 5. DC/DC equivalent circuit of two parallel-connected buck-type rectifier systems showing the circulating currents i_{C1} and i_{C2} that represent the dc-link current unbalance and the potentials φ_{pm} and φ_{nm}, $m = 1, 2$, on the left-hand side of the dc-link inductors $L_{12}^{\pm}$. The voltage sources $u_0^*/2$ are representing the buck-stage output voltages being necessary for generating the system output voltage u_0.

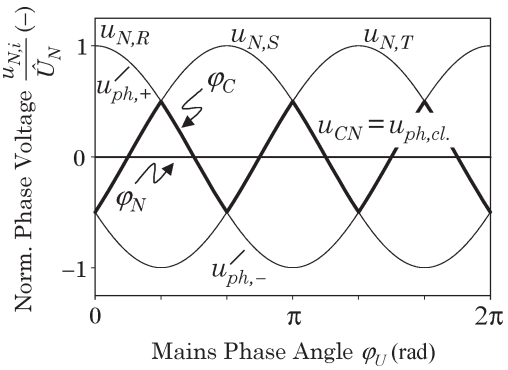

Fig. 6. Normalized mains phase voltages $u_{N,R}$, $u_{N,S}$, and $u_{N,T}$; clamped voltage $u_{\mathrm{ph,cl.}}$ at the right-hand terminals of the dc-link inductors during the free-wheeling state; voltages $u_{\mathrm{ph},+}$ and $u_{\mathrm{ph},-}$; and voltage between common point C and mains neutral point N.

influence the dc-link currents in the four dc-link inductors $L_{12}^{\pm}$. Point N is the mains neutral point.

B. Symmetrization by Different Free-Wheeling States

By definition, during the free-wheeling state, the power transistor of that phase showing the minimum absolute value is kept in the ON-state (cf. Section III). That is, the anode and—if the forward voltage drop across the free-wheeling diode D_F is neglected—the cathode, and hence the right-hand terminals of the dc-link inductors, are connected to the clamped phase (neglecting the forward voltage drops of the power semiconductors). For example, during interval 1, the power transistor in phase S is kept in the ON-state, and the right-hand terminals of $L_{12}^{\pm}$ are connected to phase S.

Therefore, the potential and hence the current change rate at this point can be influenced by keeping another power transistor in the ON-state during the free-wheeling state, which is shown by a digital simulation using CASPOC [22] in the following. If we assume, e.g., that in system 1 the free-wheeling state $j = (100)$—where the power transistor S_R in phase R is kept in the ON-state—is applied during a time interval $t_{\pm}$ (cf. Fig. 7), the potential on the right-hand terminals of dc-link inductors L_1^+ and L_1^- is increased by $(u_{\mathrm{ph},+} - u_{\mathrm{ph,cl.}})$ (cf. Fig. 6). Thereby, the current $i_{L_1^+}$ is increased by $\Delta i_{L_1^+}$ as compared to the case with the default free-wheeling state $j = (010)$ [cf. Fig. 7(b)].

In rectifier system 2, the free-wheeling state $j = (001)$ is applied during the time interval $t_{\pm}$, whereby the voltage $u_{\mathrm{ph},-} = u_{N,T}$ is applied to the right-hand terminals of L_2^+ and L_2^-. Since this voltage is smaller than the default voltage $u_{\mathrm{ph,cl.}} = u_{N,S}$, the current in L_2^+ is decreased by $\Delta i_{L_2^+}$ [cf. Fig. 7(b)]. The time behavior of currents $i_{L_1^-}$ and $i_{L_2^-}$ of the inductors in the negative dc-link rail is shown in Fig. 7(c). In Fig. 7(d), one can see that there is a minimum increase of the difference between both currents. For increasing time during the mains interval, the sign of the current change rate changes, and the difference between $i_{L_1^-}$ and $i_{L_2^-}$ is decreased.

The value of Δi_L can be increased (decreased) by increasing (decreasing) the time interval $t_{\pm}$. As described in the following section, this method is used for balancing the dc-link currents of parallel-connected three-phase/switch buck-type rectifier systems in addition to controlling the buck stage output voltages u_m.

C. Control Structure

In Fig. 8, a control structure based on the dc/dc equivalent circuit in Fig. 5 is given. If all the dc-link currents are equal and half the output current reference value $i_0^*/2$, then u_{pm} and u_{nm} are zero. In case of an unbalance, e.g., $i_{L_1^+} > i_{L_2^+}$, the potential φ_{p1} has to be decreased, and φ_{p2} has to be increased, i.e., $u_{p1} < 0$ and $u_{p2} > 0$. If the currents in the negative dc-link rails are balanced, the potentials φ_{n1} and φ_{n2} need not be changed, i.e., $u_{n1} = u_{n2} = 0$. In total, this is a reduction of the voltage reference value u_1^* of rectifier system 1 and an increase of the voltage reference value u_2^* of system 2, i.e., the modulation indices are changed to increase or decrease the dc-link current average values.

During the free-wheeling states, a modification of the potentials φ_{pm} and φ_{nm} is achieved by the application of an additional free-wheeling state (cf. Section V-B), which only shows an effect on the current change rates of the dc-link currents and does not affect the buck stage output voltages u_1 and u_2, or the system output voltage u_0. During interval 1, switching state $j = (010)$ is the default free-wheeling state, the positive potentials φ_{pm} are increased by using $j = (100)$ (due to $u_{N,R} > u_{N,S}$), and the negative potentials φ_{nm} are decreased by using $j = (001)$ (due to $u_{N,T} < u_{N,R}$).

The relative on-time of the additional free-wheeling state $t_{\pm}$ is calculated via

$$\delta_+ = \frac{u_{pm}}{u_{\mathrm{ph},+} - u_{\mathrm{ph,cl.}}} \qquad \text{for } u_{pm} > 0 \tag{17}$$

$$\delta_- = \frac{u_{pm}}{u_{\mathrm{ph},-} - u_{\mathrm{ph,cl.}}} \qquad \text{for } u_{pm} < 0 \tag{18}$$

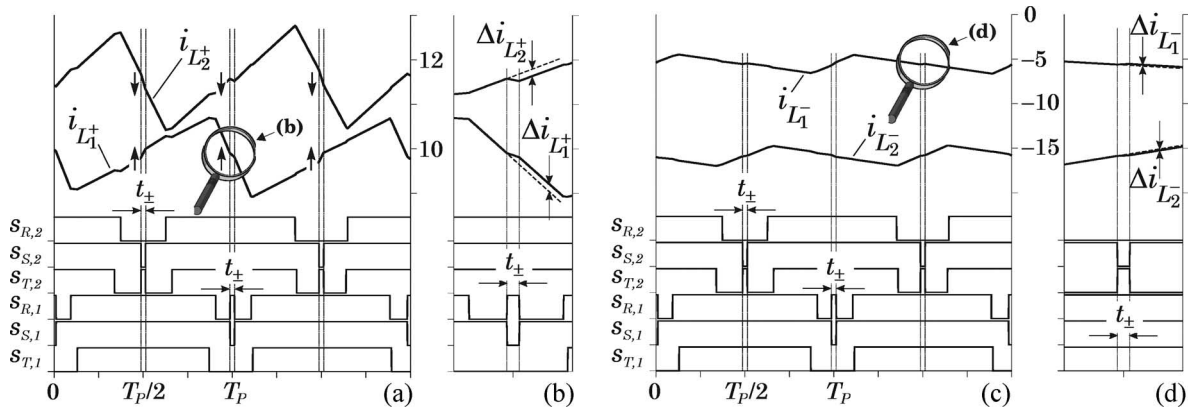

Fig. 7. Influence of the power transistor kept in the ON-state during the free-wheeling state on the current change rate di_L/dt of the dc-link current during interval 1. The behavior of the dc-link currents (a) $i_{L_1^+}$ and $i_{L_2^+}$, and (c) $i_{L_1^-}$ and $i_{L_2^-}$, is shown for a dc-link current unbalance during two pulse periods, and the according switching functions are given. (b) and (d) Detailed time behavior during the free-wheeling state. The arrows ↑ and ↓ denote the increase and decrease of the dc-link current, respectively.

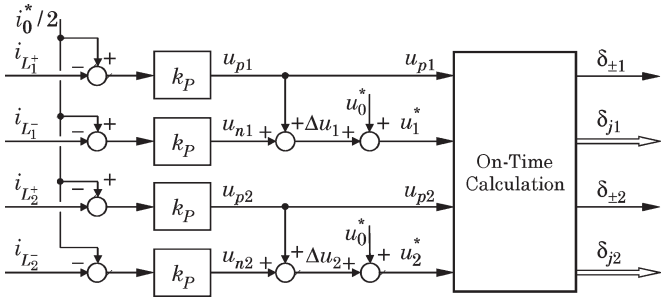

Fig. 8. Control structure for the dc-link current balancing of two parallel-connected rectifier systems based on the dc/dc equivalent circuit given in Fig. 5.

where $u_{\mathrm{ph,cl.}}$ is the voltage of that phase with the power transistor in the ON-state during the free-wheeling state by default. Voltages $u_{\mathrm{ph},+}$ and $u_{\mathrm{ph},-}$ are the voltages showing the most positive and the most negative values during one mains interval (cf. Fig. 6).

The output current reference value i_0^* in Fig. 8 is set by an outer output voltage control loop, which is not shown here, and is divided by the number n of parallel-connected rectifier systems. This value is compared with the (low-pass-filtered) dc-link currents. The p-type controller (gain k_P) sets the values of the positive and negative voltages u_{pm} and u_{nm}, and with u_{pm}, the relative on-times $\delta_{\pm,m}$ of the additional free-wheeling states are calculated using (17) and (18). The voltages u_{pm} and u_{nm} are transformed into buck-stage voltage reference values u_m^*, where a precontrol with the output voltage reference value u_0^* is provided, i.e.,

$$u_m^* = u_{pm} + u_{nm} + u_0^*, \qquad m = 1, 2. \tag{19}$$

The relative on-times of the active switching states δ_{jm} are calculated according to [9, eqs. (29)–(32)].

VI. Experimental Investigation

The experimental investigation was carried out on the parallel connection of two prototypes each having the following operating parameters:

$$\begin{aligned} P_0 &= 5\ \mathrm{kW}, & U_{N,ll} &= (208{-}480)\ \mathrm{V} \\ U_0 &= 400\ \mathrm{V} & & \\ f_N &= 50\ \mathrm{Hz}, & f_P &= 23.4\ \mathrm{kHz} \\ C_{F,i} &= 4\,\mu\mathrm{F}, & C_0 &= 750\,\mu\mathrm{F} \\ L_{F,i} &= 0.17\,\mathrm{mH}, & L_{12}^{\pm} &= 0.9\,\mathrm{mH}. \end{aligned}$$

For the dc-link current balancing of two parallel-connected rectifier systems, three dc-link currents have to be measured. At the case at hand, the currents in L_1^+, L_2^+, and L_2^- are measured, therewith the output current I_0 and the missing dc-link current in L_1^- can be calculated. The current and voltage signals are measured and adapted for signal processing, and the complete control is implemented in a 32-bit floating-point DSP ADSP-21061 SHARC (Analog Devices). For generating the switching signals for the dc-link current balancing of two rectifier systems, the PWM outputs have to be converted using two erasable programmable read-only memories (EPROMs) employing the information about the actual mains interval and which additional free-wheeling state should be added.

A. Influence of the Additional Free-Wheeling State

Ideally, if the dc-link current ripple is neglected, and ideal switching behavior and/or no switching delay are assumed, the transition between the default free-wheeling state and the additional free-wheeling state (and vice versa) does occur without additional losses since the output current is guided via the free-wheeling diode, and the power transistor that is in the ON-state during free wheeling does not carry any current. However, as a closer experimental investigation shows, the transition between two free-wheeling states does not happen directly but via an additional active switching state. For example, at the transition from free-wheeling state $j = (010)$ to $j = (100)$, the active switching state $j = (110)$ does occur, which results in additional switching losses. This is due to the fact that the power transistor that is clamped in the ON-state during free wheeling does carry the differential current $i_d = i_{L_1^+} - i_{L_1^-}$,

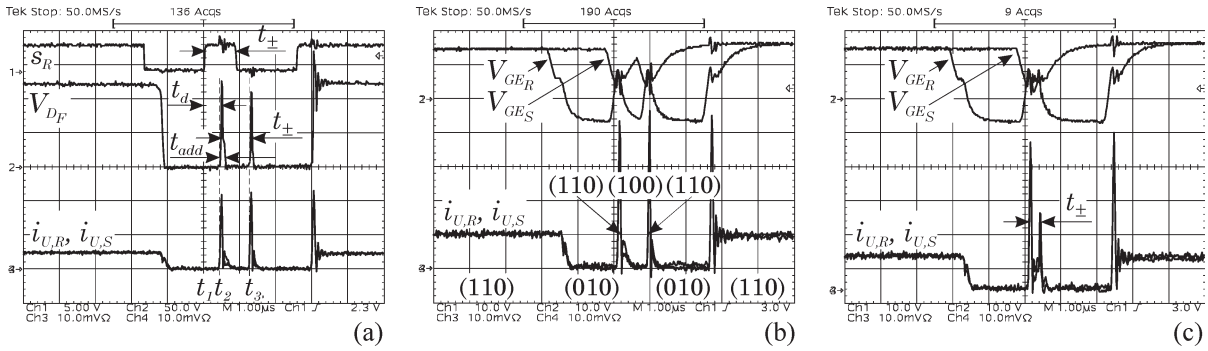

Fig. 9. Influence of the additional free-wheeling state on the rectifier input current behavior for a transition from free-wheeling state $j = (010)$ to (100) (and vice versa) in interval 1 for rectifier system 1. Additional free-wheeling state (a) and (b) $t_\pm \approx 1\ \mu$s, and (c) $t_\pm \approx 0.3\ \mu$s. Switching signal s_R and voltage V_{D_F} across the (a) free-wheeling diode, (b) and (c) gate-drive signals V_{GE_R} and V_{GE_S} for the power transistors in phases R and S, and (a)–(c) rectifier input currents $i_{U,R}$ and $i_{U,S}$. Current scales: (a) 4 A/div and (b) and (c) 2 A/div. Voltage scales: (a) V_{D_F}: 50 V/div; s_R: 5 V/div; and (b) and (c) V_{GE}: 10 V/div; time scale: 1 μs/div.

and the power transistor that is clamped during the additional free-wheeling state has to take over this differential current.

In Fig. 9, the time behavior of the discontinuous rectifier input currents $i_{U,R,1}$ and $i_{U,S,1}$ of rectifier system 1 is given for different on-times $t_\pm$ of the additional free-wheeling states. First, an additional free-wheeling state $t_\pm \approx 1\ \mu$s is applied to the rectifier system by simultaneously turning on power transistor S_R and turning off S_S at t_1 (cf. switching signal s_R in Fig. 9(a), s_S is not shown). After a time delay t_d (resulting from gate drive units and from turn-on and turn-off delay times of the power transistors), the switching action takes place at t_2, and for a time $t_{\rm add}$, both power transistors S_R and S_S are in the ON-state [cf. gate drive signals V_{GE_R} and V_{GE_S} in Fig. 9(b)]. The differential current is commutated from S_S to S_R. Therefore, an additional active switching state $j = (110)$ occurs where the current is drawn from the mains, and the free-wheeling diode D_F takes over the blocking voltage [cf. Fig. 9(a), $V_{D_F} \neq 0$ at t_2]. At the subsequent transition from (100) to (010) at t_3, the additional active switching state (110) is inserted again. Second, the additional free-wheeling state is decreased in on-time, e.g., to $t_\pm \approx 0.3\ \mu$s, whereby the duration of the inserted active state exceeds $t_\pm$; hence, no additional free-wheeling state does occur [cf. Fig. 9(c)].

The occurrence of the undesired additional active switching state has the following consequences:

- the duration of the additional free-wheeling state is decreased to $(t_\pm - t_{\rm add})$;
- the duration of the default free-wheeling state is decreased by $t_{\rm add}$;
- for a short duration $t_\pm$, the additional free-wheeling state is completely replaced by an active switching state;
- at the (ideally lossless) transition from one free-wheeling state to the subsequent free-wheeling state, switching losses that cannot be neglected do occur (+50% to +150% in dependency on which free-wheeling state is added).

In an experimental setup, the control deviation between reference and actual values of the current will always differ from zero due to errors in measurement, e.g., caused by offsets of current transducers and/or errors at the analog-to-digital conversion, etc. This results in a permanent correction and/or a permanent presence of an additional free-wheeling state and/or a permanent increase in switching losses also in case the currents in the positive and/or negative dc-link rails are (approximately) equal and no controlling action would be necessary. Therefore, a modified and simplified control structure based on the control proposed in Section V-C is chosen, where a balancing control action is determined by a hysteresis controller. This structure is described in the next subsection for the parallel connection of two rectifier systems.

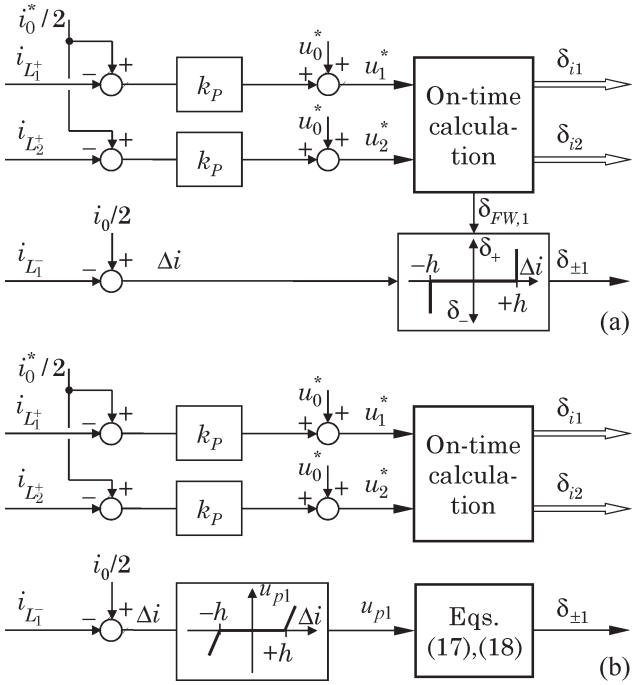

Fig. 10. Modified control structures for balancing the dc-link inductor currents based on a bang-bang control. $\pm h$ represents the width of the hysteresis. (a) Control structure 1: fixed duration of the additional free-wheeling state. (b) Control structure 2: variable on-time of the additional free-wheeling state.

B. Modified Control Structure

The modified control structure is depicted in Fig. 10(a), where the currents in the dc-link inductors L_1^+ and L_2^+ of both

rectifier systems 1 and 2 are controlled to an equal value of $i_0^*/2$. The current reference value i_0^* is again provided by an outer output voltage control loop. Voltages u_1^* and u_2^* represent the reference values for the buck-stage output voltages and are incorporated into the calculation of the relative on-times of the active switching states δ_{jm} of both rectifier systems. It is assumed that if the dc-link currents in the positive dc-link rails show equal values (by control), the output current partitioning to both negative dc-link rails is approximately equal too (cf. Section VI-C). In case a deviation from half the output current $i_0/2$ does occur, which exceeds a given value $\pm h$, an additional free-wheeling state $\delta_{\pm,1}$ is provided in rectifier system 1, which forces the current $i_{L_1^-}$—and hence the current $i_{L_2^-}$—back to its reference value, i.e., additional free-wheeling states are only added in one rectifier system, where $\pm h$ represents the width of the hysteretic band that is set to, e.g., $\pm$0.5 A, i.e., a control action only takes place if the difference of the average values of the negative dc-link currents is higher than 1 A.

For further reducing the switching losses that are occurring due to the additional free-wheeling state, the duration of the additional free-wheeling state $\delta_\pm$ is set to the maximum possible value, i.e., the duration of the default switching state δ_{FW}. Thereby, the additional switching losses are avoided for additional free-wheeling state $j = (100)$ in interval 1 due to the fact that the power transistor in phase R remains clamped in the ON-state during one pulse period instead of the transistor in phase S. For the additional free-wheeling state $j = (001)$, additional switching losses do occur at the beginning and at the end of the free-wheeling state because switching actions take place in all three bridge legs. However, the additional switching losses are limited as compared to the case where an additional free-wheeling state with $t_\pm < t_{\mathrm{FW}}$ is placed in the middle of each default free-wheeling state in every pulse period (cf. Section VI-A).

However, one has to mention that for decreasing modulation index M, $M = \hat{I}_N/I$, and for a constant source of unbalance, the time behavior of the dc-link currents that are controlled to be equal gets more and more disturbed. This is due to the fact that for decreasing modulation index, the relative on-time δ_{FW} of the free-wheeling state is increasing, whereby its influence on balancing the dc-link currents is increasing too. Therefore, an improvement of the control scheme is achieved by combining the basic control structure (cf. Fig. 8) and the modified control structure [cf. Fig. 10(a)], which results in the control structure shown in Fig. 10(b). There, the additional free-wheeling state is only used in case the difference Δi in Fig. 10 exceeds a given hysteresis value, but as compared to the control structure 1 given in Fig. 10(a), the relative on-time of the additional free-wheeling state is calculated according to (17) or (18), and the additional free-wheeling state is placed in the middle of one pulse period (cf. Fig. 7).

Both control structure 1 [which is depicted in Fig. 10(a)] and control structure 2 [which is depicted in Fig. 10(b)] were implemented in the experimental system by proper programming of the DSP and the EPROM. Measurement results and a comparison of both control structures are given in the following subsection.

C. Experimental Evaluation

The experimental investigation identifies a very good self-balancing behavior of the dc-link inductor currents, which are shown in Fig. 11(a) for a 10-A output current, a 1.5-kW output power, and a 210-V line-to-line voltage (which results in a modulation index $M = 0.6$). Since no source of unbalance is added in the experimental setup, the currents in the positive and negative dc-link rails are approximately equal (only a negligible small difference of a few 0.1 A does occur), independent on the mains phase voltage, the output voltage and current, and/or the modulation index M.

In Fig. 11(b) and (c), the performance of the proposed control structure 1 [cf. Fig. 10(a)] and control structure 2 [cf. Fig. 10(b)] is compared for the same operating point. A power resistor $R \approx 1.5\ \Omega$ is added in series to the inductor L_1^+ in order to simulate a source of unbalance. Prior to time instant t_1, the balancing control is deactivated, i.e., no additional free-wheeling states are inserted, and the currents in the negative dc-link rail show a heavy unbalance, whereas the currents in the positive dc-link rails remain balanced due to their direct control. At t_1, the balancing control is activated, and the dc-link currents are immediately controlled to equal values within a hysteresis of $\pm$0.5 A. One can see in Fig. 11(b) that for active control structure 1, the dc-link current shows noticeably higher current peaks as compared to active control structure 2 [cf. Fig. 11(c)]. This is due to the fact that for control structure 1, the default free-wheeling state—which shows a long relative on-time for low modulation indices—is totally replaced by the additional free-wheeling state, whereby the resulting current-balancing action is too heavy. For control structure 2, the duration of the additional free-wheeling state is calculated in dependency on the difference of the dc-link currents, which results in a more continuous current behavior.

The influence of the position of a source of unbalance is shown in Fig. 11(d) and (e) for a 10-A output current, a 2.2-kW output power, and 210-V line-to-line voltage (which results in a modulation index $M = 0.9$). A power resistor positioned in the positive dc-link rail [cf. Fig. 11(d)] does result in a heavier dc-link current unbalance as if the same source of unbalance is placed in the negative dc-link rails [cf. Fig. 11(e)]. This is because of the fact that the currents in the positive dc-link rails are incorporated for calculating the relative on-times of the buck input stage. Moving the source of unbalance to the negative dc-link rail, these currents are less disturbed.

Fig. 11(f) shows the limits of the proposed control concept: one can see that in the neighborhood of a boundary B between two mains intervals as defined by a combination of signs of the mains phase voltages, the effect of the additional free-wheeling state (and/or the balancing capability) is limited and/or close to zero; the current in inductor L_2^- has to be decreased; and although additional free-wheeling states are added, the current is further increasing. This is due to the decreasing difference between the mains phase voltages—which is responsible for guiding back the currents to equal values—when approaching a mains phase voltage interval boundary. For example, at the left boundary of interval 1 ($\varphi_U = 0$ in Fig. 6), the difference between mains phase voltages $u_{N,S}$ and $u_{N,T}$ is equal to zero;

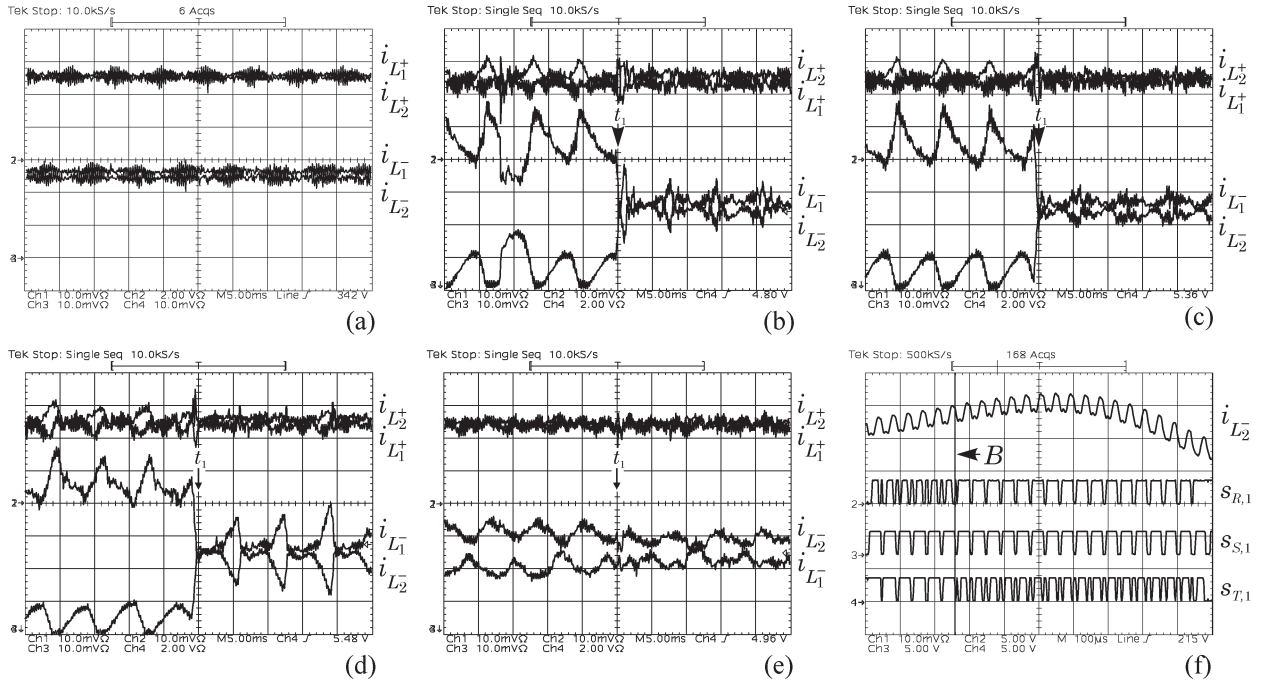

Fig. 11. Time behavior of the dc-link currents in inductors $L_{12}^{\pm}$ for a 10-A output current, 210-V line-line voltage, (a)–(c) and (f) 1.5-kW output power (modulation index $M = 0.6$), and (d) and (e) 2.2-kW output power (modulation index $M = 0.9$). (a) Self-balancing of the dc-link currents (no control for current partitioning provided). A source of unbalance ($R \approx 1.5\ \Omega$) is added in series to inductor L_1^+, and the balancing control (hysteresis value $\pm$0,5 A) is activated at t_1. (b) Control structure 1 [cf. Fig. 10(a)]. (c) Control structure 2 [cf. Fig. 10(b)]. A source of unbalance ($R \approx 1.0\ \Omega$) is added (d) in series to L_1^+ and (e) in series to L_1^-, and balancing control 2 (hysteresis value $\pm$0,5 A) is activated at t_1. (f) Detailed time behavior of the current in inductor L_1^- at an interval boundary B and corresponding switching signals $s_{i,1}$. Current scales: (a)–(e) 2 A/div; and (f) 1 A/div. Voltage scale: (f) 5 V/div. Time scales: (a)–(e) 5 ms/div; and (f) 100 μs/div.

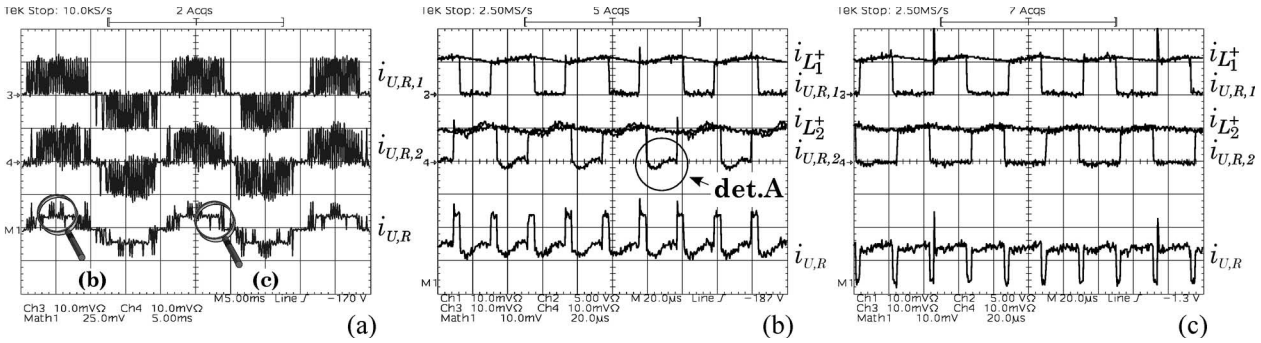

Fig. 12. Time behavior of the currents in inductors L_1^+, L_1^-, and L_2^+, time behavior of the discontinuous rectifier input currents of rectifier systems 1 and 2 in phase R, $i_{U,R,1}$, and $i_{U,R,2}$, and total rectifier input current $i_{U,R}$ (obtained by adding $i_{U,R,1}$ and $i_{U,R,2}$) within (a) one mains period and (b) and (c) detailed time behavior. The detail det. A shows the circulating differential current i_d during the free-wheeling state. Current scales: $i_{U,R,1}$, $i_{U,R,2}$, i_L: 5 A/div; $i_{U,R}$: (a) 12.5 A/div, and (b) and (c) 5 A/div. Time scales: (a) 5 ms/div, and (b) and (c) 20 μs/div.

hence, the additional free-wheeling state $j = (001)$ will have no influence on the rates of change of the currents in the dc-link inductors at $\varphi_U = 0$. The influence increases with increasing mains phase angle φ_U; therefore, the current $i_{L_2^-}$ is guided back to the reference value with increasing distance from the interval boundary. The switching signals $s_{i,1}$ show the occurrence of additional free-wheeling states.

D. Interleaved Operation Behavior

The advantage of an interleaved operation resulting in five levels of the total rectifier input current is clearly shown in Fig. 12 (cf. Fig. 2 and Section III). Rectifier systems 1 and 2 do show discontinuous rectifier input currents (cf. currents in phase R, $i_{U,R,1}$ and $i_{U,R,2}$). By phase shifting the switching signals of the parallel systems by half a pulse period, the discontinuous input currents are added in such a manner that the total rectifier input current does show five levels, cf. current $i_{U,R}$ in Fig. 12(a), i.e., a more continuous shape with reduced ripple amplitude as compared to a noninterleaved operation. There are sections where the discontinuous currents of the single rectifier systems do overlap in time [cf. Fig. 12(b)], the total rectifier input current therefore alternates between levels I and $2I$, where I is the average value of the dc-link currents. Where the corresponding mains phase current $i_{N,R} \approx i_{U,R,(1)}$ is passing through zero, the discontinuous rectifier input currents do not

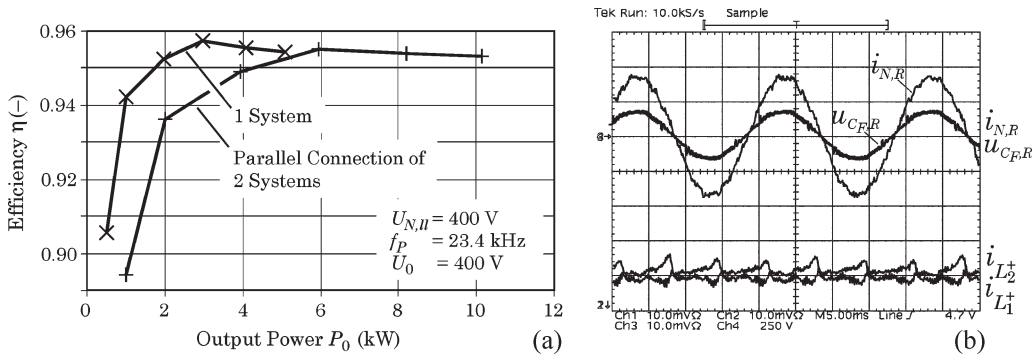

Fig. 13. Mains behavior of the parallel connection of two rectifier systems. (a) Comparison of the efficiency of a single rectifier system and the parallel connection of two rectifier systems. (b) Time behavior of mains phase current $i_{N,R}$, input filter capacitor voltage $u_{C_F,R}$ in phase R, and dc-link currents in the positive dc-link rails for a source of unbalance $R \approx 1.5\ \Omega$. Current scales: $i_{N,R}$, i_L: 5 A/div. Voltage scale: $u_{C_F,R}$: 250 V/div. Time scale: 5 ms/div.

overlap any more, which results in a total rectifier input current alternating between 0 and I [cf. Fig. 12(c)].

Furthermore, the circulating differential current i_d described in Section VI-A, which results from the difference in current ripple values in the positive and negative dc-link rails, is clearly shown in detail in Fig. 12(b) (det. A). In order to ensure a current path for this differential current, one *must not* switch all power transistors into the OFF-state during free wheeling, i.e., switching state $j = (000)$ must not be used.

E. Mains Behavior

In Fig. 13(a), the efficiency η of the parallel connection of two three-phase/switch buck-type PWM rectifier systems (considering losses of auxiliary power supply and DSP control board) is given for different output power values at 400-V mains line-to-line voltage and at rated output voltage. The comparison with measurement results of one rectifier system shows that the efficiency is noticeably increasing for a parallel connection.

Considering the total harmonic distortion of the mains phase currents for, e.g., 4-kW output power, one receives for a single rectifier system $\mathrm{THD}_{i_N} = 7.2\%$ and $\mathrm{THD}_{i_N} \approx 3.1\%$ for the parallel connection of two systems. The power factor $PF \approx 0.996$ is close to unity in the total output power range; however, a decrease for low output power can be noticed due to the higher percentage of the input filter capacitor current.

Furthermore, for a source of unbalance $R \approx 1.5\ \Omega$ added in series to L_1^+ and a hysteresis of ± 1.5 A for $U_{N,ll} = 210$ V, $P_0 = 2.2$ kW, and $I_0 = 10$ A, the total harmonic distortion was measured, $\mathrm{THD}_{i_N} = 3.12\%$, i.e., the active dc-link current-balancing control does not affect the mains current quality [cf. Fig. 13(b)].

VII. Conclusion

In this paper, three different control strategies for active dc-link current balancing for two parallel-connected three-phase/switch buck-type PWM rectifier systems have been presented based on a space vector modulation scheme that provides all the advantages of an interleaved operation and minimum ripple of the dc-link inductor currents and of the ac side filter capacitor voltages.

In addition to controlling the buck stage output voltages, the control schemes use an additional free-wheeling state for current balancing whereby the rate of change of the dc-link currents is influenced. In the basic control scheme, the duration of the additional free-wheeling state is calculated in dependency on the difference of the dc-link currents, and additional free-wheeling states do occur in each pulse period and in both rectifier systems. This control method was improved in order to minimize the additional switching losses that are present in a practical system at the transition between two free-wheeling states. There, a hysteresis controller was added whereby control action only takes place when the average values of the dc-link currents do differ by a given value, and inserting additional free-wheeling states is furthermore limited to one rectifier system. The following two possibilities for adding the additional free-wheeling state are proposed:

1) Control method 1: The total default free-wheeling state is replaced by the additional free-wheeling state whereby the additional switching losses are minimized and/or set to zero.
2) Control method 2: The duration of the additional free-wheeling state is calculated in dependency on the dc-link current unbalance, whereby the control action varies (which results in increasing additional switching losses as compared to 1).

As the experimental investigation shows, large dc-link currents spikes are resulting for control method 1 at low modulation indices due to the relatively long duration of the free-wheeling state. Therefore, it is advisable to implement control method 2, and by choosing an appropriate value of the hysteresis (e.g., 1 A), the increase in switching loss in comparison with control method 1 can be limited.

Basically, the dc-link inductor currents show a very good self-balancing. If a heavy unbalance is added in the experimental setup in series to one dc-link inductor, a current unbalance does occur, which depends on the size and position (positive or negative dc-link rail) of the source of unbalance. The current unbalance is controlled within the given hysteresis band; however, there is limited controllability at the boundaries of the mains phase intervals.

The analysis of the mains behavior shows that the values of power factor, total harmonic distortion of the mains phase

currents, and efficiency are improved as compared to a single rectifier system operation.

Furthermore, the proposed control structure can be easily extended to n parallel-connected rectifier systems, where a control action for dc-link current balancing has to take place in $n-1$ systems.

REFERENCES

[1] K. Xing, F. C. Lee, D. Borojevich, Z. Ye, and S. Mazumder, "Interleaved PWM with discontinuous space-vector modulation," *IEEE Trans. Power Electron.*, vol. 14, no. 5, pp. 906–917, Sep. 1999.

[2] T. Kawabata and S. Higashino, "Parallel operation of voltage source inverters," *IEEE Trans. Ind. Appl.*, vol. 24, no. 2, pp. 281–287, Mar./Apr. 1988.

[3] C. Rech and J. R. Pinheiro, "Line current harmonics reduction in multipulse connection of asymmetrically loaded rectifiers," *IEEE Trans. Ind. Electron.*, vol. 52, no. 3, pp. 640–652, Jun. 2005.

[4] Z. Ye, D. Boroyevich, J. Y. Choi, and F. C. Lee, "Control of circulating current in parallel three-phase boost rectifiers," in *Proc. IEEE APEC*, New Orleans, LA, Feb. 6–10, 2000, vol. 1, pp. 506–512.

[5] Y. Chen and K. Smedley, "Parallel operation of one-cycle controlled three-phase PFC rectifiers," in *Proc. IEEE APEC*, Austin, TX, Mar. 6–10, 2005, vol. 3, pp. 1689–1695.

[6] S. K. Mazumder, "Continuous and discrete variable-structure controls for parallel three-phase boost rectifier," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 340–354, Apr. 2005.

[7] C. T. Pan and Y. H. Liao, "Modeling and coordinate control of circulating currents in parallel three-phase boost rectifiers," *IEEE Trans. Ind. Electron.*, vol. 54, no. 2, pp. 825–838, Apr. 2007.

[8] J. W. Kolar, "Netzrückwirkungsarmes Dreiphasen-Stromzwischenkreis-Pulsgleichrichtersystem mit weitem Stellbereich der Ausgangsspannung," Austrian Patent Application A9/2000, Jan. 5, 2000. (in German).

[9] M. Baumann, U. Drofenik, and J. W. Kolar, "New wide input voltage range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a DC/DC boost converter output stage," in *Proc. 22nd IEEE Int. Telecommun. Energy Conf.*, Phoenix, AZ, Sep. 14–18, 2000, pp. 461–470.

[10] M. Baumann and J. W. Kolar, "Experimental analysis of a 5 kW wide input voltage range three-phase buck+boost power factor corrector," in *Proc. 23rd IEEE Int. Telecommun. Energy Conf.*, Edinburgh, U.K., Oct. 14–18, 2001, pp. 146–153.

[11] D. J. Tooth, S. J. Finney, J. N. McNeill, and B. W. Williams, "Soft switching and interleaving for sinusoidal input current AC to DC step down converters," in *Proc. IEEE PESC*, Baveno, Italy, Jun. 23–27, 1996, vol. 1, pp. 183–187.

[12] S. Kelkar and C. P. Henze, "A high performance three-phase unity power factor rectifier using interleaved buck derived topology for high power battery charging applications," in *Proc. IEEE PESC*, Vancouver, BC, Canada, Jun. 17–21, 2001, vol. 2, pp. 1013–1018.

[13] J. Rabkowski, M. Nowak, J. Matulka, and R. Barlik, "Output currents equalization for parallel connected three-phase PWM buck rectifiers," in *Proc. IEEE PESC*, Aachen, Germany, Jun. 20–25, 2004, vol. 4, pp. 2810–2816.

[14] Z. Ye and D. Boroyevich, "A novel modeling and control approach for parallel three-phase buck-rectifiers," in *Conf. Rec. IEEE IAS Annu. Meeting*, Chicago, IL, Sep. 30–Oct. 4, 2001, vol. 1, pp. 350–365.

[15] Z. Ye and D. Boroyevich, "Transformerless parallel three-phase PWM buck rectifiers," in *Proc. Conf. Rec. 9th Eur. Conf. Power Electron. Appl.*, Graz, Austria, Aug. 27–29, 2001, pp. P.1–P.9.

[16] J. W. Kolar and M. Baumann, "Verfahren zur Unterdrückung von Kreisströmen zwischen parallel geschalteten Dreiphasen-Pulsgleichrichtersystem mit eingeprägtem Ausgangsstrom," Austrian Patent Application A730/2002, May 13, 2002. (in German).

[17] M. C. Chandorkar, D. M. Divan, and R. H. Lasseter, "Control techniques for multiple current source GTO converters," *IEEE Trans. Ind. Appl.*, vol. 31, no. 1, pp. 134–140, Jan./Feb. 1995.

[18] M. Baumann and J. W. Kolar, "Minimization of the DC current ripple of a three-phase buck+boost PWM unity power factor rectifier," in *Proc. 2nd IEEE Power Convers. Conf.*, Osaka, Japan, Apr. 2–5, 2002, pp. 472–477.

[19] M. Baumann and J. W. Kolar, "Comparative evaluation of modulation methods for a three-phase/switch buck power factor corrector concerning the input capacitor voltage ripple," in *Proc. IEEE PESC*, Vancouver, BC, Canada, Jun. 17–21, 2001, pp. 1327–1332.

[20] T. Nussbaumer and J. W. Kolar, "Advanced modulation scheme for three-phase three-switch buck-type PWM rectifier preventing mains current distortion originating from sliding input filter capacitor voltage intersections," in *Proc. IEEE PESC*, Acapulco, Mexico, Jun. 15–19, 2003, vol. 3, pp. 1086–1091.

[21] Z. Ye, "Modeling and control of parallel three-phase PWM converters," Ph.D. dissertation, Virginia Polytech. Inst. and State Univ., Blacksburg, VA, 2000.

[22] *CASPOC—Power Electronics and Electrical Drives Modeling and Simulation*. [Online]. Available: www.caspoc.com

Martina Baumann was born in Vienna, Austria, in 1974. She received the Diploma and Ph.D. degrees from Vienna University of Technology, Vienna, in 1999 and 2005, respectively, both in electrical engineering.

She is currently a Research Assistant with the Institute of Electrical Drives and Machines, Vienna University of Technology. Her main fields of interest are three-phase PWM rectifier systems with low effects on the mains and matrix converters.

Dr. Baumann received the Best Paper Award from the IEEE Industrial Electronics Society in 2005.

Johann W. Kolar (S'89–M'91–SM'04) received the Ph.D. degree (*summa cum laude*) from the University of Technology Vienna, Vienna, Austria.

Since 1984, he has been teaching and working in research, in close collaboration with the international industry, in the fields of high-performance drives, process technology and uninterruptible power supplies. He has proposed numerous novel converter topologies, e.g., the VIENNA rectifier and the three-phase ac–ac sparse matrix converter concept. He was appointed Professor and Head of the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH), Zurich, Switzerland, on February 1, 2001. He has published over 250 scientific papers in international journals and conference proceedings. He is the holder of more than 50 patents. The focus of his current research is on ac–ac and ac–dc converter topologies with low effects on the mains, e.g., for the power supply of telecommunication systems, more-electric-aircraft, and distributed power systems in connection with fuel cells. Further main areas are the realization of ultracompact intelligent converter modules employing the latest power semiconductor technology (SiC), novel concepts for cooling and EMI filtering, multidomain/multiscale modeling, and simulation, pulsed power, bearingless motors, and power MEMS.

Dr. Kolar is a member of the Institute of Electrical Engineers of Japan (IEEJ) and the technical program committees of numerous international conferences in the field (e.g., Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion). From 1997 to 2000, he was an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. Since 2001, he has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS. Since 2002, he has also been an Associate Editor of the *Journal of Power Electronics* of the Korean Institute of Power Electronics and a member of the Editorial Advisory Board of the IEEJ Transactions on Electrical and Electronic Engineering. He received an Erskine Fellowship from the University of Canterbury, Canterbury, New Zealand, in 2003 and the Best Transactions Paper Award from the IEEE Industrial Electronics Society in 2005. In 2006, the European Power Supplies Manufacturers Association awarded the Power Electronics Systems Laboratory of ETH Zurich as the leading academic research institution in Europe.