Towards Virtual Prototyping and Comprehensive Multi-Objective Optimisation in Power Electronics

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***Abstract*—The constant demand for higher efficiency and power density and lower costs of power electronics systems could be met by application of new topologies and/or modulation schemes and future wide-band gap semiconductor technology. However, the performance of state-of-the-art systems also could be improved significantly by multi-domain/objective optimisation, i.e. by assigning overall optimal values to the design variables in the course of the design process.**

In order to perform such an optimisation first a comprehensive mathematical model of the main converter circuit has to be established, including thermal component models and the measures for DM and CM EMI filtering. Based on this model, an optimisation for multiple objectives, as e.g. efficiency and power density, can be performed. The optimisation makes best use of all degrees of freedom of a design and also allows to determine the sensitivity of the system performance on base technologies like Figures of Merit of the power semiconductors or properties of the magnetic core materials. Furthermore, different topologies can be easily compared and inherent performance limits can be identified.

In the paper, analytical approaches for designing the main functional elements of a power electronics converter are described and arranged to a linear design process in a first step. Moreover, the linking of the component models, i.e. of the electric, magnetic, thermal and thermo-mechanic design domains and an overall optimisation of the respective design variables based on the linked models is discussed. Finally, the coupling of the different domains and for example the utilisation of electrical equivalent circuits for implementing these couplings are investigated.

I. Introduction

The future development of power electronics is driven by requirements for higher efficiency and power density besides the continuous demand for cost reduction (Fig. 1). In mobile applications, e.g. for aircraft also the weight is an important design criteria. Additionally, the system reliability plays an important role, especially for applications where a very long life time (e.g. converter systems in future Smart Grids) or very harsh environmental conditions (e.g. hybrid or electric cars) or both (e.g. traction) have to be met.

These demands can be met by using or developing new topologies, modulation schemes and/or new semiconductor technologies as e.g. wide-band gap semiconductors (SiC or GaN) (cf. Fig. 2a). The new concepts and components represent a Disruptive Technology which enables a significant improvement over the state-of–the art shortly after its introduction (Fig. 2b) [1].

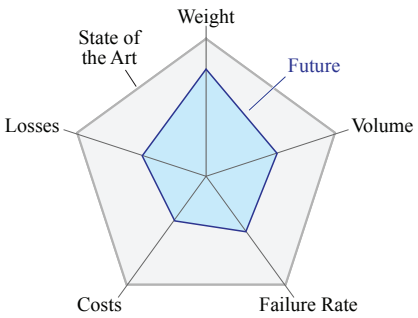

Fig. 1. Important performance indexes of power electronics systems and improvements required for future designs.

After a new concept/technology has established, the gain in performance improvement reduces over time. As the basic concept is given, a significant gain in performance can only be achieved by assigning optimal values to the design variables in the course of the design process, i.e. by comprehensive multi-objective optimisation as has been shown e.g. in [2], [3] for telecom power supplies (Fig. 2a). Moreover, by identifying the sensitivity of the system level performance on component parameters, the development of components could be adjusted for maximal impact on the system level.

In order to perform an optimisation, first a comprehensive mathematical model, i.e. a Virtual Prototype (VP), of the main converter circuit has to be established, which has to include thermal models and the measures for DM and CM EMI filtering. This model could be based on analytical equations, on numerical simulations or on a combination of both. The analytical models allow a fast calculation but are more complicated/time consuming to develop and could not be easily adapted to new topologies or modulation schemes. On the other hand, simulations are quite flexible but could require substantial computational effort.

With the VP the behaviour of the converter system could be predicted. This would include in the ideal case all component temperatures, the EMI behaviour and also reliability and would enable a significant reduction of development time and costs, as a simulation can be performed faster than the realisation of a hardware system. Furthermore, design deficiencies could be identified in a relatively early design stage and overload or overvoltage

situations could be easily evaluated without risking a destruction of the prototype.

In addition, the VP allows to observe internal signals, which could not be measured directly on ultra-compact future hardware systems. Also the manufacturing of highly integrated designs often requires expensive tools and setups, what demands a reduction of the number of different prototypes in order to limit costs.

Moreover, a VP provides the basis to study the influence of a parameter variation on the system behaviour, what finally could be used to meet multiple objectives, e.g. to maximise the efficiency in combination with the power density. An optimisation makes best use of all degrees of freedom of a design. It also allows to study the sensitivity of the system performance on base technologies like Figures of Merit of the power semiconductors or the properties of magnetic core materials. Furthermore, different converter concepts can be easily compared [4] and inherent performance limits identified [5]. Also the influence of different mission profiles on the component temperatures and the mechanical stresses could be evaluated without complicated test setups in applications such as traction, hybrid or electric vehicles or more electric aircraft.

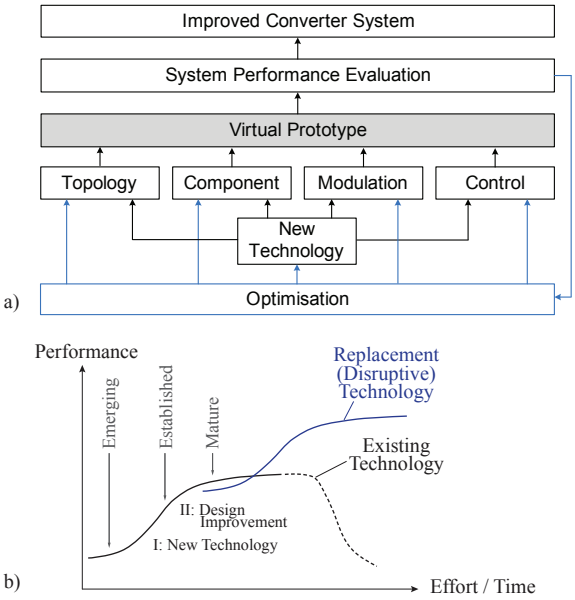

Fig. 2. a) Enabling factors for an improved converter performance. A typical technology cycle as shown in b) starts with a new technology, e.g. Super-Junction MOSFETs, which directly could result in a performance improvement. Also, a new technology might allow to use different topology/modulation concepts with higher performance, e.g. ZVS at higher voltages. The new technology develops over time, so that improved components based on the new technology evolve. In addition to the direct impact of the technology on the system performance, also the parameters and the topology/modulation can be optimised for a desired design criteria as e.g. power density or efficiency. By a sensitivity analysis furthermore the parameters of the improved components could be adjusted such, that a maximal impact on the system performance is achieved. b) New technologies and concepts could enable a significant increase in performance after emerging and being applied in products. Thereafter, significant performance improvements can only be achieved by improving the designs or by performing optimisations in order to determine the best set of parameters for a given requirement. Finally, a performance saturation occurs and new technologies are required to obtain large performance improvements.

The models for the VP must be valid and accurate over a wide range of operating conditions, e.g. in a wide temperature and load range. There, it is very important that the model output quantities can be calculated fast enough, in order to perform different design studies in a reasonable time or to optimise a design parameter, what requires multiple evaluations of the VP.

As the expertise of design engineers typically will not cover all design domains (thermal, magnetic, EMI, etc.), it is important that the models can be set up and/or parameterised easily. In best case the process of establishing the model is supported by a tool or a simplified model is generated automatically based on geometrical and material information by a tool. Such process is e.g. described in [6] for deriving the thermal equivalent circuit of high power semiconductor modules or for several power semiconductors mounted on the same heat sink.

In the following, before discussing the details of the models for the different design domains, in **section II** an overview of the linear design process, which is widely applied for power electronic systems, is presented. Thereafter, design tools for the electric, magnetic, thermal and EMI domain, which in combination could serve as basis for realising the VP, are investigated in **section III**. In addition an analytical approach for covering the various design domains is discussed which results in a significantly lower computational effort than models based on numerical simulation. This concept has been proven successfully by the design and practical implementation of converter systems of exceptional performance like ultra-compact and ultra-efficient single-phase PFC rectifier systems and DC-DC converters for telecom applications.

In **section IV** linking the tools of the different domains, which significantly simplifies the design process, is discussed. There, also the optimisation of the design variables of single components, subsystems or of the whole system is described. Finally, the cross-linking/coupling of different domains is investigated in **section V** and approaches and tools for automatically generating electrical equivalent circuits for the different domains are considered.

II. Linear Design Flow

The typical design process of power electronic converters is reviewed in the following for an AC/DC converter system. Subsequently, tools and analytical approaches for modelling the different domains of the VP will be described in Section III.

One of the first design steps is the selection of the converter topology and the modulation scheme based on the specifications and the considered application area (Fig. 3). There, different topologies as well as modulation schemes are evaluated based on published data, experience and/or calculations/simulations.

In case a *Topology Performance Map* for the considered topologies and application area, is available, the

topology selection process directly can be based on system level performance indices and could be performed very quickly. Such performance map results from multi-objective optimisations as e.g. shown in [4] for single-phase PFC rectifiers.

Next, for determining the voltage and current stresses of all components, an electric model of the selected topology and modulation is implemented in a simulation tool as for example PSPICE, SIMPLORER^{TM} or GeckoCIRCUITS^{TM}. Alternatively, an analytic model of the chosen topology could be used. Such an analytic model often allows a much faster calculation of the required quantities than a numerical simulation. However, the analytic model is only valid for a specific topology. Accordingly, changes of the topology and/or modulation often require a major modification of the model. Consequently, e.g. the comparison of different modulation concepts based on analytic models could result in a high modelling effort.

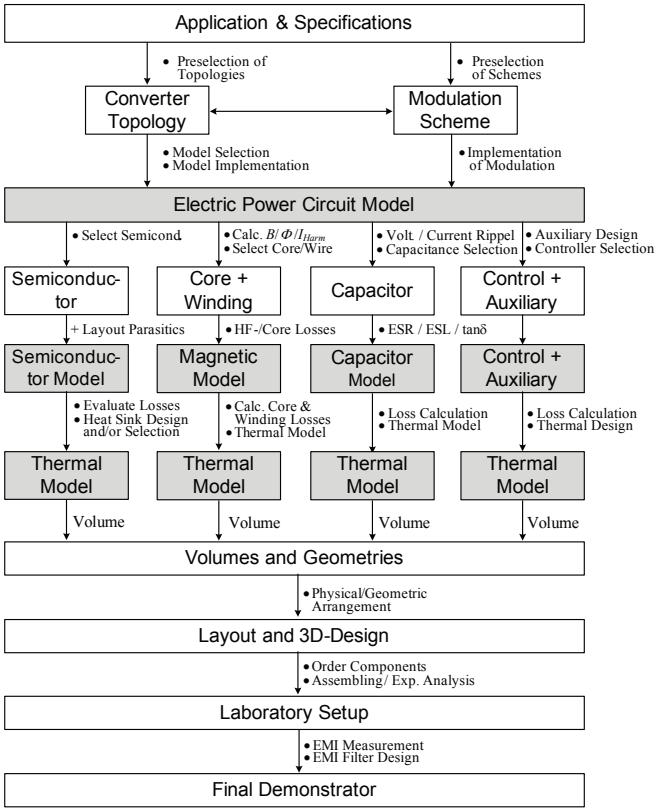

Fig. 3. Linear design flow starting with the selection of the converter topology and modulation scheme based on the specifications and the application. With the topology/modulation an electric circuit model is implemented and the currents/voltages in the system are determined. Based on these values the appropriate semiconductors are selected and the switching/conduction losses are calculated. There, the layout parasitics must be considered. In parallel the magnetic components are designed and the winding/core losses are determined. Also the DC link and/or input/output capacitors are selected with the current/voltage ripples and the auxiliary supply as well as the control is selected and designed. All the losses are fed into the thermal model to determine the temperatures of the different components. There, the different thermal models are usually not coupled. With the components and the volumes of the cooling systems, a system layout and a 3D construction is determined. After building a prototype system, EMI measurements are performed and the EMI filter is designed, what results in the final demonstrator system.

Based on the voltage and current stress of the semiconductors, the design engineer selects appropriate components and calculates the conduction and switching losses of the devices. Calculating the switching losses requires either data sheet values or measured switching losses, in case a higher accuracy is required. In the measurement of the switching losses, besides the junction temperature also the layout and packaging parasitics should be considered. There, the difficulty is, that the mechanical converter design and therewith the layout parasitics are not known at this design stage and a preliminary layout must be assumed.

With the losses in the semiconductors and the ambient and junction temperatures, an appropriate heat sink could be either selected from a heat sink manufacturer data sheet or designed based on analytic models [7] or numerical CFD simulations. There, a fixed junction temperature, which is reached at the considered operating point, has to be assumed. This removes the coupling between the heat sink/thermal design and the loss calculation given due to temperature dependent device parameters as for example the on-resistance of a power MOSFET. In case the junction temperature is also a free design parameter, a coupling between the thermal design and the loss calculation or an iterative design process is required as will be shown later. Finally, the volume and the geometry of the heat sink are given and are later used to determine the mechanical design of the converter system.

Independent of the thermal design of the heat sink, the magnetic components are designed. Based on application notes from manufacturers as e.g. EPCOS [8] or on approximative characteristic values like the area product [9], [10] a core and an appropriate core material could be selected. With the saturation flux density a first approximation of the turns number is determined and the winding and core losses can be estimated with analytical approaches or numerical simulations as shown later. The winding and core losses are fed into a thermal model for calculating the winding and core temperatures.

In case the loss density is too high/low, a different core geometry/size could be selected and the calculations repeated until a suitable design is determined. The value for the admissible loss density is defined either based on experience or must be evaluated with a thermal model (as shown later), since the maximum winding and/or core temperature is the actual design criteria. The resulting volume of the magnetic component including the cooling is then used later for the mechanical design of the converter system.

The selection of the DC capacitor is usually based on the current and the voltage ripple and – for example in telecom applications – also on the stored energy for realising e.g. a required hold up time. The losses in the capacitor can be calculated with the equivalent series resistance ESR and/or the loss factor. With the losses and

an thermal equivalent circuit of the capacitor and/or CFD simulations the temperature distribution of the capacitors and the cooling requirements of the capacitors can be calculated. These cooling requirements and the capacitor type finally determine the volume of the DC link capacitor required for the mechanical design.

In addition to the main components of the power circuit, also the losses and the volume of the control circuit and the auxiliary supply have to determined by the design engineer. There, first a design/topology for the auxiliary supply and a controller type has to be selected and then the losses have to be calculated. Finally, the cooling for the auxiliary supply must be designed and the total volume/dimensions again are required for the mechanical design.

With the volumes and geometries of all components the design engineer determines the PCB layout of the power and control circuit as well as the geometric arrangement of the components. There, the parasitic capacitances of the interconnecting traces with switched voltages and/or the parasitic inductances of circuit loops with fast varying currents must be kept as small as possible in order to reduce transient overvoltages and charging currents of parasitic capacitances. This minimises the voltage stress on the power semiconductors and improves the EMI behaviour of the circuit. Moreover, the electromagnetic coupling between different components, which could severely deteriorate the EMI performance [11], must be considered while arranging all the components. This is especially true for the EMI filter stages, where sections of the EMI filter could be shortened by parasitic couplings, what could significantly reduce the filter attenuation. Besides the electromagnetic coupling also the thermal coupling between the heat sink and other components with high temperatures to components which are temperature sensitive as e.g. electrolytic capacitors or control ICs must be considered.

Based on the selected components and the determined PCB layout, the prototype could be built and tested for compliance to safety and EMI regulations. In a first step, EMI measurements must be performed and the CM and DM EMI-filter designed and adapted until the requirements are met. There, several iterations could be necessary and even a redesign of the whole power circuit could be necessary in order to reduce parasitics and/or the filtering effort.

In the shown linear design flow, no iterations of the design process are included. However, such loops would e.g. be necessary if a desired inductance value could not be realised within the specified volume at the given inductor operating current and frequency. Another example are the semiconductors where it could be necessary to select different components in order to limit the losses and/or meet a desired efficiency target.

Design loops/iterations could be avoided by applying linked/coupled models, where e.g. the behaviour of the magnetic component is included in the electric circuit model and constraints for the volume or losses of the magnetic component are already considered during the selection of the circuit parameters. Such models are discussed below. But before software tools and analytical approaches are discussed, which can be used during the design process of the different components and the system.

III. Manual Virtual Prototyping

In the linear design process, the design engineer has to calculate the behaviour of all components, and to perform all design decisions. These can be supported either by software tools, i.e. numeric approaches, or by analytic models, which both can be used to perform iterative optimisations of the components, e.g. an optimisation of the dimensions of a transformer for minimal volume. The optimisation of single components or groups of components will be discussed in section IV.

For most simulation tools only a single domain (e.g. electric or thermal) can be modelled and the linking of different tools is not well supported, so that the user has to transfer the simulation results achieved in one domain to the software tool of another domain manually or by problem specific scripts. Therefore, a direct linking of the tools would substantially simplify the design process as will be shown in section IV.

In the following software tools and analytic approaches for the different domains are generally discussed and limitations are shown. For each domain the key design parameters are listed and the design of a single-phase bridgeless PFC rectifier (Fig. 4) is used as an example.

A. Circuit Simulation

The most flexible means to calculate the currents and the voltages in the system are numeric circuit simulators as PSPICE or GeckoCIRCUITS^{TM} (Fig. 5). Basically, these simulators could be divided into programmes with an adjustable time step, where e.g. the length of the time step is reduced around switching actions and increased when no fast transients occur, and programmes with a fixed time step. The latter are simpler, faster and often have less convergence problems, but usually are not able to practically apply full physical models of the semiconductor devices, so that it is difficult to exactly simulate switching transients.

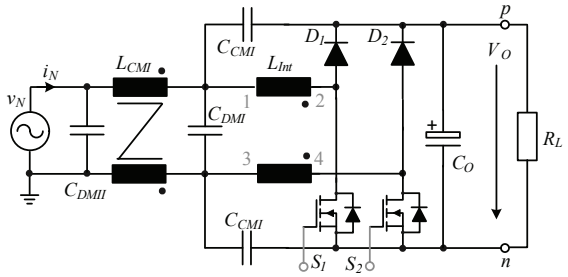

Fig. 4. Circuit schematic of the bridgeless single-phase PFC rectifier with integrated magnetics and common mode EMI filter.

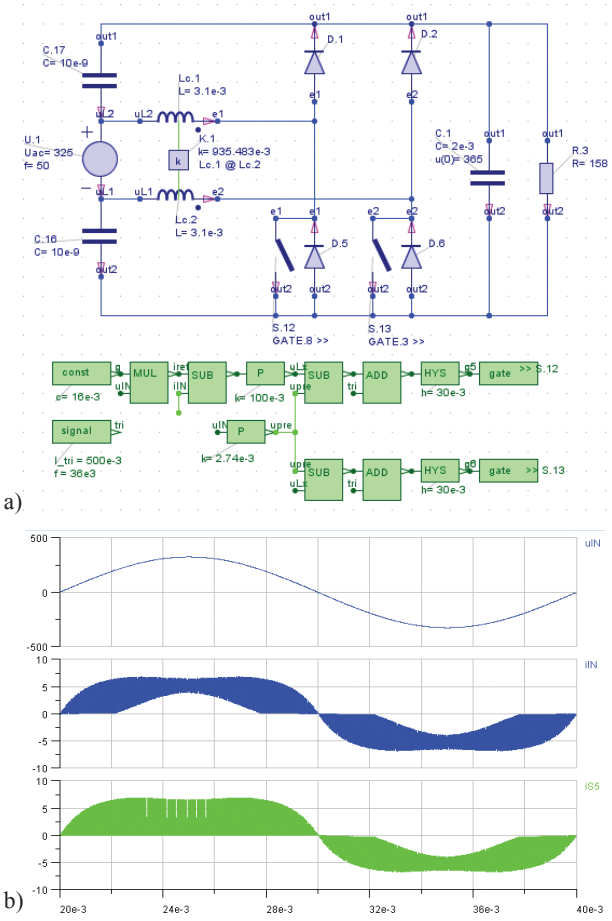

Fig. 5. a) Electrical simulation of the single-phase PFC rectifier given in Fig. 4 without EMI filter implemented in GeckoCIRCUITS^{TM} [12]. b) Simulated mains voltage, mains current, and transistor current.

In the simulator each component of the power circuit is described by an equation. Linearising the equations within one time step of the circuit simulation, results in a system of linear equations that can be solved in matrix form as given by (1)

$$\left(\varphi_1 \varphi_1 \ldots \varphi_\nu\right)^T \underline{A} = \underline{b}. \tag{1}$$

During the simulation, the time proceeds in small steps Δt from t_{START} to t_{END}, and (1) is repeatedly solved for each time step. The order n_{NC} of matrix $\underline{A}$ is directly proportional to the number of nodes in the electric circuit. As long as the order is comparably small ($n_{NC} < 10^3$), so-called direct matrix solvers can be used. By employing direct solver algorithms like LU Decomposition [13], the computational effort CE, characterised by the numbers of executions needed to solve the matrix equation, rises with the third power of n_{NC}

$$CE \sim n_{NC}^3, \tag{2}$$

so that the computation time is approximately proportional to the third power of the number of nodes in the power circuit. The required memory space is proportional to the second power of node number, i.e. n_{NC}^2 [6].

This scaling is especially important for the integration of equivalent circuits of other domains into the electric circuit simulation, as e.g. thermal networks as described in the next section [6]. In order not to run into excessive computation times a model order reduction of the equivalent circuit and/or a computationally efficient implementation of the multi-domain models is necessary as will be discussed later.

In Fig. 5 the implementation of the single-phase PFC rectifier depicted in Fig. 4 in GeckoCIRCUITS^{TM} and the simulated mains voltage/current as well as the simulated switch current are shown. For calculating a full mains cycle the simulation needs less than 10s with a simulation time step of 100ns. Based on the simulation all required component currents and voltages can be derived.

Alternatively, for the considered circuit also analytical expressions could be used to describe the dependency of the RMS currents, the voltages and also the switched currents on the circuit parameters. The resulting formulas allow a very fast calculation of the results, but the effort to consider a different modulation scheme or a topological modification of the circuit is large, since all expressions have to be adapted.

For the considered single-phase PFC rectifier, the input current for continuous conduction mode (CCM) could simply be calculated by

$$i_N(t) = i_{N(1)}(t) + i_{N,r}(t) \tag{3}$$

with the fundamental component of the input current

$$i_{N(1)} = \frac{P_N}{V_N}\sqrt{2}\sin(\omega_N t) \tag{4}$$

and the ripple current

$$i_{N,r} = \frac{1}{2}\frac{V_O T_P}{L_{DM}}\frac{1}{M}\sin(\omega_N t)\sin\left(d(t)\right) \tag{5}$$

as shown in [14]. There, V_N is the RMS value of the mains voltage, P_N the input power and M the modulation index defined by $M = V_O/\left(\sqrt{2}V_N\right)$. The local duty cycle is given by

$$d(t) = 1 - \frac{1}{M}\sin(\omega_N t). \tag{6}$$

With the input current, the time behaviour and the RMS/average values of the currents in the input inductor, the switches, the boost diodes and the output capacitor can be calculated. This allows to calculate the losses in all the devices and to determine also the conducted differential mode (DM) noise emissions for designing the EMI filter as will be shown later. In [2] equations for the single-phase PFC rectifier describing the discontinuous operation mode (DCM) are presented, so that pure DCM or CCM as well as mixed mode operation can be calculated.

Design parameters: Topology, modulation, component selection and values.

Couplings: Component values.

B. Cooling of Power Semiconductors

With the electric circuit model, the current and voltage stress on the semiconductor components is determined and an appropriate semiconductor device could be chosen bearing the switching frequency in mind.

The conduction losses of the semiconductors are usually calculated based on data sheet values or measured data for the on-resistance and/or forward voltage drop at the considered current level. There, the junction temperature plays an important role as the parameters are temperature dependent. Accordingly, the electric and the thermal domain are coupled in this case as will be discussed in section V. Since the losses and the design of the cooling system are not known yet, the junction temperature could not be calculated.

In order to perform the conduction and switching loss calculations two approaches could be used. Either a fixed junction temperature of e.g. 125°C is assumed for the considered operating point and the cooling system is designed in the next step such that this assumption is fulfilled. In this case no iteration is necessary. The volume of such a cooling system could be approximately calculated based on the $CSPI$ (Cooling System Performance Index), which is defined as

$$CSPI\left[\tfrac{W}{Kdm^3}\right] = \frac{G_{th,S-A}\left[\tfrac{W}{K}\right]}{Vol_{HS}\,[dm^3]} \tag{7}$$

and has been introduced in [7]. The required thermal conductance $G_{th,S-A}$ of the heat sink could be derived with the assumed junction temperature, the ambient temperature and the losses.

Alternatively, one starts with a guess of the junction temperature and/or thermal resistance and calculates the losses for the assumed temperature and designs the cooling system. In case the resulting junction temperature is not equal to the assumed value, iterations are required, in order to determine the final junction temperature and the final size of the cooling system. This iterations could be avoided by linking the electric and the thermal model as will be described below.

For calculating the switching losses, the layout of the power circuit and the gate drive circuit must be considered as these significantly influence the switching transients and the switching losses. Therefore, the loss data given in the data sheets is only of limited usability and measurements with a layout close to the final circuit layout have to be performed. There, again the problem arises that information, which is not available at this design stage, would be required for the calculations. Often with a test layout for measuring the switching transients lower switching losses than for the final layout could be achieved due to smaller parasitics, since for the final layout further design constraints have to be considered during the geometrical arrangement of the components and the routing of the electrical interconnections. Also the gate drive might have to be adapted to the layout parasitics in order to limit over-voltages and/or di/dt.

With the loss data given as function of junction temperature, operating voltage and switched current, the semiconductor losses can be determined. This is relatively simple for steady state operation of a DC-DC converter, where the modulation index is constant, i.e. the switched currents/voltages do not change over time. In case of PFC rectifiers or inverter systems with inherently time-varying modulation index, the switching losses have to be calculated for each switching interval within a mains cycle and then summed up to obtain the total switching losses. This could be simplified by a simulation tool which links the electric model and the thermal design of the semiconductors as will be shown in section IV.

Measuring the switching losses in dependency of the switched current/voltage, temperature, PCB layout and gate drive could be very time consuming and requires iterations in case the layout is changed significantly. Alternatively, the switching losses could also be estimated by simulations based on behavioural models of the switches, extracted layout parasitics and a gate drive model as shown in [15] for unipolar devices. In case of bipolar

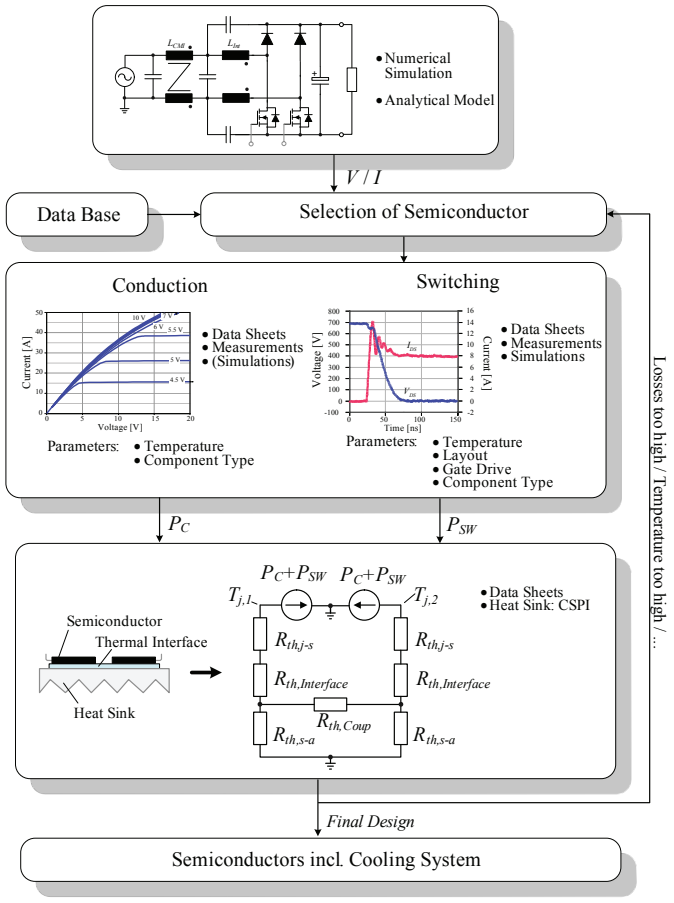

Fig. 6. Design flow for determining the required cooling of the semiconductors and the junction temperatures. Based on the currents/voltages in the devices, which are calculated with the circuit simulator, the conduction and switching losses are determined based on data sheet values or measurements. In some cases it is also possible to simulate the switching losses. The losses are the input of the thermal model, with which the temperatures could be calculated and an appropriate heat sink could be chosen.

devices this is significantly more difficult as the stored charge must be modelled, what requires a more detailed physical device model.

With the selected semiconductors and the selected heat sink, an electric equivalent circuit of the thermal system describing the heat transfer from the junction to the ambient could be set up. The values for the thermal resistances of the semiconductors and the heat sink could be found in data sheets. The thermal resistance between semiconductor case and heat sink could either also be taken from a data sheet (in case of solid interface materials [16]) or determined by measurements in case thermal grease or other interface materials are employed.

In the thermal equivalent circuit also the thermal coupling of different semiconductors mounted on the same heat sink could be included. There, the value of the coupling resistors could be determined by numerical heat conduction simulations, which could e.g. be performed with ICEPAK^{TM} [17] or with the thermal equivalent circuit extractor of GeckoHEAT^{TM} [12]. Furthermore, also thermal capacitances could be added, so that the transient junction temperature e.g. during overload conditions or varying loads could be determined [18]. Moreover, by calculating the time behaviour of the junction temperatures for a given load/mission profile, the life time and/or reliability of the power semiconductor packages in the considered application could be evaluated as shown e.g. in [19].

Design parameters: Heat sink geometry, gate drive, junction temperature.

Couplings: Junction temperature, layout.

C. Design of Magnetic Components

The design of magnetic components starts with the specification of either the inductance value and the time behaviour of the inductor current in case of an inductor or with the specification of the turns ratio, the winding voltage and the winding current in case of a transformer.

Subsequently, an appropriate magnetic core must be selected, what could be done with reference to the area product [10], which is e.g.

$$A_C A_W = \frac{L I_p I_{RMS}}{J_{RMS} k_W B_s} \tag{8}$$

for an inductor with the peak current I_p, the RMS current I_{RMS}, the desired current density J_{RMS}, the saturation flux density B_s and the window fill factor k_W. For the calculation of the area product a current density J_{RMS} is assumed to determine the size of the winding window A_W; the cross sectional area of the core A_C is determined with the maximum saturation flux density B_s and flux linkage $LI_p = \Psi$. There, the high frequency losses in the winding(s) and the core losses are neglected, i.e. no thermal limitations are considered. However, this allows to easily select a possible core. For this selected core, then the high frequency winding losses and the core losses can be determined as discussed in the following.

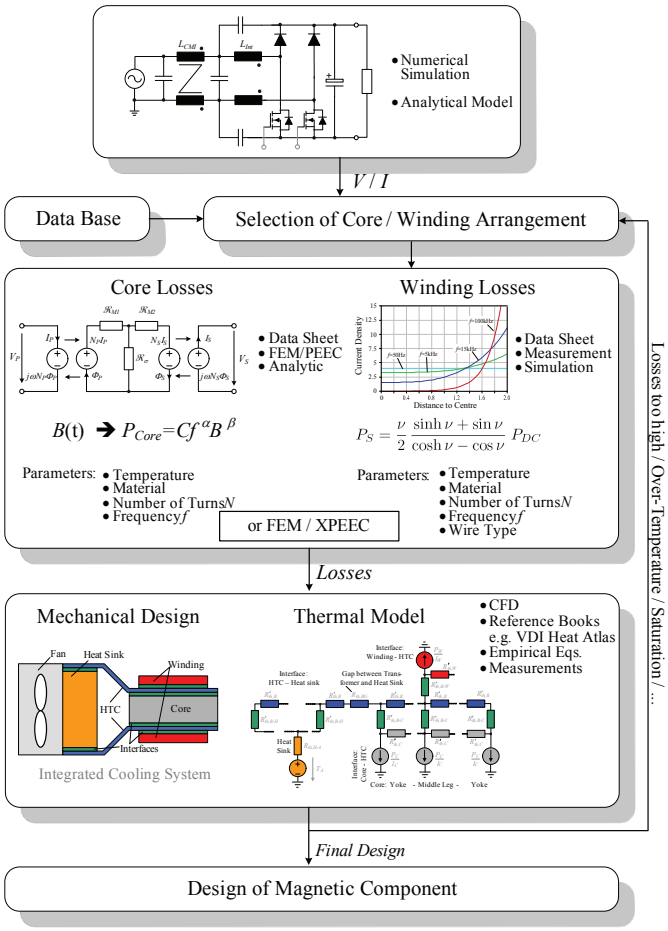

Fig. 7. Design of magnetic components applying currents and voltages determined with the electric model. With the voltages and currents the core losses and the winding losses are calculated either with analytical formulas or numerical simulations. The losses are fed into a thermal model or into a numerical simulation for determining the winding and the core temperature.

For calculating the core losses, the flux density in the different core sections must be known. These can e.g. be determined with 2D or 3D FEM simulations, which allow an accurate calculation of the flux distribution. The 2D simulations can be performed with comparably low computational effort, i.e. simulation times are typically in the range of a few seconds with modern computers.

With the FEM simulations the average amplitude of the flux density for the different core sections and the considered operating points is calculated. In the core material data sheets, the losses are usually specified for different frequencies of sinusoidally varying flux densities and a number of different flux amplitudes. Based on the Steinmetz equation [20], the loss data then can be inter- and extrapolated.

Since in power electronic systems the flux density typically is not varying sinusoidally over time, modifications of the original Steinmetz equation have been proposed, where the rate of change of the flux density dB/dt is the basis for the loss calculation [21], [22].

For the approach presented in [21], a piecewise linear

description $V_{L,j}$ and t_j ($j = 1 \dots \nu$) of the voltage across the inductor winding is required for calculating the losses with

$$P_{Core} = \frac{k_i (\Delta B)^{\beta-\alpha}}{T} \sum_j \left(\frac{V_{L,j}}{N_L \, A_C} \right)^{\alpha} (t_j - t_{j-1}) Vol_C \quad (9)$$

with

$$k_i = \frac{k}{2^{\beta+1} \pi^{\alpha-1} \left(0.2761 + \frac{1.7061}{\alpha+1.354} \right)}.$$

The coefficients α and β are material parameters, which could be derived from data sheet values, N_L is the number of turns and Vol_C is the core volume. In case of the considered single-phase PFC rectifier, $V_{L,i}$ is equal to the mains voltage v_N when the switch is turned on and equal to $V_o - v_N$ when the diode is conducting. The flux swing ΔB describing the major flux loop is the difference of the minimal and maximal flux density occurring in a mains cycle.

Instead of performing FEM simulations for determining the flux density, it is often sufficiently accurate to calculated the flux density distribution by reluctance models as shown in Fig. 8, where a reluctance model of the integrated magnetics for the single-phase PFC rectifier boost inductor is depicted. Each core section, for which a constant flux is assumed, as well as the air gaps are described by magnetic resistances and the winding is modelled as controlled voltage source with the magnetomotive force (MMF) $N \cdot I$ as voltage value. The coupling to the electric circuit is performed by controlled voltage sources (left and right in Fig. 8) with the amplitude proportional to the derivative of the flux as electric model of the winding. For calculating the magnetic resistance of the air gaps for example Schwarz-Christoffel Transformations as described in [23] or approximations could be used.

The reluctance model is based on Ohm's law for magnetic circuits which is the magnetic analogue to the Ohm's law for electric circuits, $R \cdot I = V$, i.e. the flux corresponds to the current and the MMF to the voltage. With this equation Kirchhoff's voltage law (KVL) and Kirchhoff's current law (KCL) can be applied to the magnetic circuit based on the assumptions discussed e.g. in [24]

$$\begin{aligned} &\text{KVL:} \quad N \cdot I = \phi \cdot (\Re_1 + \Re_2 + \dots + \Re_n) \\ &\qquad \text{(for a given path)} \\ &\text{KCL:} \quad \phi_1 + \phi_2 + \dots + \phi_n = 0 \\ &\qquad \text{(for a given node).} \end{aligned} \quad (10)$$

The winding losses can be determined either with numerical FEM simulations or with analytic formulas. For the analytic approach, determining the H-field distribution in the winding window around the conductors is one of the most challenging tasks. In many applications 1) a simplified 1D H-field distribution [25] (Fig. 9) is assumed and 2) the influence of the current distribution in the conductors on the magnetic field distribution is neglected. This allows a sufficiently accurate approximation of the winding losses.

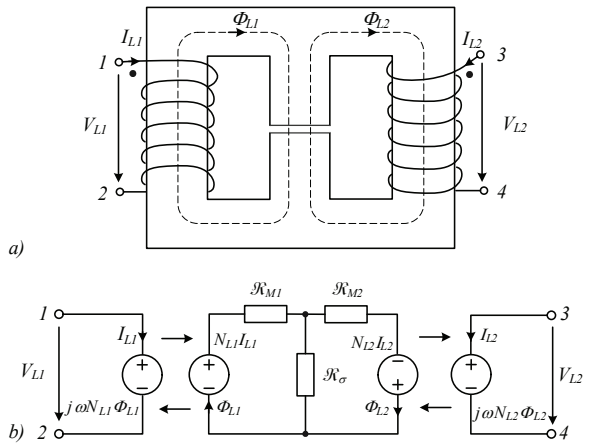

Fig. 8. Reluctance model of the integrated boost inductor of the single-phase PFC rectifier depicted in Fig. 4.

In the 1D H-field approximation, the magnetic field shows only a z-component, i.e. it is parallel to the foil windings shown in Fig. 9. Round wires can also be approximately transformed into foil windings as shown in Fig. 9b). There, the conductivity of the wires is modified by a so called porosity factor so that the DC resistance remains unchanged. This is not based on physics but results in relatively good approximations in case the round wires are densely packed [26]. Alternatively, the losses in the round wires can directly be calculated as described in [27].

Under these assumptions, the losses e.g. in a foil winding can be calculated with

$$P_S = \sum_i \frac{l_W}{2\sigma dh} \hat{I}^2_{L(i)} \frac{\nu_i}{2} \frac{\sinh \nu_i + \sin \nu_i}{\cosh \nu_i - \cos \nu_i} \quad (11)$$

$$P_P = \sum_i \sum_m \frac{d l_W \nu_i}{\sigma h} \frac{\sinh \nu_i - \sin \nu_i}{\cosh \nu_i + \cos \nu_i} \hat{H}^2_{S(i)m} \quad (12)$$

where the magnetic field is expressed by

$$\hat{H}_{S(i)m} = \frac{2m-1}{2} \frac{\hat{I}_{L(i)}}{d}$$

for the integrated inductor of the single-phase PFC rectifier. Since the losses generated by the different harmonics of the inductor current simply can be added as explained in [27], first the harmonics of the boost inductor current are calculated with Fourier analysis. There, the time behaviour of the current is determined either numerically with a circuit simulator of with the analytic formulas presented above. Thereafter, the losses for each harmonic are calculated with (11) and (12) and finally added up. Further information on the winding loss calculation could e.g. be found in [28], [29]. Similar approaches also exist for litz wire.

Instead of calculating the field analytically based on rough approximations, the H-field also could be determined by 2D FEM simulations. The average of the resulting field across a considered round/litz wire could then

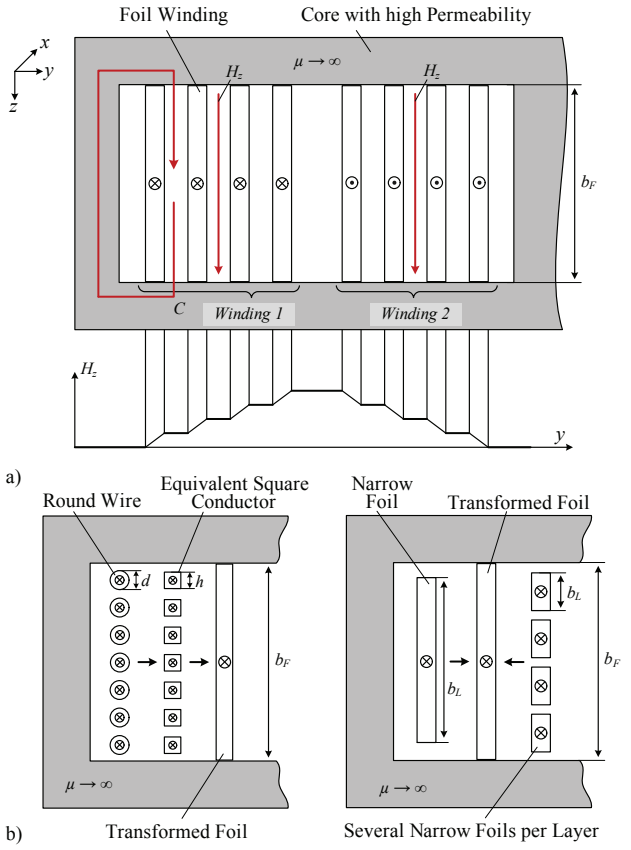

Fig. 9. a) Winding window of an E-core with two windings for a transformer. Below the E-core the distribution of the H-field is shown. b) Transformation of round wires (left) or narrow foils to an equivalent foil, which extends over the whole winding window.

be used in the analytic formulas for the proximity effect losses in solid or litz wire. This is especially important in case of gapped cores, where in vicinity of air gaps large fringing fluxes, i.e. strong H-fields, are present and the 1D assumptions for the H-field is violated.

With foil windings, the loss calculation in the vicinity of air gaps is more complicated, as there a current redistribution in the foils in 2 directions occurs, what also could result in an H-field distribution, which is significantly influenced by the redistributed current in the foils. In [30] a hybrid approach, combining analytical calculations with numerical simulations has been proposed for foil windings in order to address this issue. Purely analytical approaches are given in [31] and [32].

In order to account also for 3D effects occurring for example in E-cores the ”double 2D” method is proposed in [33], where the authors use two 2D simulations in two orthogonal planes. This method allows to avoid time consuming full 3D simulations and the results could be used either to improve the accuracy of the core loss or of the winding loss calculations. This approach is especially interesting for magnetic devices with gapped cores.

With the loss distribution, the temperatures in the winding and the core could be calculated based on a thermal model as shown in Fig. 10 for a magnetic devices

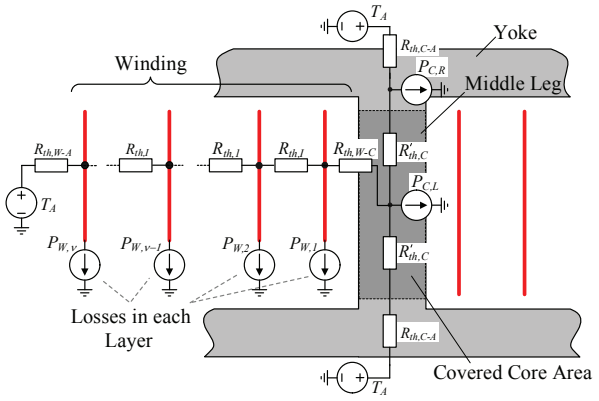

Fig. 10. Thermal model for a magnetic device with an E-core and foil windings. The insulation between the layers is represented by a thermal resistance and each turn generates its own losses. Also the core is split into different sections. There, especially the middle leg, around which the foil winding is wound, is important, since there also losses from the winding are transferred to the core.

with E-core and foil winding. There, each turn is modelled separately and the losses $P_{W,\nu}$ ($\nu = 1 \ldots N$) are fed into the thermal model at the location of the turn. Also the model for the core is separated into different sections with respective losses.

In the magnetic component, the heat transfer is mainly caused by thermal conduction and the main difficulty is to determine the thermal contact resistances between the different components of the magnetic device. With foil windings as considered in the example, the thermal resistance $R_{t,I}$ could be determined via the area and the thermal conductivity of the insulation. However, it is important to note that the mechanical force, with which the foil is wound on the bobbin/core, takes significant influence on the thermal resistance. In [34], [35] empirical equations for the thermal resistances are presented, which could be supplemented by own measurements and experiences.

The heat transfer from the surface to the ambient is often described by boundary conditions, i.e. heat transfer coefficients. These can either be determined with numerical simulations or similar approaches [36], [37] and included in the equivalent circuit as thermal resistors to ambient (e.g. $R_{th,C-A}$ and $R_{th,W-A}$ in Fig. 10). In order to improve the heat removal and/or to increase the admissible loss density, alternatively a direct cooling method as described in [38] could be employed. There, the heat is extracted by solid heat conduction paths (e.g. heat pipes) connected to a heat sink. In [38] also methods for deriving the thermal equivalent circuit of the direct cooling method are presented.

With the values of the resistances and the thermal equivalent circuit, the temperature distribution now could be relatively easy calculated in the circuit simulator.

Design parameters: Turn number, material, cooling, core geometry/size.

Couplings: Parasitics, thermal, geometry.

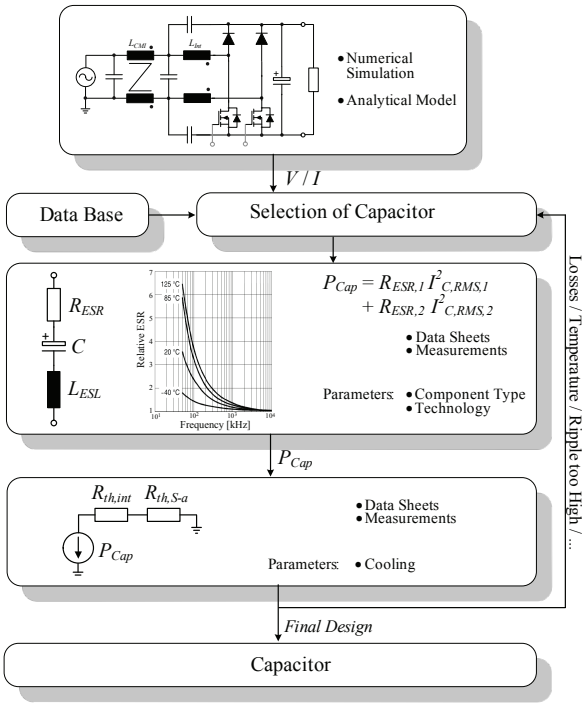

Fig. 11. Loss calculation in capacitors based on the currents/voltages resulting from the electrical model and the equivalent series resistance ESR given in the data sheet or determined by measurements. With the thermal model, which is often not given by the manufacturer, the temperature distribution within the capacitor is calculated.

D. DC Capacitor

For power electronic systems with DC input or output or a DC voltage link, the DC capacitor contributes significantly to the converter volume and hence influences the power density of the total system. For example, in [39] an ultra-compact active three-phase rectifier is presented, where the capacitors consume approximately 20%-30% of the system volume. The task of the DC capacitor is to absorb the HF switching currents, to balance temporary differences of input and output power (pulsation of input power with twice the mains frequency in case of a single-phase PFC rectifier) and to serve as an energy storage, e.g. for realising a hold-up time in telecom applications. Hence, the selection of the capacitor must consider its rated current as well as the required energy storage capacity.

Typically, the choice of capacitors is between electrolytic, foil and ceramic types, where electrolytic capacitors are characterised by a significantly higher stored energy per volume than foil capacitors, but show a limited life time especially for higher operating temperature. Foil capacitors and also ceramic capacitors allow high ripple currents and feature a long life time. Additionally, ceramic capacitors are available for a wide operating temperature range. However, with ceramic capacitors mechanical issues have to be considered carefully due to the brittleness of the material.

The losses of all capacitor types can simply be calculated using an equivalent series resistance ESR, which includes contact resistances, the resistance of the dielectric and also dielectric losses. The ESR is decreasing with frequency, accordingly the loss calculation is performed for two frequency ranges, i.e. split into two parts. The first part considers the losses and the ESR at low frequency, i.e. at twice the mains frequency for PFC rectifier systems. For the second part, the RMS current of switching frequency harmonics and its multiples is used in combination with the ESR value at switching frequency. This approach is justified as the ESR does not change significantly at higher frequencies. The respective ESR values are usually given in the capacitor data sheet, but could also be measured with an impedance analyser.

Knowing the losses, the capacitor temperature could be calculated based on a thermal equivalent circuit, which is sometimes provided by the manufactures, but could also be measured with special test capacitors with thermocouples embedded in the dielectric. The thermal resistance between surface and ambient depends heavily on the cooling condition, i.e. it is significantly lower for forced air cooling than for natural convection, if the capacitor e.g. is placed in the air flow of the heat sink fan.

Design parameters: Component, technology type.
Couplings: Parasitics, thermal, geometry.

E. EMI-Filter Design

Typically, one of the last steps of the converter design process is the determination of the EMI-filter topology and filter component values based on measured EMI noise levels. There, the influence of e.g. the layout on the EMI cannot be directly evaluated and if a change of the layout/circuit parameters is necessary to meet the EMI emission limits, a time-consuming and expensive redesign of the converter system is necessary. Without any means to predict the EMI emissions, it could happen that several design iterations are necessary.

However, it is possible to estimate the noise emission analytically based on equivalent circuits and/or approximations as will be shown in the following first for the DM and subsequently for the CM filter stage.

1) DM Filter Design: In a first step, the required attenuation of the DM filter must be determined. This is usually performed by calculating or simulating the input current of the converter with which the voltage $V_{LISN}(t)$ at the line impedance stabilisation network (LISN) is calculated. By transferring $V_{LISN}(t)$ into the frequency domain by Fourier analysis, the noise spectrum is obtained. As the EMI test receiver performs a bandpass filtering of the measured signal, also $V_{LISN}(f)$ must be bandpass filtered with a bandwidth of 9kHz around the sweep frequency f_{sweep} [40]. Thereafter, the bandpass filtered voltage for the frequency f_{sweep} is transferred back into the time domain, where the quasi-peak voltage is calculated with a quasi-peak detection circuit as described in [41] and the signal is low-pass filtered [41] to obtain the noise level at f_{sweep}. These steps must be repeated

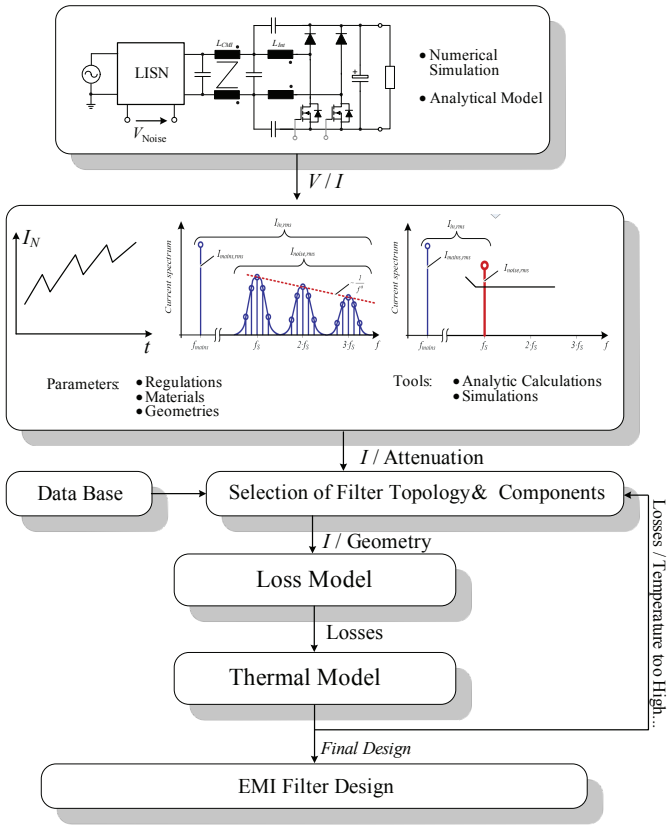

Fig. 12. Design of the DM EMI filter based on simulated input currents and the calculated LISN output voltage. Based on an approximative routine, which determines the required attenuation based on the noise emission level and the limits, the values of the filter inductance and capacitance are calculated. There, the input current as well as the LISN output voltage could also be calculated analytically.

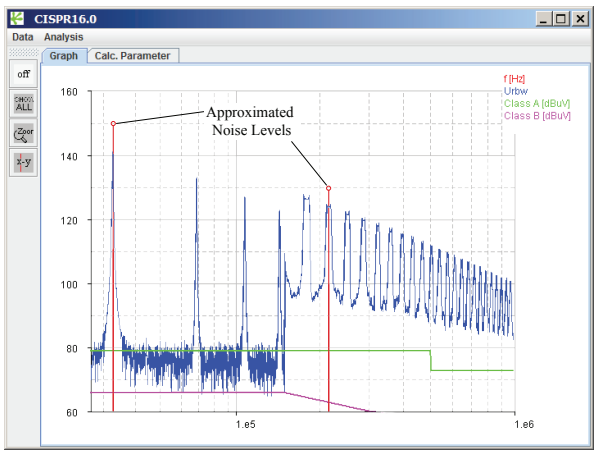

Fig. 13. Simulated noise emission of a single-phase PFC rectifier measured with an EMI test receiver in quasi-peak mode. The considered ultra-efficient PFC rectifier operates at an switching frequency of 30kHz [2], [14].

for each f_{sweep}, what finally leads to the emitted noise level, which is compared with the limits defined by EMI standards resulting in the required attenuation of the filter. The obtained EMI noise emission of a single-phase PFC rectifier is given in Fig. 13.

This procedure is time consuming, but could also be performed automatically in a circuit simulator as implemented e.g. in GeckoCIRCUITS^{TM}, which has a model of the LISN and the calculation procedure described in [41] integrated.

In [42] a simplified worst case approach is presented which assumes, that the total noise current $I_{Noise,RMS}$ (which consists of several harmonics at multiples of the switching frequency with according sidebands) would appear only at the switching frequency. This harmonic would then cause an according noise voltage V_{LISN} at the test receiver. The noise current and V_{LISN} are given by

$$I^2_{Noise,RMS} = I^2_{DM,RMS} - I^2_{N,RMS} \quad (13)$$

$$V_{LISN} = 50\Omega \cdot I_{Noise,RMS}, \quad (14)$$

where $I_{N,RMS}$ denotes the RMS value of fundamental mains current.

With V_{LISN} the required attenuation could be calculated by comparing the noise voltage with the limit value. In case the switching frequency is below 150kHz, the required attenuation is defined by the first harmonic above 150kHz. There, a decay of the amplitudes of the harmonics with increasing frequency must be considered [42]. In Fig. 13 also the noise levels of a single-phase PFC rectifier approximated with the described method are given for the switching frequency and the first harmonics above 150kHz. Besides the simulated noise emission spectrum Fig. 13 also shows the approximated noise levels.

This approach either could be implemented in a circuit simulator or used for the analytic calculation of the required attenuation. There, also the input current could be determined analytically as shown in [2] for a single-phase PFC rectifier.

With the required attenuation, an appropriate filter topology could be chosen. A symmetrical arrangement of the filter inductors allows to attenuate also mixed mode noise in combination with the DM capacitors [43], [44]. As shown in [45] realising the n_f filter stages with the same inductance and the same capacitance values leads to a minimum filter volume. The component values for the DM inductors and capacitors can be determined with equations given in [42], which have been derived by minimising the filter volume. There, the volume is given as empirical function of the component value, the current/voltage and the number of filter stages n_f. With these equations, the volume is calculated for different numbers of filter stages and the solution with the lowest volume is chosen.

In case of the single-phase PFC rectifier, the DM filter consists of a single DM stage with L_{DM} = 88μH and C_{DM} = 16μF in order to achieve the required attenuation of approximately 70dB. The required DM inductance could be realised as leakage inductance of the CM inductor in order to increase the power density and efficiency. The simulated and measured resulting noise emission are given in Fig. 14.

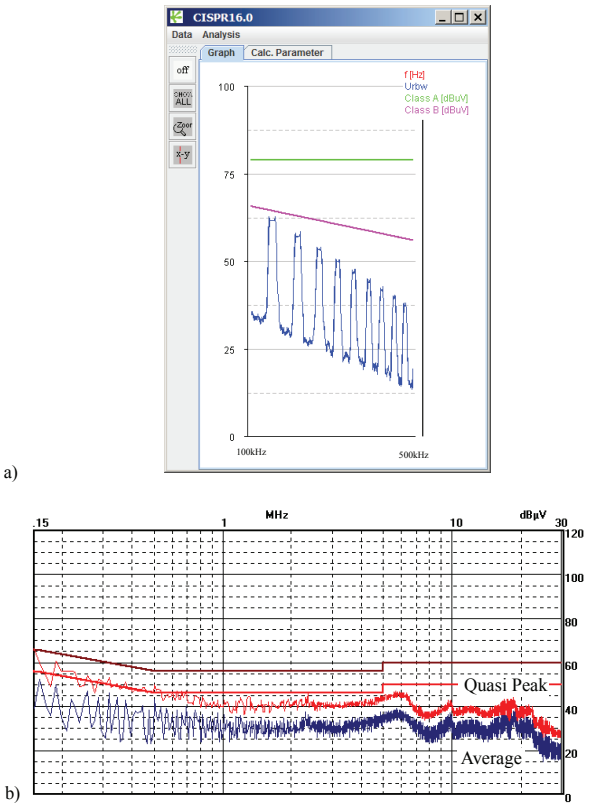

Fig. 14. a) Simulated DM quasi-peak noise in the range from 100kHz to 500kHz with DM EMI filter designed with the calculated spectrum given in Fig. 13. b) Measured quasi-peak and average noise emission of the PFC rectifier. The noise floor fills in the valleys between the harmonics, which are visible in the simulated spectrum.

Design parameters: Component values, filter topology, layout, switching transients.

Couplings: Parasitics, thermal, geometry.

2) CM Filter Design: CM noise emissions of converter systems are often mainly caused by the CM voltage of the output terminals besides internal circuit nodes with fast varying potential with respect to earth, which generate corresponding CM noise currents. The noise currents and/or the CM noise level could be either determined by simulations as shown e.g. in [46] for a three-phase AC/AC matrix converter or by equivalent circuits as shown e.g. in [47] for single-phase PFC rectifiers or in [11] for three-phase PFC rectifiers.

With both methods, the mentioned parasitic CM capacitances from points with high $\mathrm{d}v/\mathrm{d}t$ with respect to earth, such as the capacitances of semiconductor packages to grounded heat sinks or the capacitances of motor cables to a grounded cable shield must be identified in a first step. In Fig. 15 the most important parasitic capacitances for a single-phase bridgeless PFC rectifier are given. There, the capacitors C_S represent the parasitic capacitances of the semiconductors and C_n/C_p are the parasitic capacitances of the DC output and load to earth.

After identifying the important parasitic capacitors, the capacitance values must be determined. This could be

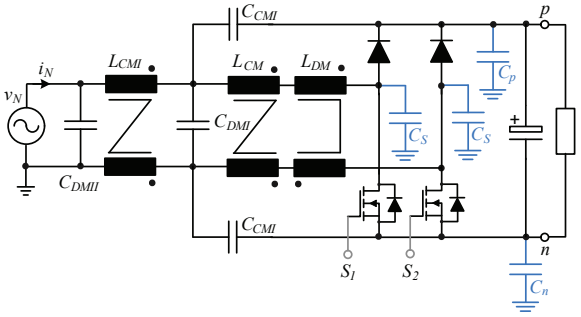

Fig. 15. Schematic of the single-phase PFC rectifier including the parasitic capacitances from nodes with high $\mathrm{d}v/\mathrm{d}t$ to earth, which cause CM currents. The two capacitors C_S describe the parasitic capacitances from the drains of the power MOSFETs / anodes of the diodes to earth and/or against the grounded power semiconductor heat sink. With C_n and C_p the parasitic earth capacitances of the output capacitor and the load are described. In the schematic, the integrated boost inductor is split into its CM and its DM part.

performed by using approximative simplified models (e.g. approximations by plate capacitors), by numerical simulations with FEM/PEEC software tools or by measurements on test setups.

In case the parasitic capacitances are part of the converter design, again the problem arises, that at this design stage the detailed information about the mechanical design and/or the respective parasitics is not yet available and a possible design must be assumed or – if available – values of previous designs/prototypes can be used as a first approximation.

In case the CM noise emission should be determined with simulations, the parasitics must be inserted into the electric circuit model and additionally a LISN circuit has to be included. For calculating the spectrum of the input current up to 30MHz, the simulation time step has to be sufficiently small, what could result in considerable simulation times, especially if a mains cycle must be simulated and the simulation requires time to reach steady state. There, it could be helpful to first simulate the system with a larger time step until a steady state is reached and to subsequently decrease the simulation time step. Alternatively, a periodic operating point analysis as described in [48] could be used which would significantly reduce the calculation effort.

The calculation is simplified if a fixed time step is used. Otherwise, the signals must be re-sampled in order to perform a DFT. The basic calculation steps for obtaining the signal measured by the EMI test receiver are the same as discussed for the DM filter.

In alternative to a numerical simulation, also a CM equivalent circuit could be used to numerically or analytically calculate the CM emission levels. The equivalent circuit additionally gives some insight into the noise generation, what could help to reduce the CM noise emission by changes of the topology or the operating mode instead of filtering. This could reduce the overall EMI filtering effort.

In [47] a procedure for deriving the CM equivalent circuit is described. This is based on the following steps:

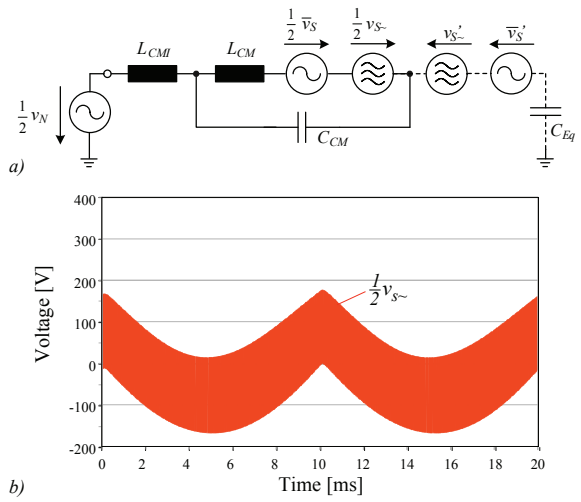

Fig. 16. CM equivalent circuit of the single-phase PFC rectifier with the parasitics given in Fig. 15. Capacitor C_{CM} represents the parallel connection of the two capacitors C_{CMI}, i.e. $C_{CM} = 2C_{CMI}$. With a varying potential of the negative DC output rail n, also a CM current is flowing via capacitors C_S, C_p and C_n. There, additionally the CM voltage v_S' must be considered.

- Insertion of parasitic ground capacitances into the electrical model.
- Simplification of the circuit by shortening of low impedance paths, as e.g. the DC link capacitor and low frequency voltage sources.
- Replacement of switches with pulsed voltage sources.

In Fig. 16 the resulting CM equivalent circuit for the single-phase PFC rectifier is shown. Voltage v_S is the voltage occurring across the switching power transistor, i.e. across S_1 for $v_N > 0$ and across S_2 for $v_N < 0$. In the equivalent circuit this voltage is split into a low frequency (LF) component $\overline{v}_S$ (twice the mains frequency and lower) and a high frequency (HF) part $v_{S\sim}$. Due to the parasitic capacitances of the drain connections of the MOSFETs to earth, the CM voltage v_S', which is a fraction of the CM voltage v_S, and acting via the equivalent earth capacitance C_{Eq}, must be additionally considered. The amplitude of the sources, which are again split in a LF and a HF component, are

$$\overline{v}_S' = \frac{C_S}{C_{Eq}}\overline{v}_S \qquad v_{S\sim}' = \frac{C_S}{C_{Eq}}v_{S\sim} \tag{15}$$

and the equivalent coupling capacitance is $C_{Eq} = 2C_S + C_n + C_p$.

Based on the CM equivalent circuit, the components of the CM filter could be designed. Furthermore, also the resulting CM flux in the magnetically integrated boost inductor could be calculated, what is important for designing the magnetic core of the inductor as described in [2].

Design parameters: Component values, filter topology, layout, switching transients.

Couplings: Parasitics, thermal, geometry.

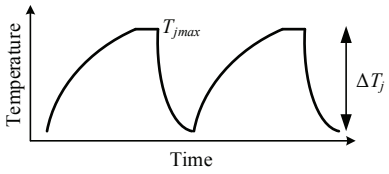

Fig. 17. A temperature cycle of a power module with peak junction temperature T_{jmax} and amplitude ΔT_j.

3) Arrangement of EMI Filter Components: In the previous two sections, the components and the values for the DM and CM filter have been determined. There, the parasitics of the layout and the geometrical arrangement of the power components and the cooling system are basically considered.

However, also the parasitics of the EMI filter components and the capacitive and/or magnetic couplings of the filter components, which are determined by the geometric arrangement and the mechanical design of the inductors and capacitors, significantly influence the achievable HF attenuation of the EMI filter. For example in [49] the effects of the component parasitics and the magnetic coupling of different filter inductors on the attenuation is described. The attenuation reduction could be partly avoided by cancelling the parasitics of the components as described e.g. in [50] for the parasitic capacitance of filter inductors and in [51] for the parasitic inductance of filter capacitors.

Methods for reducing undesired couplings of different filter components, which could deteriorate the filter attenuation, are e.g. described in [52]. There, only basic considerations are discussed, i.e. how the coupling could be reduced, but no means to predict the coupling and the reduction of the filter performance are presented. The prediction could e.g. be achieved with simulation tools based on the PEEC method [53] and could also be used to automatically optimise the filter component placement for minimal coupling as described in [54], [55].

Design parameters: Layout and geometric arrangement.

Couplings: Thermal, geometry.

F. Reliability

It would be of significant benefit to manufacturers to be able to predict and also guarantee the lifetime of components e.g. of power modules or for the complete converter systems in a given application. Therefore reliability modelling and lifetime estimation is of paramount importance.

It has been shown in [56] that a significant amount of device failures is due to mechanical deformation arising during temperature cycling and stress, caused by the different coefficients of thermal expansion of the different materials used in a power semiconductor module. This for example leads to the cracking of solder layers [57] or wire bond lift off.

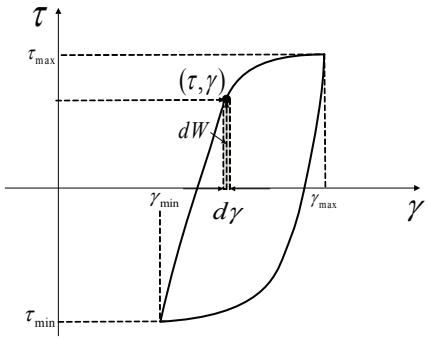

Fig. 18. Stress-strain hysteresis loop for one temperature cycle.

Typically in industry, the Coffin-Manson analytical model [58] is used to estimate lifetime. There, usually a mission profile for a given device is transformed into a series of temperature cycles, and then the device is subjected to these cycles until failure. The number of cycles to failure from these experimental tests is then used to parameterise the model, which then gives the basis to estimate lifetime. The problem is that the transformation from a mission profile to a set of temperature cycles can cause lifetime estimation errors up to a factor of 14 [59], and that the Coffin-Manson model accounts only for cycle amplitudes, ignoring cycle frequency, which can result in errors up to a factor of 12 [60].

The solution is to use a physics based model [19], [61] of the solder deformation mechanisms in power modules. The model is based on Clech's Algorithm and on a Deformation Mechanism Map [59], [62] where the different types of temperature, time-independent and time-dependent stresses and strains are calculated in order to determine the total deformation energy of a particular temperature cycle or mission profile. Most of the model parameters relate to the physical properties of solder and can be taken from literature. However, two parameters must be determined empirically on the basis of cycling tests, which is quite time-consuming. Cycling tests must be performed for every different power module type due to differing geometries. Since two parameters must be found experimentally, at least two different cycling test must be performed. However, once these tests are performed and the model is parameterised, the achievable lifetime of the device could be evaluated for any arbitrary temperature profile.

The model is parameterised through an iterative parameter search. The stress-strain response of the solder to a temperature cycle (Fig. 17) is a hysteresis loop as given in Fig. 18. The integral of the loop is then the deformation energy W_{hys} caused by one cycle. Knowing the number of cycles to failure N_f,

$$W_{tot} = N_f W_{hys} \tag{16}$$

is the total deformation energy until failure.

The parameter search continues until the total deformation energies to failure calculated by the model for the two different performed cycling tests are equal. The parameterised model can now be used for lifetime estimation: the stress-strain response of a mission profile

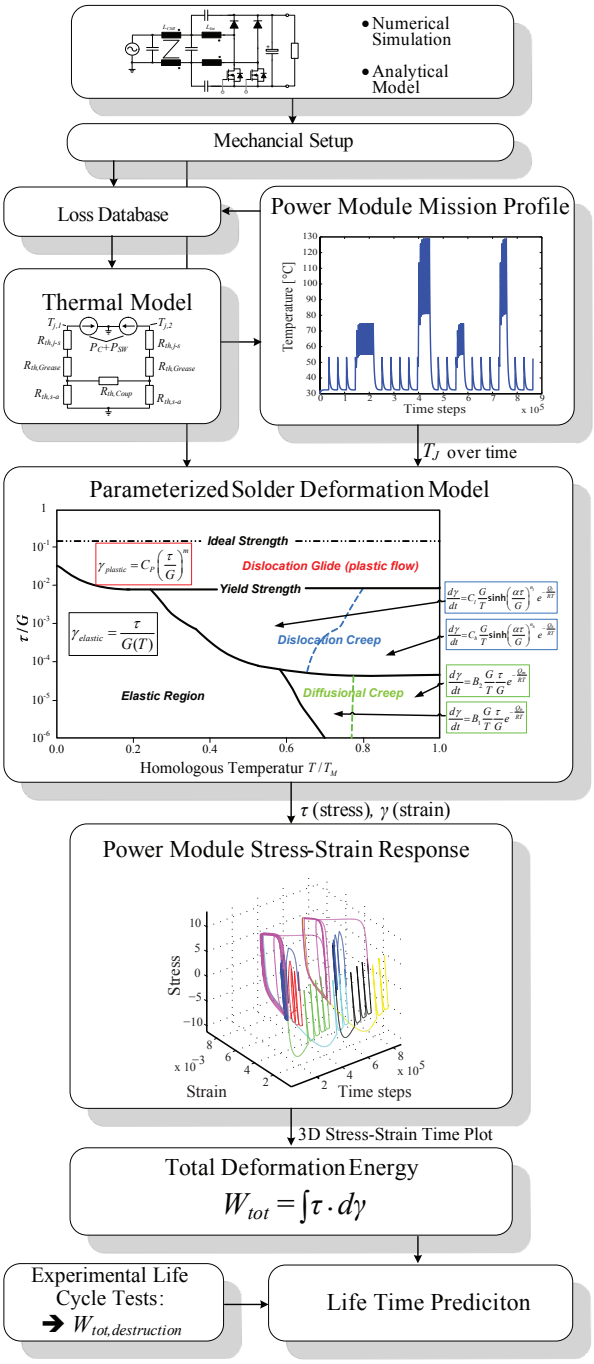

Fig. 19. Flowchart for reliability prediction of power semiconductor devices. Based on the electrical model in combination with a thermal equivalent circuit, the junction temperature as a function of time is calculated. There, the mechanical setup/arrangement is required for deriving the thermal model. The temperature profile is used to determine the stress-strain response (cf. Fig. 18) of the solder junction with a deformation model, which is also dependent on the mechanical setup and where different types of deformation are included. The stress-strain response is integrated and the resulting total energy W_{tot} is compared to the energy required for destruction of the device, so that finally a life time prediction results. The energy for destroying the device $W_{tot,destruction}$ is determined experimentally.

can be simulated and the total deformation energy W_{tot} calculated. The total deformation energy is then compared to the deformation energy $W_{tot,destruction}$ required for destruction of the device. This energy is evaluated by experimental life cycle tests and could be stored for different devices in a data base.

A flowchart of the calculation is shown in Fig. 19. There, the difficulty is to determine the junction temperature as function of time for the whole mission profile. This could result in long simulation times, as the considered time constants vary in a wide range – from the ns-level for simulating the switching intervals to minutes/hours/days for the mission profile [63].

A possibility to calculate the results faster is to generate a database of losses for the different operating points as shown in Fig. 19 and then just calculate the thermal equivalent circuit and feed the losses into the circuit. There, the smallest time constant to consider is the one of the thermal circuit, which is much larger than the one for the switching transients.

For two mission profiles, with deformation energies W_{tot1} and W_{tot2}, the relative lifetime r can be calculated as:

$$r = \frac{W_{tot2}}{W_{tot2}}. \tag{17}$$

The developed physical model allows for the simulation of mission profiles directly, omitting the errors of transformation present in the conventional approach, and it accounts for all parameters of temperature cycles as it models the stresses and strains occurring directly. This allows for much more accurate lifetime and reliability estimation.

Design parameters: Temperature cycles, i.e. cooling system or component type, junction technology.

Couplings: Thermal, geometry, layout.

IV. Linked Models and Optimisation

In the manual virtual design discussed in the previous section, analytical models or software tools are utilised in the different domains and/or design steps. However, the tools are not linked, so that the user has to transfer the data between the different tools.

In [64]–[66] the authors proposed to use the programme iSIGHT^{TM} [67] for automated data translation between the tools for the different domains. A similar approach is presented in [68], where commercial software is coupled with self made tools for the design of magnetics and semiconductor loss calculations by iSight^{TM} in order to design a full bridge DC-DC converter with high output power density. However, a basic limitation of such approach is that the individual tools are available only from different manufactures, i.e. one has to pay the license fees for all tools. Furthermore, the automatic data exchange might not work any more after installing an update of a tool. This is also true for controlling commercial tools via scripts as has been done in [69] without linking different domains for the optimisation of electric component parameters of a half bridge and a three-phase inverter. Additionally, for maintenance of the tools, experts for the different software packages are required.

Linking of the models in the different domains means in the considered case, that the results of the calculation of one model are transferred to the next model via an automated interface. An example for such data exchange is the transfer of losses calculated in the semiconductor model to the thermal model. However, then the models are not evaluated at the same time as will be discussed in section V, as it would be required for considering also couplings of the different domains without iterative loops.

In Fig. 20 a possible structure of the data flow between the different domains/models is shown by black arrows. There, e.g. the electric circuit model is linked with a data base of the power semiconductor conduction/switching losses and with the thermal model describing the cooling of the semiconductors, so that the junction temperature of the semiconductors could be determined. There, the thermal model does not need to include the cooling of the passives or other components, if a thermal coupling between different components is neglected.

Other important links are between the electric circuit and the magnetics and capacitor models, which allows to calculate the losses and to determine the geometrical properties of the respective components. All component losses are then fed into an associated thermal model, which describes the heat transfer from the individual component to the ambient. There, the coupling between the different cooling systems could not be considered, as this information is not available prior to the mechanical design. Accordingly, this coupling could only be included into an iterative design process.

The mechanical design is performed based on the dimensions of the single components and of the cooling system(s). This finally results in a layout/3D design, which could be used to determine the EMI-filter requirements. There, also knowledge of the parasitics of the magnetics and of the output capacitor and the semiconductor switching behaviour is required in order to comprehensively calculate the EM noise emissions.

In a first step with the software tools and/or the analytical models a local optimisation of single components could be performed as indicated with the blue arrows in Fig. 20. This is also possible with linking the models. For example, the operating point or the component parameters of the electric circuit could be optimised for minimal RMS currents, or the geometry of a transformer core or the number of turns as well as the diameter/thickness of the conductors realising the windings could be optimised with an analytical model as explained in [5].

For the design/optimisation of magnetic components also e.g. PExprt^{TM}, a software tool by ANSOFT could be utilised, which automatically performs designs with different magnetic cores from a database and the user could select the one which fits best his needs.

Another option is to optimise the geometry of the heat sink. In [7] e.g. the optimisation of the fin and/or heat sink

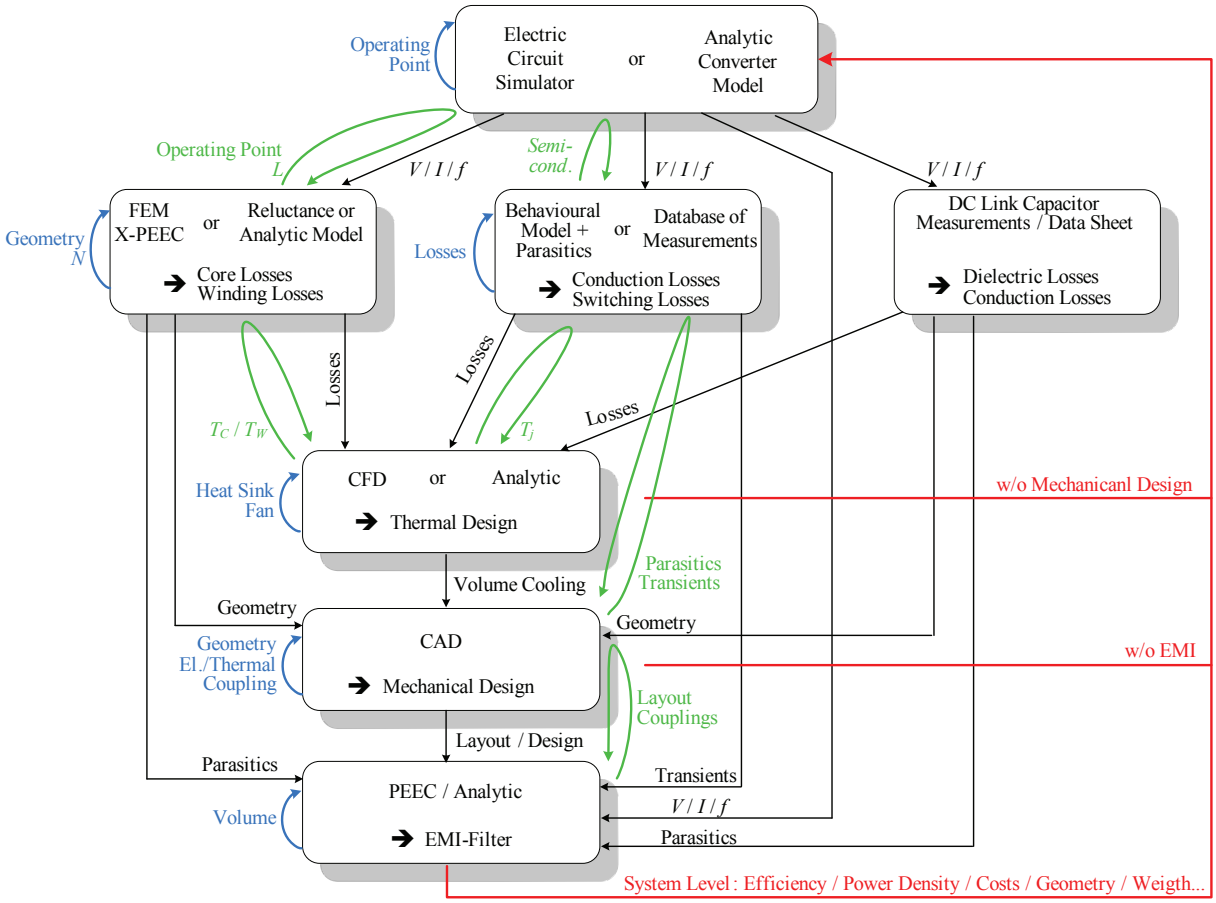

Fig. 20. Automated data transfer by linking the models of the different domains (black arrows). With the models an optimisation of the components could be performed by local optimisation loops as shown by blue arrows. Also parts of the system, e.g. the cooling of the semiconductors, can be optimised by considering more than one domain. Examples for this are shown by the green loops. Finally, also system level performance indices as e.g. efficiency or power density could be optimised via the red loops. There, it is also possible, to neglect the EMI filter and/or the mechanical design.

geometry for a given fan is explained.

In the course of the mechanical design, the thermal and electromagnetic coupling of the different components, as well as the parasitics can be minimised. Finally, the volume of the EMI filter could be minimised while meeting the emission limits.

By linking the models during the optimisation more design aspects can be considered at the same time. For example in [69] linked electrical and semiconductor loss models are used to minimise the semiconductor losses. If a thermal model would have been included, the design of the heat sink could have been optimised, too. Another interesting optimisation loop is the link between the electric and the magnetics model. There, e.g. the operating point could be adapted such that the losses or the volume of the magnetic component are minimised. Alternatively, the core could be designed so that it has enough safety margin to saturation in all operation points. By linking the transformer loss model and the thermal model, also the operating temperature of the winding T_W and of the core, T_C, could be minimised or kept below a desired limit.

The mechanical design, i.e. the layout and the parasitic capacitances and inductances, and their influence on the EMI emissions could be minimised by linking the model for the mechanical design and the EMI filter model.

In case all models are linked, a system optimisation for minimal overall losses or maximal power density could be performed as shown by red arrows in Fig. 20. There, the mechanical design and/or the EMI filter could be included or neglected in a first step for simplifying the process. Accordingly, the thermal coupling of the components due to the mechanical arrangement would be neglected and the EMI filter would have to be designed subsequently. Such simplification provides a good starting point for the design process, especially in cases, where the influence of the arrangement of the components on the temperature or parasitics is small. Examples are designs, where the individual components are placed with large distances, or e.g. each component has its own heat sink or the components are mounted on a water cooler where most of the heat is dissipated directly via this cooling system.

The system optimisation based on multi-domain models is like building prototypes with different parameters and finally select the system with best performance. However, the optimisation can be performed much faster and

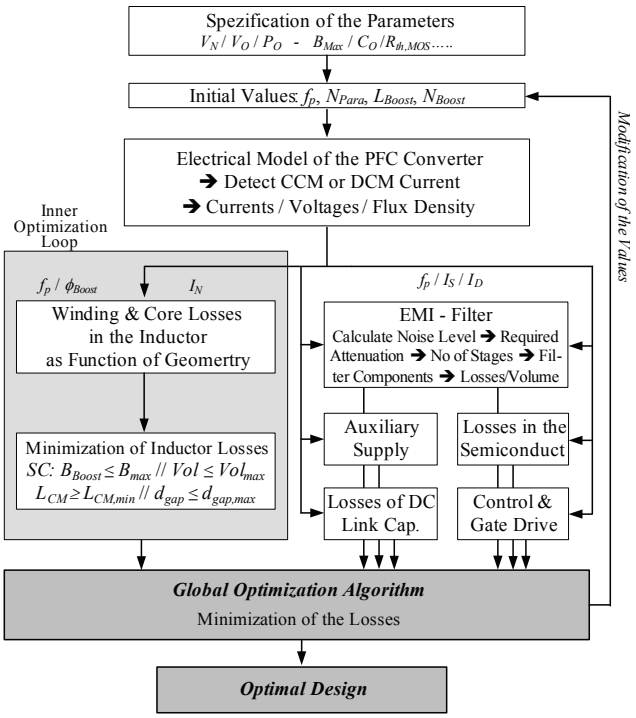

Fig. 21. Flow chart of the optimisation procedure for maximising the efficiency of the single-phase PFC rectifier shown in Fig. 4

a far higher number of parameter sets can be evaluated in the course of the optimisation. Furthermore, it definitely identifies the best parameter set for a given design, what cannot be achieved even with the best simulation tool without optimisation.

However, it is important to note, that the optimisation result significantly depends on the accuracy of models, i.e. with coarse models only a roughly optimised parameter set could be determined. However, setting up the optimisation always forces the designer to formulate a clear design goal and not only a vague idea of the final goal. Furthermore, it also gives insight how far the design approaches the technological limits.

The design flow given in Fig. 20 could be realised by linking different software packages or extending one package to cover all the domains. Alternatively, also analytic models could be used, which allow a very fast optimisation of converter systems. Examples for ultra-compact or ultra-efficient PFC rectifier and DC-DC converter systems for telecom power supplies are given in [2], [3], [70], [71].

The flowchart for the efficiency optimisation of a single-phase PFC rectifier system (Fig. 4) is given in Fig. 21. Based on this procedure the design variables (f_P, chip area of power MOSFETs and diodes, number of turns and geometry of boost inductor) are optimised for minimal losses. There, the models for the different domains are linked, but no coupling as described in the following section is included.

The starting point of the procedure is the specification of the converter system, including input/output voltages and the output power but also component limits as e.g. the maximal allowed flux density or the maximal junction temperature of the MOSFETs, which are constraints during the optimisation. Also the starting values of the design variables are set. With these values the currents and voltages of all components and the losses in the semiconductor elements are calculated. There, for each switching action first the operation mode is determined, so that also combined DCM/CCM operation can be considered. Additionally, the time behaviour of the currents is determined, which is required for the EMI filter design.

Furthermore, the magnetic flux variation within in each pulse interval is calculated by means of a reluctance model. The flux values are used in an inner optimisation loop, which determines the number of turns and the geometry of the core and the winding resulting in minimum boost inductor losses. Since the aim of the optimisation is ultra-high efficiency, no thermal models of the core and the windings are required, which would limit the design in case the volume of the inductor would be minimised. In the ultra-high efficiency system all components are operating well below their thermal limits, what is also advantageous with respect to lifetime and reliability.

The global optimisation algorithm adds the losses of the boost inductor, the CM filter inductor, and the semiconductors and varies then the free parameters such that the overall system losses are minimised. In the system losses also the losses of the control circuit, of the output capacitor and of the EMI filter, which are assumed to be independent of the design variables, are included. Furthermore, the gate drive losses and the auxiliary power which slightly depend on the MOSFET´s chip area are added.

V. Coupled Domains

In the previous section, linear design processes based on software tools and/or analytic models, which are linked, i.e. have an automated data transfer, have been discussed. There, only the data transfer is automated, so that after the calculation of a model is finished the data is transferred to the next model, but the models are not calculated at the same time. This means a coupling between different domains could not be considered directly, but only via a time consuming iterative approach where first model 1 is evaluated based on an initial data set, then the results are transferred to model 2, model 2 is calculated, and data is transferred back to model 1 replacing the initial data set. Subsequently, this sequence is repeated until the results converge to a final result.

The major couplings between the different domains/models are due to:

- Component values which dependent on other domains as e.g. temperature or flux density;
- Thermal couplings via heat conduction paths, heat radiation or flow of a coolant (dependent on geometry);
- Magnetic, electric / capacitive or electromagnetic couplings;

- Component parasitics which depend on the component geometry and/or /mechanical design.

If a set of equations describing the system behaviour as function of all degrees of freedom is available these couplings would be visible as mixed terms in the equations, i.e. variables of more than one domain would be present in a mathematical expression and could not be separated. Uncoupled variables only would occur in additive terms, that easily could be analytically separated, i.e. considered separately during the design process.

1) Component Values: A well known example for the first item is the temperature dependence of power MOSFET losses. For calculating the losses, the junction temperature is required, which could only be calculated based on knowledge of the losses and a thermal model. A solution is to calculate the semiconductor losses and the thermal MOSFET model simultaneously. This could e.g. be done by including a thermal equivalent circuit and a semiconductor loss model into an electric circuit simulator as shown in Fig. 23 for GeckoCIRCUITS^{TM}. There, the electric circuit model is linked with a data base of the semiconductor conduction and switching losses and with a thermal model describing the semiconductor cooling as could be seen in Fig. 22, where the coupling is shown by the blue arrow from the semiconductor model to the electric circuit model. The junction temperature determined with the thermal model is directly used in the loss model and the electric models, and calculated in each time step by the circuit simulator. The current junction temperature is used in all models. This is also a kind of iterative approach in the time domain, where the simulation has to be continued until a steady state is reached.

The coupling of the electric and the thermal equivalent circuit could be accomplished relatively easy as the fundamental structure of the differential equations of the equivalent circuits is approximately the same and only the physical units/variables must be exchanged. In a thermal equivalent circuit for example, the temperature is exchanged with the voltage and the heat flow/losses is replaced by the current, so that the thermal equivalent circuit could be simulated with the same solver as the electric circuit.

With this approach the design engineer still has to determine the value of the thermal resistances / capacitances based on data sheets and/or numerical thermal simulations. Furthermore, the engineer must decide on the topology of the thermal equivalent circuit and the number of equivalent circuit elements/nodes. This could be a difficult task, especially for the case where several semiconductors are mounted on the same heat sink or in the same power module and a thermal coupling between the elements has to be considered. For simplifying this problem, in [6] an approach is presented which allows to automatically derive the thermal equivalent circuit of a 3D model of a power module or of power semiconductors mounted on a heat sink as shown in Fig. 23. There additionally, the simplified implementation of the thermal

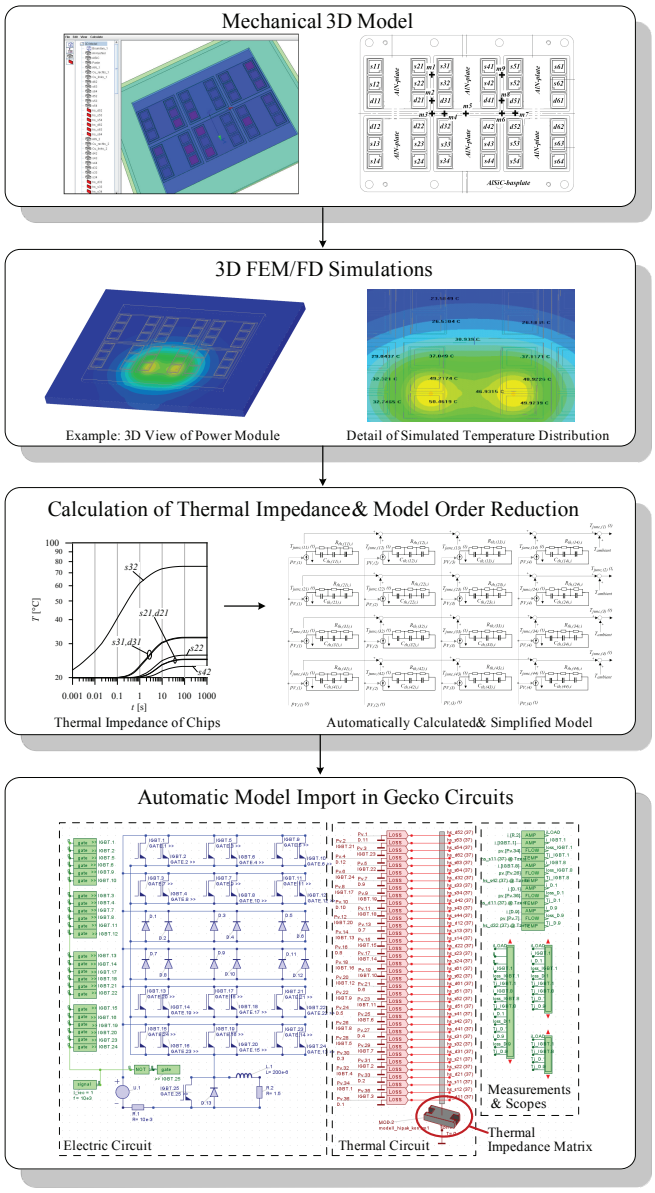

Fig. 23. Flowchart of an automatic generation of a thermal equivalent circuit based on a 3D mechanical design, FEM simulations and an automatic model order reduction. Finally, the equivalent circuit of the power module or of different semiconductors on a heat sink is directly imported into GeckoCIRCUITS^{TM} and could be used to calculate the junction temperatures.

model, i.e. a model order reduction is discussed, which guarantees a sufficient simulation speed as the thermal model otherwise could have a large number of nodes which would result in a significantly increased computational effort (proportional to n_{NC}^3). This approach is implemented in GeckoCIRCUITS^{TM} in combination with a 3D modeler, which derives a thermal equivalent model based on a 3D finite difference calculation and links this model to the electric circuit simulator.

A similar approach could be used for magnetic devices, which could be described by electric equivalent circuits based on reluctance models. The reluctance models can easily be coupled with the model of the actual electric circuit as described in [24]. This coupling could also

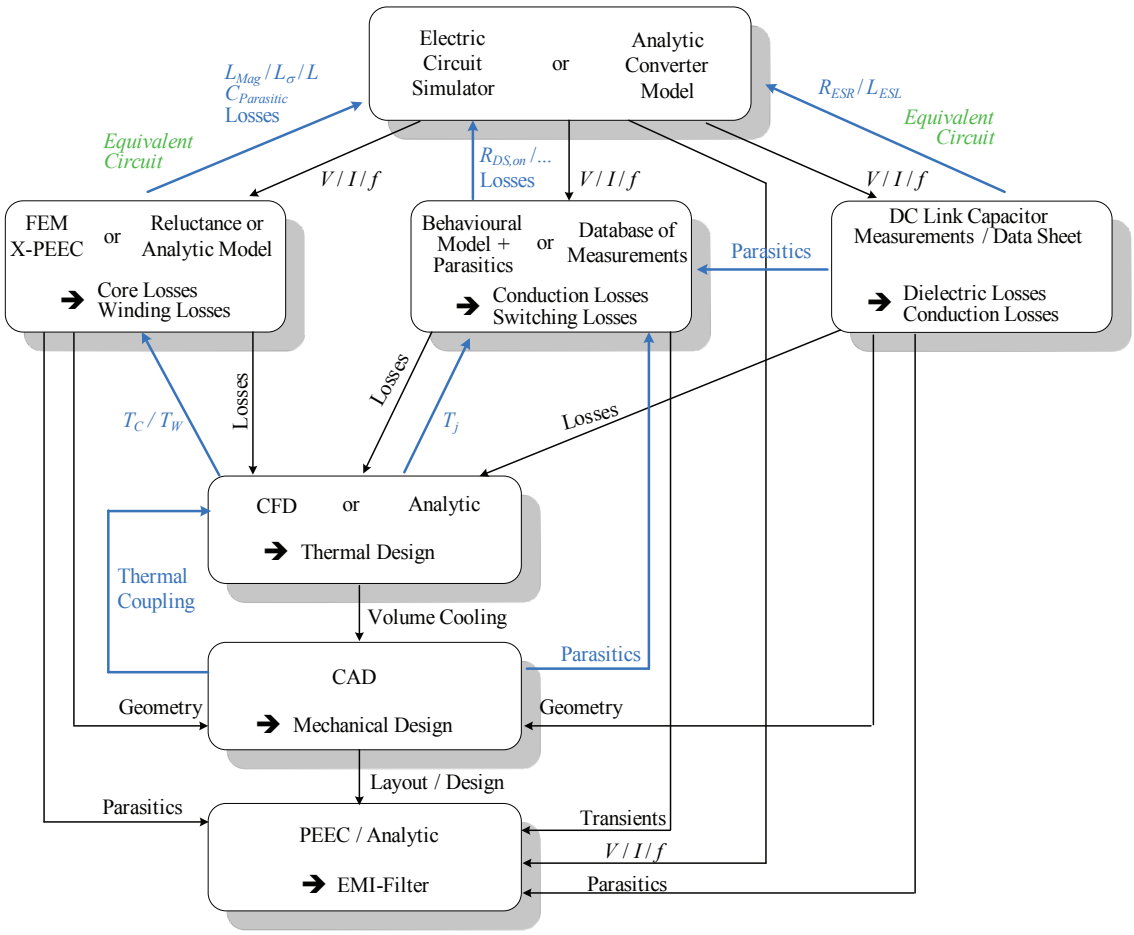

Fig. 22. Models for the different domains with the data exchange shown by black arrows. Examples for coupling of different domains are shown by blue arrows.

be seen on the upper left hand side in Fig. 22, where the magnetic model could feed the inductance values, the parasitic capacitances and/or the losses back to the electric model. There, also the saturation behaviour or the dependence of inductance values on the operating point could be considered.

The software PExprt^{TM} by ANSOFT^{TM} performs an automatic equivalent model generation of magnetic components based on double 2D FEM simulations [33]. This model can directly be inserted into SIMPLORER^{TM} and PExprt^{TM} could perform a kind of automated design for specific cores in the database. Furthermore, the software allows to calculate the temperature distribution of the magnetic component. However, a thermal coupling to other components can not be considered.

Applying electrical equivalent circuits for modelling and coupling effects in different domains could be extended from thermal/magnetics also to mechanical or other domains. Such approaches are used e.g. in SIMPLORER^{TM} or SABER^{TM} by SYNOPSIS^{TM} for drive systems or hydraulics.

Besides the cooling system and the magnetics, also capacitors can be easily modelled and coupled to the electric domain via an equivalent circuit. In the simplest case, only a resistor R_{ESR} is added. More detailed models for describing also the HF behaviour often use parallel connections of different capacitance values in series with resistors and include a series inductance L_{ESL} [72]. In addition, the dependence of the capacitance value on the voltage and, in combination with a thermal model, also on the temperature could be included. There, a data base for the equivalent circuits of the capacitors would be very helpful and would simplify the design process significantly. However, in many applications, the influence of the capacitor parasitics is relatively low, so that this often can be neglected without significantly impairing the overall accuracy of the system model.

2) Thermal: So far, only thermal models for describing selected temperatures of the component itself and the heat transfer to the ambient have been considered. However, in ultra-compact designs, which become more and more important due to the general demand for higher power density, also a heat transfer between the components due to radiation, heat conduction and/or heat transport via the coolant could take place. In order to model this effect the thermal models of the single components must be coupled. There, the geometrical arrangement of the components plays a significant role.

Up to now this coupling could only be addressed by complex CFD tools, which allow a linking of the tools but not a real coupling of the models. In loosely packed converter system this is not an issue as the thermal coupling is relatively weak. Also in compact systems the thermal coupling could be neglected, if the cooling system is designed such that each component mainly dissipates its heat directly to the ambient. An example of such system is the telecom DC/DC converter shown in [70], where the semiconductors and the magnetics have independent heat sinks.

3) Geometric: Based on the dimensions of the components and the cooling system, the mechanical design of the converter system could be determined supported by CAD tools. In case the converter system should fit into a given volume and/or shape, the mechanical dimensions of the components are strongly coupled (for compact designs).

4) Electromagnetic: Besides the volume/shape of the converter system, the arrangement and size of the components determines the layout of the power circuit and many of the parasitics capacitances and/or inductances. The layout of the power circuit is strongly coupled with the switching transients and losses, what could be included in the electric model via the parasitics which could be derived with a PEEC based tool [46].

As mentioned above, by using a circuit simulator and considering the different domains by equivalent circuits, the solution is automatically determined in an iterative fashion until a steady state condition is reached. There, also the models could be changed in the course of the simulation in case e.g. a junction temperature exceeds its limits and a larger heat sink or a different semiconductor is required.

With analytical models/equations, also an iteration is necessary. However, in this case the models usually are solved consecutively, i.e. for example first the electric model, and afterwards the magnetic model is evaluated, as the modelling of a coupling of different domains is difficult and would results in complicated mathematical expressions. Consequently, the iteration takes places by solving the sequence of models more than once, and via feedback of the results of the consecutive model. An example is the sequence electric/magnetic model. First, the currents and voltages are calculated with the electric model. Then the magnetic component is determined and the losses and the resulting inductance value are fed back to the electric circuit, which is recalculated.

An alternative to electric equivalent circuits would be numeric FEM/CFD simulations, which could cover all domains, e.g. by using multi-physics tools such as COMSOL^{TM}. This approach would allow to include all physical effects simultaneously. However, there it would be difficult and very time consuming to determine a switching waveform of a power semiconductor or even the input current of a PFC rectifier within a mains cycle.

In Fig. 24 an overview of the different couplings is given. The electric model which describes the circuit

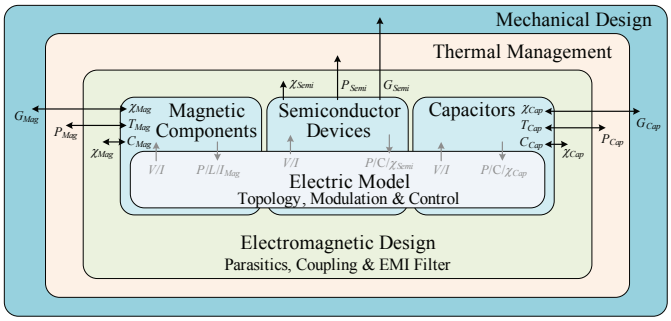

Fig. 24. Diagram showing the inter-domain couplings. These couplings are arranged such, that the domains which influence other domains are enclosing these domains. There, the main direction of influence is considered and e.g. the influence of the parasitics on the losses, i.e. the design of the cooling system, is neglected.

function considering the modulation and control schemes is depicted in the centre. The electric model is coupled via component values, which depend on other domains, as well as through parasitics and losses to the magnetic components, semiconductor devices and capacitors. The next three layers – thermal management, electromagnetic and mechanical design – are depicted such, that a larger layer area indicates couplings which influence the inner layers. For example, the geometrical design and the arrangement of the components significantly influences the thermal couplings of the components. It also influences the electromagnetic coupling of the components and the parasitics of the interconnections. Furthermore, the thermal management, i.e. for example the size of the heat sink, also influences the parasitics e.g. of the heat sink to ground. There, it is assumed that the influence of the parasitics on the total losses is relatively small, so that the main direction of influence is from thermal to electromagnetic design.

During the design process, some of the couplings may cause some undesired behaviour e.g. an electromagnetic coupling could cause noise, so that either directly the coupling components are changed, or the mechanical arrangement, which also influences the couplings, is modified. Thus, the values of the inner layers finally also take influence on the outer layers. However, this feedback/inverse coupling direction is more due to non-desirable behaviour than due to physical reasons.

5) Simplification: The coupling via component values, where e.g. the design of the heat sink takes influence on the losses as these are dependent on the junction temperature, could be avoided if the design is performed for one operating point and a fix junction temperature. There, the design of the heat sink must be chosen in the second step such, that the assumption is fulfilled. This means in the considered case that the junction temperature reaches the assumed value at the considered operating point. Such an approach is also possible, if e.g. a fixed leakage inductance value for a transformer is assumed in the electrical circuit, which is then realised in the course of the transformer design. Also magnetic

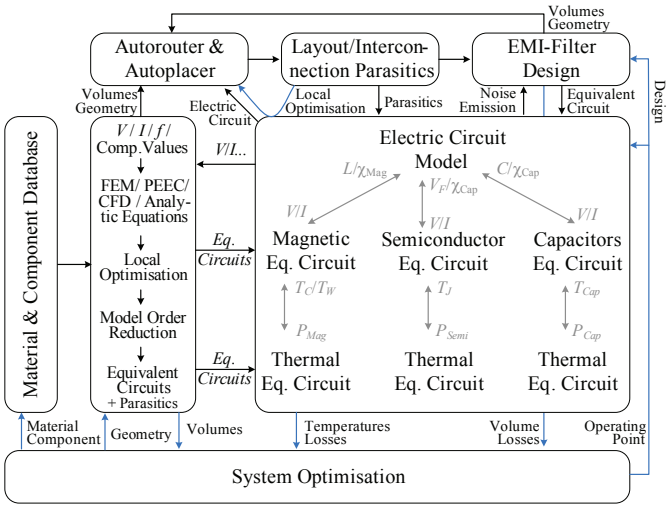

Fig. 25. Implementation of a coupling of the electric, magnetic, semiconductor, capacitor and thermal domains by equivalent circuits. For deriving the equivalent circuits tools are used, which are linked with material/component data bases. These tools automatically derive the equivalent circuit based on data base information and/or geometrical data provided by the user and perform a model order reduction, such that the circuits can be implemented computationally efficient in the circuit simulation. Based on the geometry of the components and the electrical circuit an autorouter/autoplacer automatically performs a mechanical design and a routing of the interconnections, so that the layout parasitics can be derived. These parasitics and the noise emission of the circuit are used to determine an EMI-Filter design. The losses and the volumes of all the individual components are fed into an optimisation algorithm, which could optimise e.g. the power density or the efficiency. There, also cost models could be implemented for minimising costs. In the long run this modelling approach could be extended with reliability models, in order to estimate also the converter lifetime.

saturation and/or the dependence of the inductance value on the current could be neglected in the circuit simulation. If furthermore, the components are designed such that the parasitic elements take negligible influence on the voltages and currents, the design process of the components could be decoupled. This approach is widely applied, as it simplifies the design and is often accurate enough.

6) Design Platform – Next Steps: In Fig. 25 a possible setup of a flexible design platform is shown, which implements the different domains as equivalent circuits and provides tools for the domains for automatic generation of the equivalent circuits. These tools are linked with data bases for materials and components and have several interfaces. First, the currents and voltages and other important component data is provided by the electrical model. Based on these values, the components are designed with numerical tools such as FEM, PEEC, CFD, Finite-Difference or analytical equations. There, a local optimisation of the single components could be performed as shown for magnetic components in [3], [70] where PXpert^{TM} or analytical expressions could be employed. In this optimisation constraints must be considered. A direct coupling to other domains is neglected, but the result usually will provide a good starting point for the design.

For the designed and/or optimised components automatically equivalent circuits are derived and a model order reduction is performed as shown e.g. in [6] for thermal equivalent circuits of power modules. The model order reduction is very important in order to avoid excessive calculation times of the circuit simulation. Finally, the simplified equivalent circuits are inserted into the electric model. Additionally, for the components thermal models are generated, which are also included in the electric circuit simulation.

The tools for deriving the equivalent circuits provide the information about the geometry of the components to an autorouter/-placer, which also is connected to information on the electrical circuit. Based on this data, the mechanical layout and the interconnections are automatically determined and in the next step the parasitics of the layout are determined. There, a local optimisation loop including the electric model and the autoplacer/-router could be performed in order to minimise parasitics and/or overvoltages/noise generated due to the parasitics.

The parasitics are fed into the EMI filter design, where also the generated noise calculated in the circuit model is considered. Based on this an EMI filter is designed and the equivalent circuit is transferred to the circuit model. The volume/geometry of the filter is transferred back to the autoplacer/-router, so that the volume of the filter could be integrated into the mechanical design. The parasitics and the couplings of the EMI filter components are directly considered within the EMI filter design approach. An electromagnetic coupling of the filter components to the remaining circuit could be reduced by spatially separating the filter or enclosing it in a shielding box. This separation is supported by the electric circuit, since the filter is located at the input of the converter/power flow, i.e. at the boundary of the system.

In order to achieve an optimal system setup, an optimisation of the design parameters could be performed.

VI. Conclusion

In the design process of power electronic systems several domains/aspects as e.g. electric, magnetic, thermal, EMI, mechanic, etc. have to be considered in order to achieve a high system performance. For most of these domains software tools and/or analytical approaches already exist, which substantially support the design process. These tools also allow a deeper insight and understanding of the components/domains physics what results in an improved and more reliable system design. Furthermore, many design errors can be identified before building a time and cost intensive prototype system, what allows to reduce the time to market and the development costs.

However, interfaces for data transfer between these tools are still missing, so that the user has to manually transfer the data or write scripts/programmes, which link the different tools. This is cumbersome and time consuming and finally increases again development costs. By linking the tools of different domains, this problem

could be avoided. The best option, however, is to have an integrated tool, which covers all domains and furthermore cuts license costs.

Another problem of available tools is, that these are typically designed for very detailed simulations covering all aspects of the considered domain. This impairs the handling of the tools and/or often comprehensive expertise is required for using the tools. For power electronic systems, however, many design issues could be solved by simplified tools, which do not cover all aspects of each domain. Such tools also should be able to automatically derive simplified electrical equivalent circuits, which directly could be implemented in the electrical circuit simulations. Based on this approach and by integration of the tools, i.e. by automatic data transfer, the virtual design process would be more widely applied.

With the linked tools also an optimisation on the system level (e.g. efficiency or power density) could be performed. This would enable a much more direct approach for meeting the design demands. Moreover, it could be guaranteed, that the finally chosen set of design parameters is really the optimal solution for the given problem, which fully utilises the components and consequently also reduces costs.

Going one step further, also the couplings between the different domains could be included into the simulations. This requires a strong interaction of the tools covering the different domains. A relatively simple method to consider the coupling is to apply electrical equivalent circuits, which are solved together with the electrical circuit. There, it is important to have tools, which allow to derive these circuits.

Often, the coupling could be reduced by the system design as e.g. by shielding, by spatial separation or by fixing values for the coupling variables, that have to be fulfilled by both coupling domains. Thus, only a few strong couplings, as e.g. via the geometry of the components, must be considered in the course of the design.

Due to the constantly rising demand for higher power density and/or a closer integration, the influence of the couplings will increase in future. Furthermore, virtual prototyping becomes more and more important, since manufacturing of integrated systems is more time and cost intensive and for an integrated system not all signals could be monitored in the hardware prototype but only via simulations.

In future, also simulation of reliability and lifetime prediction will play a more important role. Tools covering this area for power electronics applications are missing so far. There, especially the large gap between the time constants for switching transient and a mission profile simulation must be considered and solutions, as e.g. utilising loss data bases, are required for addressing this issue.

Finally, in order to prepare the design engineers better for these tasks, the comprehensive modelling/simulation and optimisation of power electronic systems must be also covered in power electronics education in order to prepare young engineers for the challenges of the future mainly VP based design concepts in the area.

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