Design of a 5-kW, 1-U, 10-kW/dm^3 Resonant DC–DC Converter for Telecom Applications

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***Abstract*—The demand for decreasing cost and volume and also for increasing efficiency leads to a constantly increasing power density of converter systems. For maximizing the power density of a 5 kW telecom supply, an optimization procedure that automatically balances the switching frequency, semiconductor and passive losses, and thermal performance has been developed. This procedure and the belonging analytical converter and transformer models are presented in this paper. Moreover, the resulting optimized design, which has a power density of 10 kW/dm^3 and an efficiency of 94.5% at a height of 1 U, is presented.**

***Index Terms*—DC–DC converter, optimization, resonant converter, telecom power supply.**

I. Introduction

In THE area of power electronic converter systems, there is a general trend to higher power densities that is driven by cost reduction, an increased functionality, and in some applications by the limited weight/space (e.g., automotive, aircraft). In order to reduce the volume of a system, first the most appropriate topology for the intended application must be chosen.

Applying resonant dc–dc converters can help to reduce the switching losses and/or to raise the switching frequency of the power switches. On this account, the overall system size in many industrial applications, e.g., telecom power supplies [1], high-voltage generators [2], or inductive heating [3] could be reduced and the power density could be increased. Especially, the series–parallel resonant converter [see Fig. 1(a)] is a promising converter structure since it combines the advantages of the series resonant converter and the parallel resonant converter. On the one hand, the resonant current decreases with the decrease of the load, and the converter can be regulated at no-load, and on the other hand, good part-load efficiency can be achieved [4], [5]. Furthermore, the converter is naturally short-circuit proof.

During the design of a resonant converter, one has to determine, for example, the values of the resonant circuit elements (C_S, L_S, and C_P), the turns ratio, and the number of primary turns so that the design constraints (temperature rise, operating frequency, etc.) are met for the given specifications (input voltage, output power, load, etc.). In order to find the values for the components that lead to an optimal design (optimal with respect to the given design aim—e.g., minimal converter volume, maximal efficiency, minimal costs, etc.), one needs an automatic optimization procedure. A possible flowchart for such an optimization procedure is shown in Fig. 4.

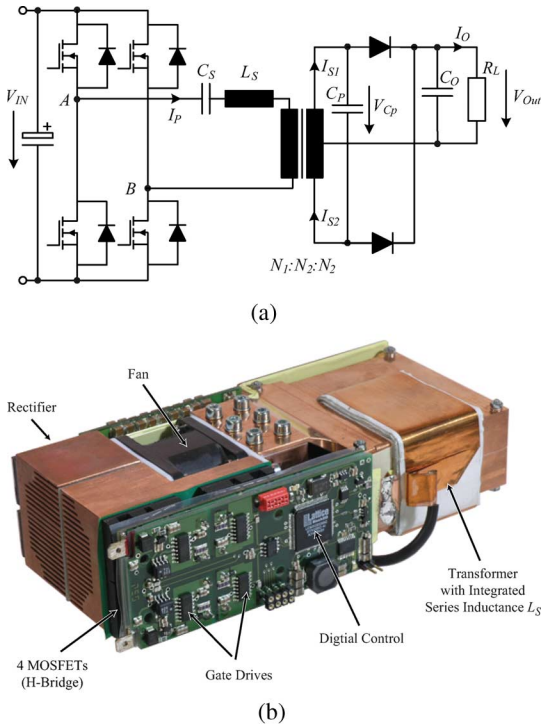

Fig. 1. (a) Schematic and (b) picture of the telecom power supply.

First, the specifications of the application and the initial values of the resonant circuit elements are fed into the analytic model of the resonant converter. Within the model, the operating frequency, all voltages, and currents of the converter inclusive phase shift and also the flux values in the transformer are computed. With this information, the design of the transformer is optimized in an inner optimization loop (cf., Fig. 4) so that the resulting transformer volume is minimal. In parallel, the volume of the heat sink for the power semiconductors is calculated using the semiconductor losses and an analytic thermal heat sink model. The resulting volumes are fed into the global optimization algorithm that varies the resonant circuit elements, the cooling conditions, and the parameters of the semiconductors within given limitations based on a Lipschitz global optimizer (LGO) [6] until a minimal overall converter volume is obtained.

Before the optimization procedure is compiled, the type of output filter must be chosen. Therefore, the standard *LC* filter is compared to a capacitive output filter in Section II.

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TABLE I
SPECIFICATION OF THE TELECOM POWER SUPPLY IN FIG. 1

Input voltage	400V
Input current	13.0A
Output voltage	48-56V
V_{Ripple} at Output	300mV_{pp}
Output current	104A@48V, 90A@56V
Output power	5kW
Maximum ambient temp.	45°C

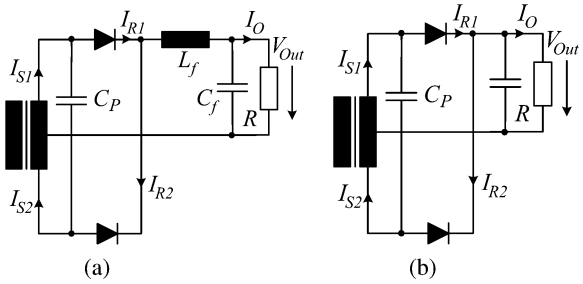

Fig. 2. Schematic of the *LC* and the capacitive output filters for the telecom supply shown in Fig. 1. (a) LC-Output Filter. (b) Capacitive Filter.

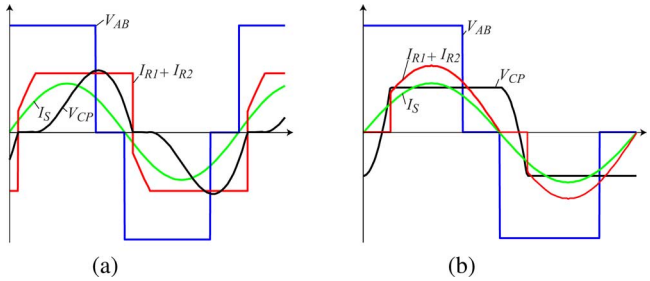

Fig. 3. Typical waveforms for a series–parallel resonant converter with *LC* and capacitive output filters. (a) LC-Output Filter. (b) Capacitive Filter ($I_S = I_{S1} + I_{S2}$).

TABLE II
COMPONENT VALUES OF THE *LC* AND THE CAPACITIVE OUTPUT FILTERS SHOWN IN FIG. 2 FOR AN OUTPUT VOLTAGE RIPPLE OF 300 mV_{pp}

LC-Filter		Capacitive Filter	
C	30μF	C	470μF
-		R_{ESR}	50$\mu\Omega$
L	5μH	-	
$I_{C,Ripple,RMS}$	4.6A	$I_{C,Ripple,RMS}$	52A

In Section III, the optimization procedure for series–parallel resonant converters is described in detail. For this routine, an accurate model for the resonant converter is needed, which must not be too extensive in order to limit the computation time. The used model is based on the extended fundamental frequency analysis and is discussed in Section IV. There, also the equations for calculating the semiconductor losses, the model for calculating the capacitor volumes, and the model for optimizing the transformer in the inner optimization loop are presented.

The resulting design of the optimization, with a target volume of 10 kW/dm^3, for the data given in Table I is presented in Section V [the input voltage is controlled by a power factor correction (PFC)]. There, the influence of different parameters on the optimal operating point and measurement results are also discussed. Finally, a conclusion is drawn in Section VI.

II. *LC* VERSUS CAPACITIVE OUTPUT FILTER

With the chosen series–parallel resonant topology, there are basically two different output filter configurations possible: one with an *LC* low-pass filter, as shown in Fig. 2(a), and one with a pure capacitive filter, as shown in Fig. 2(b). There, the output filter topology influences the waveforms of the dc–dc converter significantly, since the *LC* filter acts more like a current source at the output and the capacitive filter as a voltage source.

Typical waveforms for the two filter structures are given in Fig. 3. In case of the *LC* output filter, the continuous capacitor voltage (CCV) and the discontinuous capacitor voltage (DCV) modes must be distinguished [7], [8]. Since the DCV mode usually occurs at heavy load conditions in Fig. 3(a), the waveforms for this mode are shown. There, the voltage waveform of the parallel capacitor V_{C_P} is clamped by the output current to zero for a certain period of time, which leads to a discontinuous and very distorted parallel capacitor voltage V_{C_P}. At the time when V_{C_P} falls to zero, the resonant current I_{S1} is smaller than I_O. As long as the resonant current I_{S1} is smaller, the capacitor voltage V_{C_P} is clamped to zero by the negative difference between I_{S1} and I_O $[-(I_{S1} - I_O)]$ that flows through the rectifier diodes. From the angle when I_{S1} is larger than I_O, the positive difference between the currents $(I_{S1} - I_O)$ charges the capacitor C_P.

Due to the sinusoidal resonant current and the output inductor, the current in the rectifier diodes starts more smoothly resulting in a lower diode turn-ON stress. In the secondary winding, however, flows a constant dc current plus ac component causing higher transformer losses.

With the capacitive output filter, the current in the rectifier jumps from zero to the value of the output current. This could result in higher diode switching losses depending on the diode semiconductor technology and in an increased electromagnetic interference (EMI) noise level. The transformer secondary current is, however, lower that results in a compact transformer design.

Based on the required output voltage ripple of maximum 300 mV_{pp} and a maximum inductor ripple current of $\pm 7.5\%$ for the *LC* filter, the component values for the two topologies can be determined (cf., Table II). The ripple current in the filter capacitor in the topology with capacitive filter is much higher than the one for the *LC* filter. Applying electrolytic capacitors, this high ripple current results in a large filter volume due to the relatively high equivalent series resistance (ESR)/low-current-carrying capability of electrolytic capacitors. This is shown in the second line of row "*LC*-Filter Size" in Table III. The first line represents the volume of the capacitor if just the capacitance value is considered and the ripple current is neglected. With the ripple current, the capacitor volume increases more than by a factor of 10. Both values are based on the cuboid volume of cylindrical electrolytic capacitors.

TABLE III
COMPARISON OF LC AND CAPACITIVE OUTPUT FILTERS WITH ELECTROLYTIC OR CERAMIC CAPACITORS

	Electrolytic		Ceramic	
	Cylindrical	Cuboid	SMD-Device	Mounted
μF/cm³	170	134	111	90
I_{AC}/cm³	0.25 A	0.19 A	41.6 A	35.1 A
LC-Filter Size in [cm³]	μF only: **0.22** + **40.9** (L)		**0.32 + 40.9** (Inductor)	
	I_{AC}: **24.2** + **40.9** (L)		(Max. I_{AC} <11.3A)	
C-Filter Size in [cm³]	μF only: **3.7**, $I_{AC} < 1.5A$		**5.4**	
	I_{AC}: **273** ⇒ C=36mF		(Max. $I_{AC} < 233$A)	

For electrolytic capacitors, two volumes are given. The first one gives the volume if just the capacitance value is realized—neglecting the ripple current I_{ac} and the current-carrying capability of the capacitors. With the second value also, the ripple current is accounted for. The indicator of the LC filter has a volume of 40.9 cm³.

If the capacitance is realized by ceramic capacitors, the volume decreases down to 0.32 cm³ including ripple current considerations. In both cases, the volume of the inductor (40.9 cm³) is based on very compact commercially available inductors, e.g., [10] and [11]. Due to the large inductor volume, the size of the LC filter is relatively large and would consume approximately 10% (including interconnection) of the target volume of 0.5 dm³ for the overall system. Furthermore, the size of the transformer becomes larger with an LC output filter as mentioned before. Since the size of the resonant tank elements in the final design is relatively small, as could be seen in Figs. 1 and 11, the influence of the volume share of the resonant tank elements, which is influenced by the type of output filter, on the system volume is small. Since the volume share of the LC filter is too big for achieving a power density above 10 kW/dm³ and the focus of this paper is to achieve the maximal possible power density, the LC filter is not considered any more in the following.

With a capacitive filter and ceramic capacitors, the volume of the filter elements decreases down to 5.4 cm³ including the volume of the printed circuit board (PCB) for mounting, and the maximum thermally possible ripple current increases to 233 A. A capacitive filter with electrolytic capacitors would result in a filter volume of 273 cm³ and a capacitance value of 36 mF if the ripple current is considered. Taking just the required capacitance value into account, this volume decreases to 3.7 cm³.

III. OPTIMIZATION PROCEDURE

After the selection of the appropriate topology [cf., Fig. 1(a)], the components values must be chosen so that the system volume becomes minimal and the power density maximal. Since the volume of the single components, which are mainly limited by the respective maximum operation temperature, interdepend to some extent on each other, the optimization of the overall volume is a quite difficult task with many degrees of freedom.

Therefore, an automatic optimization procedure is applied for determining the optimal component values of the telecom supply.

In Fig. 4, a possible flow chart of this procedure is given, where the specification of the design parameters like the input and output voltage, the output power, temperature limits, material characteristic, etc., is the starting point of the procedure. These parameters as well as initial values for C_S, C_P, L_S, and for the number of turns of the transformer (N_1 and N_2) must be specified by the user. The initial values have no influence on the final result of the optimization procedure, but could influence the computation time until the best solution is found.

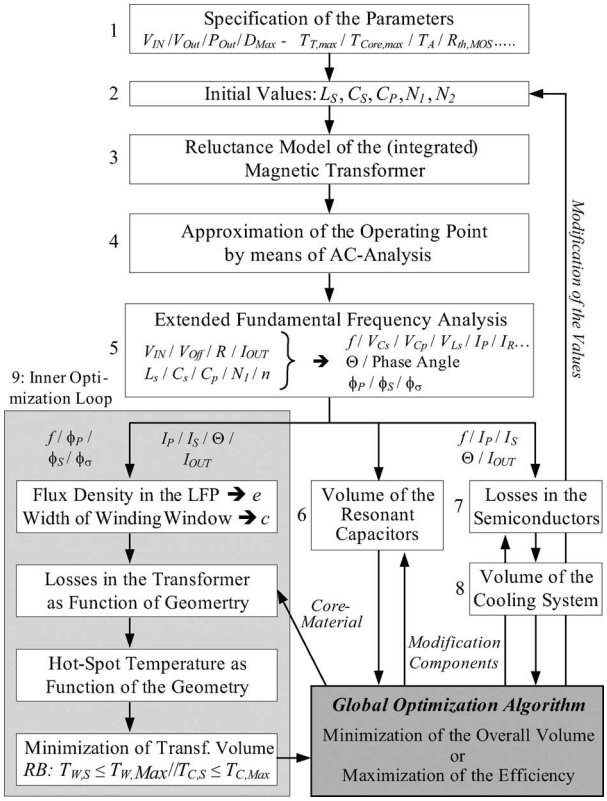

Fig. 4. Automatic procedure for optimizing the volume/efficiency of a series–parallel resonant converter while keeping the device temperatures below given limits.

Based on the values for the series inductance and the turn numbers, the reluctance model of the transformer with integrated series inductance is calculated in step 3. Thereafter, the operating point of the dc–dc converter is estimated by an approximated fundamental frequency analysis [9] (step 4). With the estimated values, the solution space for the analytic converter model (cf., Section IV-A) is restricted and the calculation time is reduced (step 5). The converter model is based on a set of equations that are derived with the extended fundamental frequency analysis and solved numerically. The solutions are the operating frequency, the voltages, and currents as well as the flux distribution of the integrated transformer including phase information.

With the frequency and the voltages across the resonant tank capacitors, the volumes of these components are calculated (step 6). Furthermore, the switching and conduction losses in the MOSFETs and rectifier diodes are determined (step 7). These losses, the ambient temperature, and the maximum junction temperatures of the semiconductor devices are used for calculating the volume of the semiconductor heat sink including the fan based on the cooling system performance index (CSPI) (in

watts per kelvin per cubic decimeter), which is defined by

$$\text{CSPI} = \frac{1}{R_{\text{th},S\text{–}A}[\text{K/W}]\, Vol_{HS,Magn.}[\text{dm}^3]} \tag{1}$$

and has been introduced in [17] (step 8).

The volume and the shape of the transformer core and the two windings are determined in a second inner optimization procedure (step 9). There, the volume of the transformer is minimized while keeping the temperatures below the allowed limits. For this purpose, first two geometrical degrees of freedom are eliminated by setting the flux density in the leakage path to the same value as in the middle leg conducting the main flux and by calculating the core window width using the optimal winding thickness and the turns number [9].

Thereafter, the core and winding losses are calculated as a function of the three remaining geometrical variables (a, b, and c, cf., Fig. 7). With the losses and the thermal model of the transformer, the temperature distribution in the core and the winding could also be calculated as function of the variables a, b, and c/d. The peak temperatures in the windings and the core together with the maximum allowed temperatures are the constraints for the following minimization of the transformer volume. Furthermore, the variables $a - e$, defining the transformer geometry, can be restricted in order to preserve certain limitations resulting from the manufacturing process.

In the inner optimization loop, it is also possible to maximize the efficiency of the transformer, if an upper limit for the transformer volume is given.

Together with the volumes of the capacitors/heat sink, the minimized transformer volume is passed to the global optimization algorithm. This algorithm systematically varies the values of the resonant tank elements and the number of turns until a minimal system volume or a maximal efficiency is obtained. The whole procedure is implemented in Maple and requires approximately 20–30 s computation time per operating point on a Intel T7200 processor with 2 GB memory. Depending on the starting point, the complete optimization process requires two to three days time.

The procedure presented in this paper is limited to series–parallel resonant converters with capacitive output filters and to converters in the considered power/voltage range. Such a kind of optimization procedure basically could also be applied to other converter types or for optimizing, for example, the efficiency of the converter. There, the models must be exchanged and the flowchart must be adapted so that all interdependencies of the volumes, losses, etc., are considered. The basic generalized optimization methodology is not the focus of this paper for the sake of brevity but will be discussed in a separate paper.

IV. Modeling of the Converter

In the subsequent paragraphs, the different models of the optimization procedure are explained shortly. First, the analytical converter model is derived, and then, the equations for the semiconductor losses and the model for the resonant tank capacitor volumes. There, some of models are based on best-in-class devices for the given application, since, for example, the switching losses of the MOSFETs depend significantly on the device technology. A more general approach would require a database of different devices, which could be selected by the optimization algorithm. This would significantly increase the computational effort, so that in the considered case, devices are determined by the user and fixed before the optimization. Finally, the loss and the thermal model of the transformer are presented.

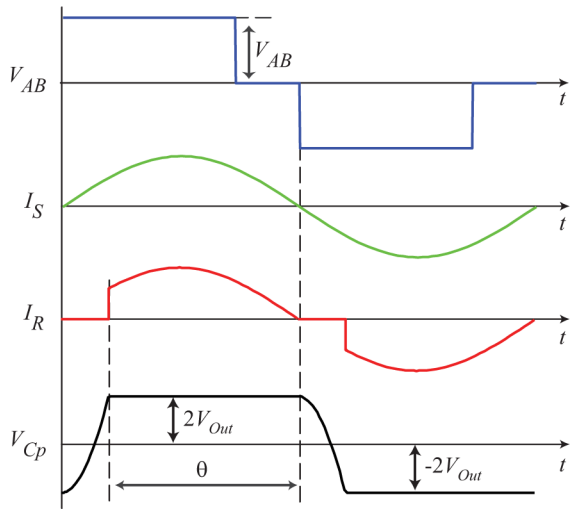

Fig. 5. Converter voltage V_{AB}, resonant current I_S, rectifier current I_R $(= I_{R1} + I_{R2})$, and parallel capacitor voltage V_{C_P}.

A. Analytical Converter Model

The following calculations for the series–parallel resonant converter shown in Fig. 1 are partly based on the extended fundamental frequency analysis proposed in [16] and [7]. Furthermore, the control method described in [7] (cf., Fig. 5) with zero-voltage switching (ZVS) condition in one leg and zero-current switching (ZCS) condition in the other leg as well as control by frequency and duty cycle is considered in the equations. This control method reduces the switching losses significantly. For details on the strategy, refer to the mentioned publication.

The presented calculations are based on the assumptions that both the primary resonant current I_P and the secondary resonant current I_S $(= I_{S1} + I_{S2}$ the sum of the two sections of the secondary) are sinusoidal with a third harmonic component, that the output voltage is constant, and that the components are ideal. The major procedure of the analysis is to determine the fundamental frequency impedance $Z_{C_{PR}}$ of the parallel connection of C_P and the rectifier at first. With this impedance, the input impedance Z_{AB} of the resonant circuit, seen by the H-bridge/voltage source V_{AB} (cf., Fig. 6), could be calculated. In the impedance Z_{AB}, the reluctance model of the transformer is also included.

In the next step, two equations can be set up. The first one describes the relation between the phase shift of the primary current I_P and the fundamental component of the H-bridge voltage $V_{AB(1)}$, which is determined on the one hand by the duty cycle D and on the other hand by Z_{AB}. The second expression relates the input impedance of the resonant tank to the amplitude of the

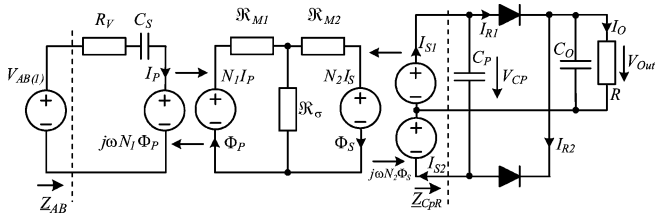

Fig. 6. Equivalent circuit of the series–parallel resonant converter with the capacitive output filter.

resonant current. These equations are derived in the following paragraph.

1) Derivation of the Model: For the derivation of the system equations, first the run of the parallel capacitor voltage $V_{C_P}(t)$ is expressed by the analytical function

$$V_{C_P}(t) = \begin{cases} \dfrac{2V_{\mathrm{Out}}}{1+\cos\theta}\left(1-\cos\theta-2\cos\omega t\right), & \text{for} \quad 0\le\omega t<\pi-\theta \\ 2V_{\mathrm{Out}}, & \text{for} \quad \pi-\theta\le\omega t<\pi \end{cases} \tag{2}$$

and the current in the resonant tank on the secondary side I_S is described by

$$I_S = I_{S,1}\sin(\omega t) + I_{S,3}\sin(3\omega t). \tag{3}$$

With the current in the resonant tank, the average rectifier current is calculated, where it is important to note that the effective transformer ratio is $N_1 : N_2$ when a rectifier diode is conducting and $N_1 : 2N_2$ in case no rectifier diode is conducting. Therefore, the resonant current I_S must be multiplied by 2 during the interval from $\pi-\theta$ to π [cf., (4)], since in the equations, a transformer ratio of $N_1 : 2N_2$ is generally assumed

$$\begin{aligned} \frac{V_{\mathrm{Out}}\pi}{R} &= \int_{\pi-\theta}^{\pi} 2I_{S,1}\sin(\omega t) + 2I_{S,3}\sin(3\omega t)d\omega t \\ &= 2I_{S,1}\left(1-\cos\theta\right) + \frac{2}{3}I_{S,3}\left(1-\cos 3\theta\right). \end{aligned} \tag{4}$$

Since the average rectifier current must be equal to the load current, the rectifier conduction angle θ could be calculated by solving

$$\frac{2I_{S,1}\left(1-\cos\theta\right)+\frac{2}{3}I_{S,3}\left(1-\cos 3\theta\right)}{\pi} = \frac{V_{\mathrm{Out}}}{R} \tag{5}$$

for θ, which results in a relatively long expression that is not presented here for the sake of brevity.

In the next step, the equivalent load impedance for each harmonic ($\nu = 1, 3$) is calculated with the harmonics of the parallel capacitor voltage

$$V_{C_P,\nu} = \frac{2j}{\pi}\int_0^{\pi} V_{C_P}(t)\, e^{-j\nu\omega t} d\omega t \tag{6}$$

by ac analysis

$$Z_{C_P R,\nu} = \frac{V_{C_P R,\nu}}{I_{S,\nu}}. \tag{7}$$

With the load impedance and the reluctance model of the transformer described in [7]

$$N_1\underline{I}_{P,\nu} = \Re_{M1}\underline{\Phi}_{P,\nu} + \Re_\sigma\left(\underline{\Phi}_{P,\nu} - \underline{\Phi}_{S,\nu}\right) \tag{8}$$

$$N_2\underline{I}_{S,\nu} = -\left(\Re_{M2}\underline{\Phi}_{S,\nu} + \Re_\sigma\left(\underline{\Phi}_{S,\nu} - \underline{\Phi}_{P,\nu}\right)\right) \tag{9}$$

and the flux in the primary winding $\Phi_{P,\nu}$ and thereby the primary voltage could be calculated. Thereafter, the mesh equation for the resonant tank on the primary side of the transformer could be set up

$$V_{AB,\nu} = \frac{I_{P,\nu}}{j\nu\omega C_S} + I_{P,\nu}R_V + j\nu\omega N_1\Phi_{P,\nu} \tag{10}$$

and the input impedance of the resonant tank including the load is given by

$$Z_{AB,\nu} = \frac{V_{AB,\nu}}{I_{P,\nu}}. \tag{11}$$

Based on the input impedance, the system equations are given by

$$0 = \frac{\nu\pi}{2}(1-D) - \arctan\left(\frac{\Im(Z_{AB,\nu})}{\Re(Z_{AB,\nu})}\right) \tag{12}$$

for the phase shift of the input current and

$$I_{P,\nu} = \frac{4V_{\mathrm{IN}}}{\nu\pi\left|Z_{AB,\nu}\right|}\cos\left(\frac{\nu\pi}{2}(1-D)\right) \tag{13}$$

for the amplitude of the primary current. By numerically solving these equations, the operating frequency and the duty cycle of the converter can be calculated. With the frequency and duty cycle, all voltages, currents, and also the flux distribution can be determined.

B. Semiconductor Losses

For calculating the volume of the heat sink for the semiconductors with (1), the maximum operating temperature and the thermal resistance between junction and heat sink of the semiconductors are required. These values can be derived from the data sheets. Furthermore, the losses in the four MOSFETs including antiparallel diode and the two rectifier diodes must be calculated. Due to the different switching conditions in the two legs, the losses/current waveforms are also different.

With the fundamental component $I_{P,1}$ and the third harmonic $I_{P,3}$ of the resonant current on the primary side, the rms currents in the leg with ZCS and in the leg with ZVS condition can be calculated by

$$I_{T_{\mathrm{ZCS}}} = \frac{1}{2}\sqrt{I_{P,1}^2 + I_{P,3}^2} \tag{14}$$

$$I_{T_{\mathrm{ZVS}}} = \sqrt{\frac{1}{T}\int_0^{\frac{DT}{2}}\left[I_{P,1}\sin(\omega t) + I_{P,3}\sin(3\omega t)\right]^2 dt}. \tag{15}$$

With the rms currents, the conduction losses in the MOSFETs can be determined. For the diodes, an approximately constant forward voltage drop is assumed, so that for calculating the conduction losses in the antiparallel MOSFET diodes of the ZVS leg and the rectifier diodes, the average currents are required.

These are given by

$$I_{D_{\mathrm{ZVS}}} = \sqrt{\frac{1}{T}\int_{\frac{DT}{2}}^{\frac{T}{2}} I_{P,1}\sin(\omega t) + I_{P,3}\sin(3\omega t)\,dt} \tag{16}$$

for the MOSFET diodes and by

$$I_{D,\mathrm{Rec}} = \frac{3I_{P,1}(1-\cos\Theta) + I_{P,3}(1-\cos 3\Theta)}{3\pi} \tag{17}$$

for the rectifier diodes.

Due to the assumed control method where one leg switches at ZCS and one at ZVS condition, the switching losses are relatively low. If the ZCS leg, which should switch at the zero crossing of the resonant current, is switched a bit before the zero crossing, the MOSFET has to turn off a small current. Because of the fast switching and the large output capacitance of the MOSFET, this current does not cause relevant turn-OFF losses. In case the turned-OFF current is large enough, so that it charges the MOSFET capacitances during the interlocking delay [7], the opposite MOSFET is turning on at zero voltage. Consequently, the switching losses in the ZCS leg are negligible [9].

In the ZVS leg, the MOSFET has to turn off larger currents, which causes losses in case the current is large enough. In order to determine the losses, measurements with APT50M75 MOSFETs from Microsemi (former Advanced Power Semiconductors) have been performed [9]. Based on these measurements, the losses can be determined by

$$P_{Sw,\mathrm{ZVS}} = 2\big(1.9\times10^{-7} I_{p,\mathrm{OFF}}^2 - 3.8\times10^{-6} I_{p,\mathrm{OFF}} + 1.4\times10^{-5}\big) f_{Sw} \tag{18}$$

in case the turned-OFF MOSFET current is

$$I_{p,\mathrm{OFF}} \geq 15\ \mathrm{A} \tag{19}$$

and they are negligible if the turned-OFF current $I_{p,\mathrm{OFF}}$ is below 15 A.

With the presented loss/current equations, the overall losses can be calculated by

$$P_{\mathrm{Semi}} = R_{DS,\mathrm{ON}}\left(2I_{T_{\mathrm{ZCS}}}^2 + 2I_{T_{\mathrm{ZVS}}}^2\right) + 2V_{F,D} I_{D_{\mathrm{ZVS}}} \tag{20}$$

$$+ 2V_{F,R} I_{D,\mathrm{Rec}} + 2P_{Sw,\mathrm{ZVS}}. \tag{21}$$

To these, the losses in the gate drive circuits, which can be calculated with the gate charge/capacitance and which increase linearly with frequency, must be added.

With the semiconductor losses dissipated via the heat sink and the maximal heat sink temperature T_{Sink}, the maximal allowed thermal resistance of the heat sink could be calculated by

$$R_{\mathrm{th},S\text{–}A} \leq \frac{T_{\mathrm{Sink}} - T_{\mathrm{Amb.}}}{P_{\mathrm{Semi}}}. \tag{22}$$

There, the heat sink temperature is given by

$$T_{\mathrm{Sink}} \leq \min\{T_{J,T_{\mathrm{ZVS}},\max} - R_{\mathrm{th},T_{\mathrm{ZVS}}} P_{V,T_{\mathrm{ZVS}}},\ T_{J,T_{\mathrm{ZCS}},\max} - R_{\mathrm{th},T_{\mathrm{ZCS}}}(P_{V,T_{\mathrm{ZCS}}} + P_{V,D_{\mathrm{ZCS}}}),\ T_{J,D_{\mathrm{Rec}},\max} - R_{\mathrm{th,Rec}} P_{V,\mathrm{Rec}}\}. \tag{23}$$

The volume of the semiconductor heat sink directly follows with (1).

C. Resonant Tank Capacitors

In the series and the parallel capacitor of the resonant tank, approximately sinusoidal currents with a high amplitude and frequency are flowing. In order to limit the losses and the temperature rise, dielectrics with a low loss factor $\tan\delta$ are required. There are basically two good choices: either foil capacitors with polypropylene or ceramic capacitors with C0G/NP0 material. Since the resulting volume with foil capacitors is significantly larger than with the ceramic ones as could be derived from data sheets, the latter are chosen for the considered telecom power supply.

For calculating the volume required for realizing the series and parallel capacitor, a commercial 3.9 nF/800 V COG ceramic capacitor in a 1210 SMD housing from Novacap [12] has been chosen as a reference component, since it offers the highest capacitance per volume ratings at ac voltages with an HF and amplitude. Based on this capacitor, the ratio (i.e., volume per capacitance in millimeter per farad)

$$\frac{V_C}{C} = \frac{(3.18+0.75)(2.54+0.25)(1.65+0.75)}{3.9\times10^{-9}} \tag{24}$$

has been calculated. There, it has been assumed that the capacitors are mounted on both sides of a double-sided 1.5-mm standard PCB with a 0.75-mm gap in direction of the connections and a 0.25-mm gap orthogonal to this direction. Additionally, the volume of the PCB is considered by adding half the thickness of the board to the thickness of the capacitor.

In the optimization procedure, the volume of the resonant tank capacitors is calculated by multiplying the aforementioned ratio by the respective capacitance value. Furthermore, the dielectric losses in the capacitors are calculated by

$$P_C = \omega C \tan\delta U_C^2 \tag{25}$$

and compared with the maximal allowed ones. These can be calculated by multiplying the ratio (i.e., losses per capacitance)

$$\frac{P_{C,\max}}{C_{\mathrm{ref}}} = \frac{0.35}{3.9\times10^{-9}}\left(1 - \frac{T_A - 40\ ^\circ\mathrm{C}}{125\ ^\circ\mathrm{C} - 40\ ^\circ\mathrm{C}}\right) \tag{26}$$

which is based on the loss limit of 0.35 W per 1210 housing (maximum operating temperature 125 °C), by the capacitance value. In case the losses in the capacitors are too big, no feasible design is possible for this set of parameters and the parameters are varied by the optimization procedure so that the losses are below the limits.

D. Transformer Model

In the optimization procedure shown in Fig. 4, the shape of the transformer is also optimized for minimal volume in the inner loop while the hot spot temperatures are kept below the limits. For this inner optimization loop, the volume, the losses, and the temperature distribution in the transformer are needed as a function of the geometry. The geometry could be described

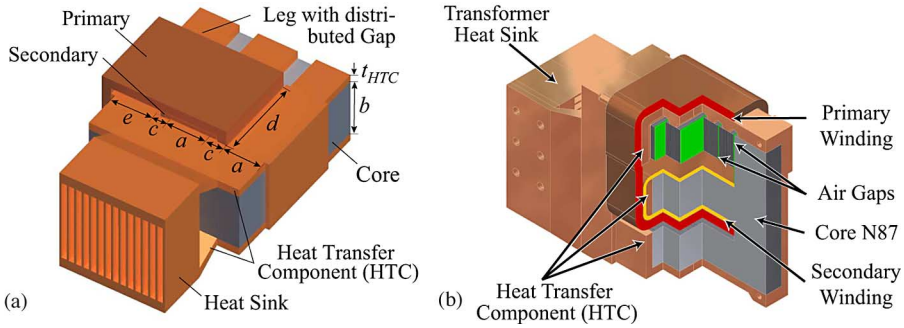

Fig. 7. (a) Geometry of transformer with integrated series inductance and HTC/heat sink for cooling. (b) Cut view of the transformer.

by five variables, as shown in Fig. 7(a), where the construction of the transformer and the definition of the variables are given.

In order to maximize the power density of the transformer, an advanced cooling method, as described in [13], has been applied. With this method, the losses in the windings and the core are transferred via a heat transfer component (HTC) to an additional heat sink for the transformer.

At the beginning of the inner optimization procedure, the degrees of freedom, i.e., the number of independent variables a–e in Fig. 7(a), are reduced. First, the width of the leakage flux path (LFP) e with distributed gap (e.g., the gap is divided into five distributed gaps in Fig. 7) is chosen so that the flux density in this leg is the same as in the middle leg. Second, the width of the winding window c is determined by the optimal thickness of the foils, the number of turns, the copper fill factor, and a fixed mounting space. The optimal thickness of the foils depends on the frequency and the harmonics and can be derived by minimizing the copper losses [14]. By eliminating e and c, only three independent variables a, b, and d are left, which are used for minimizing the transformer volume.

In the next step, first the losses in the windings and the core and then the hot spot temperatures are calculated as function of the three remaining variables. In the optimization algorithm, where the volume is minimized, these functions are used for calculating the hot spot temperatures and keeping them below the maximal allowed operation temperature of the transformer while varying the geometry.

The losses in the different core sections can be calculated by applying the Steinmetz law [15] parameterized (C_m, α, β) with the manufacturer data sheets

$$P_{\mathrm{Core}} = C_m f^{\alpha} B_{\nu,AC}^{\beta} V_{\mathrm{Core},\nu}. \tag{27}$$

There, $V_{\mathrm{Core},\nu}$ is the volume of the considered core section, which can be expressed by the variables a–e.

For analytically calculating the winding losses including the skin and proximity effects, a 1-D approach, as presented in [9], [14], and [18], is applied. Due to the approximately sinusoidal current in the primary winding, only the first and the third harmonics of the current are considered in the loss and optimal foil thickness calculation (cf., Section IV-A1).

The current in the two sections of the secondary winding, however, significantly deviates from a sinusoidal shape in contrast to the resulting secondary resonant current I_S ($= I_{S1} + I_{S2}$ the sum of the currents in the two sections of the secondary).

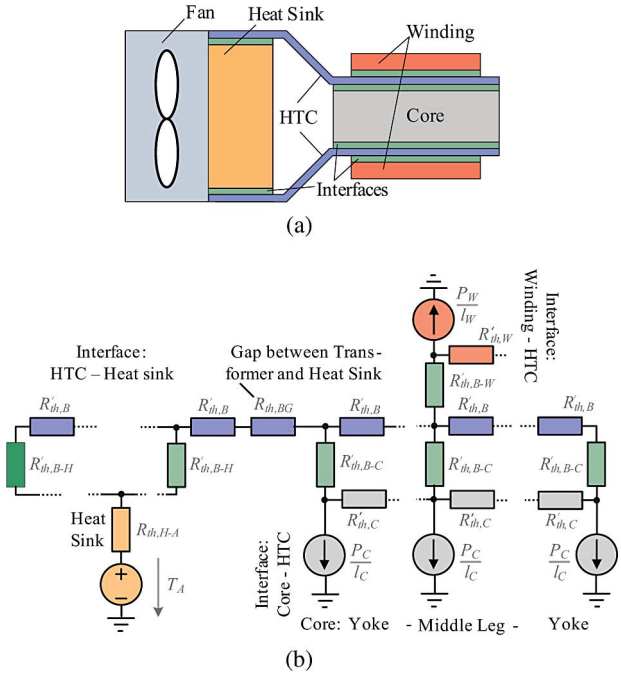

Fig. 8. (a) Cut through middle leg of transformer with cooling system/heat sink shown in Fig. 7. (b) Distributed thermal model of the cooling system shown above with the heat sink on the left-hand side, a gap between heat sink and transformer, and the transformer with winding on the right-hand side.

Therefore, higher harmonics (here up to the 12th harmonic) have to be considered in the loss and optimal foil thickness calculations. There, mainly the height of the winding window d and the mean turn length describe the influence of the geometry on the winding losses.

Due to the high secondary currents, the losses in the secondary winding dominate the windings losses.

With the losses, the temperature distribution in the transformer could be calculated based on the thermal model shown in Fig. 8. This model describes the heat flow from the winding/core via the thermal interfaces and HTC to the heat sink/ambient by distributed thermal resistances (R_{th} per length). The calculation of the temperature profile is based on transmission-line equations, which is described in detail and validated in [13]. There, it also shown that in case of an electrically conductive HTC, the additional losses due to eddy currents are relatively small and

TABLE IV
RESULTING SPECIFICATION OF THE OPTIMIZED 5-KW TELECOM SUPPLY

Volume: 0.49dm^3	**Efficiency: 96.1%**	**Power Density: 10.2kW/dm^3**	
		Transformer	
		• Width	6.4cm
		• Breadth	6.4cm
		• Height	4.0cm
		• Volume	0.21dm^3
		• Flux Density	0.23mT
Operation Point			
• Output Power	5kW	• Output Voltage	54V (48)
• Output Current	92.6A (104)	• Input Voltage	400V
• Nominal Freq.	92.9kHz (90.1)	• Duty Cycle	0.75
Resonant Circuit			
• Series C_S	160nF	• Parallel C_P	120nF
• Series L_S	40μH	• Turns Ratio	7
• Vol. C_s+C_p	3.2cm^3	• Primary Turns	14

the benefits of the improved thermal management outweigh this small disadvantage.

For improving the heat flow within the winding made of foil and also from the winding to the HTC, a thermally conductive insulating material is used [19]. Moreover, thermal grease between the core and the HTC and a cover pressing the winding on the HTC are used. This cover is not shown in Fig. 1 for showing more transformer details.

After the volume has been minimized, it is passed to the global optimization algorithm, where it is used for calculating the system volume and for varying the parameters systematically.

V. RESULTING DESIGN

Based on the presented procedure shown in Fig. 4, a telecom supply with the specification given in Table I has been optimized and the results are presented in the following. The data, the component values, and a photograph of the transformer (with HTC but without winding) of the optimized system are summarized in Table IV, where it could be seen that the aimed power density of 10 kW/dm^3 has been reached, which is a factor 2–4 higher than best-in-class commercial converters, and that the efficiency of the system is 94.5% at rated power. These result for the optimization is based on the following data/limits:

1) core material: N87 from Epcos ($T_{\mathrm{Max}} \leq 115$ °C);
2) winding: foil winding ($T_{\mathrm{Max}} \leq 125$ °C);
3) center tapped secondary winding;
4) MOSFETs: APT50M75 from Microsemi (former APT);
5) rectifier diode: APT100S20 from Microsemi;
6) capacitors C_S and C_P: reference 3.9 nF, 800 V COG series from Novacap;
7) CSPI: 23 (transformer and semiconductor heat sink);
8) maximal junction temperature $T_{j,\max} \leq 140$ °C
9) controller: Lattice MachXO 2280C;
10) gate drive: 4×IXYS IXDN414SI.

A further requirement is the overall height of the supply, which should be below 1 U (≈44 mm), that significantly influences the design of the transformer as well as the cooling system and the layout of the converter system. There, the interconnections must be made as short as possible and any "death air" in the system must be avoided. The final design of the system was obtained by 3-D mechanical constructions using INVENTOR.

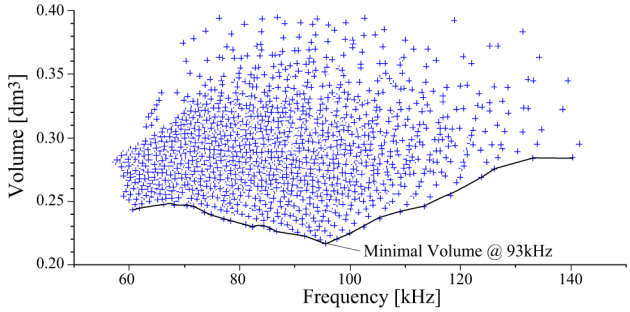

Fig. 9. Volume of the resonant circuit ($C_S + C_P + L_S$ + transformer) for the parameter ranges: C_S = 50–300 nF/C_P = 100–500 nF/L_S = 5–70 μH/N_1 = 14/N_2 = 2.

In the considered optimized power supply, a custom core, which has been determined by the optimization procedure, is applied in order to achieve the maximal possible power density. In case only standard cores are available, the power density would decrease significantly, since the series inductance of the resonant tank is integrated in the transformer resulting in three legs, which approximately have the same cross section in the considered case. With a standard E-core, the center leg has twice the cross section of the two outer legs resulting in large transformer volume and also larger mean turn lengths of the windings.

During the optimization, the volume of the transformer, the heat sink, and the resonant tank components is minimized. There, the volume of the component packages, the gate drive, the auxiliary supply, and the control circuit, which are relatively independent of the operating point, are also considered. Since most telecom dc–dc converters are utilized in combination with a PFC controlling the 400 V input of the dc–dc converter, no EMI filter is considered in the presented optimization. The EMI filter and the PFC converter have been investigated in [20].

In order to judge the sensitivity of the converter volume on the operating frequency, the "Global Optimization Procedure" (bottom box in Fig. 4) has been replaced by three nested for–next loops. In these loops, the component values have been varied within the following range: C_S = 50–300 nF/C_P = 100–500 nF/L_S = 5–70 μH. The result of this is shown in Fig. 9 where each cross marks the system volume for one set of the three variables $\langle C_S, C_P, L_S \rangle$. The turns ratio has been fixed to 14:2 since this results in the smallest overall system volume with the given constraints.

As one can see in Fig. 9, there is a distinct minimum of the volume close to 100 kHz. Increasing the operating frequency leads to a larger system volume since the transformer needs a larger volume due to a significant increase in the required window height d (cf., Fig. 7) because of the HF losses in the windings. Also for a decreasing frequency, the system volume is increasing due to increasing core sizes. There, the constraints

TABLE V
COMPARISON OF THE ANALYTICALLY CALCULATED PARAMETERS WITH SIMULATION AND MEASUREMENT RESULTS

	Calculated	Simulated	Measured
V_{IN}	400.0V	400.0V	400.2V
I_{IN}	13.0A	13.1A	12.97A
P_{IN}	5.20kW	5.24kW	5.19kW
I_P	15.3A	15.1A	15.3A
V_{Out}	54.0V	54.0V	53.4V
I_O	92.6A	92.5A	91.8A
P_{Out}	5.00kW	5.00kW	4.91kW
f_{Sw}	120kHz	114kHz	120.1kHz
D	0.73	0.78	0.85

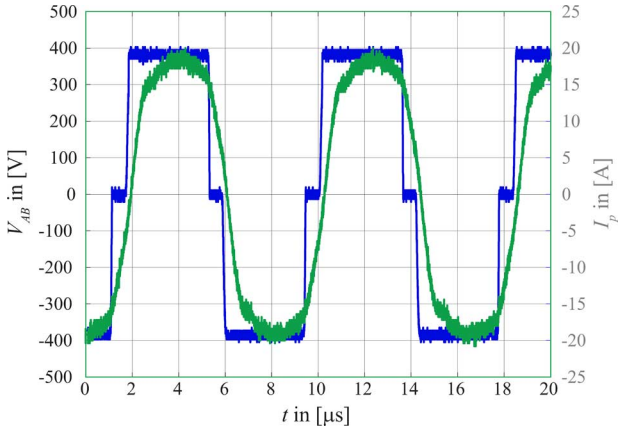

Fig. 10. Measurement results of the resonant tank input voltage V_{AB} and the primary current I_P for $V_{\rm IN} = 400$ V, $I_{\rm IN} = 13$ A, $V_O = 53.4$ V, and $I_O = 91.8$ A.

like overall height, materials, etc., significantly influence the position of the minima.

The related data of the converter system are given in Table IV. The flux density in the transformer core reaches a peak value of 0.23 T at full-load. This results in a relatively high power loss density in the core but due to the low core volume, the overall core losses are just 27 W. The losses in the winding are 5 W for the primary and 14.3 W for the secondary. Due to the indirect cooling via the HTC and the heat sink, the peak temperature in the core is below 115 °C and in the winding below 114 °C at an ambient temperature of 45 °C. For validating the analytical models applied in the optimization procedure, measured values are compared with calculated as well as simulated ones (cf., Table V). The simulation has been performed with SIMPLORER, and more parasitic values are considered than in the analytical models. As one can see in Table V, the analytic models predict the circuit behavior very well. Also, the measured waveforms correspond very well with the theoretical ones, as shown in Fig. 10.

The losses in the four MOSFETs are 73 W and in the two rectifier diodes are 113 W plus dielectric losses and HF losses in the interconnections. In the resonant capacitors, only 0.5 W is dissipated due to the low loss factor of the ceramic capacitors. Summing up all the losses results in approximately 287 W overall losses for the resonant converter at full-load.

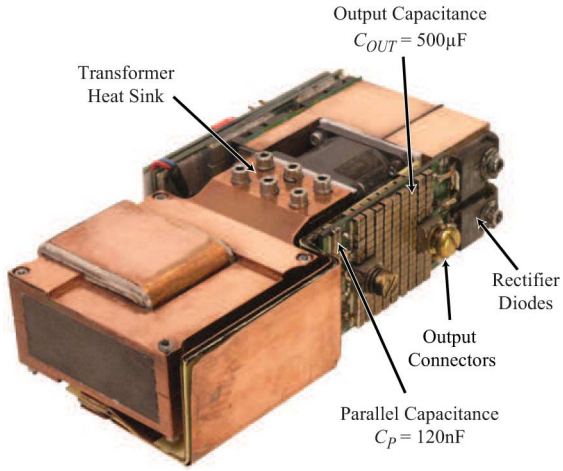

Fig. 11. Backside view of the 5-kW, 10-kW/dm^3 telecom power supply.

In Fig. 11, the backside of the test setup with the two rectifier diodes, the parallel capacitor, and the output capacitor is shown.

VI. CONCLUSION

In this paper, the design of a 5 kW, 1 U series–parallel resonant dc–dc converter for telecom applications has been presented. To meet the demands of high efficiency and low volume resulting in a high power density, an automatic optimization procedure has been developed and is explained in detail in this paper.

In the optimization procedure, the model of the converter, with capacitive output filter, is based on extended fundamental frequency analysis.

Furthermore, the control structure, the losses in the semiconductors as well as the thermal and magnetic behavior of the integrated transformer, whose geometry is also optimized within the procedure, are included. With the presented optimization procedure, a 5 kW dc–dc converter with a power density of more than 10 kW/dm^3 has been developed. For validating the analytical models, a prototype of the converter has been constructed and measurements have been presented in this paper.

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