Double-stage Gate Drive Circuit for Parallel Connected IGBT Modules

D. Bortis, P. Steiner, J. Biela and **J. W. Kolar**
Power Electronic Systems Laboratory, ETH Zurich
Physikstrasse 3, 8092 Zurich, Switzerland

ABSTRACT

Solid state modulators are increasingly being used in pulsed power applications. In these applications IGBT modules must often be connected in parallel due to their limited power capacity. In a previous paper, we introduced a control method for balancing the currents in the IGBTs. In this paper, we investigate techniques to minimize the modules' rise and fall times, which can positively impact the modulator's output pulse parameters, which in turn must meet the application's specifications. Further, a reduction in rise and fall times lowers switching losses and thus increases the modulator's efficiency. To reduce the voltage rise time of the pulse without increasing the maximal over-voltage of the parallel IGBTs we have investigated a double-stage gate driver with protection circuits to avoid over-voltages and over-currents. Additionally voltage edge detection has been implemented to improve current balancing. Our measurement results reveal the dependency of the rise-time and turn-off losses on the design parameters of the gate drive. We show that our design achieves a 62% reduction in the turn-off rise time, and a 32% reduction in the turn-off losses.

Index Terms — **Gate drive circuit, turn off behavior, switching losses, protection circuits, parallel connected IGBT modules, power modulator.**

1 INTRODUCTION

MANY pulsed power applications place stringent requirements on the rise/fall times. In solid state power modulators, the design of the gate drive circuit can strongly influence the switching behavior and losses [1, 2]. At high power levels, where IGBT modules must be connected in series or in parallel, simultaneous switching must be guaranteed in order to limit the device voltage and distribute the current equal. In [3] we presented an active gate control for current balancing in parallel IGBT modules, and a current measurement circuit. In this paper we investigate the voltage switching times of the device, and introduce a modified gate drive circuit which significantly improves the switching behavior (synchrony) and losses, and show that our design compares favorably against existing commercially available gate drives. Furthermore, the new design ensures simultaneous switching transients of the parallel IGBT modules.

With conventional gate drive circuits (single-stage driver) the switching losses of the IGBT modules are mainly generated during turn off, because, as the turn off time approaches zero over-voltages are generated by parasitic inductance in the commutation path [1]. Therefore, a high gate resistance is needed during turn off, to decrease the current slope, and thereby limit the resulting over-voltage [4, 5]. This results in excessively high turn off losses.

For reducing the turn off time and corresponding switching losses without increasing the over-voltage, multistage driver concepts [1, 2, 6, 7] have been proposed for smaller IGBT devices. These vary the value of the turn off gate resistor during the turn off transient. Based on this concept and results presented in [3], we designed a new double-stage driver for parallel IGBT modules for a 20 MW, 5µs solid state power modulator, which is depicted in Figure 1.

To ensure safe operation of the IGBT modules, collector-emitter-voltage monitoring and protection circuits have been introduced to prevent going over voltage or over current. The monitored IGBT voltages v_{ce} are also used to improve the

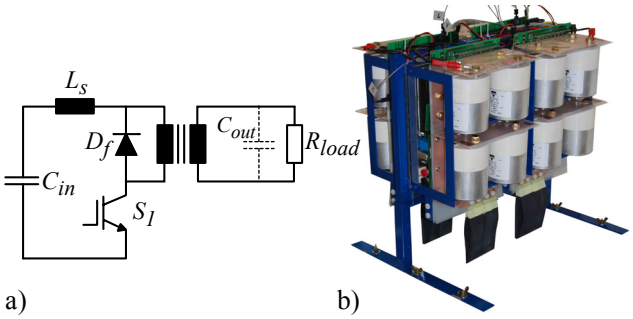

Figure 1. a) Schematic of the solid state pulsed power system. **b)** 20MW, 5µs solid state pulse modulator with four parallel connected IGBT modules.

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Table 1. Specification of the 20MW, 5µs pulse modulator with four parallel connected IGBT modules.

DC Link Voltage V_{dc}	1000 V
Output Voltage V_{out}	200 kV
Pulse Duration T_{pulse}	5 µs
Output Power P_{out}	20 MW
Repetition Frequency f_{rep}	200Hz
Turns ratio	1:200

synchrony of the switching transients for magnetically coupled IGBT modules. In contrast to directly connected parallel IGBTs, v_{ce} for the magnetically coupled IGBTs can differ in time despite the currents in the IGBTs being equally distributed.

Finally, we have introduced voltage edge-detection circuits. These improve current balancing, and increase the synchrony of the voltage transients between the magnetically coupled IGBT modules compared to the control method presented in [3].

The basic operating principle and the block diagram of the proposed double-stage driver are explained in Section 2. The over-voltage and over-current protection implementations, the combination of the gate driver with an improved zener clamping circuit, and the current balancing by means of the voltage edges for magnetically coupled IGBT modules is discussed in Section 3. In Section 4**,** experimental results for the double-stage gate drive and the dependency of the rise-time and turn-off losses on the gate resistor are presented. In addition to the shorter rise times and the smaller turn off losses, the turn off delay can be drastically reduced with the proposed double-stage driver. Furthermore, we evaluate the impact on the rise-time and turn-off losses for gate drives consisting of a single stage, a double-stage, and a double-stage with improved zener clamping for the modulator system shown in Figure 1.

2 MULTI-STAGE DRIVER

Many solid-state pulsed- power applications require fast rise/fall times. Furthermore, the switching losses are reduced by fast switching transients. Consequently, powerful gate drives with low resistance and inductance are required to quickly switch the devices on and off.

At turn on the falling time and switching losses can be minimized by decreasing the external gate resistor. However, at turn-off a high switching speed with high dv_{ce}/dt and high di_c/dt would result in large over-voltages v_{ov} due to the parasitic inductance L_s of the commutation path (cf. Figure 1a).

$$v_{ov} = L_s \frac{di_c}{dt} \qquad (1)$$

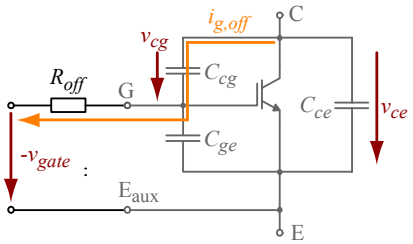

Figure 2. Influence of the gate resistor R_{off} on the current and voltage slope di_c/dt respectively dv_{ce}/dt.

The over-voltage v_{ov} could be reduced by minimizing the stray inductance L_s of the commutation path, i.e. the series inductance of the input capacitor, the bus bar, and the power module. However, in the existing system the total inductance is already smaller than 40nH and is mainly determined by the components, which can not be influenced by the system designer. Alternatively, the current slope di_c/dt / or the voltage slope dv_{ce}/dt could be decreased with a larger gate resistor R_{off} (cf. Miller-effect and Figure 2), resulting in higher turn off losses E_{off} due to the slower turn off transient [5]. To avoid the limitation of the di_c/dt, double-stage drivers for IGBT modules have been proposed [1, 2, 4, 7]. By utilizing more than two stages a further refinement of the turn off control is possible [6]. In the following the operating principle of the proposed double-stage driver for high power modules is explained.

2.1 OPERATION PRINCIPLE

Generally, multi-stage drivers split the turn-off transient into individual successive switching sections and apply individual gate resistors for controlling the rate of gate discharge or the dv_{ce}/dt depending on the IGBT voltage v_{ce}.

The proposed double-stage driver consists of a low and high resistive turn-off stage splitting the switching operation in two different switching sections, as depicted in Figure 3.

In the first section, during T_1, the IGBT voltage v_{ce} is below the reference voltage v_{ref} and the gate is quickly discharged to achieve a short turn off time and small switching losses. Consequently, both stages S_1 and S_2 are turned on during T_1, what results in a turn off resistor $R_{off,1}||R_{off,2}$ (cf. Figure 3). As soon as the IGBT voltage v_{ce} exceeds the specified voltage level v_{ref} at t_1, the low-resistance stage S_1 is turned off and the gate will be discharged through the high-resistance stage S_2 with $R_{off,2}$ during T_2. Due to the Miller capacitance, the change of the gate resistor from $R_{off,1}||R_{off,2}$ to $R_{off,2}$ results in a decreased current/voltage slope (cf. Figure 3b). The reference voltage v_{ref} is

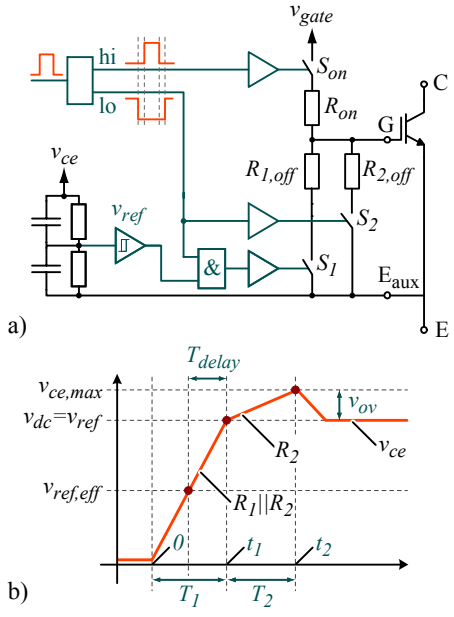

Figure 3. a) Block diagram of the double stage driver circuit and **b)** resulting voltage and current waveform of v_{ce} and i_c during double-stage turn off.

usually set to a value close to the dc-link voltage v_{dc} , to achieve a fast turn-off over the highest possible voltage range, while still limiting the over-voltage. In principle however, the reference level could be set to a lower voltage reference v_{ref} , leading to lower limit on the voltage.

Due to the delays in the comparator and driver circuit (T_{delay}), the effective reference voltage $v_{ref,eff}$ has to be set below the dc-link voltage v_{dc} to achieve a change of the gate resistor at $v_{ce} \approx v_{dc}$. To minimize this effect, the signal delay T_{delay} has to be minimized to guarantee a stable performance for various operating conditions. In the proposed system the signal delay T_{delay} from detection to driver output of the implemented hardware is approximately 40ns.

The IGBT voltage v_{ce} is monitored with a balanced ohmic-capacitive voltage divider, where the overstepping of the reference voltage v_{ref} is detected with a high speed comparator. There, attention has to be paid to the layout to keep the signal disturbances on a minimum level. The reference voltage v_{ref} for the high speed comparator can be adjusted with a potentiometer to an arbitrary value. For more complex systems, where an adjustment also during operation is needed, the reference could be set with a DSP via a digital analog converter. With a fixed reference voltage the complexity of the signal logic for the double-stage driver can be kept low (cf. Figure 3).

3 PROTECTION CIRCUITS

In normal operation the double-stage driver ensures a limitation of the over-voltage to safe values. However, in fault conditions such as over-current (which can result in over-voltage), the IGBT modules must be protected by additional circuits. Either passive snubber circuits [1, 8, 9], which generate high losses, or protection circuits which influence the gate voltage, such as zener clamping [1, 8, 9, 10], can be used. Therefore, the proposed double-stage gate driver is extended by an over-voltage and an over-current protection.

3.1 OVER-VOLTAGE PROTECTION

A well known and commonly applied over-voltage protection is the zener clamping, which directly influences the gate voltage. A high-voltage, or several series-connected low-voltage zener diodes are inserted between the collector and gate connections to realize a control loop as shown in Figure 4a.

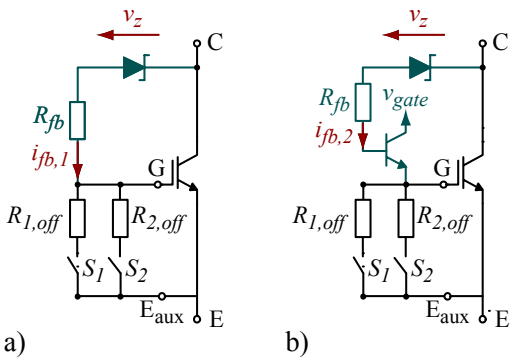

Figure 4. Implementation of **a)** the conventional zener clamping circuit and **b)** the improved zener clamping circuit.

As soon as the IGBT voltage v_{ce} exceeds the zener voltage v_z, a current determined by the zener characteristic flows to the gate. This current recharges the gate capacitance or reduces its discharge rate, depending on the value of the turn off resistor $R_{off,2}$ Additionally, to control the influence/value of the feedback current through the zener diodes, a series resistor R_{fb} is usually inserted (cf. Figure 4a).

In the combination of the zener clamping with the double-stage driver, the current $i_{fb,1}$ flowing through the zener diodes can be limited to small values, due to the high resistance value of the gate driver during T_2. Therefore, the power dissipation in the zener clamping circuit can be considerably reduced compared to a conventional single-state driver with a small value for the turn-off resistor. To further reduce the feedback current $i_{fb,1}$ flowing through the zener clamping circuit a NPN bipolar transistor for current amplification is inserted, as shown in Figure 4b.

A bipolar transistor can reduce the losses of the zener clamping circuit further, so that the losses become negligible. This allows the zener clamping circuit to be applied for repetitive switching operation and is no longer limited to protection of the IGBT. By combining the double-stage driver and the improved zener clamping for normal operation it is possible to reduce the switching time as well as the switching losses for a given over-voltage. Furthermore, the zener voltage v_z is almost constant due to the low current $i_{fb,2}$ through the zener diodes. This allows a better prediction of the resulting over-voltage $v_{ce,max}$, so that the devices can be better utilized.

For safe operation, the double-stage driver must change to the high gate-resistor value, before a zener current i_{fb} is flowing, which starts when v_{ce} exceeds v_z. The zener clamping circuit with the appropriate series resistor R_{fb} will keep the over-voltage below the maximum allowed over-voltage $v_{ce,max}$. In order to achieve a high di_c/dt the over-voltage has to be clamped to the maximum allowable over-voltage $v_{ce,max}$ as long as possible.

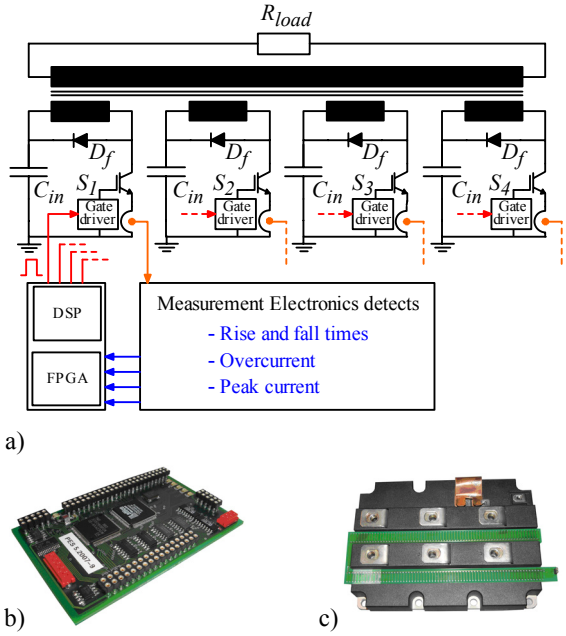

Figure 5. a) Over-current protection loop with **b)** the applied DSP-board and **c)** PCB Rogowski coil.

3.2 OVER-CURRENT PROTECTION

We consider pulsed-power applications which require output power of 20 MW (20 kA at 1 kV). Due to the high power rating four IGBT modules must be connected in parallel. In Figure 5, the schematic of the realized solid-state modulator with its four magnetically paralleled pulse generator branches is shown. Additionally, the block diagram of the active gate control, which is described in the next section, is illustrated. Each branch consists of a storage capacitor C_{in}, an IGBT module S_i, a freewheeling diode D_f, and a primary winding. The control loop of the active gate control, which is presented in [3] (cf. Figure 5) and shortly discussed in the next section, ensures symmetrical current distribution between magnetically and directly connected IGBTs. It embodies the gate drive circuit, which is presented in this paper, a PCB Rogowski coil to measure the current in each IGBT module, and measurement electronics for detecting the rising and falling edges (time instant, where 50% of the collector-emitter voltage is reached) as well as the peak values of the current pulses. Finally, the control loop of each branch is closed with one control unit (DSP-Board) for all four IGBT modules.

Because of this simple and low cost current measurement circuit, where also over-currents can be detected, no additional over-current protection circuit has to be implemented on the gate drive unit. In case of an over-current, which is detected by the measurement electronics, the IGBTs are turned off immediately by the DSP and the over-voltage is limited by the gate drive as presented above.

This protection circuit has the advantage that the current is always monitored, i.e. also during the switching transients. Most of the circuits presented in the literature, as for example in [2, 11, 12], just monitor the IGBT current in a specific interval of the switching cycle. For example, circuits monitoring the desaturation of the IGBT can only detect over-currents during the interval where the IGBT module is fully turned on, but not, for example, when the IGBT is turned on and the load has a short-circuit or the current is too high.

3.3 CURRENT BALANCING FOR PARALLEL CONNECTED IGBT MODULES

As already mentioned, in the considered application four IGBT modules must be connected in parallel as a result of the high output power (cf. Figure 5). Due to IGBT tolerances, system asymmetries and variation in propagation delays a joint trigger signal for the parallel IGBT modules usually leads to an unbalanced current distribution between the modules. In [3], an active gate signal control was presented, where a balanced current distribution between the IGBT modules can be achieved by detecting the edge times of the currents in the IGBT modules with the described control loop of Figure 5, and to appropriately shift the turn on and off times of each IGBT for the next pulse. This results in an equal current distribution between the magnetically or directly connected IGBT modules. In case of directly connected IGBT modules, the same collector-emitter voltage is applied to all IGBT modules and therefore only the described current edge control has to be implemented.

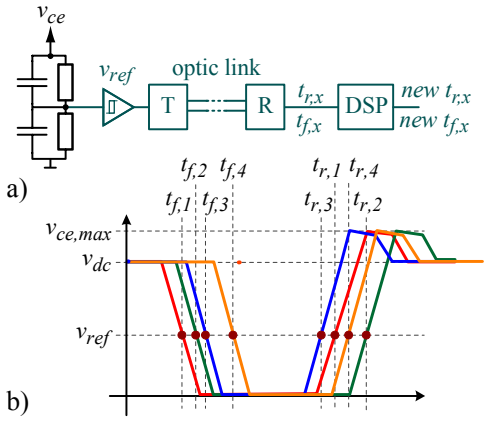

Figure 6. a) Signal processing and **b)** schematic of the v_{ce} edge detection for switching synchronisation.

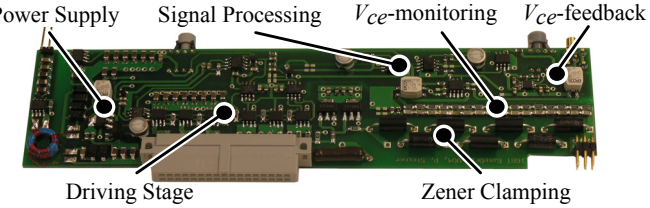

Figure 7. Prototype of the proposed multi-stage gate drive.

However, due to the circuit behavior, which is especially influenced by the pulse transformer with its parasitic inductances, for magnetically connected IGBT modules synchronous edge times of the collector-emitter voltage v_{ce} can not be guaranteed even though the edge times of the currents are synchronized. Therefore, an additional control loop for the voltage edges has to be implemented, which results in synchronous collector-emitter voltage transients for all IGBT modules.

One possibility to synchronize the voltage transients is to introduce time offsets to the gate signals in the software. However, the time differences of the current and voltage transients of the IGBTs are considerably influenced, especially at turn off, by the operating point v_{dc} of the modulator and the temperature of the IGBTs. Therefore, also the time offsets depend on these parameter fluctuations. Consequently, in order to achieve synchronous edge times in current and voltage, either a table with time offsets for all operating points and depending on all influencing parameters is needed, or the IGBT voltages v_{ce}, which are already monitored for over-voltage protection and double-stage turn off, are used to detect the edge times $t_{f,1}$-$t_{f,4}$ and $t_{r,1}$-$t_{r,4}$ (cf. Figure 6) of the IGBT voltage v_{ce}.

Hence, the voltage edge-times can be used to calculate the appropriate time offsets of the current edge control for each operating point. The turn on and off times of each IGBT are controlled in a combined control structure, where the time offset will be adjusted out of the voltage edge times as soon as the current edge times are regulated.

As already mentioned, in general a parallelization of the IGBTs could be implemented using only voltage edge control. However, in the considered system the turn off behavior of the IGBT and the voltage rise time is heavily influenced by the transformer and the klystron load due to the parasitic capacitance C_{out} (cf. Figure 1). Therefore, the parallelization is mainly controlled by the current edge control, and the voltage edge

control only adjusts the time offsets after a balanced current distribution is achieved. Additionally, the combination of current and voltage edge control improves the reliability of the system, because the time instant of each pulse edge is always measured in the current and voltage waveform, whereby failures due to signal distortion in the measurement electronics, i.e. wrong edge time detection, can be minimized.

4 EXPERIMENTAL RESULTS

For testing the proposed double-stage gate drive the prototype shown in Figure 7 has been built and measurements have been performed with FZ2400R17KF6C_B2 IGBT modules made by Eupec. Pulse currents of 5800A per IGBT module at 1000 V for 5 µs were generated with the power modulator depicted in Figure 1.

To compare the different turn off strategies: single-stage, double-stage, and double-stage with zener clamping, measurements of the voltage rise time and the turn off losses at a maximum over-voltage of 1230V have been performed. The reference voltage for the double-stage turn off was set to v_{ref}= 1000V.

In Figure 8 the voltage and current waveforms v_{ce}, v_{ge} respectively i_c, $i_{off,1}$ and $i_{off,2}$ during double-stage turn off for $R_{off,1}$ = 0.85 Ω and $R_{off,2}$ = 510 Ω are shown. There, during the first section T_1 the current $i_{off,1}$ is flowing through both turn off resistors $R_{off,1}$ and $R_{off,2}$, with the main part of approximately 10 A is flowing through $R_{off,1}$. As soon as the IGBT voltage v_{ce} exceeds the reference voltage v_{ref}, the low resistive stage with $R_{off,1}$ is turn off and during T_2 the gate is discharged through $R_{off,2}$ with $i_{off,2}$ ≈ 10-15 mA.

In Figure 9 the turn off losses E_{off}, the rise time t_{rise} of v_{ce} (10%-90%) and the turn off delay time $t_{off,delay}$ of the double-stage driver for different turn off resistors R_1 and R_2 are given. Additionally, the according values for the single-stage driver are shown.

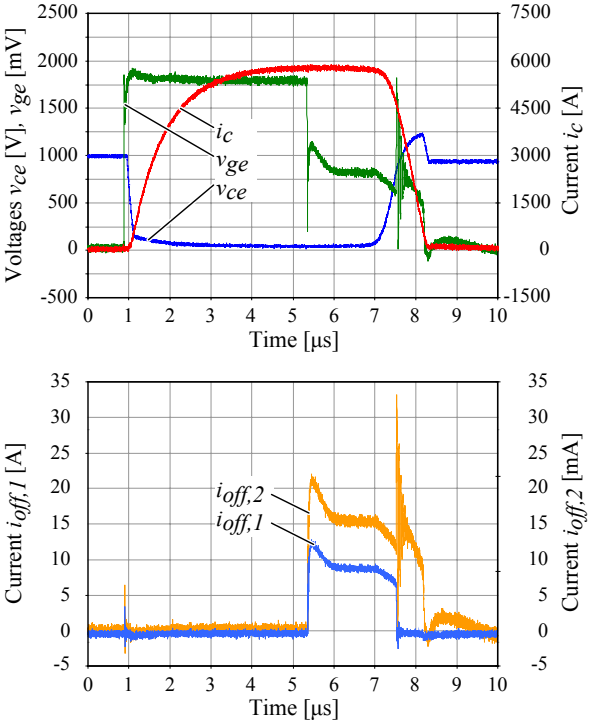

Figure 8. a) Voltage and current waveforms v_{ce}, v_{ge} respectively i_c and **b)** the according gate current $i_{off,1}$ and $i_{off,2}$ during double-stage turn off.

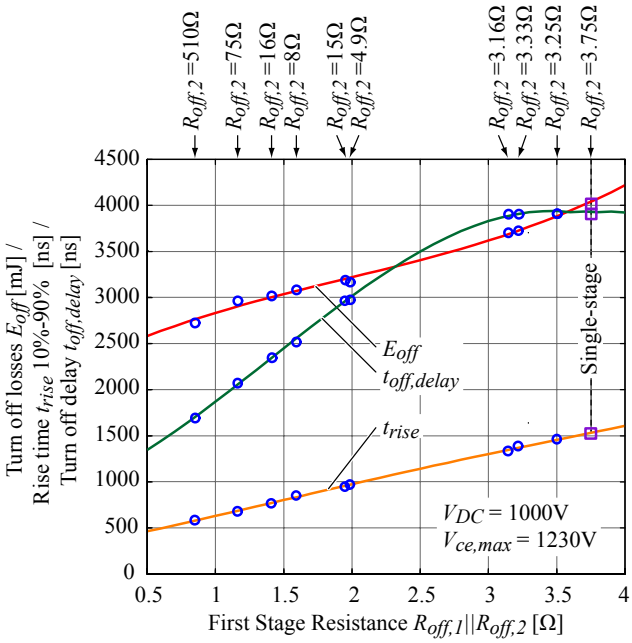

Figure 9. Turn off losses E_{off}, rise time t_{rise} of v_{ce} (10%-90%) of the double-stage driver and dependency of the turn off delay $t_{off,delay}$ for different $R_{off,1}||R_{off,2}$ and $R_{off,2}$ values and for the single-stage driver.

As expected, a smaller turn off resistor $R_1||R_2$ in the first stage leads to a faster rise time t_{rise} of v_{ce}, which results in reduced turn off losses E_{off}. To keep the maximum voltage $v_{ce,max}$ below 1230 V the resistance of the first stage of the double-stage driver must be bigger or equal 0.85 Ω. There, with $R_1||R_2$ = 0.85 Ω, the minimal turn off losses for the FZ2400R17KF6C_B2 IGBT module are achieved, where E_{off} is 2724mJ and t_{rise} is 580ns.

With a single-stage driver a turn off resistance of 3.75 Ω has to be used to keep the IGBT voltage v_{ce} below 1230 V. There, the measured turn off losses E_{off} are 4014 mJ and the rise time is 1.530 µs. Therefore, with a double-stage driver the rise time t_{rise} and the turn off losses E_{off} can be reduced by 950µs (62%) respectively by 1290 mJ (32%), which equals 258 W per IGBT module at a pulse repetition frequency of 200 Hz.

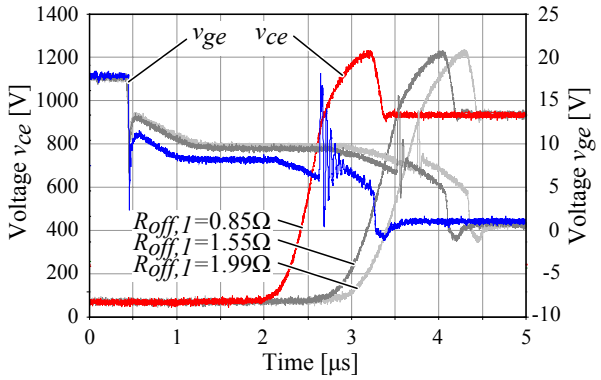

Figure 10. IGBT voltage v_{ce} and appropriate gate voltage v_{ge} for $R_{off,1}||R_{off,2}$ = 0.85 Ω, $R_{off,1}||R_{off,2}$ = 1.55 Ω and $R_{off,1}||R_{off,2}$ = 1.99 Ω.

Additionally, for faster turn off times t_{rise} also the turn off delay $t_{off,delay}$ can be decreased. In Figure 10 the IGBT voltage v_{ce} and the corresponding gate voltage v_{ge} for three different turn off gate resistors are shown. The turn off delay $t_{off,delay}$ decreases with smaller turn off gate resistors $R_{off,1}$ during double-stage turn off, which shows for a turn off resistor $R_{off,1}||R_{off,2} \leq 3\ \Omega$ an almost proportional behavior as can be seen in Figure 9. For $R_{off,1}||R_{off,2} > 3\ \Omega$ the turn off delay $t_{off,delay}$ stays almost constant.

To further improve the turn off time t_{rise}, the double-stage driver can be combined with the zener clamping circuit. The zener clamping voltage was set to 1100 V and the series resistor R_{fb} was adjusted to keep the over-voltage below 1230V, in order to have a comparable utilization of the IGBTs for the three gate drives.

In Figure 11 the voltage and current waveforms v_{ce}, v_{ge} respectively i_c and $i_{fb,2}$ during double stage turn off in combination with the improved zener-clamping for $R_{off,1} = 0.33\ \Omega$, $R_{off,2} = 20\ \Omega$ and $R_{fb,1} = 10\ \text{k}\Omega$ are shown. As soon as the IGBT voltage exceeds the breakdown voltage v_z of the zener diode, the current $i_{fb,2}$ through the zener path is approximately constant, which results in an recharging of the gate. Afterwards, when the IGBT voltage v_{ce} falls below v_z, the zener diode will change into the blocking state again and the gate is discharge through $R_{off,2}$. Additionally, due to the parasitic capacitance in the zener path and the fast voltage slope dv_{ce}/dt during turn on a negative current peak of $i_{fb,2}$ can be measured.

In Figure 12 the turn off losses E_{off} and the resulting maximum IGBT voltage $v_{ce,max}$ of the improved zener clamping with $v_z = 1100$ V and $R_{off,1} = 0.33\ \Omega$ for different series resistors R_{fb} are shown. As expected, the turn off losses E_{off} will decrease, if a higher maximum IGBT voltage $v_{ce,max}$ is

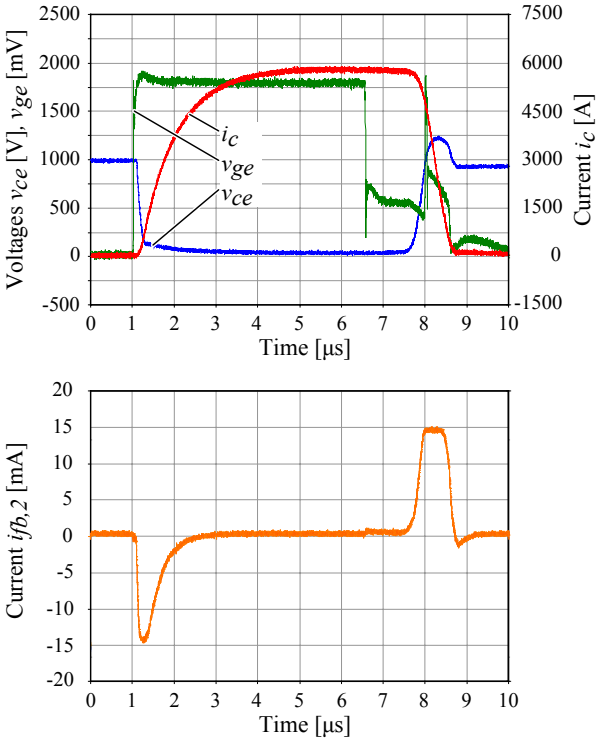

Figure 11. a) Voltage and current waveforms v_{ce}, v_{ge} respectively i_c and **b)** the according gate current $i_{off,1}$ and $i_{off,2}$ during improved zener clamping.

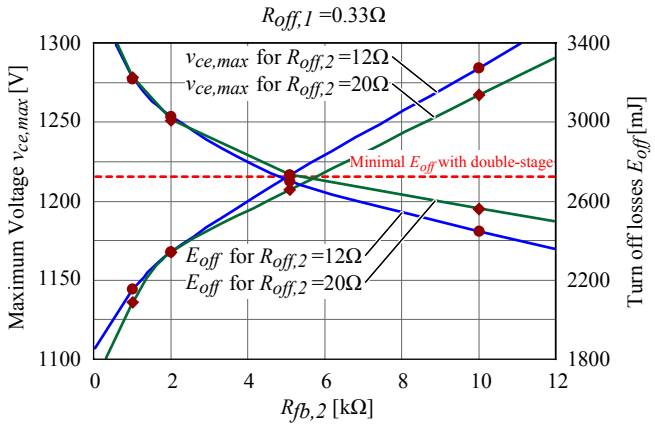

Figure 12. Turn off losses E_{off} and $v_{ce,max}$ of the improved zener clamping for different $R_{fb,2}$.

allowed. Accordingly, the feedback current $i_{fb,2}$ decreases from 160mA for $R_{fb,2} = 1\ \text{k}\Omega$ to 33 mA for $R_{fb,2} = 10\ \text{k}\Omega$, whereas the voltage $v_{Rfb,2}$ increases from 160 V to 330V. For the improved zener clamping with $v_{ce,max} = 1230$ V, $R_{off,2} = 12\ \Omega$ and $R_{fb,2} = 5.1\text{k}\Omega$ the turn off losses E_{off} are 2704mJ, which are approximately equal to the minimal achievable losses with the double-stage driver. However, the rise time can be further reduced to 360ns. Additionally, the turn off delay can be reduced to $t_{off,delay} = 1100$ ns.

Due to the current amplification of the introduced bipolar transistor, the peak power in the conventional zener clamping circuit of 36.5 kW can be reduced to 200 W for the improved zener clamping. This significantly lowers the stress of the zener diodes. Also the power loss of 7.2 mJ (1.44W at 200 Hz) in the diodes is reduced to 46 µJ (9.2 mW at 200 Hz).

In Figure 13 the voltage waveforms v_{ce} for the different turn off strategies are shown. There, the fastest rise time can be achieved with the combination of double-stage driver and improved zener clamping. The double-stage is only slightly slower, and results in slightly higher turn off losses than the combination with improved zener clamping.

In addition to the switching transients, the current balancing and the synchrony of the voltage transients have been tested.

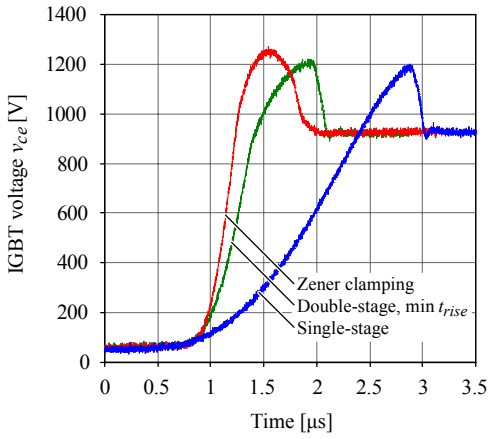

Figure 13. Voltage v_{ce} during turn off for **i)** single-stage driver, **ii)** double-stage driver with minimal turn off losses E_{off}, **iii)** double-stage driver with minimal rise time t_{rise} and iv) driver with combination of double-stage and zener clamping).

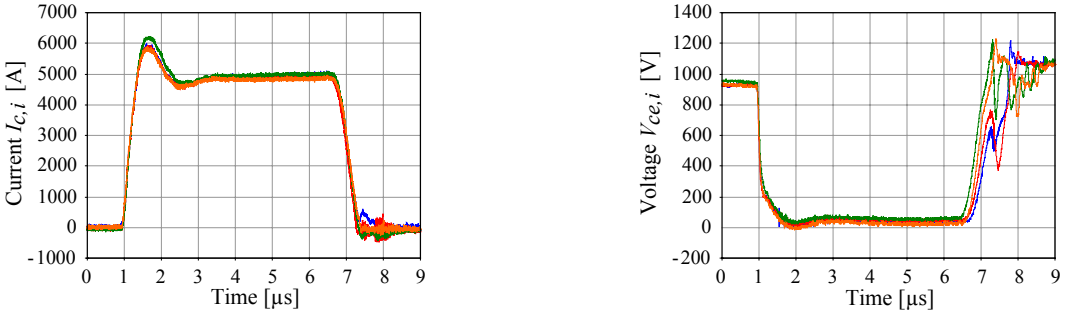

Figure 14. Current and voltage waveforms of the four parallel connected IGBT modules for the active gate control, as described in [3], without any time offsets and v_{ce} = 1000V.

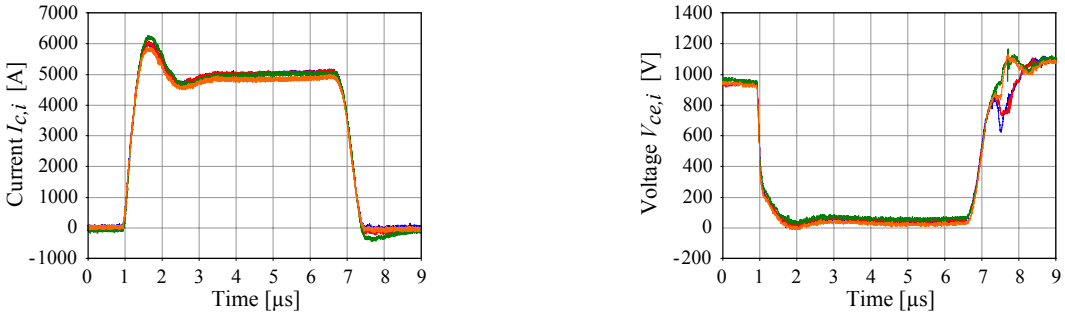

Figure 15. Current and voltage waveforms of the four parallel connected IGBT modules for the active gate control, as described in [3], with additional time offsets and v_{ce} = 1000 V.

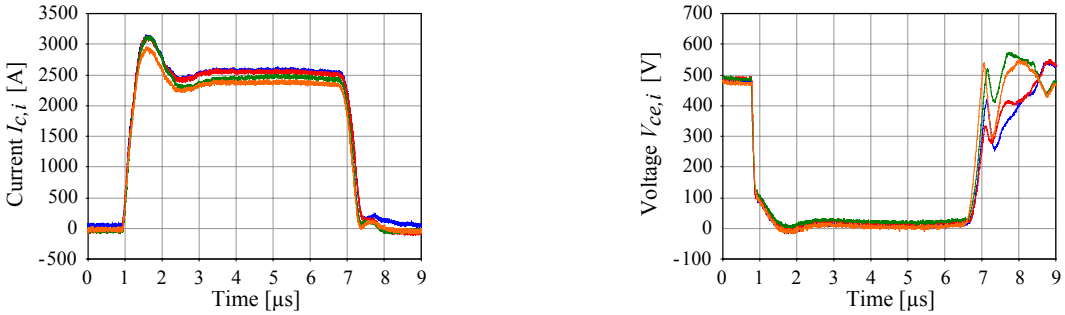

Figure 16. Current and voltage waveforms of the four parallel connected IGBT modules for current edge control with constant time offsets and v_{ce} = 500 V.

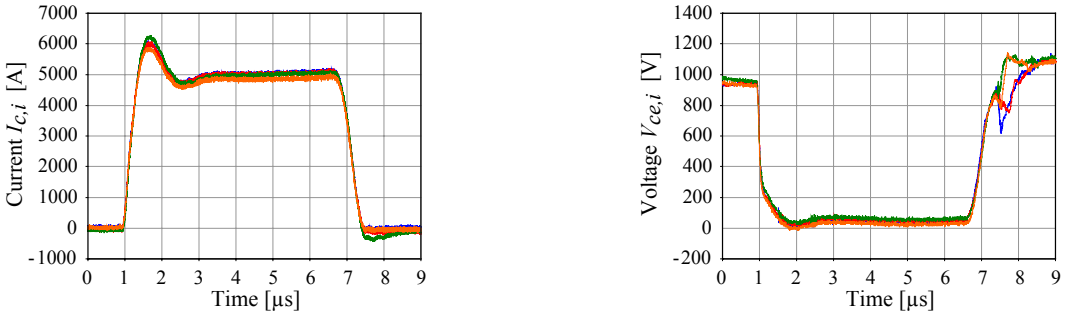

Figure 17. Current and voltage waveforms of the four parallel connected IGBT modules with current and voltage edge control for v_{ce} = 1000 V.

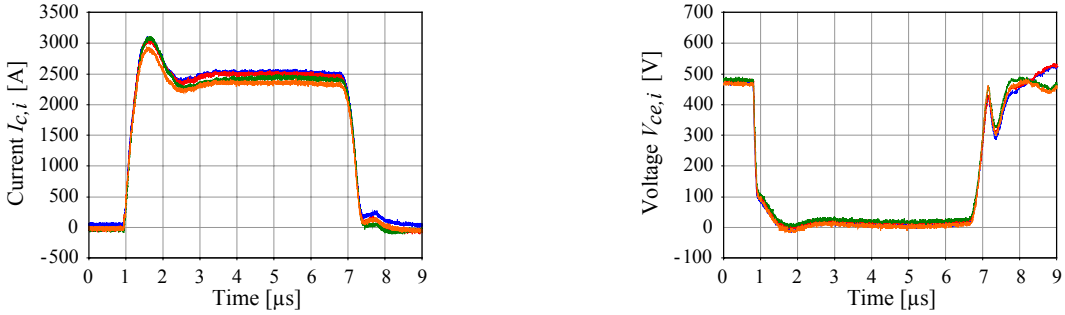

Figure 18. Current and voltage waveforms of the four parallel connected IGBT modules with current and voltage edge control for v_{ce} = 500 V.

active gate control (described in [3]), without any time offsets and with an input voltage of v_{dc} = 1000 V are shown. Although the edge times of the currents are synchronized, a variation in the voltage transients, especially at turn off, is measured.

Afterwards, additional time offsets have been introduced in the software, whereby synchronous voltage transients could be achieved (cf. Figure 15). However, as already mentioned, the time offsets are considerably influenced by the operating point/pulse voltage, which was reduced to v_{ce} = 500 V (cf. Figure 16).

In Figure 17 and 18 the current and voltage waveforms for the proposed combined control structure for the two pulse voltages 1000 V and 500 V are shown. Due to the additional detection of the voltage edge times the time offsets can be adjusted depending on the operating point, which results in balanced IGBT currents and synchronous voltage transients of the magnetically parallel connected IGBTs.

5 CONCLUSION

In this paper a compact and cost efficient double-stage gate driver for parallel high power IGBT modules in power modulator systems is presented. Besides the improved turn off behavior and current/voltage balancing, the gate drive also includes an over-current and an over-voltage protection.

With the proposed double-stage gate driver and the FZ2400R17KF6C_B2 IGBT module made by Eupec we have achieved a reduction of 62% in the turn-off rise-time and a 32% reduction in the turn-off losses, when compared to a single stage driver. The maximal allowed collector-emitter voltage was limited to 1230 V for both drivers. A further reduction of the rise time of 14% was achieved by combining the double-stage gate drive with an improved zener clamping circuit.

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Dominik Bortis (S'06) was born in Fiesch, Switzerland on 29 December 1980. He studied electrical engineering at the Swiss Federal Institute of Technology (ETH) Zurich. During his studies he majored in communication technology and automatic control engineering. In his diploma thesis he worked with the company Levitronix, where he designed and realized a galvanic isolation system for analog signals. He received the M.Sc. degree in 2005, and he has been a Ph.D. student at the Power Electronic Systems Laboratory, ETH Zürich, since 2005.

Patrick Steiner was born in Biel, Switzerland on 25 May 1983. He started his Bachelor degree in electrical engineering at the ETH Zurich in 2003, which he finished in 2008. There, he focused on high voltage electronics and mechatronic systems. Since then he is working on his Masters degree in biomedical engineering at the ETH Zurich.

Juergen Biela (S'04) studied electrical engineering at the FAU Erlangen, Germany. During his studies he dealt in particular with resonant dc-link inverters at the Strathclyde University, Scotland and the active control of series connected IGCTs at the Technical University of Munich. After he had received his diploma degree with honours from FAU Erlangen in 2000, he worked on inverters with very high switching frequencies, SiC components and EMC at the research department of A&D Siemens, Germany. In 2002 he was a Ph.D. student at the PES, ETH Zurich and since January 2006 he has been a Post doctoral Fellow.

Johann W. Kolar (M'89-SM'02) studied industrial electronics at the University of Technology Vienna, Austria, where he also received the Ph.D. degree (summa cum laude). From 1984 to 2001 he was with the University of Technology in Vienna, where he was teaching and working in research in close collaboration with industry. He has proposed numerous novel converter topologies, e.g., the VIENNA Rectifier and the Three-Phase AC-AC Sparse Matrix Converter concept. Dr. Kolar has published over 200 scientific papers in international journals and conference proceedings and has filed more than 50 patents. He was appointed Professor and Head of the Power Electronics Systems Laboratory at the ETH Zurich in 2001.