Design of a Multi-Cell, DCM PFC Rectifier for a 1mm thick, 200W Off-line Power Supply – The Power Sheet

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Abstract

For applications like LED lightning, flat screens, mobile electronics or smart surfaces converter systems with extreme aspect ratios are increasingly under investigation. Many of these systems include an AC-DC rectifier as mains interface with an input voltage of 230Vac and an output voltage of 400Vdc. In this study the design of an ultra-flat 200W PFC rectifier with a thickness of 1mm and a footprint similar to an A4 paper is presented. Due to the low profile components have to be integrated in the PCB which results in several limitations for the design of the devices. Designs for integrated inductors and transformers are discussed and the state of the art of integrated capacitors is presented. The integration of active switches is particularly important since the heat transfer has to be performed through the PCB. The paper shows that a distributed topology with soft switching is advantageous to meet the limitations of the components. This leads to distributed losses as well as to smaller inductances since the transmitted power is divided.

1 Introduction

Converter systems with extreme aspect ratios are increasingly under demand in industry and research for applications like LED lightning, flat screens, mobile electronic or smart surfaces [1], since a built-in solution of power unit in the housing could be achieved. Starting about two decades ago, the miniaturization and integration of power electronic systems have emerged [2]. At the beginning the main focus of investigations lay on inductive-capacitive component integration (LTCC). There, capacitors have been integrated in the transformer's winding using ceramic materials. However, due to the high manufacturing effort and due to different temperature coefficients of materials which causes the bridle ceramic to crack this technology has a limitation.

Another approach is to integrate the components into the PCB. Conventional power converters consist of several discrete components which are assembled on a PCB. To achieve extreme aspect ratios the PCB not only has to provide mechanical stability and the interconnections but also include electrical and thermal functionalities. Due to the low profile, the performance of inductive, capacitive and active devices which have to be integrated in the PCB is limited.

This method has already been successful applied for power electronic systems where the passives are integrated in the circuit board [3,4]. Consequently, the next step is to integrate active components as well and hence to build an ultra flat power electronic converter system.

In this study a brief introduction to a project called Power Sheet is given in Section 2. There, a converter system is to be designed with a thickness of no more than 1mm. To achieve this goal three main issues have to be considered. First, the integration of active components is discussed in Section 3 whereas the thermal design is of special interest since the power loss of switches has to be dissipated to the ambient through the PCB.

Second, section 4 deals with the integration of inductive and capacitive components. For inductors and transformers two different integration methods are shown. The integration of capacitors is strongly dependent on the state of the art of capacitive materials. Therefore a brief overview of the available materials is given.

Third, the achievable values for inductances and capacitances as well as the power handling capabilities of switches determine the topology of the converter system. Therefore, in Section 5 a distributed topology is presented which has beneficial properties concerning the integration of components.

2 The Power Sheet

A PCB integrated converter system with a thickness of no more than 1mm is beneficial for ultra flat applications. A project focusing on this issue has been initiated which is called Power Sheet. The Power Sheet consists of a PFC rectifier followed by a DC-DC converter with galvanic isolation. Figure 1 shows the specifications of the power sheet. The challenge is to achieve a converter system with a footprint similar to an A4 page at a thickness of 1mm.

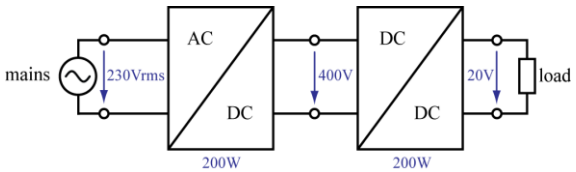

Figure 1 Specifications and structure of the Power Sheet.

3 Integration of Active Components

The integration of active components into the PCB is a major step for a low profile electronic system. Integrated actives not only have the advantage of allowing a compact setup but also have improved electrical and thermal properties compared to wire bonded chips. There, bonding wires limit the thermal performance and the current rating. Furthermore, in case of power switches the bonding implies a parasitic inductance which causes overvoltages during the turn-off transition of the switch.
Since integrated chips are directly bonded to a substrate or a foil bond wires are avoided and hence the parasitic inductance is reduced and since a large area of the DIE is bonded the current capabilities as well as the thermal conductivity increase. Another advantage is 3D routing which allows flexibility of the interconnection compared to 2D routing.
Recent studies have investigated the integration methods [5-8] whereas the flip-chip assembly, the chip-in-polymer (CiP) approach and the molded interconnect device (MID) are of particular interest for power electronic converter systems since prototypes have already been built.
Flip-chip assemblies have been state of the art for many years. Originally, it was used for processor chips with many pins which could no more be wire bonded. Nowadays this technique is used for almost any kind of chip. So the flip-chip integration has also applied for power electronic switches which is discussed in [6]. The integration principle can be seen in Figure 2 where in (a) the flipped chip with solder bumps is placed on a flex foil. The flex foil allows an integration of chips with different thicknesses next to each other. After the bumps are soldered in a reflow process and an underfill is placed (b) the assembly is flipped and the other side of the chip is soldered to a substrate (c).
The chip in polymer approach can also be applied for power switches [6]. On contrary to flip-chip methods here the connections to the die are realized by micro vias which are laser drilled and subsequently metalized as is indicated in Figure 3. If several chips are to be embedded with different thicknesses the lamination process step balances the differences so that a planar layer can be achieved.

Table I Implemented prototyps

Flip Chip	Half bridge leg [6] Infineon OptiMOS 100V (Area: 26mm^2) Diodes: IXYS DWS (36-80A) V =40V I = 50A
CiP	Half bridge leg [6] Infineon OptiMOS 55V Diodes: Microsemi 30CPQ100 V = 30V, I = 25A
MID	3D package stack [5] 76 I/O's
Embedded power technology	Half bridge leg with gate drive circuit [7] Switches: IXFD24N50-7X V = 400V, I = 10A

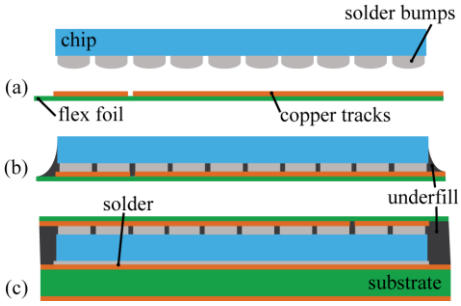

Figure 2 Flip-chip integration principle where in (a) the bumped chip is placed on a flexfoil. (b) Soldering of the bumps and underfill. (c) Die bonding on a substrate.

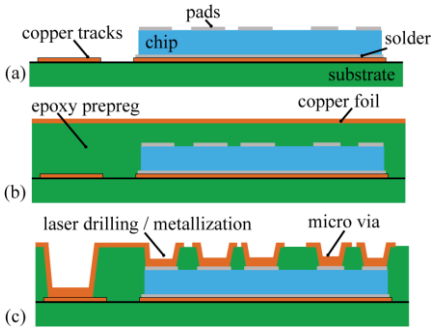

Figure 3 Chip in polymer setup. (a) Soldering or adhesion of the chip on a substrate. (b) Lamination of the chip with a epoxy prepreg layer covered by a copper foil. (c) Laser drilling and metallization of micro vias.

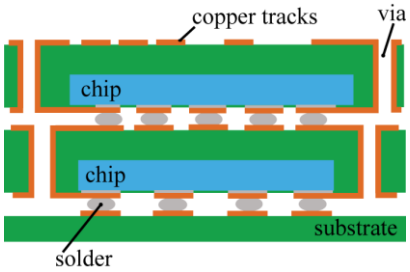

Figure 4 Schematic of MID stack. Through to the vertical configuration only short interconnections are required.

The integration of microcontrollers, memory chips and FPGAs can be done with the molded interconnection device (MID) technology [5]. This integration method stacks the dies which allows vertical interconnections. Hence the parasitic inductance is reduced.
In Table I parameters of already implemented prototypes are given. Voltages up to 400V and currents up to 50A have been applied to the integrated switches.

4 Integration of Passive Components

4.1 Inductors and Transformers

In principle there are two possibilities for integrating transformers and inductors in a printed circuit board (PCB).

The first is to realize the winding as PCB tracks and place the core on top and bottom of the PCB as can be seen in Figure 5(a). There, the core material reduces the magnetic resistance of the setup resulting in a larger inductance value for a given number of turns. The distance between the two core plates is usually determined by the thickness of the PCB. This distance is basically an air gap. To reduce the copper resistance several layers could be connected in parallel.
The second possibility is to integrate the core in the PCB and realize the winding as PCB tracks on top and bottom of the PCB and by vias. In this case no multilayer PCB is required. The core could be a wound magnetic foil (e.g. amorphous or nanocrystalline) and hence almost arbitrary toroid dimensions can be considered. This setup can be seen in Figure 5(b).

Calculation methods for the PCB integrated windings can be found in literature [9-11]. However, these methods are only applicable to special cases where certain symmetry is given or boundary effects are neglected. Hence an optimization cannot be performed. Therefore, FEM simulations are necessary to obtain the inductance values, the coupling coefficients and the losses. Although 3D simulation of the components would be beneficial since effects in each direction are considered these simulation are too time consuming. Hence 2D simulations are preferred to optimize losses and size in inductive devices. An optimization of a planar transformer is discussed in [12]. There, the geometric parameters are optimized in order to achieve a maximum efficiency of the total converter.
In 2D simulations, however, eddy current losses in magnetic sheets cannot be estimated accurately. Consequently, additional loss models are necessary which consider these effects [13]. A 2D simulation result of a planar inductor can be seen in Figure 6. In (a) no core material is applied whereas in (b) a TDK IRJ04 sheet is placed on top and bottom of the inductor. As can be seen the emitted field in the latter case is significantly reduced which lowers the EMI stress of the system.
An important point is the maximum current density of tracks. The copper cross-section of the tracks is determined by the copper thickness and hence a large track width is necessary to achieve a moderate current density. Consequently, a large area is necessary for planar inductive components.
Concerning PCB transformers, it has to be considered that the coupling factor is in the range of 0.8 – 0.9 which results in a considerable leakage inductance. Compensation of the leakage with capacitors in primary and secondary winding can reduce the current and hence the losses in the transformer [12],[14].
The realization of an inductive component with an integrated toroidal core is determined by the low profile of the core which results in a low core cross-section area. Consequently, to achieve a considerable core area a large ratio between outer and inner radius is required. The inner radius, however, determines the number of vias and hence the number of turns. Figure 7(b) shows inductors with integrated cores.

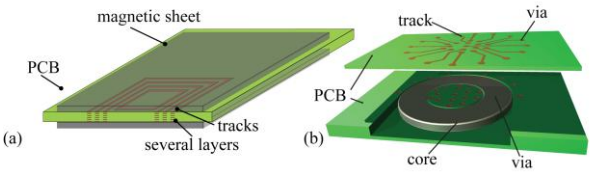

Figure 7 Integration methods of inductive components: (a) winding realized as tracks on several layers and (b) integrated core (e.g. foil wound to a toroid) in the PCB.

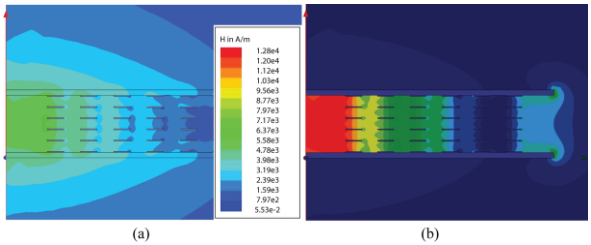

Figure 5 Field simulation of a PCB integrated inductor with 6 layers and 6 turns / layer whereas in (a) no magnetic sheet (L = 6.5µH) and in (b) a magnetic sheet (L = 14.3µH) is considered.

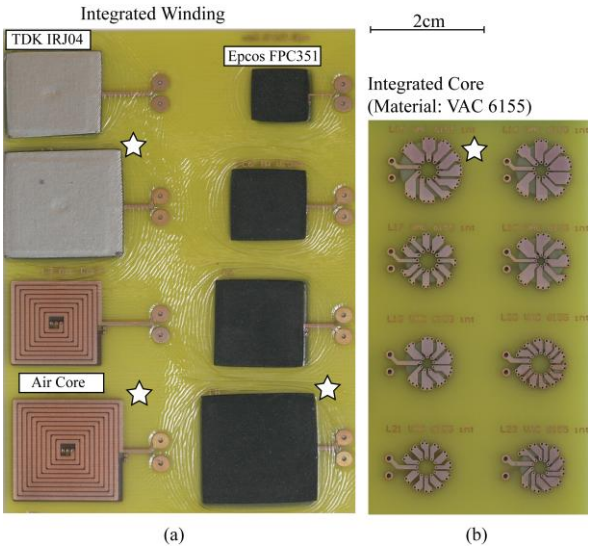

Figure 6 Planar Inductors: (a) Integrated windings whereas different core materials are used. (b) Integrated Core which is realized by a toroidal wound core.

Table II Parameter of integrated inductances

	Air Core	Epcos FPC351	TDK IRJ04	Integrated Core
L [µH]	30	29	27	26.6
R_{350kHz} [Ω]	7.6	8	12.3	8.7
A [cm^2]	4	4	4	1.13

A comparison between the two integration methods cannot be done very easily because not only electrical properties are important but also manufacturing effort and EMI issues. In Table II the electrical properties of four inductances are shown which are indicated with a star in Figure 7. It points out that the integrated core offers a smaller setup and almost no EMI problems. However, the manu-

facturing effort is larger compared to the integrated windings.
The large ac resistance at 350kHz is due to skin- and proximity effects in case of integrated windings respectively due to core losses in case of integrated cores. To reduce the high losses other core materials could be considered.

4.2 Capacitors

Integrated capacitors are state of the art in high frequency applications where the capacitors are used as filter and/or matching devices. There, only small values in the range of several pF are required. However, in power electronic systems capacitances in the range of up to several µF are necessary as output or dc voltage link capacitor.
Furthermore, in power electronic systems the voltage requirements for capacitors are more severe since the output voltage of a PFC rectifier with an input voltage of 230Vrms is roughly 400V. Thus capacitors have to withstand this high voltage. Up to now there have only been a few approaches to integrate capacitors for power electronic systems [3],[15] where resonance and filter capacitors are embedded. However, in order to achieve a very low converter profile the integration of capacitors in the range of several tens of µF is essential.

The integration methods of capacitors are discussed in [3] and important manufacturer data is summarized in Table III. As can be seen the capacitance density of the proposed materials is low if several µF are required. However, materials (e.g. by DuPont) with a capacitance density of over 2µF/cm^2 are under development and should enter the market in next months.

Table III Embedded capacitors

	Sanmina Faradflex	**DuPont** HK04	**3M** C-Ply	**Würth** FLATcomp	**LTCC**
C/Area [nF/cm^2]	1.5	0.26	0.2	2	0.26
tan δ	0.014 @ 1 GHz	0.005 @1MHz	0.02 @1MHz	?	0.03 @1MHz
$V_{Breakdown}$ [kV]	?	4	1.2	0.34	?
Thickness [µm]	16	12	40	20	?
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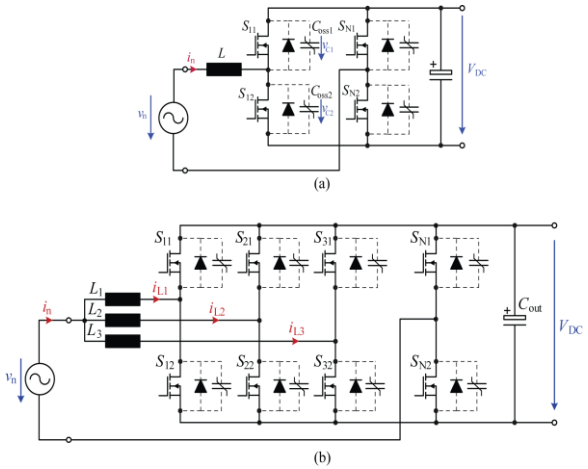

Figure 8 (a) Schematic of a bridgeless boost PFC rectifier whereas the boost diodes are replaced by active switches. (b) Multi-cell configuration of a bridgeless PFC rectifier.

5 Distributed Topology for a PFC rectifier system

Based on the integration methods discussed in the previous sections an ultra flat PFC rectifier will be designed in the following.
It is important to distribute the power losses in an ultra flat converter because the generated heat has to be transmitted to the ambient through the PCB. Therefore, a distributed topology is required where the power loss is divided to several components. Consequently, the thermal stress for a component is reduced.

5.1 Topology

As it is of interest to achieve low losses a bridgeless topology [16] is beneficial which is shown in Figure 8(a). There, the boost diodes are replaced by active switches which allow synchronous rectification in order to reduce conduction losses. Operation in discontinuous conduction mode (DCM) avoids reverse recovery losses in the bulk diodes of the switches. However, due to the high input current ripple a large EMI filter would be required in order to obtain a low THD value.
To overcome this problem a multi-cell configuration could be applied as is shown in Figure 8(b). The superposition of the interleaved inductor currents i_{L1}, i_{L2} and i_{L1} leads to a smooth input current i_n.
Moreover, the multi-cell configuration is beneficial since the transmitted power is distributed on several components which results in a distributed loss generation.

In order to reduce the size of the passive components a high switching frequency is required. This, however, results in severe switching losses in the MOSFETs. To avoid high switching losses zero voltage switching (ZVS) could be applied.
Conventional bridgeless PFC rectifiers can only achieve ZVS in a defined input voltage range [17]. The proposed topology, however, is able to achieve ZVS for the whole mains period.
In Figure 9 the simulated switching waveforms for an input voltage v_n of 325V and an output voltage V_{DC} of 400V for a single boost cell (cf. Figure 8(a)) are shown. In Figure 9(a) it can be seen that ZVS cannot be achieved with conventional switching. However, switch S_{12} is turned on at minimal voltage v_{C2} which results in minimal switching losses. This switching method is called valley switching [17].
To achieve ZVS over the complete half line cycle the switching scheme of Figure 9(b) can be considered. After zero crossing of current i_n switch S_{11} keeps turned on until the current i_R is reached. Consequently, after turn-off of S_{11} the current i_n in the inductor discharges the parasitic

capacitors C_{oss2} of S_{12} while charging C_{oss1}. As soon as the voltage over S_{12} reaches 0V switch S_{12} can be turned on at zero voltage. Figure 10 shows measurement results for the simulated waveforms in Figure 9.
Utilizing this switching scheme ZVS can be achieved and hence switching losses can be avoided which is a major problem in high frequency converter systems.

The bridge leg consisting of S_{N1} and S_{N2} switches synchronous to the mains frequency and hence either the output voltage bus or the ground bus is always connected to mains. Consequently, common-mode noise is reduced significantly.

5.2 Loss Calculation

The heat distribution of the integrated components can be obtained by performing a loss calculation. Considering Table IV where circuit parameters are given the power loss in a MOSFET can be calculated to 128mW. Due to the beneficial topology no switching losses have to be considered.
Consequently, the heat generated by the losses is very small and due to the reduced thermal conductivity of integrated chips compared to wire bonded chips this heat can easily be dissipated to the ambient.

Considering an inductance with an integrated core the calculation can be done by

$$L = N^2 \cdot \mu_0 \mu_r \cdot \frac{h}{2\pi} \cdot \ln\left(\frac{D}{d}\right)$$

whereas D is the outer, d is the inner diameter and h is the height of the core. As core material VC6155F by VAC is be considered. A power loss of 413mW in the core can be calculated using the Steinmetz equation for a parameter set given in Table V. This power loss leads to a temperature rise in the core of 35°C as can be seen in Figure 11 where a thermal simulation with ICEPAK is shown.
A loss calculation considering the losses in the switches, the inductances and the output capacitance gives a total power loss of about 10W. Hence an efficiency of 95% could be achieved.

6 Conclusion

For power electronic converter systems with extreme aspect ratios it is crucial to integrated both actives and passives. In this study the integration methods of active and passive components for power electronic systems are investigated. A brief overview of integration techniques is given whereas the thermal conductivity to the ambient is of special interest.
Furthermore, the design of ultra flat PFC rectifier is discussed which offers two important properties for integrated components. On one hand ZVS is achieved over the whole mains period which avoids switching losses. This is of particular interest since a high frequency is necessary to get small inductors and capacitors. On the other hand this topology consists of several boost cells which operate interleaved. This not only results in a smooth in-

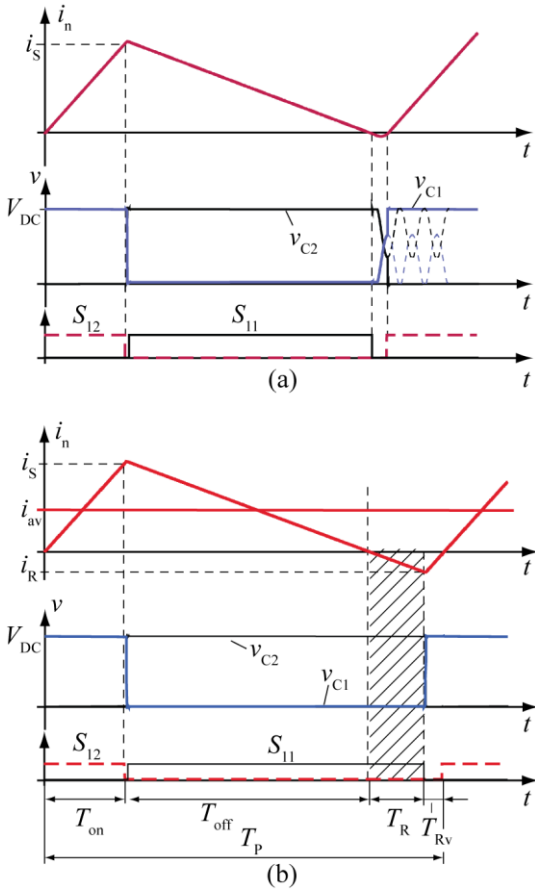

Figure 9 Switching period of a half bridge.
(a) Switching cycle employing valley switching.
(b) Switching cycle with and enlarged on-time of S_{11} which allows ZVS.

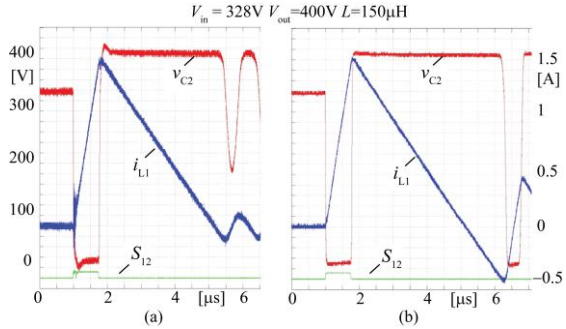

Figure 10 Measurement results for valley switching (a) and ZVS (b). It can be seen that by enlarging t_{on} of S_{11} ZVS can be achieved in (b).

Table IV Circuit parameters

I_{MOSFET}	= 0.4A	$R_{DS(on)}$	= 0.8Ω
I_L	= 0.44A	L	= 150µH
f_{avg}	= 400kHz		

Table V Inductor parameters

Inductance L	=150µH	InnerDiameter d	=10mm
OuterDiameter D	=25mm	Height h	=0.8mm
Saturation B_{sat}	=0.8T	Permeability μ_r	=1800
Curie Temp. T_c	>250°C	α	=1.82
β	=1.98	c	=6.3e-3

put current but also gives a distributed heat generation which is important for ultra flat systems.

7 Literature

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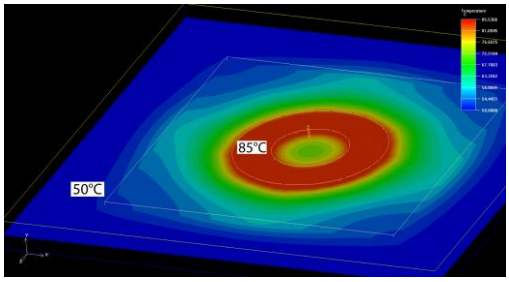

Figure 11 Thermal Simulation of the integrated core for an ambient temperature of 50°C. The temperature rise is 35°C.