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Eidgenössische Technische Hochschule Zürich
Swiss Federal Institute of Technology Zurich

What are the "Big CHALLENGES" in Power Electronics?

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What are the "Big OPPORTUNITIES" in Power Electronics?

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Power Electronics 2.0

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*Royal Institute of Technology (KTH) Stockholm

Outline

- ▶ Application Areas & Performance Trends
- ▶ Conv. Component Technologies → Challenges
- ▶ Conv. Topologies & Modulation / Control → Challenges
- ▶ Conv. Design & Testing Procedure → Challenges
- ▶ Future BIG CHALLENGES → Opportunities (!)
- ▶ Future Univ. Research & Education
- ▶ Conclusions

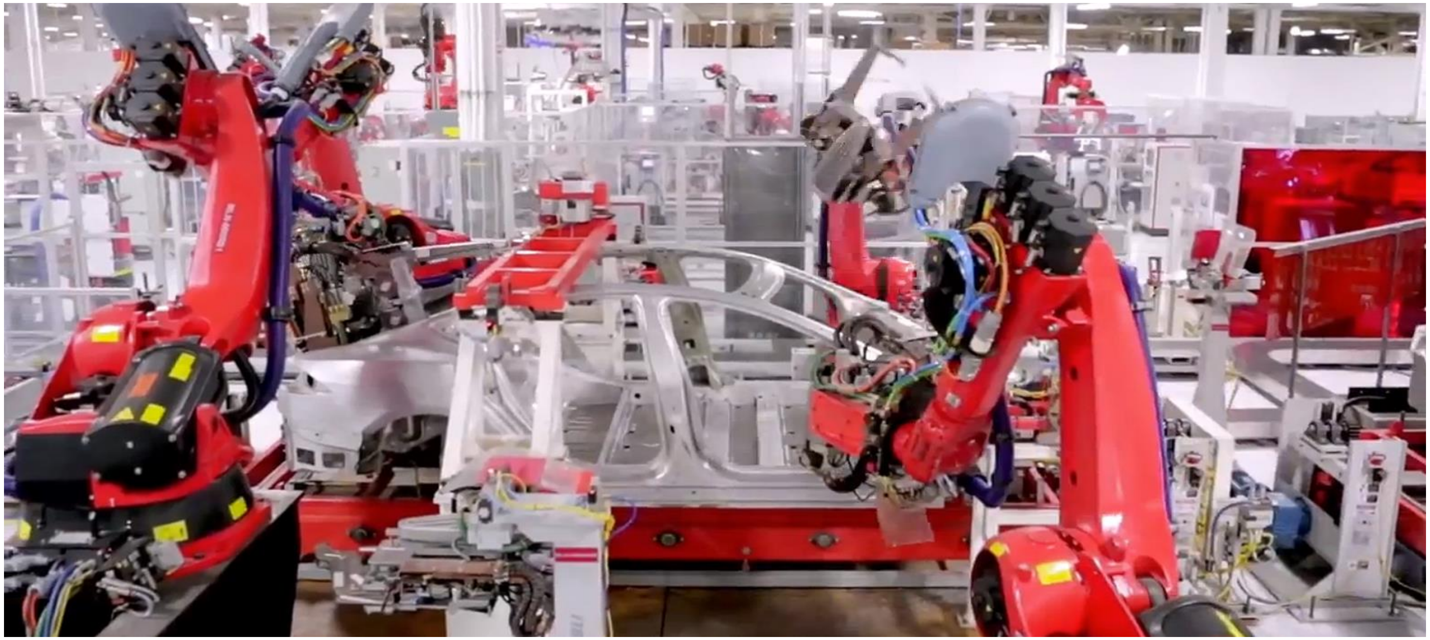
Application Areas
Performance Trends

▶ Application Areas

- Industry Automation / Processes
- Communication & Information
- Transportation
- Lighting
- etc., etc.

.... Everywhere !

Source: TESLA MOTORS

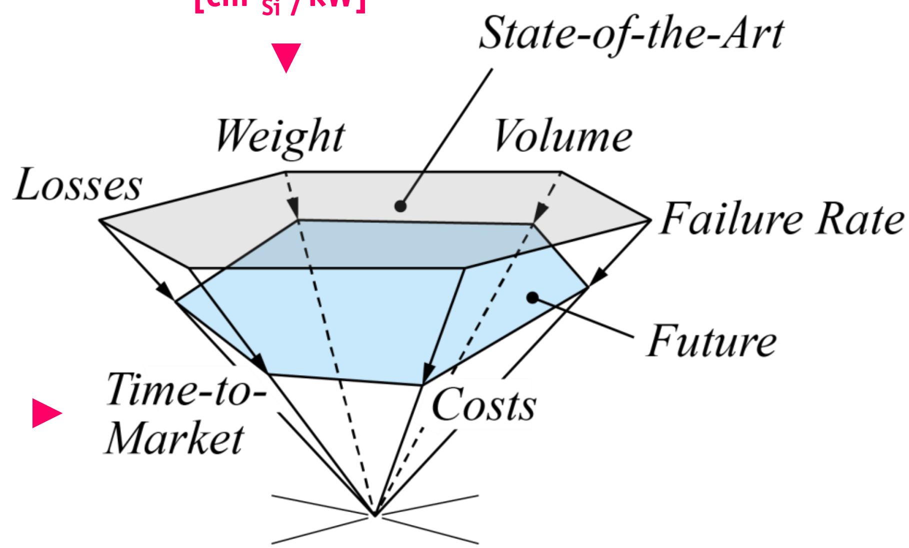


▶ Power Electronics Converters Performance Trends

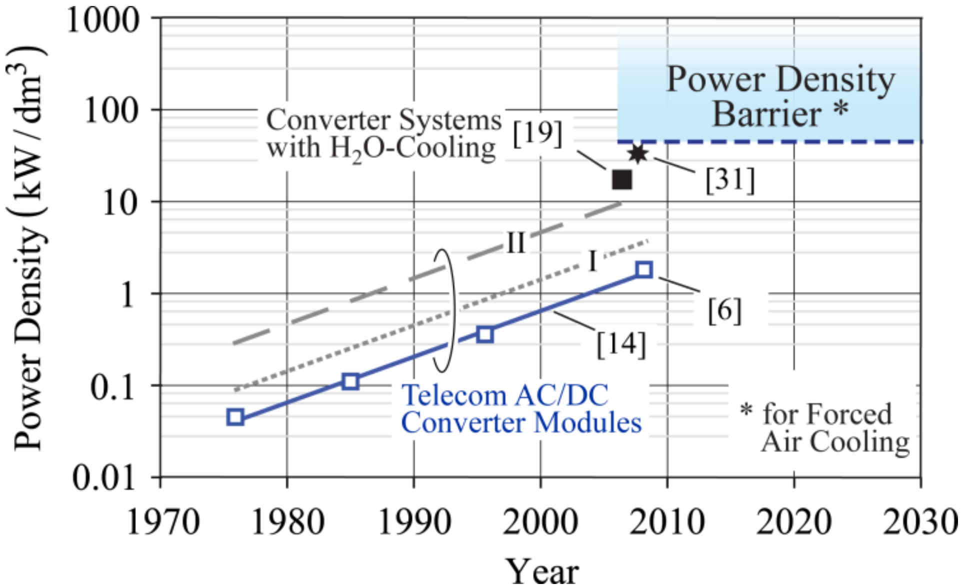
Environmental Impact... [kg_{Fe} /kW]
[kg_{Cu} /kW]
[kg_{Al} /kW]
[cm^2_{Si} /kW]

■ **Performance Indices**

- Power Density [kW/dm^3]
- Power per Unit Weight [kW/kg]
- Relative Costs [kW/$]
- Relative Losses [%]
- Failure Rate [h^{-1}]



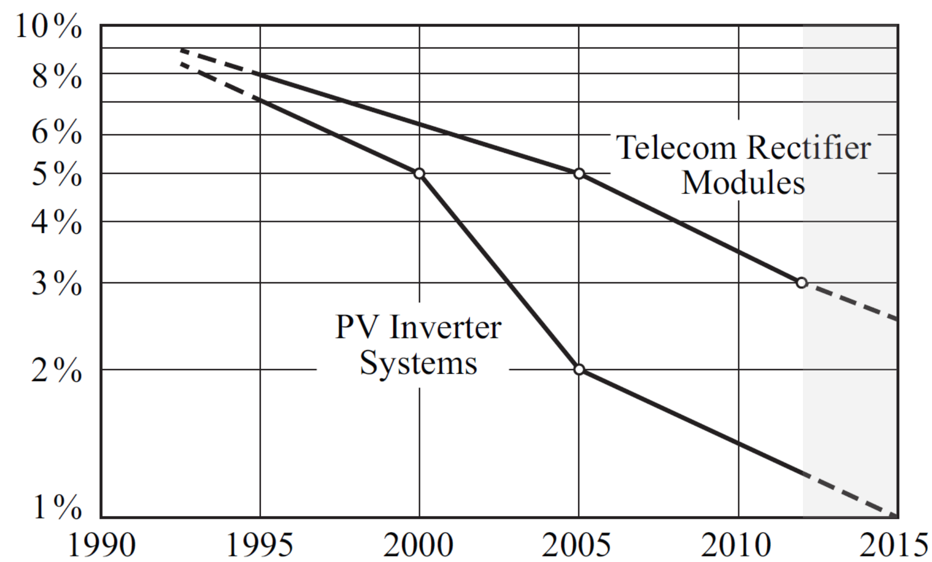
► Performance Improvements (1)



- **Power Density**
  - **Telecom Power Supply Modules: Typ. Factor 2 over 10 Years**

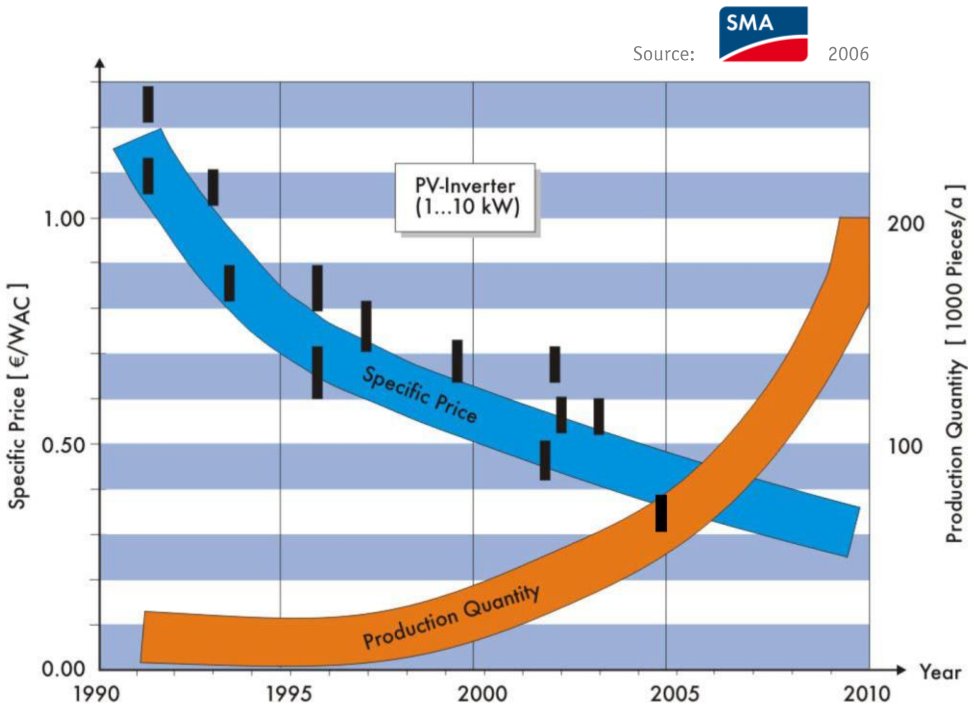
▶ Performance Improvements (2)

Inefficiency (Losses)... $1\text{-}\eta$



- **Efficiency**
  - PV Inverters: Typ. Loss Reduction of Factor 2 over 5 Years

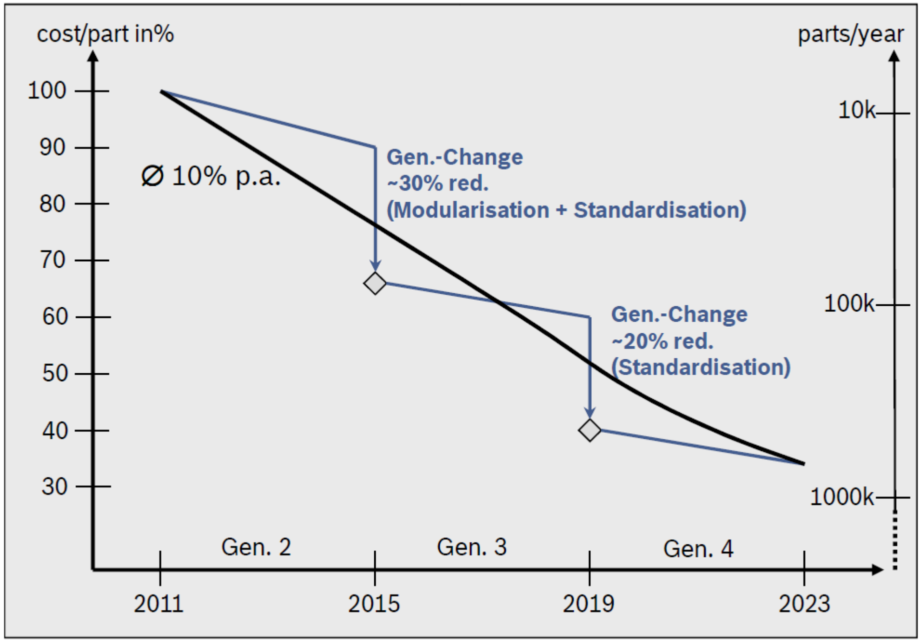
▶ Performance Improvements (3)



- **Costs**
  - — **Importance of Economy of Scale**

▶ Performance Improvements (4)

Source: PCIM 2013

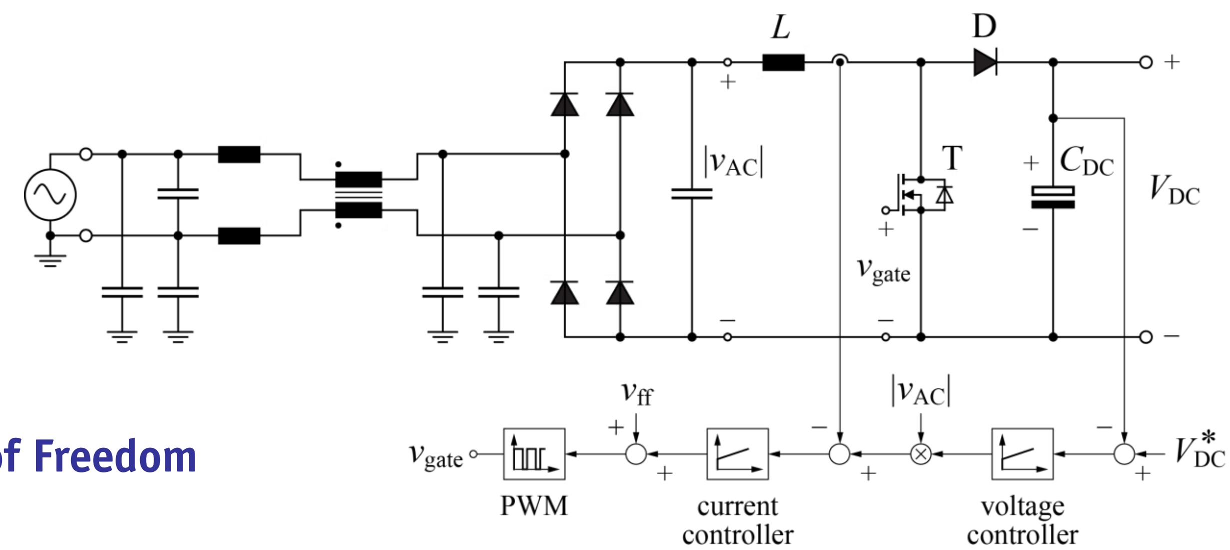


■ Costs

— Automotive: Typ. 10% / a
— Economy of Scale !

▶ Challenge

■ How to Continue the Dynamic Performance Improvement (?)



■ Degrees of Freedom

- Components
- Topologies
- Modulation & Control
- Design Procedure
- Modularization / Standardization / Economy of Scale
- Manufacturing
- New Applications

Components

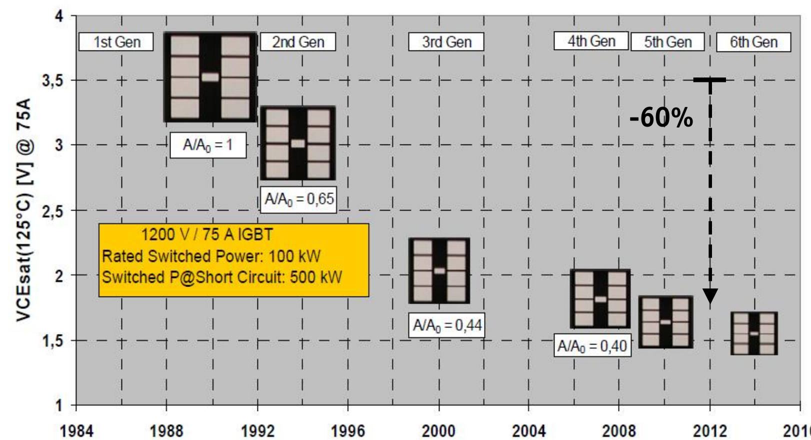
→ Potentials & Limits

Power Semiconductors

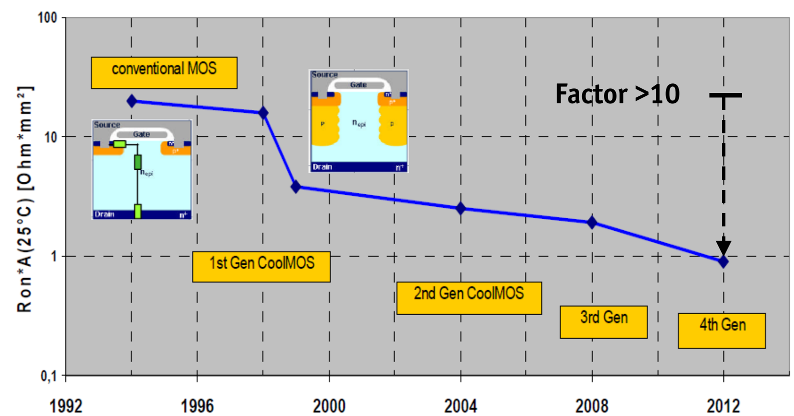
→ Si / SiC / GaN

▶ Si Power Semiconductors

Source: Dr. Miller / Infineon / CIPS 2010



600V Devices



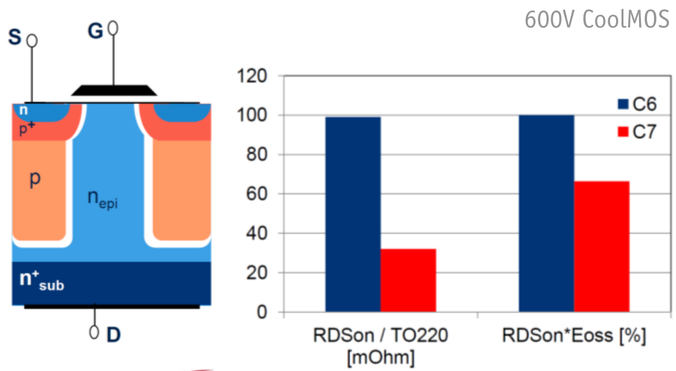
■ Past Disruptive Changes

— IGBT Trench & Field-Stop
— MOSFET Superjunction Technology

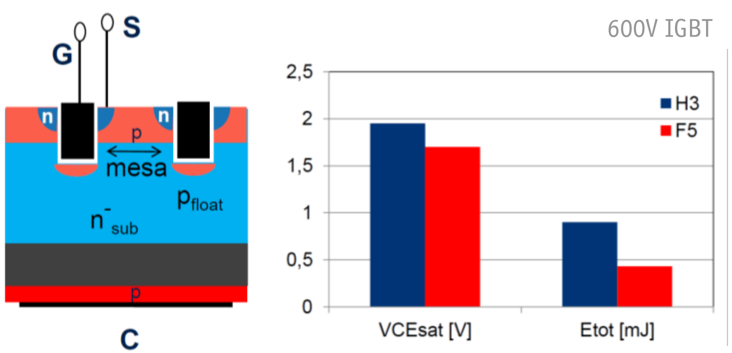
▶ Si Power Semiconductors

- **Continuous Further Improvement**

— Ultra Thin Wafers (Lower On-State & Sw. Losses of IGBTs) → Wafer Handling Challenge
— Higher Switching Speeds → Dyn. Clamping & Low L_s Packaging
— Smaller Chip Sizes (Higher R_{th} , Lower C_{th}) → Low R_{th} Packaging
— Long Lifetime IGBTs for T_j=200° & ΔT_j=120° → Advanced Packaging (LTJT)



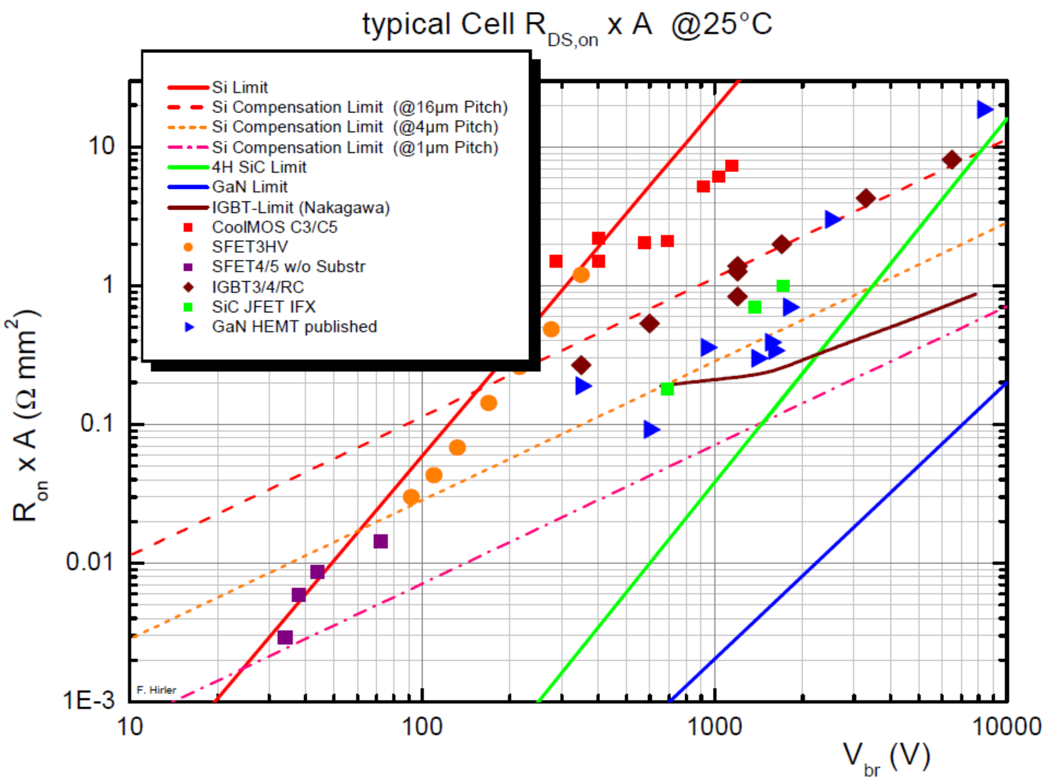
Source: Dr. Deboy Infineon IECON 2013



- **Main Challenges in Packaging (!)**

▶ WBG Power Semiconductors

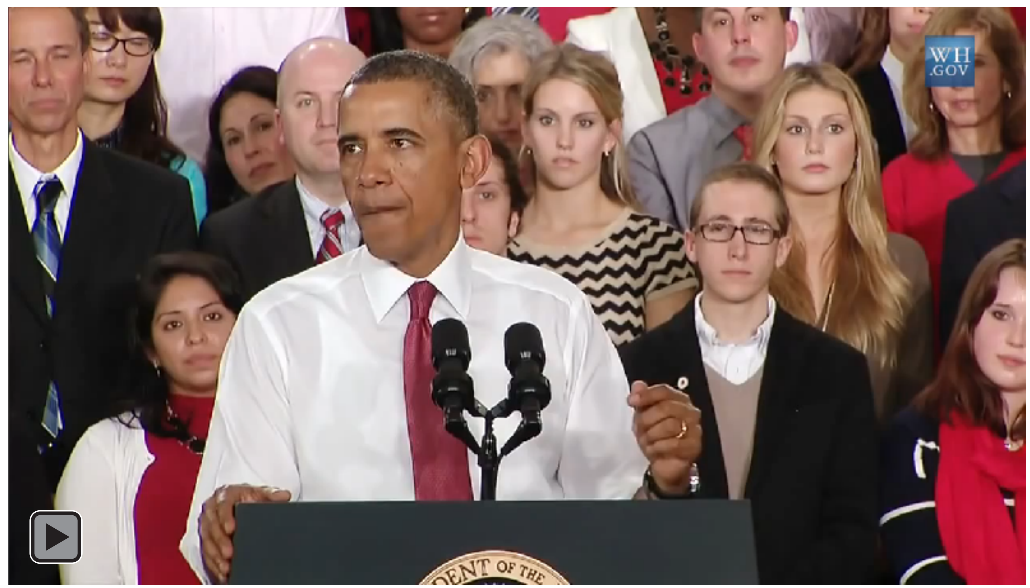
Source: Dr. Miller Infineon CIPS 2010



- **Disruptive Change**
  - Extremely Low $R_{DS(on)}$
  - Very High $T_{j,max}$
  - Extreme Sw. Speed

- **Utilization of Excellent Properties → Main Challenges in Packaging (!)**

▶ WBG Power Semiconductors



- **Disruptive Change**

— Extremely Low $R_{DS(on)}$
— Very High $T_{j,max}$
— Extreme Sw. Speed

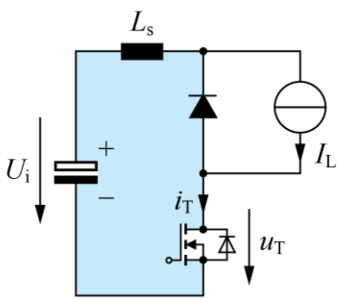
- **Utilization of Excellent Properties → Main Challenges in Packaging (!)**

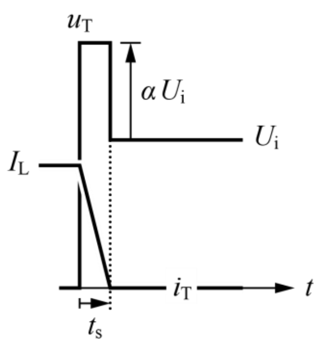
▶ Low Inductance Packaging Challenge

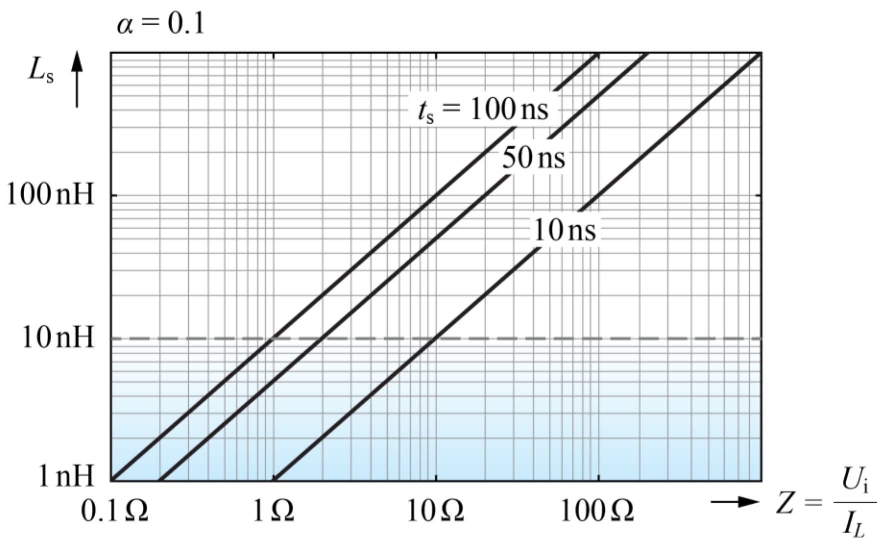
- Allowed L_s Directly Related to Switching Time t_s →
- Ensure Very Low Gate Inductance & Kelvin Source
- Ensure Min. Coupling of Gate and Power Circuit

$$L_s \leq \frac{\alpha U_i}{\frac{I_L}{t_s}} = \alpha t_s \frac{U_i}{I_L}$$

Z







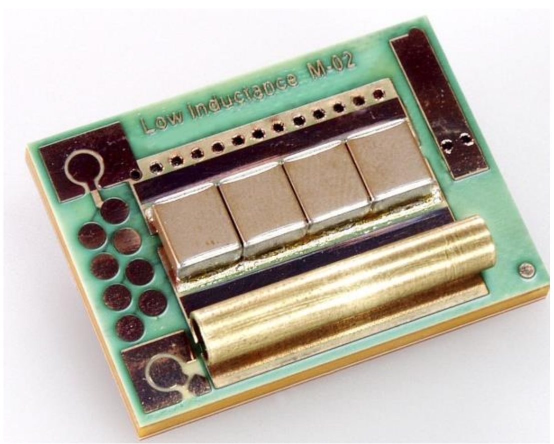
- Planar Interconnections / Parallel Connection (Increase of Z)

▶ Low-Inductance Packaging Challenge

- 600pH DC Link Inductance → Record in Low Ind. Packaging
- "Switching Cell in the Package"

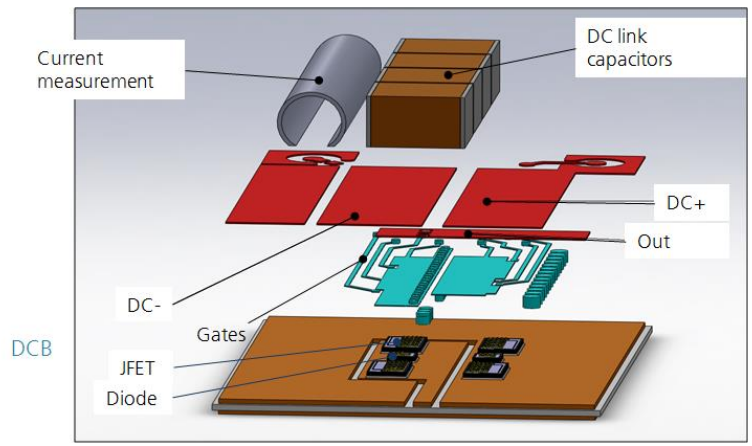
— SiC Switches on Ceramic Substrate (DCB) Embedded in Top Layer PCB
— 1200V J-FET Half Bridge (50A) incl. DC Link Cap. Soldered to the Module

Source: Fraunhofer IZM Dr. Hoene



Technische Universität Berlin
Forschungsschwerpunkt Technologien der Mikroperipherik

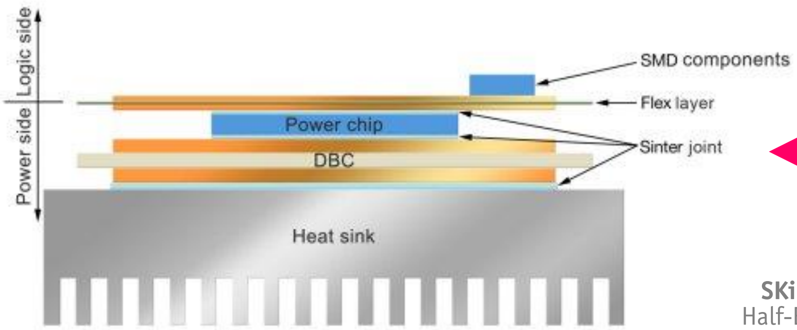
ECPE

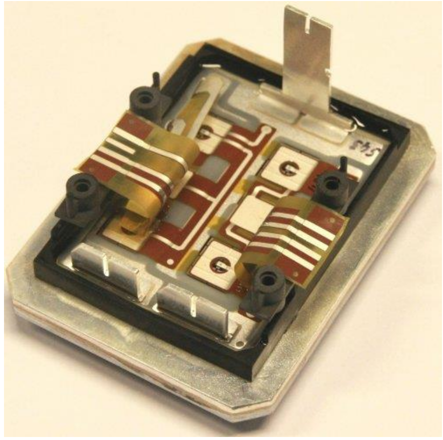


▶ SKiN Technology

- No Bond Wires, No Solder, No Thermal Paste
- Ag Sinter Joints for all Interconnections of a Power Module (incl. Heatsink)
- Extremely Low Inductance & Excellent Thermal Cycling Reliability

Source: SEMIKRON innovation+service Dr. Scheuermann Dr. Beckedahl CIPS 2008



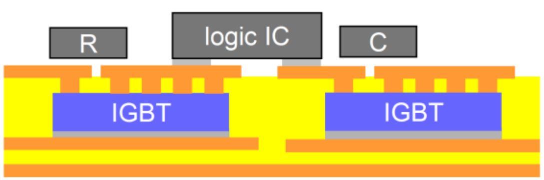


SKiN 600V/400 A
Half-Bridge Module

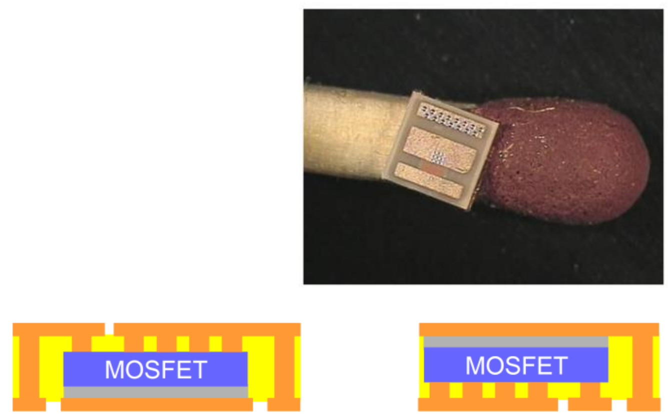
- Allows Extension to 2-Side Cooling (Two-Layer Flex-Foil)
- Allows Integration of Passive & Active Comp. (Gate Drive, Curr. & Temp. Measurem.)
- Disruptive Improvement (!)

▶ Planar Power Chip Package

- **Novel Concepts for Power Packages and Modules**



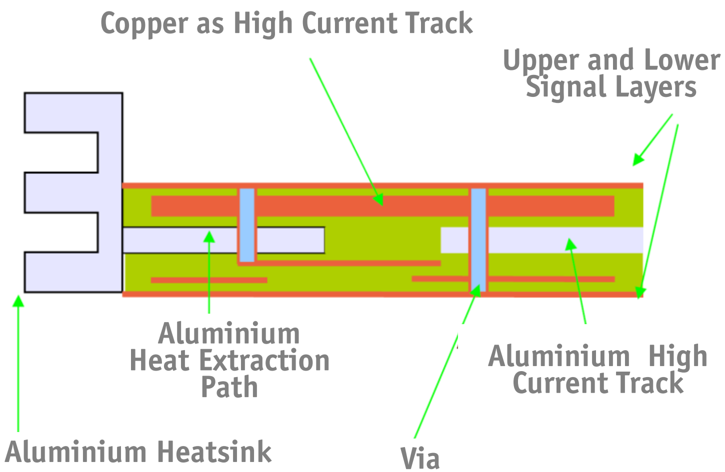
Module with Power and Logic Devices

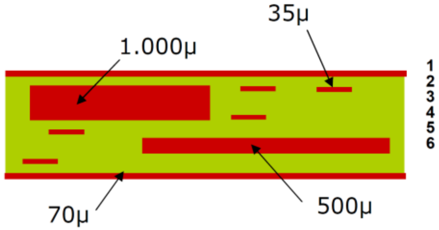


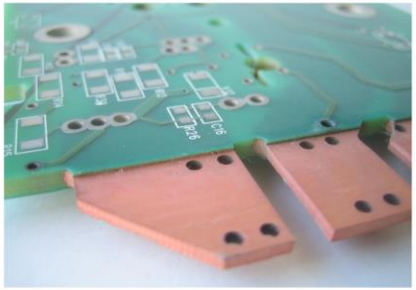
Single Chip Package for MOSFETs and IGBTs

▶ Multi-Functional PCB

- Multiple Signal and High Current Layers
- Integrated Thermal Management







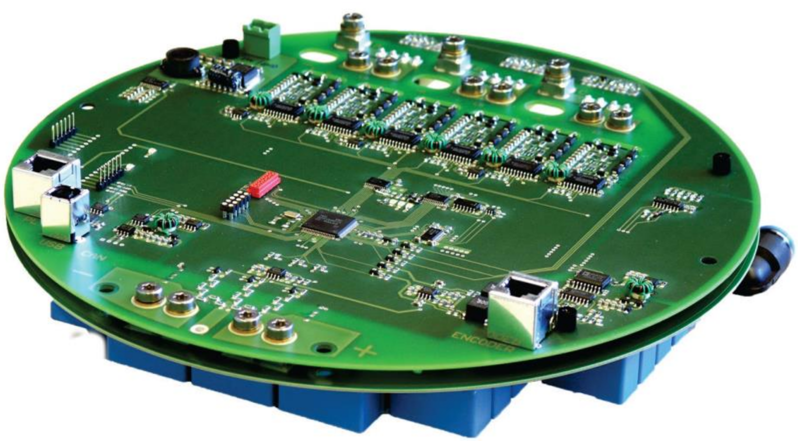
- Substantial Change of Manufact. Process → "Fab-Less" Power Electronics
- Advanced Simul. Tools of Main Importance (Coupling with Measurem.)
- Testing is Challenging (Only Voltage Measurement)
- Once Fully Utilized – Disruptive Change (!)

▶ 3ph. Inverter in p²pack-Technology

- Rated Power 32kVA

- Input Voltage $700V_{DC}$
- Output Frequency 0 ... 800Hz
- Switching Frequency 20kHz

Source: SCHWEIZER ELECTRONIC, enertronics



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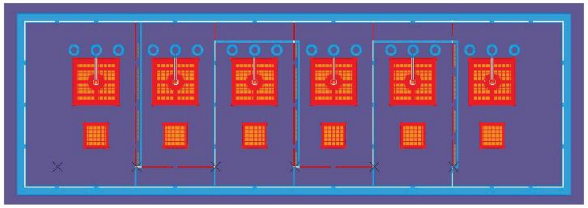
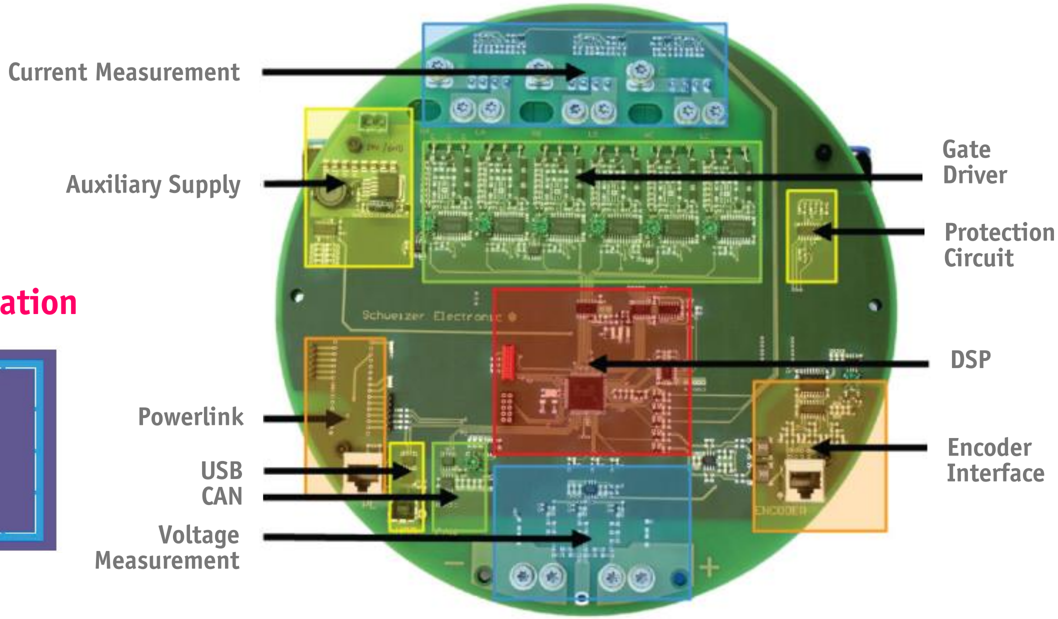
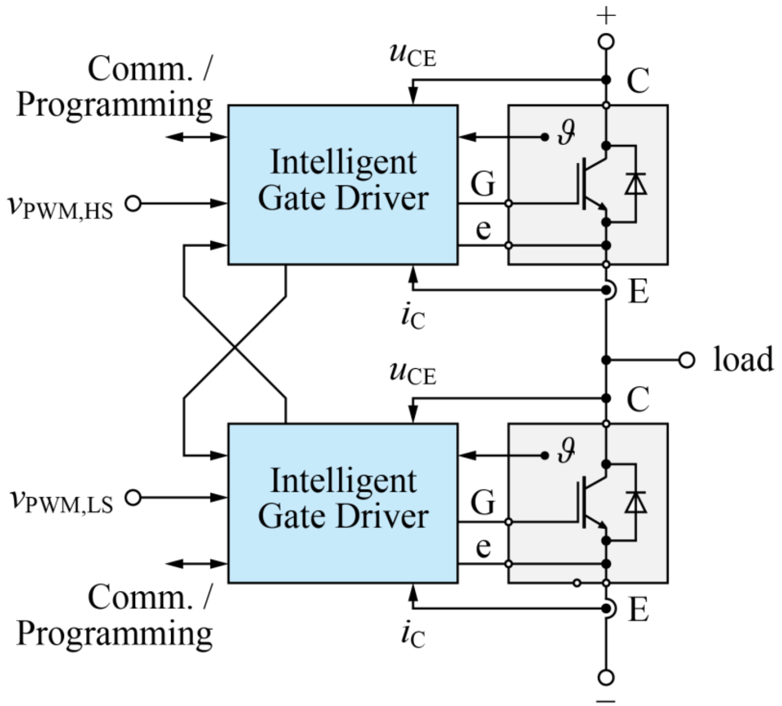
Source: SCHWEIZER ELECTRONIC, enertronics

– Power Semiconductor PCB Integration





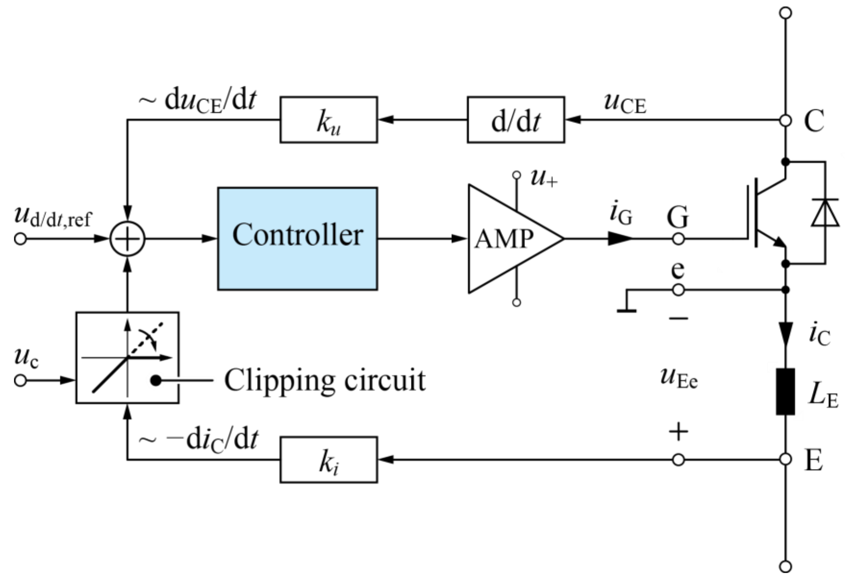
▶ Active Closed Loop Gate Drive



- Continuous (!) Control of the Switching Trajectory incl. Short Circuit & Overvoltage
- Minimization of Interlock Delay Time / PWM Distortion
- Options for Monitoring / Lifetime Prediction etc.

▶ Active Closed Loop Gate Drive

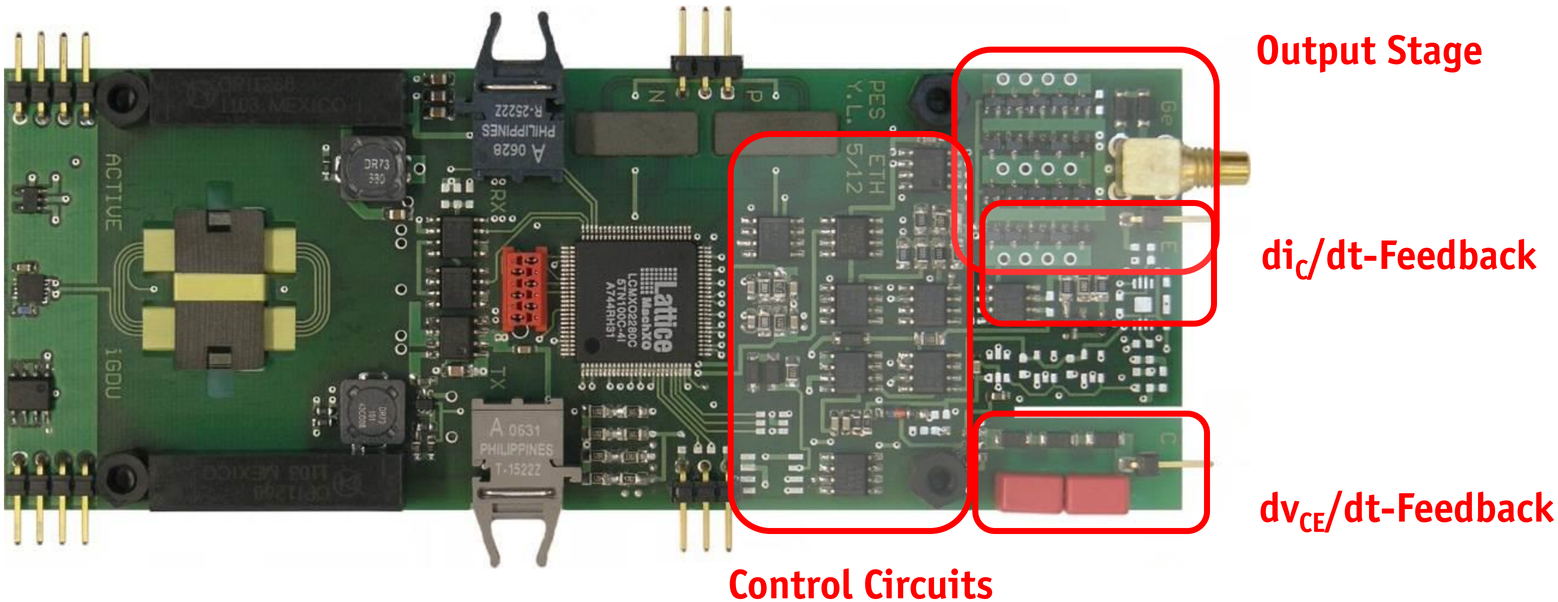
– Single Contr. for du_{CE}/dt & di_C/dt



■ Continuous (!) Control of the Switching Trajectory incl. Short Circuit
■ Options for Monitoring / Lifetime Prediction etc.

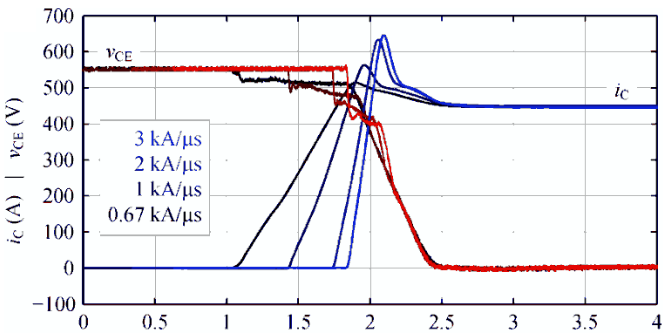
▶ Hardware Prototype

- **PCB Dimensions** 50 mm x 130 mm (2 in x 5.1 in)



▶ Experimental Results – Individual Variation of References

■ Turn-On: Variation of di_C/dt



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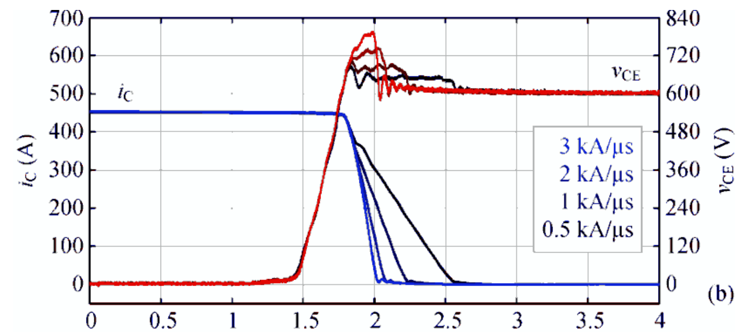
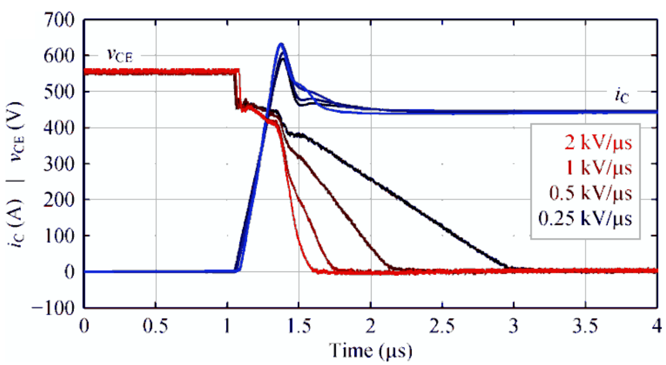
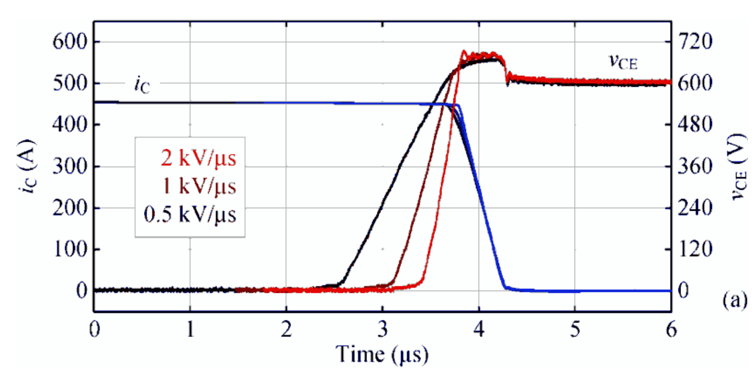


■ Turn-On: Variation of dv_{CE}/dt



■ Turn-Off: Variation of dv_{CE}/dt

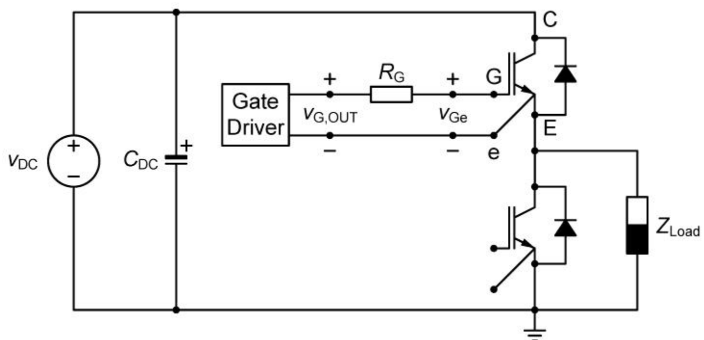


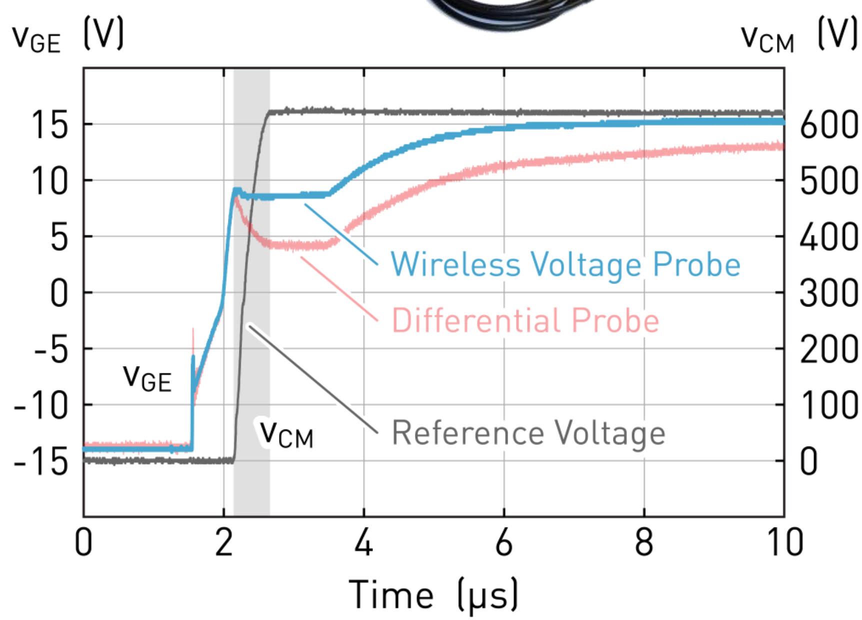
▶ New Wireless Measurement Technology

- **Bandwidth 100 MHz**
- **Sampling Rate 400 MS/s (8 Bit)**

- **Bluetooth Communication**
- **NO dv_{CM}/dt Limit (!)**

Source: enertronics





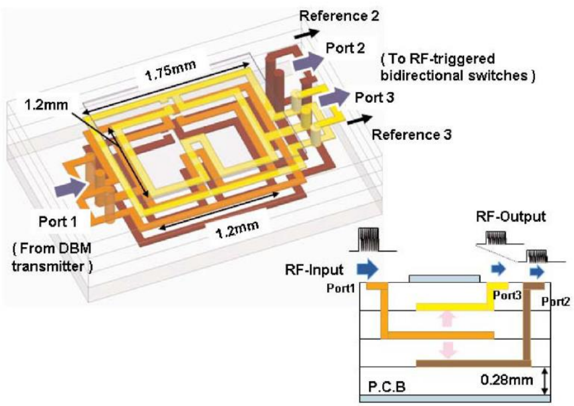
▶ Latest Systems Using WBG Devices → GaN

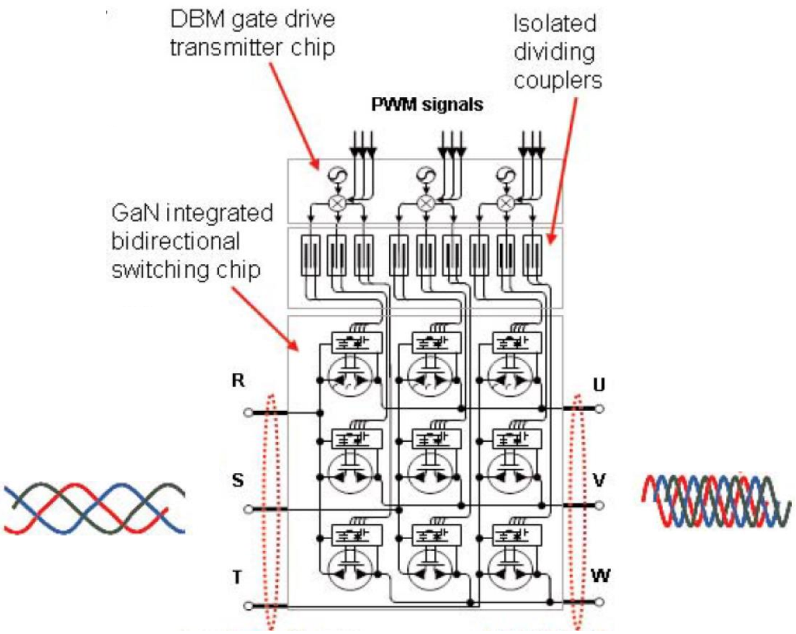
Source: Panasonic ISSCC 2014

■ GaN 3x3 Matrix Converter Chipset with Drive-By-Microwave (DBM) Technology

- 9 Dual-Gate Normally-Off Gate-Injection Bidirectional Switches
- DBM Gate Drive Transmitter Chip & Isolating Dividing Couplers
- Extremely Small Overall Footprint - 25 x 18 mm² (600V, 10A – 5kW Motor)

5.0GHz Isolated (5kVDC) Dividing Coupler

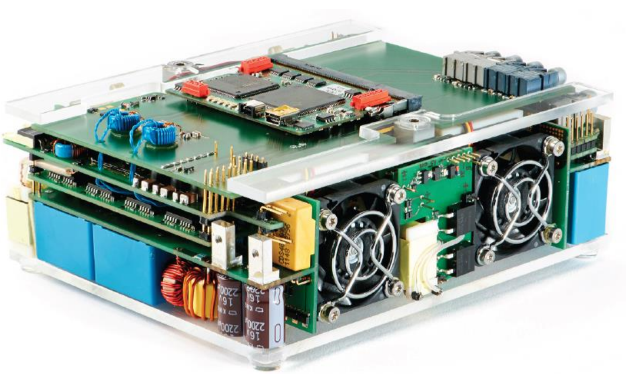


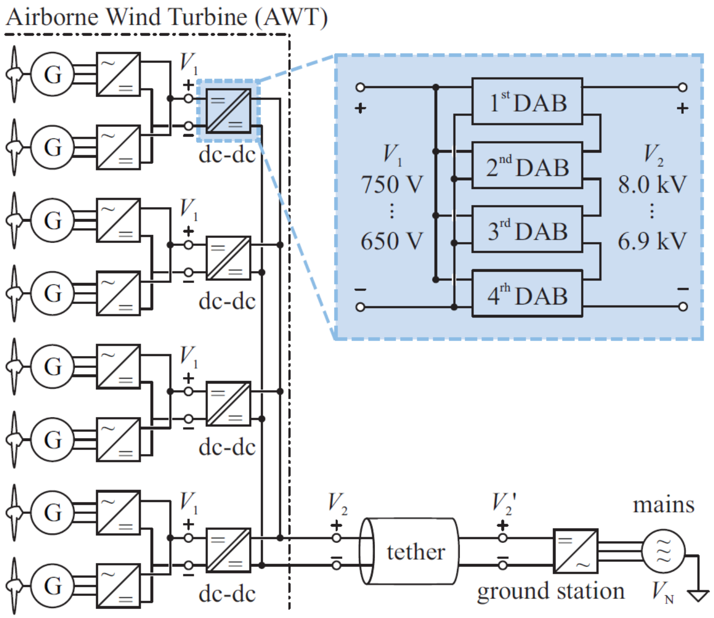


▶ Latest Systems Using WBG Devices → SiC

■ All-SiC Conv. Cell of a 100kHz 25kW Ultra-Light Weight Solid-State Transformer

- Medium Voltage Port 1750 ... 2000 V_{DC}
- Low Voltage Port 650 ... 750 V_{DC}
- Rated Power 6.25 kW
- Power Density 5.2kW/dm³
- Specific Weight 4.4kW/kg

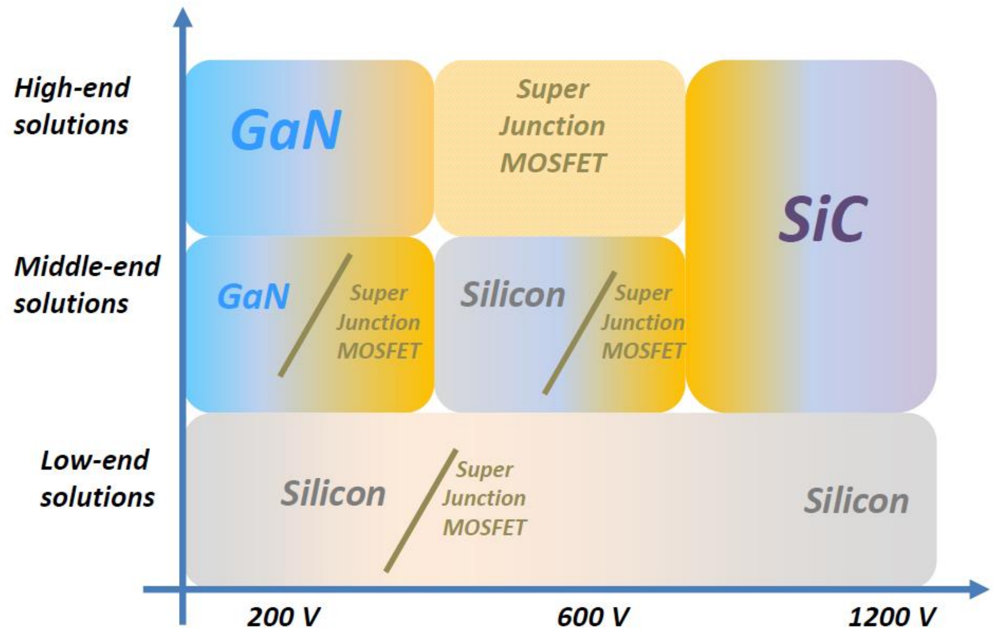




■ High Switching Frequ. @ Med. Voltages Enabled by SiC

▶ WBG Power Semiconductors

■ Application Perspectives

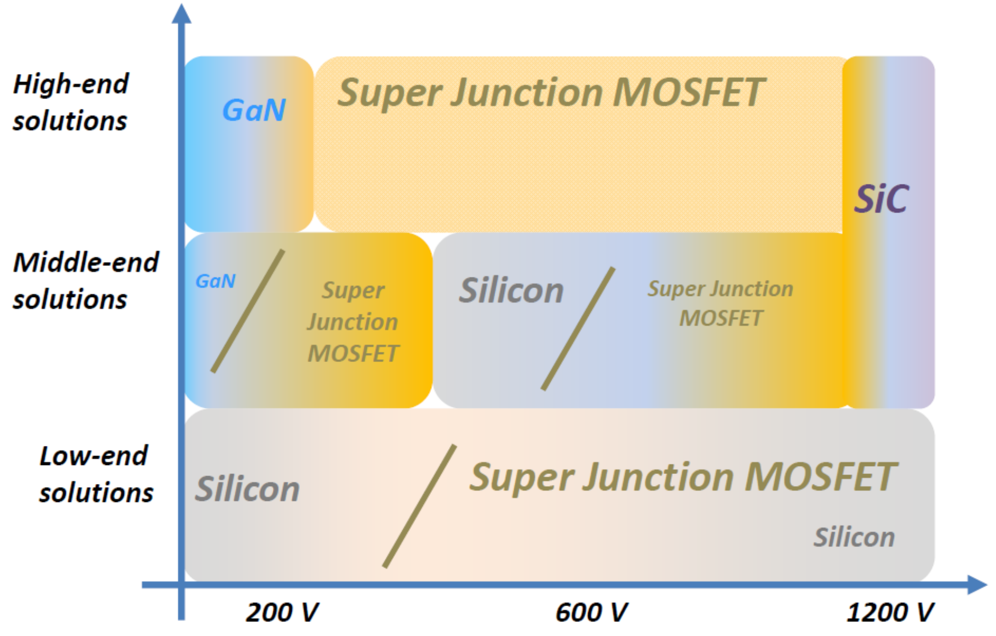


Source: Dr. Honea
PEDG 2013
transphorm

What Yole Developement showed in 2011 as future view

▶ WBG Power Semiconductors

■ Application Perspectives

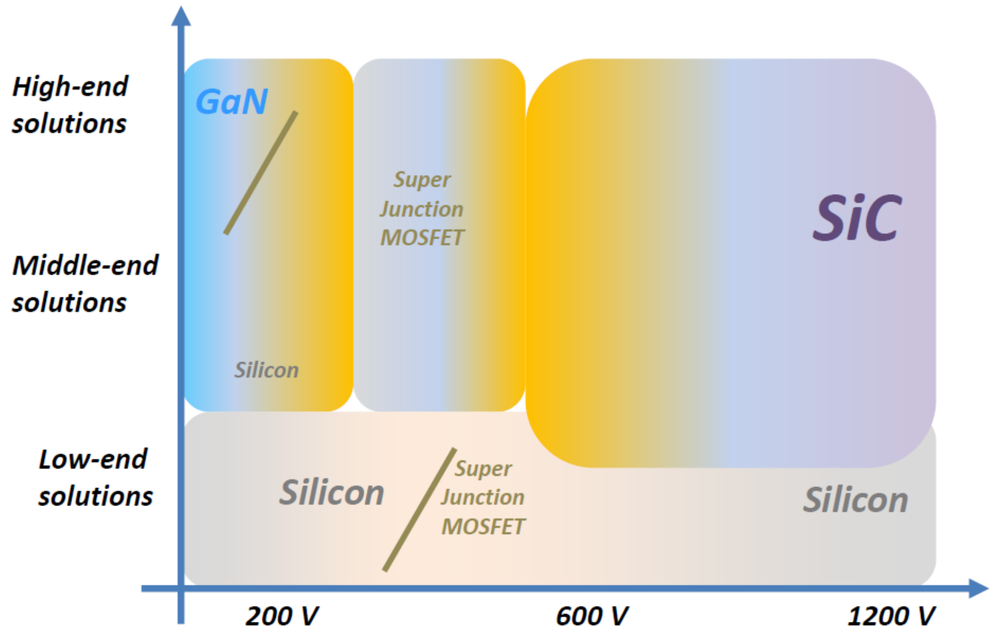


Source: Dr. Honea
PEDG 2013 transphorm

A Super Junction supplier's view of future N

▶ WBG Power Semiconductors

■ Application Perspectives

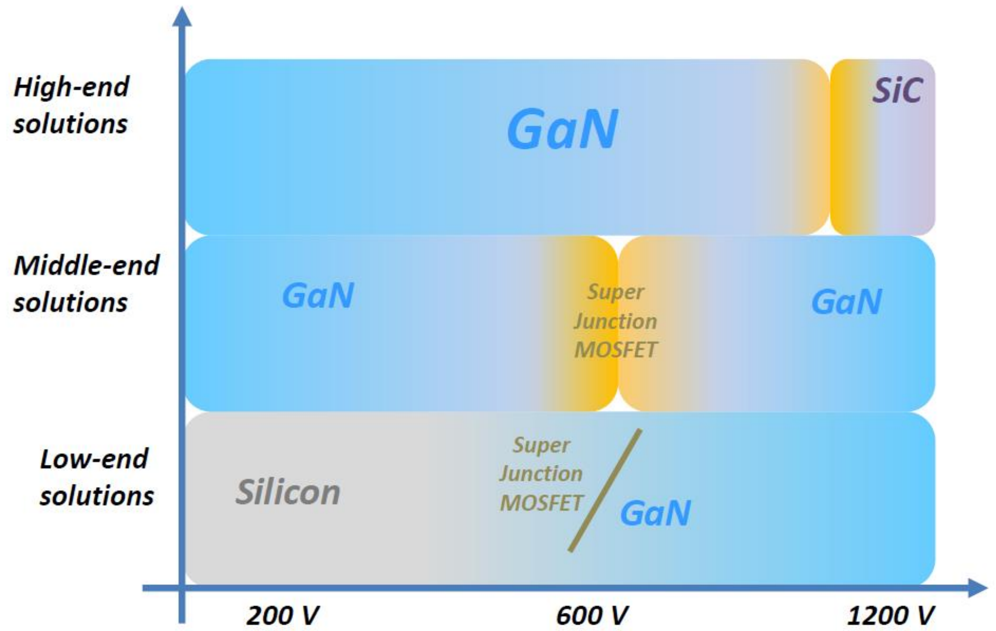


Source: Dr. Honea
PEDG 2013
transphorm

A SiC supplier's view of future

▶ WBG Power Semiconductors

■ Application Perspectives



Source: Dr. Honea PEDG 2013 transphorm

GaN solution supplier's view for future

Σ

Power Semiconductors
Gate Drive
Packaging

- Disruptive Changes Happened (WBG, LTJT)
- Cont. Further Improvements – Packaging, Reliability (!)

→ Main Challenges to Module Manufacturers
- Electromagnetically Quiet Packaging
- Integrated Programmable Gate Drive
- Ensuring Reliability & Reliability Testing Procedures (!)
- Local Measurement and Condition Monitoring
- Large Scale Applications of WBG (Chicken & Egg Problem)

→ Main Challenges to General Users
- Higher Level of Integration (e.g. PCB)
- Fund. Changes in Design / Manufacturing / Measurement Techniques
- Clarification of Cost/Performance of WBG Semiconductors

Passive Components

→ Capacitors / Magnetics / Cooling

Capacitors

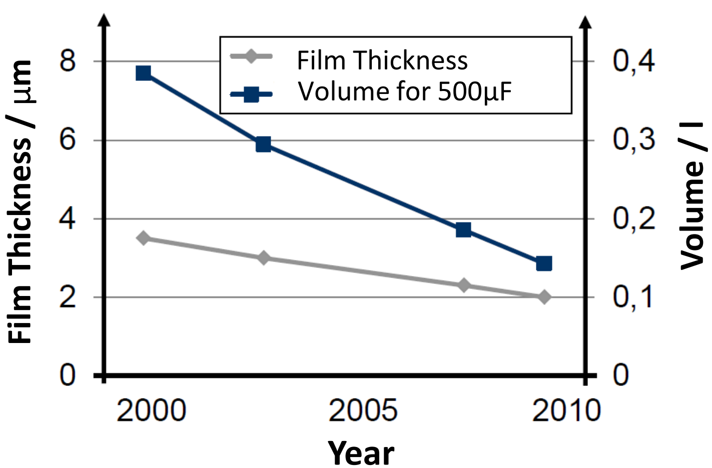
- Relatively (Slow) Technology Progress
- Recently Significant Improvement (Packaging) – e.g. CeraLink

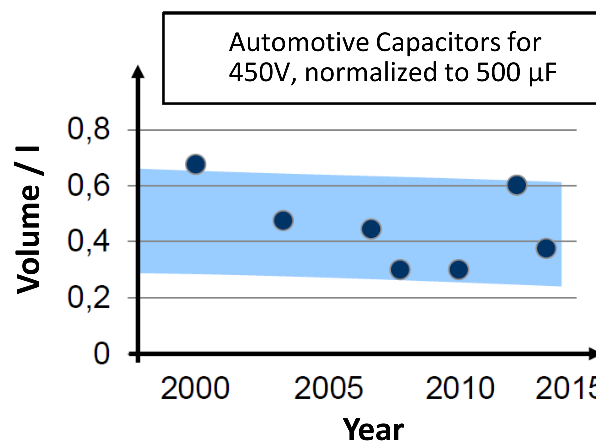
– Foil Capacitors

OPP = Oriented Polypropylene
PHD = Advanced OPP
COC = Cycloolefine Copolymers

Source: EPCOS

	2000	2005	2010	2015
Energy Density	100%	100%	110%	120%
Film Material	OPP	PHD	COC	?
Max. Temperature	105 °C	115 °C	150 °C	160 °C
Self Inductance	60 nH	30 nH	15 nH	10 nH

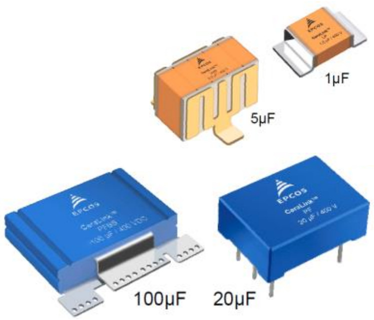




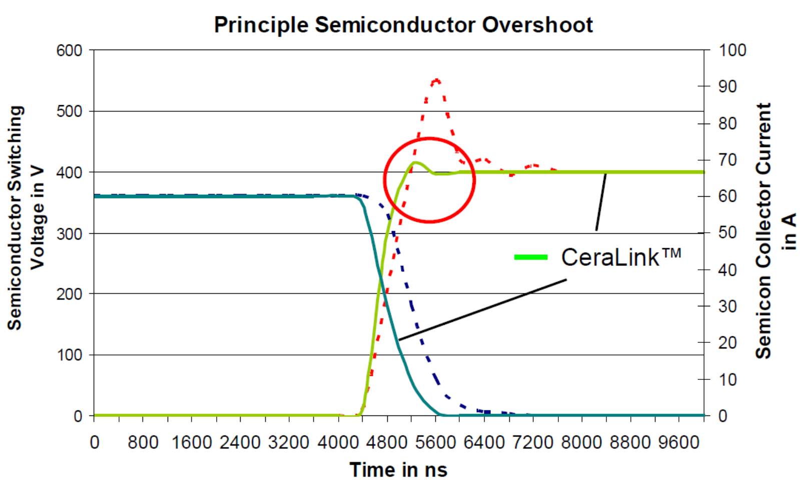
Source:
Dr. Plikat et al.
Volkswagen AG
PCIM 2013

▶ Power Chip (Foil) Capacitors

- Targeting Automotive Applications up to 90kW
- High Voltage Ratings / High Current Densities (>2A/µF)
- Low Volume / High Volume Utilization Factor
- Low Ind. Busbar Connection / Low Switching Overshoot

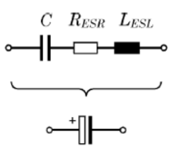


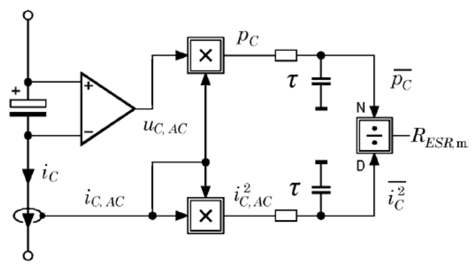
Source: EPCOS TDK

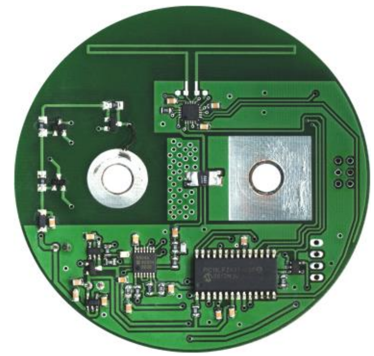


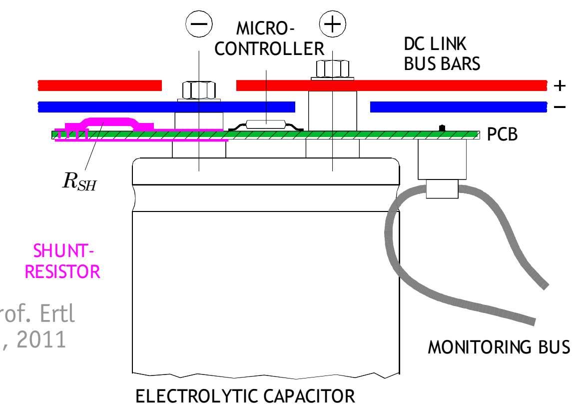
▶ Condition Monitoring of DC Link Capacitors

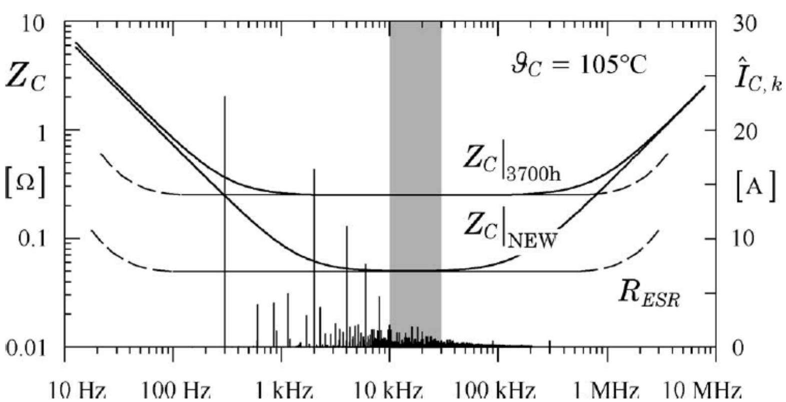
- On-Line Measurement of the ESR in "Frequency Window" (Temp. Compensated)
- Data Transfer by Optical Fibre or Near-Field RF Link
- Possible Integration into Capacitor Housing or PCB
- Additionally features Series Connect. Voltage Balancing











Source: Prof. Ertl
TU Vienna, 2011

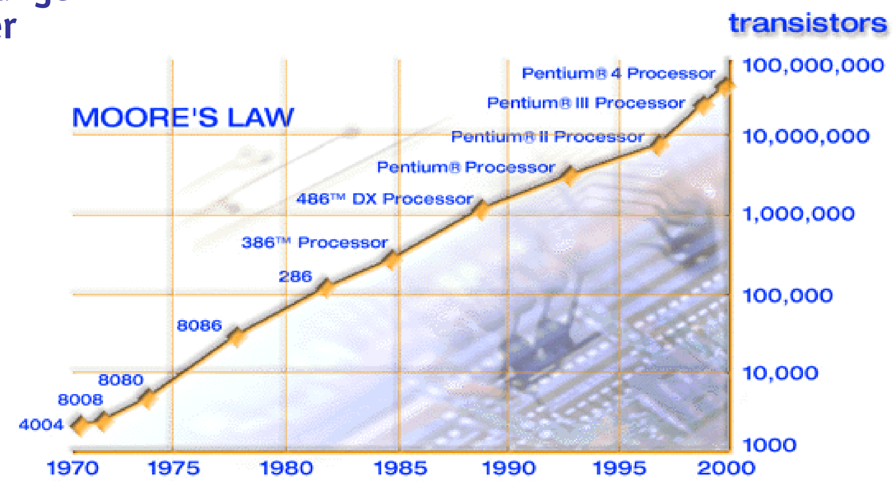
▶ Magnetics

→ **There is No "Moore's Law" in Power Electronics !**

■ **Example: Scaling Law of Transformers**

$$A_{Core} A_{Wdg} = \frac{\sqrt{2}}{\pi} \frac{P_t}{k_W J_{rms} \hat{B}_{max} f}$$

$\hat{B}_{max}$ ... Relatively Slow Technology Progress
J_{rms} ... Limited by Conductivity – No Change
f ... Limited by HF Losses & Converter
& General Thermal Limit



■ **No Fundamentally New Concepts of**

→ **We have to Hope for Progress in Material Science**

▶ Magnetics

→ **There is No "Moore's Law" in Power Electronics !**

■ **Example: Scaling Law of Transformers**

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f ... Limited by HF Losses & Converter & General Thermal Limit

■ **No Fundamentally New Concepts of**

→ **We have to Hope for Progress in Material Science (Magnetic, Thermal – Could take > 10Years)**

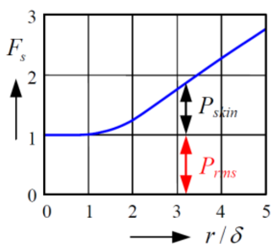
▶ Operation Frequency Limit

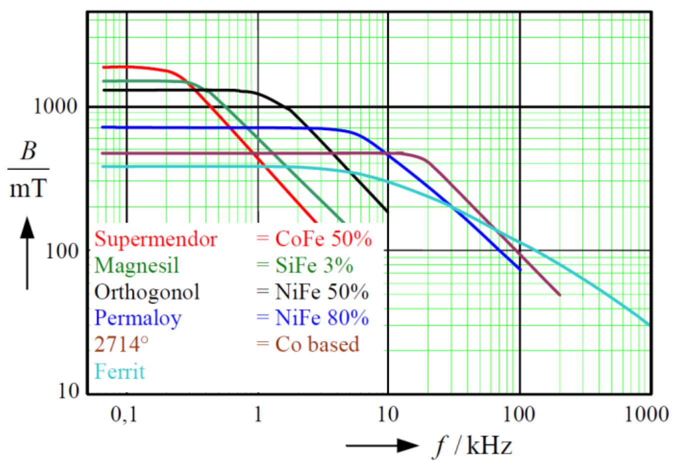
■ Serious Limitation of Operating Frequency by HF Losses

Source: Prof. Albach, 2011

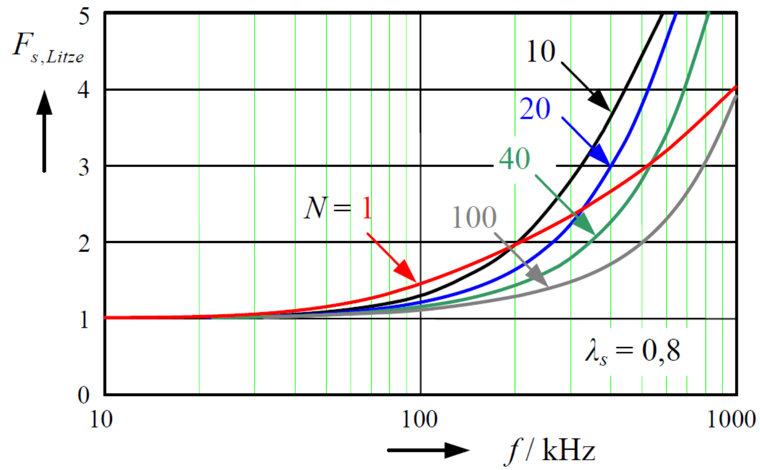
- Core Losses (incr. @ High Frequ. & High Operating Temp.)
- Temp. Dependent Lifetime of the Core
- Skin-Effect Losses
- Proximity Effect Losses

$r_s = r / \sqrt{N}$





■ Adm. Flux Density for given Loss Density



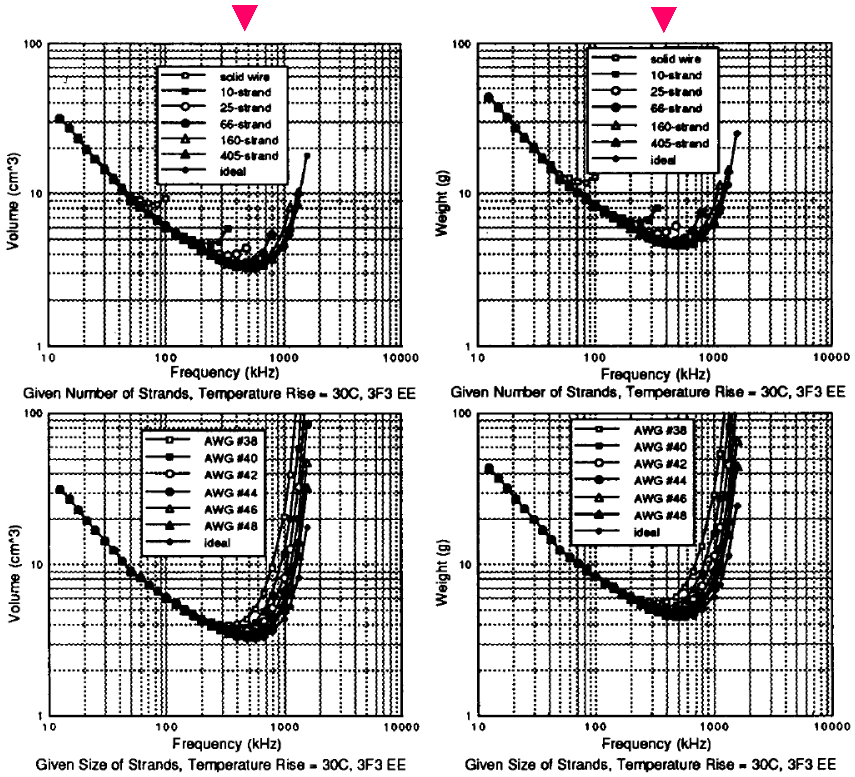
■ Skin-Factor F_s for Litz Wires with N Strands

▶ Operation Frequency Limit

■ **Relationship of Volume and Weight vs. Frequency**

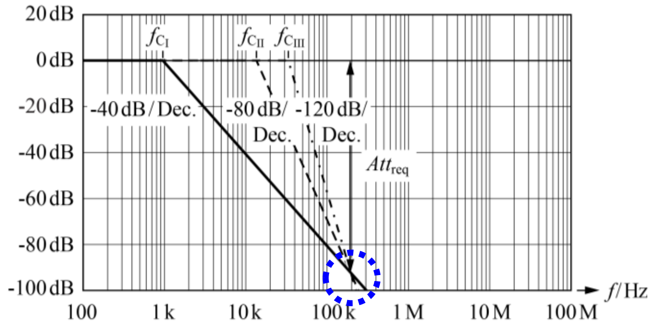
— **Higher Frequency Results in Smaller Transformer Size only Up to Certain Limit**
— **Opt. Frequencies for Min. Weight and Min. Volume (!)**

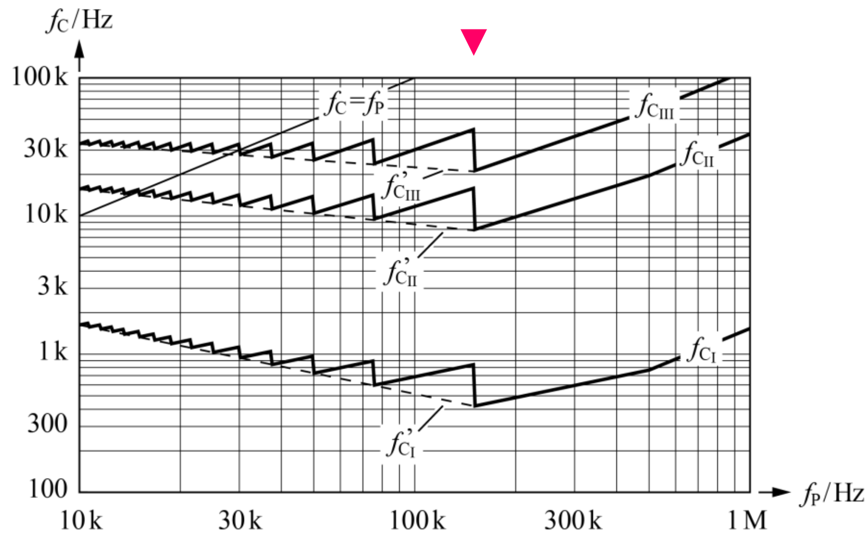
Source: Philips



■ 100Vx1A 1.1 Transformers, 3F3, 30°C Temp. Rise

Required EMI Filter Attenuation

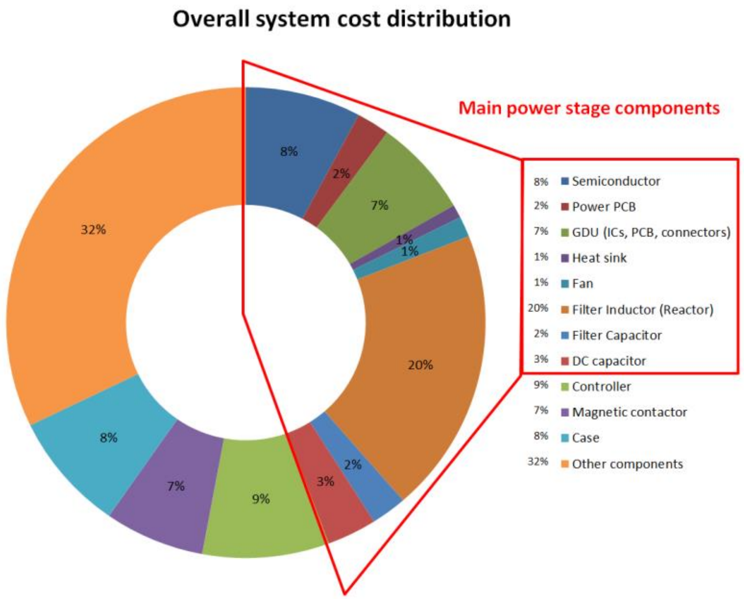


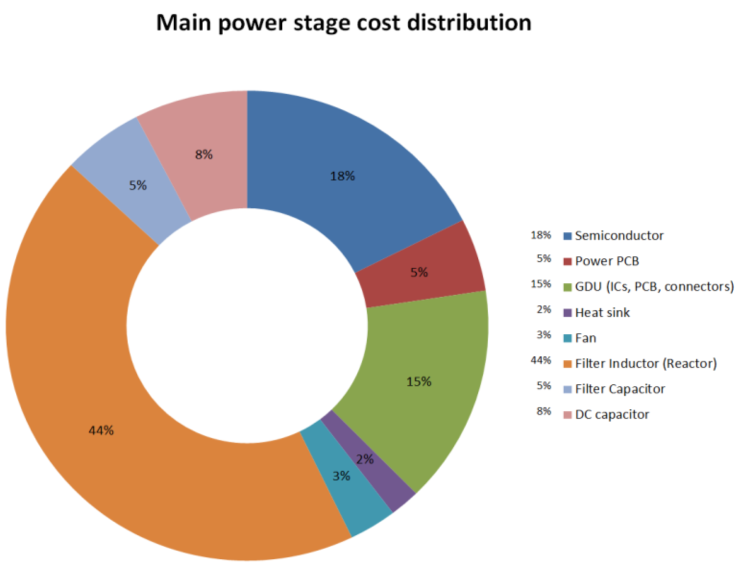


► **Higher Switching Frequ. Increases Required Att.** → **Only Option f_s >500kHz**

▶ Influence of Magnetics on System Costs

- **Example of 20kVA UPS System (Single-Stage Output Filter)**

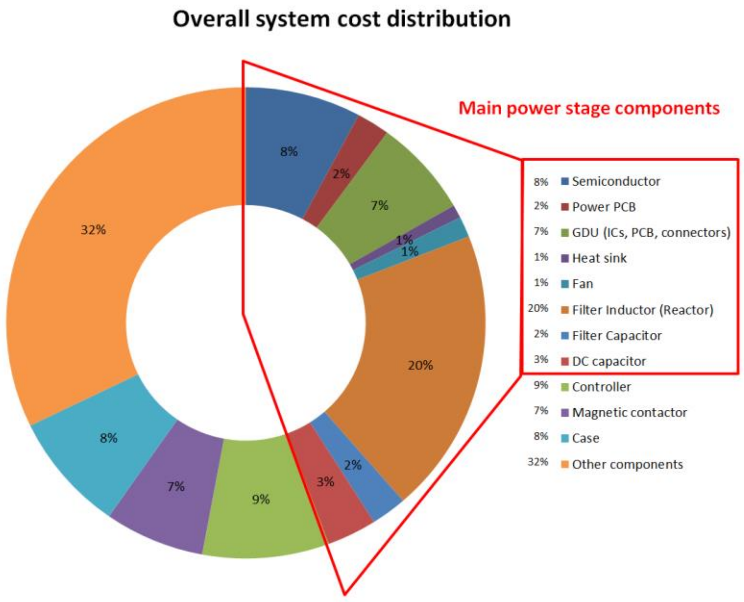




- **44% of Main Power Stage Costs (!)**

▶ Influence of Magnetics on System Costs

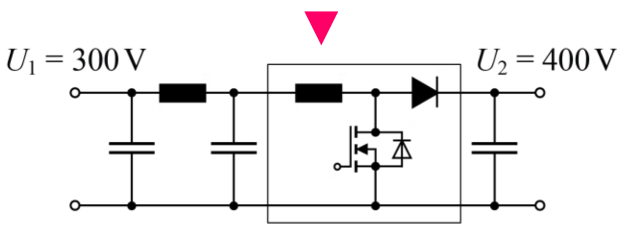
- Example of 20kVA UPS System (Single-Stage Output Filter)

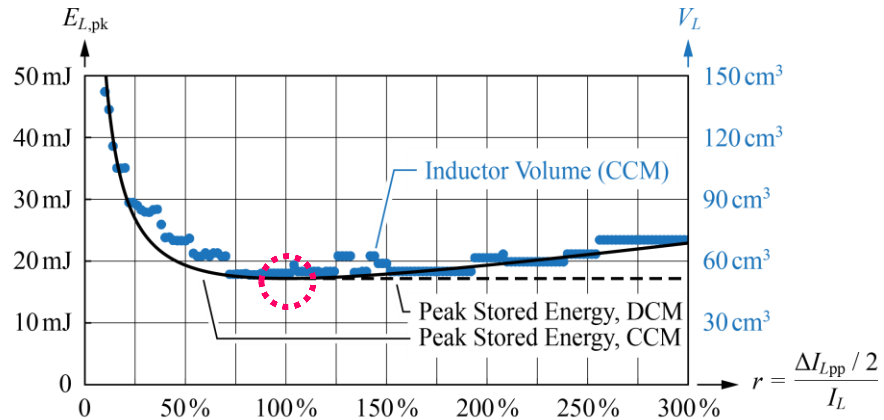


- 44% of Main Power Stage Costs (!)

▶ Energy Storage and Volume of Inductors

■ Example of DC/DC Boost Converter





$300\,V \rightarrow 400\,V$ @ $3.3\,kW$, $f_s = 48\,kHz$

■ **Minimize Magn. Volume for High Relative Current Ripple (DCM) & HF**

Σ Magnetics Capacitors

- Large Volume Share / Cost Factor
- Only Gradual Improvements

→ Magnetics
- Careful Design Absolutely Mandatory (!)
- Hope for Adv. Power Transformer Materials
- Improved Heat Management
- Magnetic Integration or DCM
- RF Air Core Inductors - Shielding (!)
- Integration of Sensors etc.

→ Capacitors
- High Frequ. Operation for Minim. Vol. (e.g. DC Link)
- Hope for Adv. Dielectrics
- Improved Heat Management
- Local Lifetime Monitoring

Converter Topologies

History and Development of the Electronic Power Converter

E. F. W. ALEXANDERSON
FELLOW AIEE

E. L. PHILLIPI
NONMEMBER AIEE

THE TERM "electronic power converter" needs some definition. The object may be to convert power from direct current to alternating current for d-c power transmission, or to convert power from one frequency into another, or to serve as a commutator for operating an a-c motor at variable speed, or for transforming high-voltage direct current into low-voltage direct current. Other objectives may be mentioned. It is thus evidently not the objective but the means which characterizes the electronic power converter. Other names have been used tentatively but have not been accepted. The emphasis is on electronic means and the term is limited to conversion of power as distinguished from electric energy for purposes of communication. Thus the name is a definition.

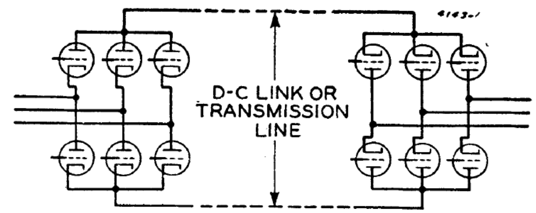


Figure 1. Electronic converter, dual-conversion type

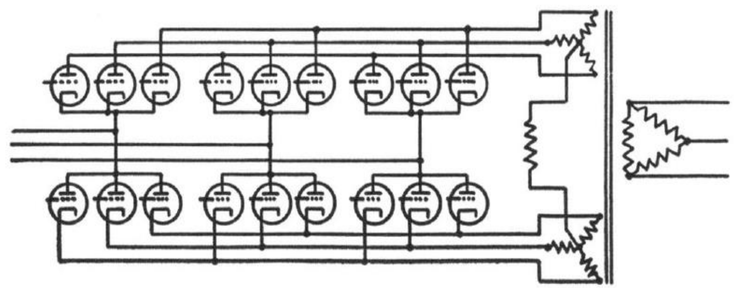
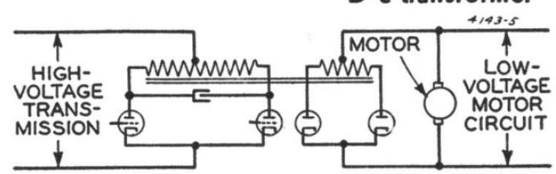


Figure 4 (left). Single - conversion-type frequency changer

Figure 5 (below). D-c transformer



Paper 44-143, recommended by the AIEE committee on electronics for presentation at the AIEE summer technical meeting, St. Louis, Mo., June 26–30, 1944. Manuscript submitted April 25, 1944; made available for printing May 18, 1944.

E. F. W. Alexanderson and E. L. Phillipi are with the General Electric Company, Schenectady, N. Y.

1944 !

United States Patent [19] [11] **4,412,277**

Mitchell [45] **Oct. 25, 1983**

1983 !

[54] **AC-DC CONVERTER HAVING AN IMPROVED POWER FACTOR**

[75] Inventor: **Daniel M. Mitchell,** Cedar Rapids, Iowa

[73] Assignee: **Rockwell International Corporation,** El Segundo, Calif.

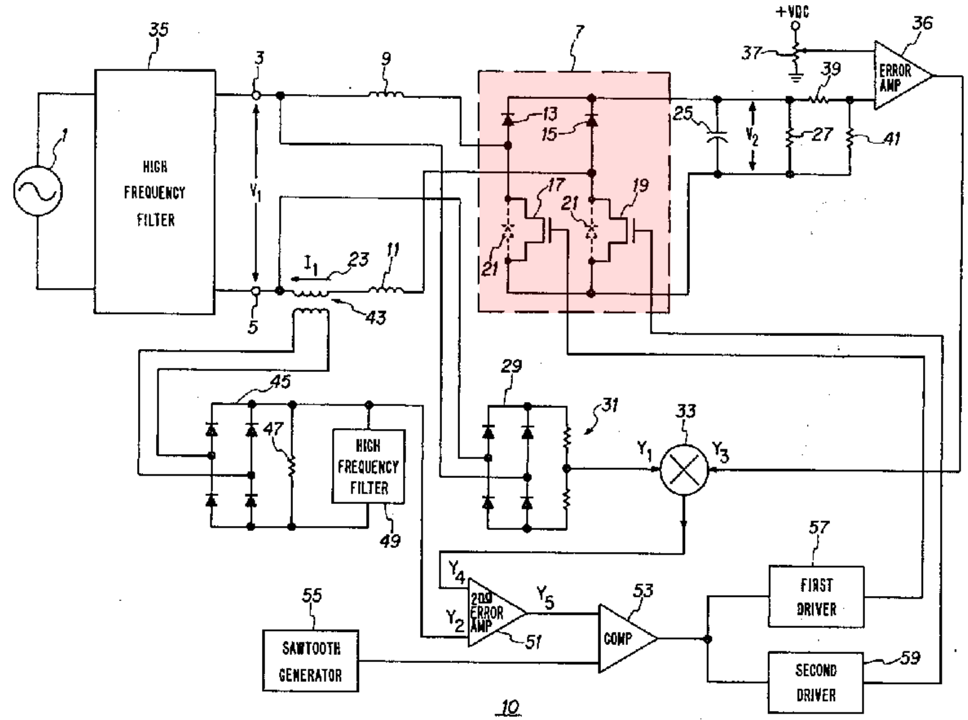
[21] Appl. No.: **414,757**

[22] Filed: **Sep. 3, 1982**

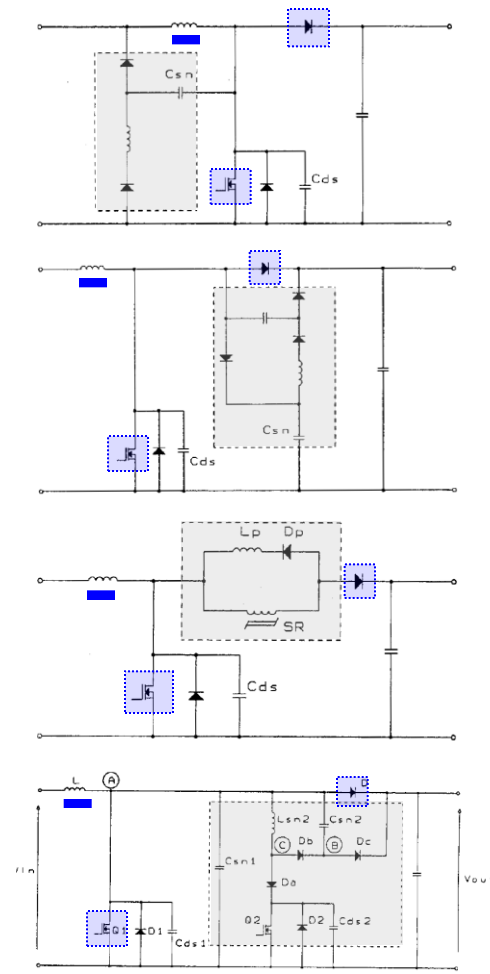
[57] **ABSTRACT**

An AC to DC converter utilizes a first power converter for converting an AC signal to a DC signal under the control of a control signal. The control signal is generated by a control circuit that includes a first analog generator that provides a first signal that is analogous to the voltage of the AC signal that is to be converted. A second analog generator generates a second signal that is analogous to the current of the AC signal that is to be converted and a third analog generator generates a third signal that is analogous to the voltage of the DC output signal. The third signal and the first signal are multiplied together to obtain a fourth signal. The control signal is generated from the fourth signal and the second signal and is used to control the power converter such that the waveform of the current of the AC signal is limited to a sinusoidal waveform of the same frequency and phase as the AC signal.

8 Claims, 2 Drawing Figures

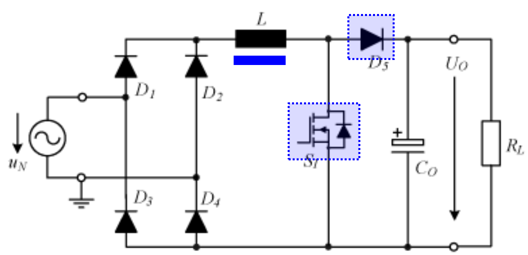


▶ Auxiliary Circuits (1)



R. Streit/
D. Tollik 1992

– **Example: 1-ph. Telekom Boost-Type PFC Rectifier**

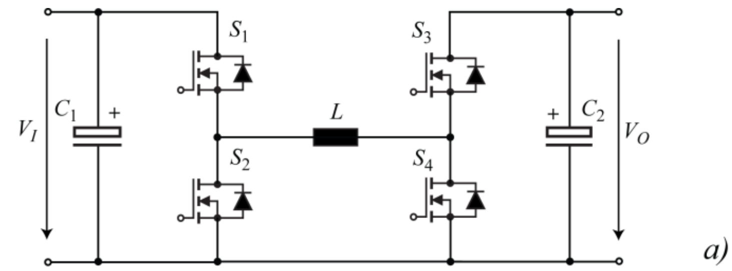


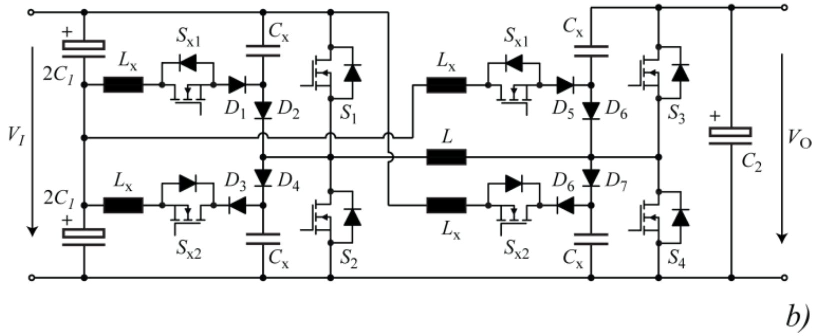
- **Complexity Increases Exp. if "Natural" Limit of a Technology is Approached**
- **Next Step in Semiconductor Technologies Makes Snubbers Obsolete → SiC Diodes**

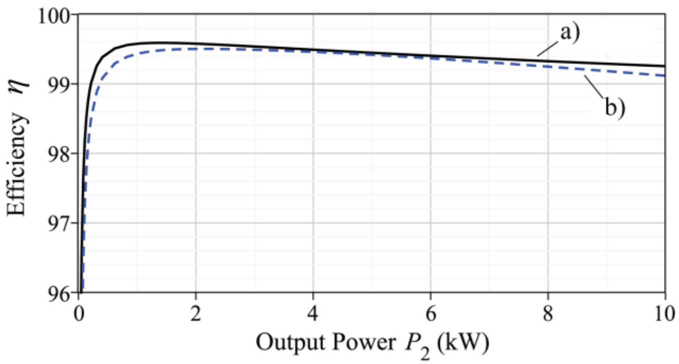
▶ Auxiliary Circuits (2)

– **Example: Non-Isolated Buck+Boost DC-DC Converter for Automotive Applications**

98% Efficiency
29kW/dm³







■ Instead of Adding Aux. Circuits
Change Operation of BASIC (!) Structure –
"Natural" Performance Limit

▶ New Converter Topologies

- **Very Large Number of Options !**

  – **Example**

IEEE TRANSACTIONS ON POWER ELECTRONICS, VOL. 7, NO. 1, JANUARY 1992

Topologies for Three-Element Resonant Converters

Rudolf P. Severns

  – **26 out of 48 Topologies are of Potential Interest**

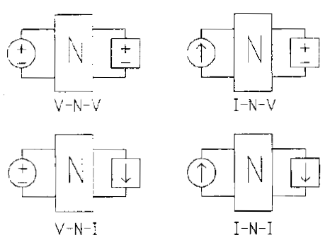


Fig. 13. Source-network-load combinations.

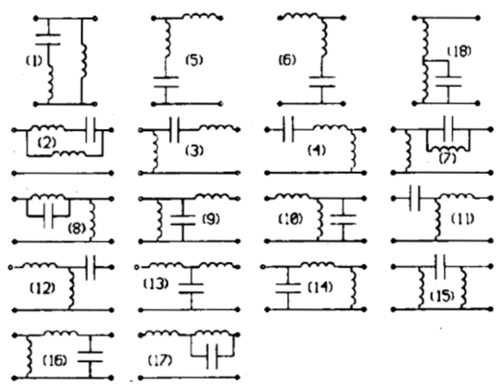


Fig. 17. Networks with 2L and 1C.

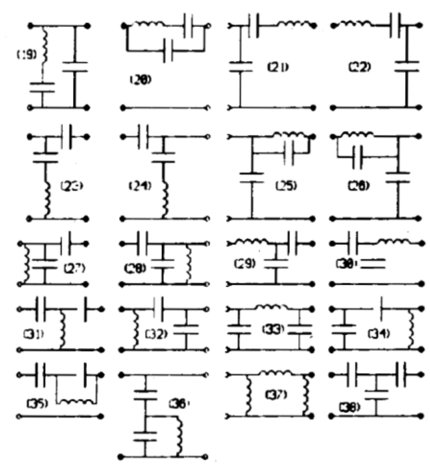
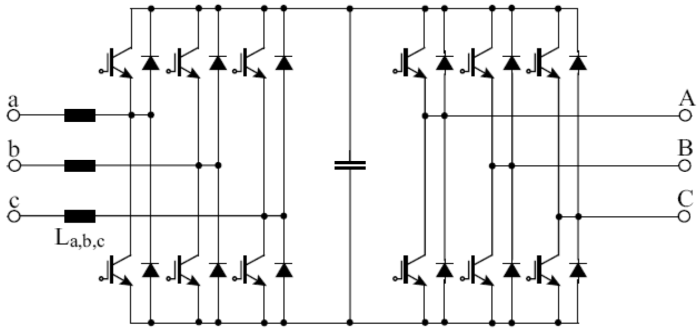


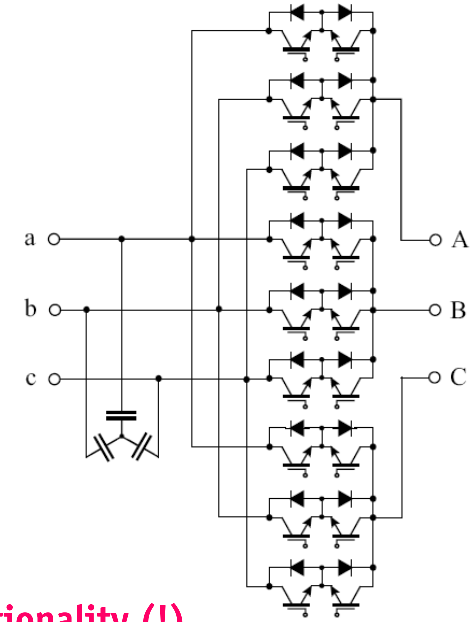
Fig. 18. Networks with 2C + 1L, 3C, and 3L.

- **Not New Topologies but Tools for Comprehensive Comp. Eval. Urgently Needed !**

▶ Integration of Functions

— **Examples:**
* Single-Stage Approaches / Matrix Converters
* Multi-Functional Utilization (Machine as Inductor of DC/DC Conv.)
* etc.

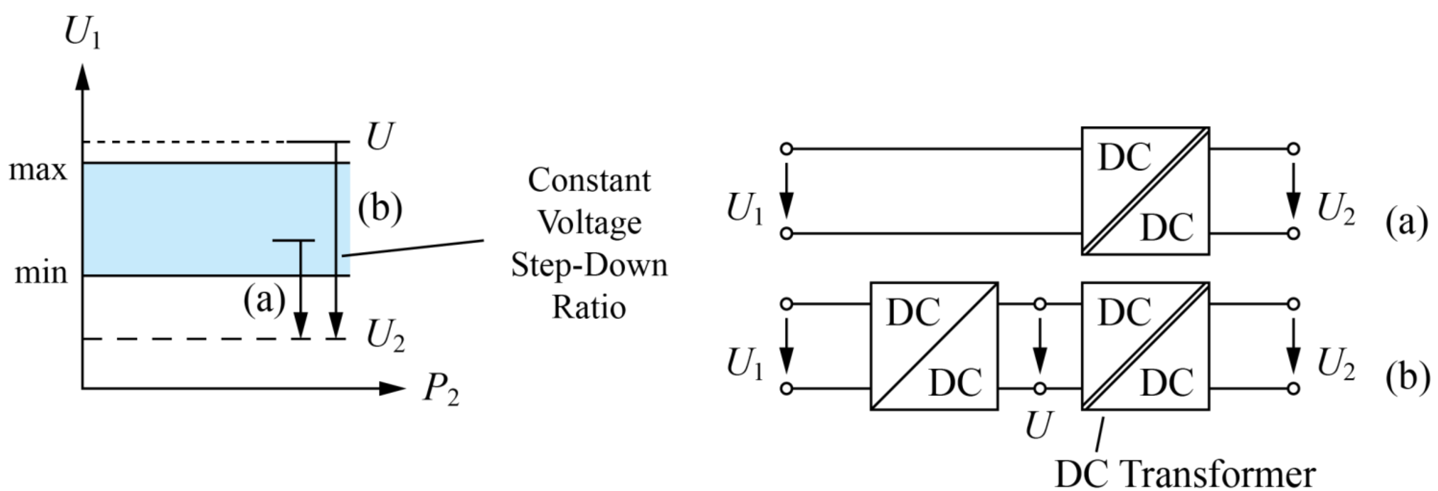




- Integration Restricts Controllability / Overall Functionality (!)
- Typ. Lower Performance / Higher Control Compl. of Integr. Solution
- Basic Physical Properties remain Unchanged (e.g. Filtering Effort)

▶ Extreme Restriction of Functionality

- Highly Optimized Specific Functionality → High Performance for Specific Task
- Restriction of Functionality → Lower Costs

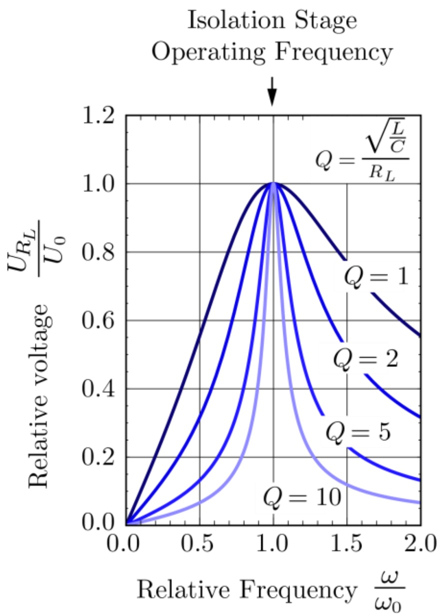


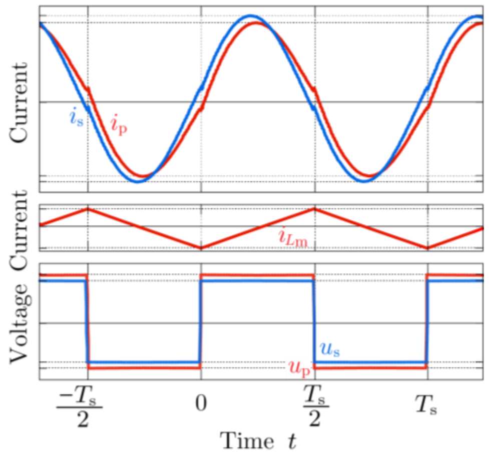
- Example of Wide Input Voltage Range Isolated DC/DC Converter

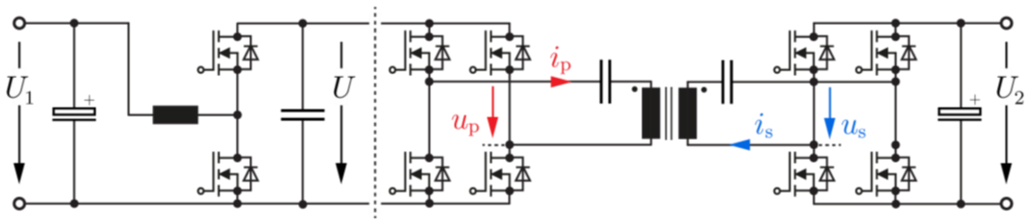
▶ Extreme Restriction of Functionality

– **Example:** DC-Transformer → Isolation @ Constant (Load Ind.) Voltage Transfer Ratio

E.g. adopted by VICOR –
"Sine Amplitude Converter" -
for Fact. Power Architecture





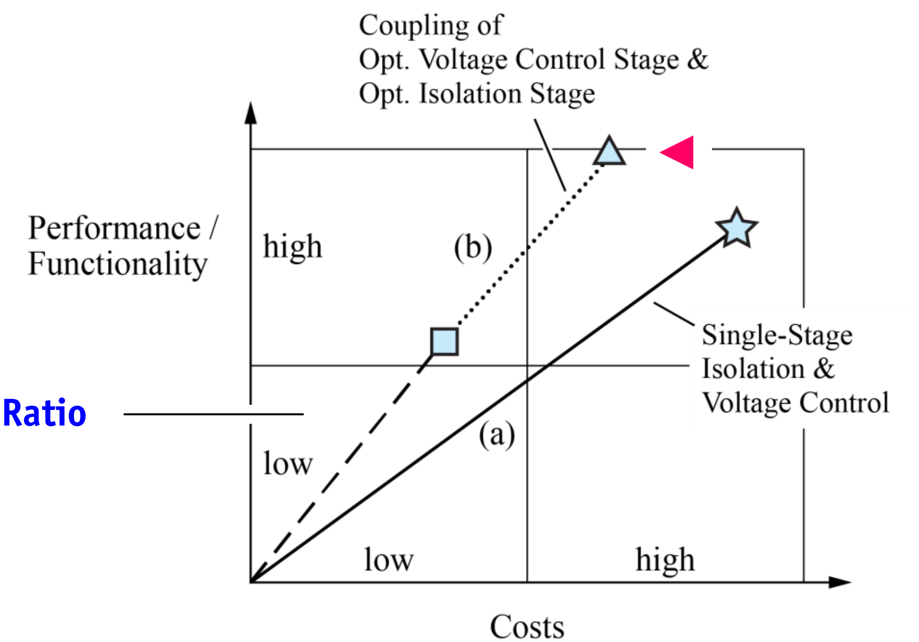


■ Resonant Frequ. ≈ Switching Frequ. → Input/Output Voltage Ratio = N_1/N_2 (Steigerwald, 1988)

▶ Extreme Restriction of Functionality

- Highly Optimized Specific Functionality → High Performance for Specific Task
- Restriction of Functionality → Lower Costs

Improved $\frac{\text{Cost}}{\text{Performance}}$ Ratio



- Cost / Performance Ratio is a Key Metric for Industry Success (Sales Argument)

Σ New Topologies

→ **Some Exceptions**

- Multi-Cell Converters
- 3-ph. AC/DC Buck Converter
- etc.

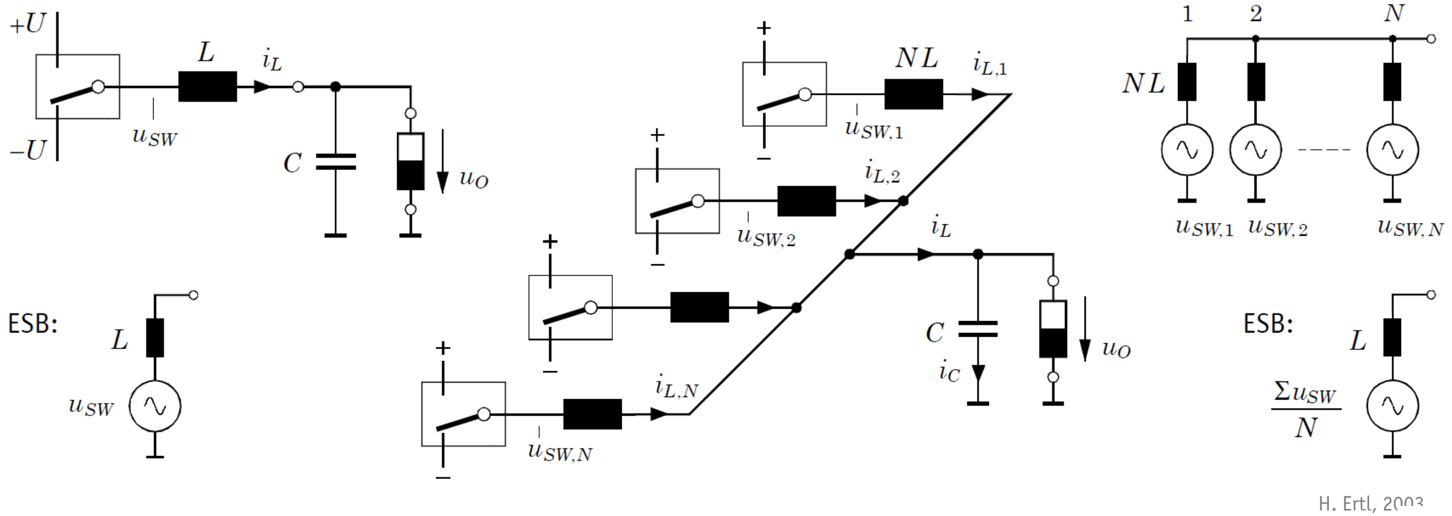
Multi-Cell Converters

→ Parallel Interleaving
→ Series Interleaving

▶ Multi-Cell Converters (Homogeneous Power)

- Example of Parallel Interleaving

— Breaks the Frequency Barrier
— Breaks the Impedance Barrier
— Breaks Cost Barrier - Standardization
— High Part Load Efficiency



- Fully Benefits from Digital IC Technology (Improving in Future)
- Redundancy → Allows Large Number of Units without Impairing Reliability

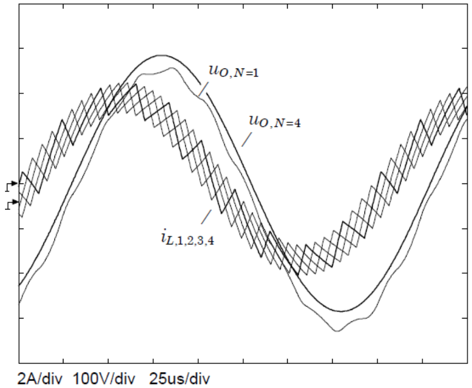
▶ Multi-Cell Converters

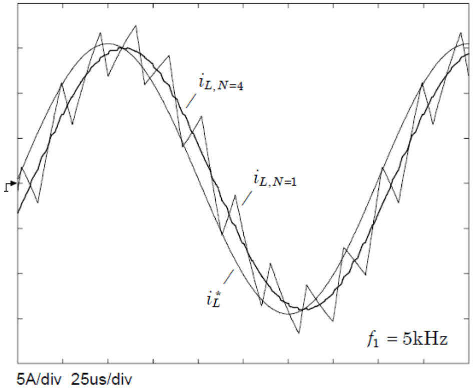
■ **Basic Concept @ Example of Parallel Interleaving**

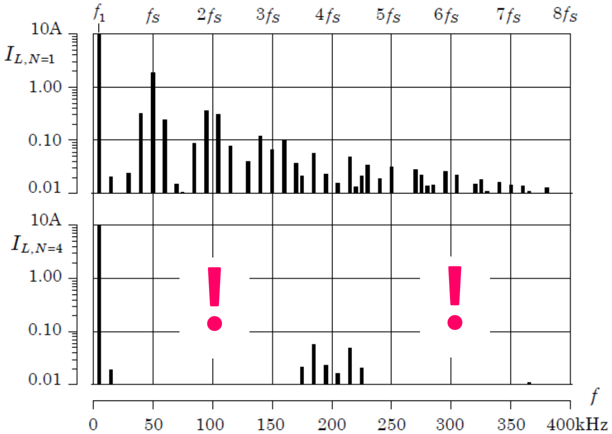
— **Multiplies Frequ. / Red. Ripple @ Same (!) Switching Losses & Incr. Control Dynamics**

$$\Delta U_{max,N} = \Delta U_{max} \cdot \frac{1}{N^3} \qquad \Delta I_{max,N} = \frac{\Delta I_{max}}{N^2}$$

H. Ertl, 2003







***N* = 3**

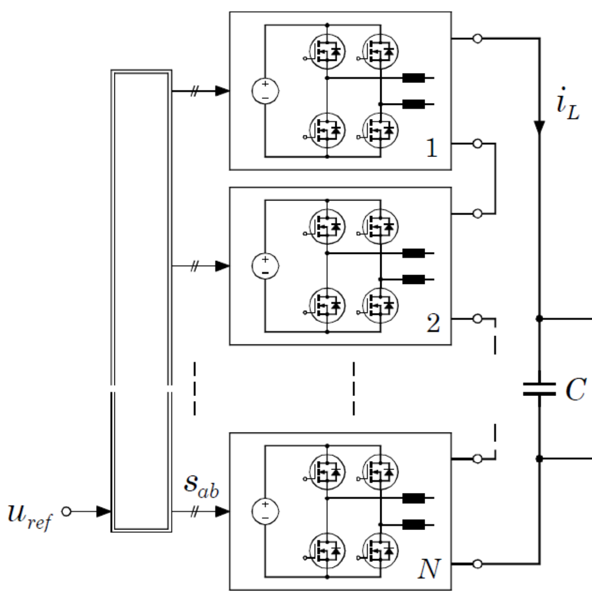
■ **Fully Benefits from Digital IC Technology (Improving in Future)**
■ **Redundancy → Allows Large Number of Units without Impairing Reliability**

▶ Multi-Cell Converters

■ **Example of Series Interleaving**

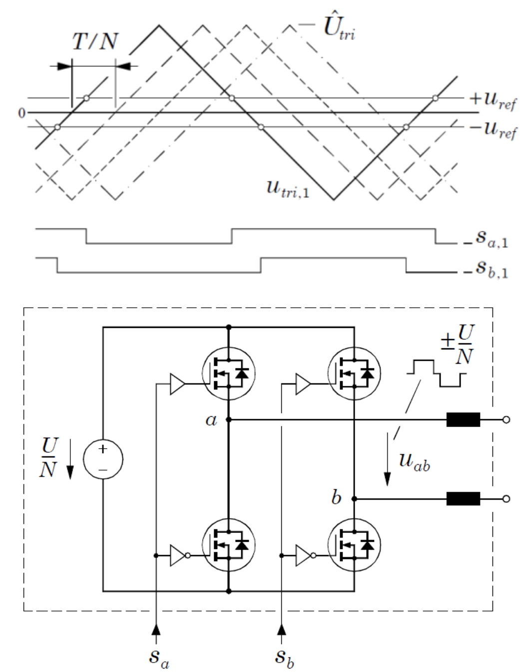
— Breaks the Frequency Barrier
— Breaks the Silicon Limit 1+1=2 NOT 4 (!)
— Breaks Cost Barrier - Standardization
— Extends LV Technology to HV

$$\frac{\Delta U_{\max,N}}{U} = \frac{\pi^2}{32}\left[\frac{f_0}{f_S}\right]^2 \cdot \frac{1}{N^3}$$



$$\frac{U}{8Lf_S}$$

$$\Delta I_{\max,N} = \frac{\Delta I_{\max}}{N^2}$$



▶ Multi-Cell Converters

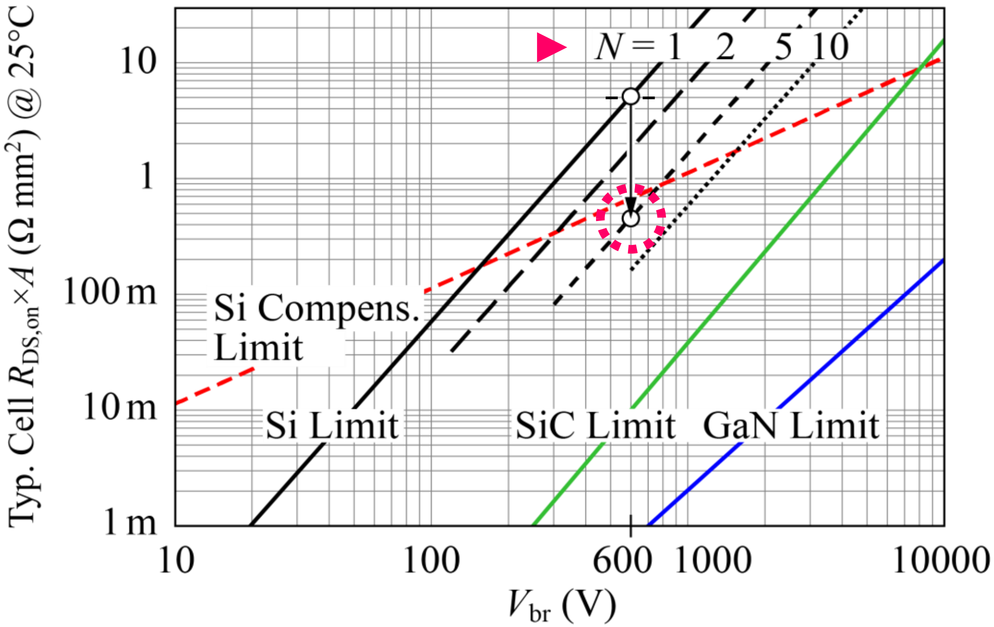
■ Series Connection of LV MOSFETs (LV Cells) Effectively *SHIFTS the Si-Limit* (!)

Assumption:

Chip Area of each LV Chip Equal to the Chip Area of the HV Chip

– Scaling of Specific On-State Resistance

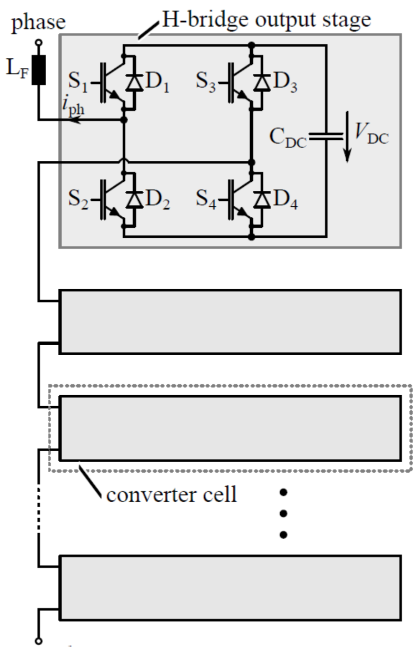
$$(R_{\mathrm{DS,on}} \times A)_{\mathrm{eff}} \approx \frac{1}{N^{1.5}} (R_{\mathrm{DS,on}} \times A)$$

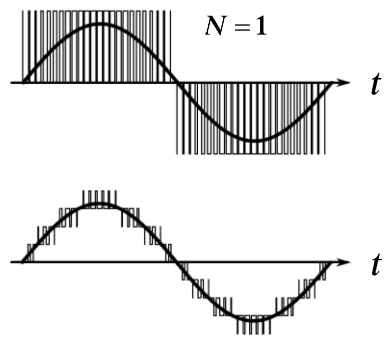


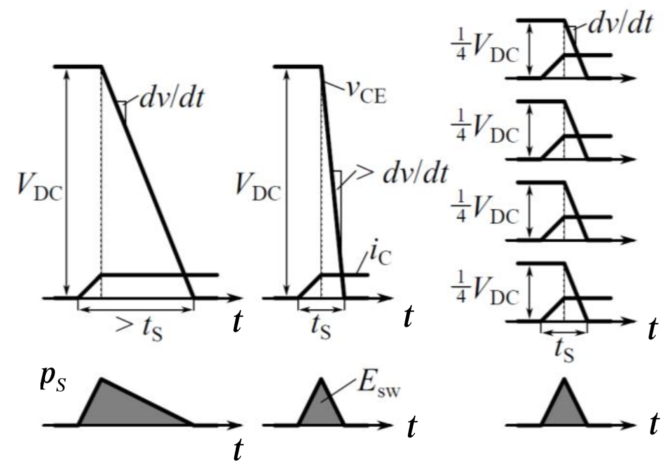
■ Excellent Opportunity for Extreme Efficiency Ultra-Compact Converters

▶ Multi-Cell Converters

- **Interleaved Series Connection Dramatically Reduces Switching Losses (or Harmonics)**







– **Scaling of Switching Losses for Equal $\Delta i/I$ and dv/dt**

$$P_{S,N} \approx P_{S,N=1} \cdot \left(\frac{1}{2N^2} \dots \frac{1}{N^3}\right)$$

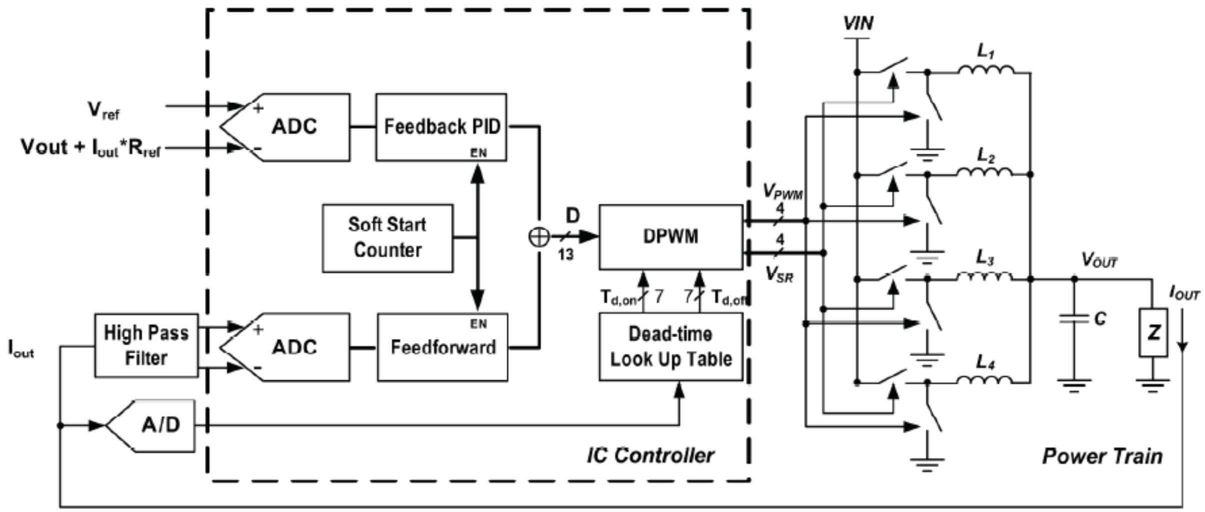
- **Converter Cells Could Operate at VERY Low Switching Frequency (e.g. 5kHz)**
- **Minimization of Passives (Filter Components)**

Examples of Multi-Cell Converters

→ VRM
→ Ultra-Efficient 1ph. PFC
→ Telecom Power Supplies

▶ Voltage Regulator Module

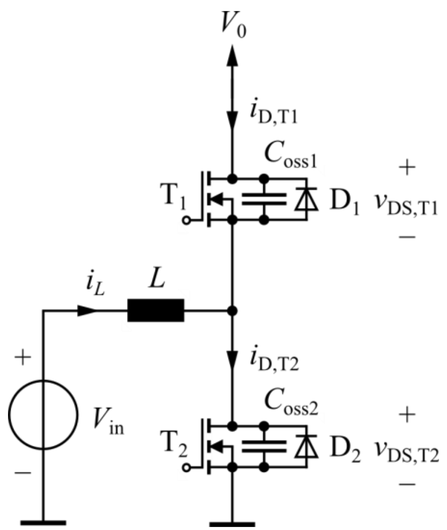
- Multi-Channel / Parallel Interleaving of up to 12 Channels

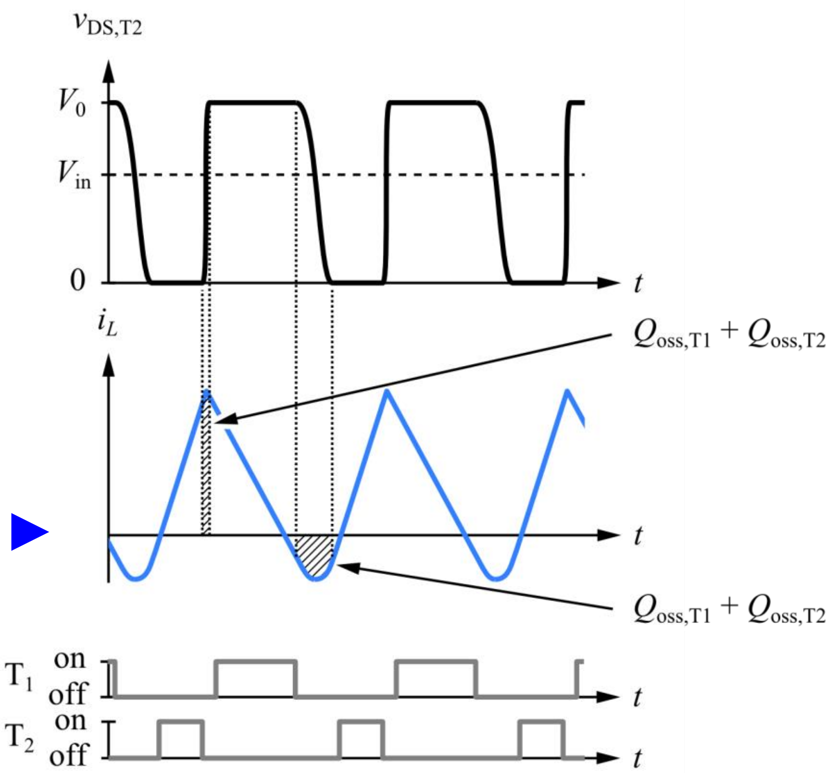


- Coupling Inductors (Interphase Inductors) allows Further Reduction of Ind. Comp. Volume
- For On-Chip Integration Challenged by Switched Capacitor Converters

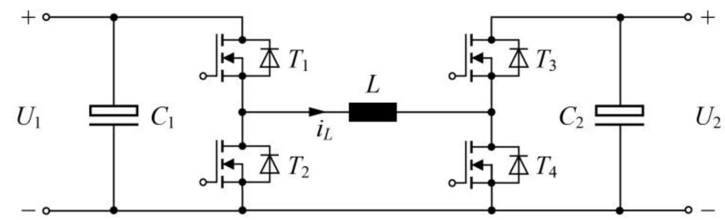
Zero Voltage Switching – Triangular Current Mode

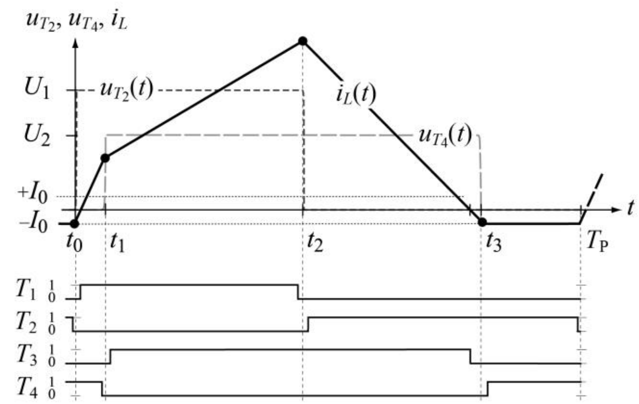
- Synchronous Rectification
- Negative Current Ensures ZVS





12kW TCM Buck+Boost DC/DC Converter





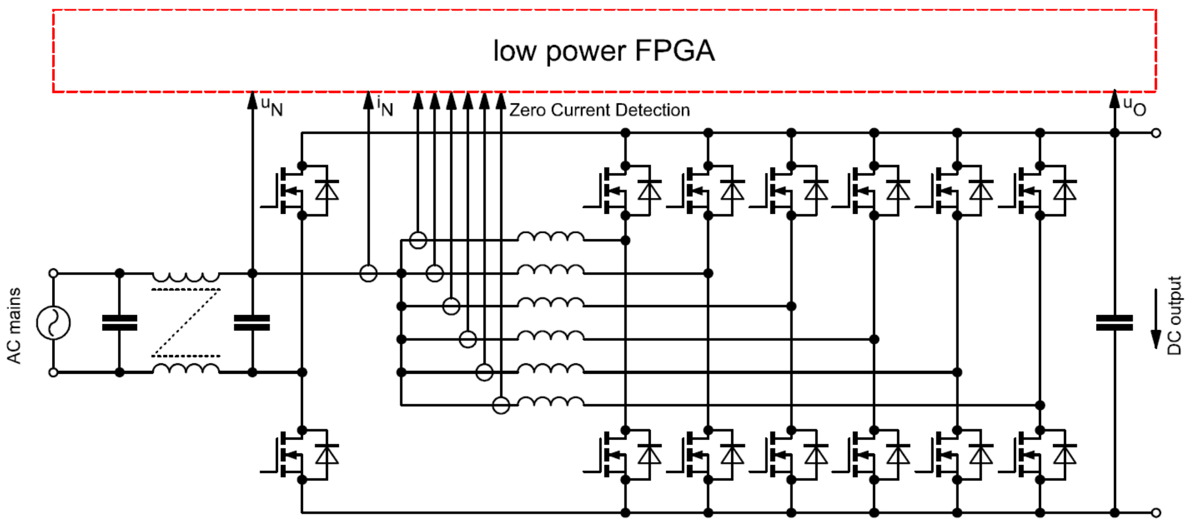
- **Overlapping Input and Output Voltage Ranges**

  U_1=150...450V
  U_2=150...450V

- **Max. Eff. = 99.3% @ 30kW/l**

► Bidirectional Ultra-Efficient 1-Φ PFC Mains Interface

★ 99.36% @ 1.2kW/dm³



- Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only

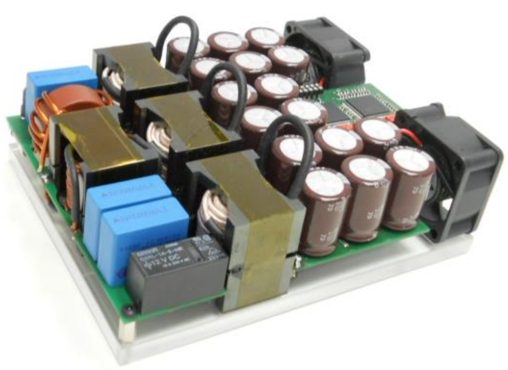
► Bidirectional Ultra-Efficient 1-Φ PFC Mains Interface

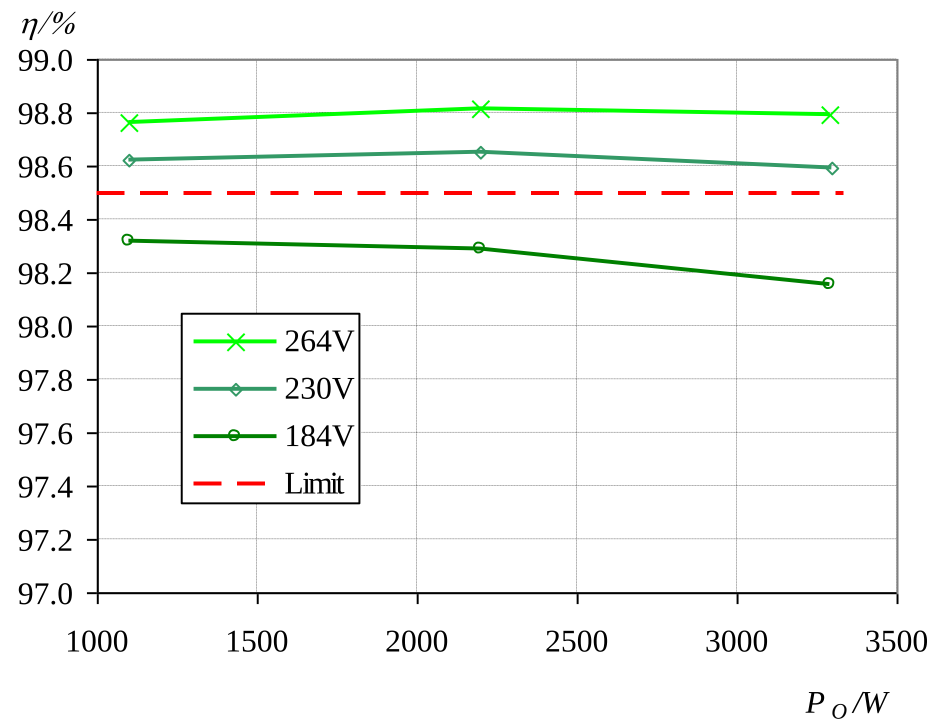
★ 99.36% @ 1.2kW/dm³

■ Employs NO SiC Power Semiconductors -- Si SJ MOSFETs only

▶ 1-Φ Telecom Boost-Type TCM PFC Rectifier

- **Input Voltage** 1-ph. 184…264V_{AC}
- **Output Voltage** 420V_{DC}
- **Rated Power** 3.3kW





★ 98.6% @ 4.5kW/dm^3

► KEYS for Achieving the Performance Improvement

… despite Using "Old" Si Technology

- ■ Basic Topology – Low Complexity
- ■ ZVS Only Achieved by Modified Operation Mode – No Aux. Circuits
- ■ Active ZVS – No (Low) Switching Losses
  – No Direct Limit of # of Parallel Trans.
- ■ Triangular Current Mode (TCM) – Simple Symm. of Loading of Modules
- ■ Variable Switching Frequency – Spread & Lower Ampl. EMI Noise
- ■ No Diode On-State Voltage Drop – Synchr. Rectification
- ■ Continuously Guided u, i Waveforms – No Free Ringing → Low EMI Filter Vol.
- ■ Interleaving – Low EMI Filter Vol. & Cap. Curr. Stress
- ■ Utilization of Low Superjunct. $R_{DS,(on)}$ – Low Cond. Losses despite TCM
- ■ Utilization of Digital Signal Processing – Low Control Effort despite 6x Interl.

… the Basic Concept is Known since 1989 (!)

Σ Topologies Modulation Schemes Control Schemes

→ **Topologies**

- Basic Concepts Extremely Well Known - Mature
- Comprehensive Comparative Evaluations Missing (!)
- Promising Multi-Cell Concepts (!)

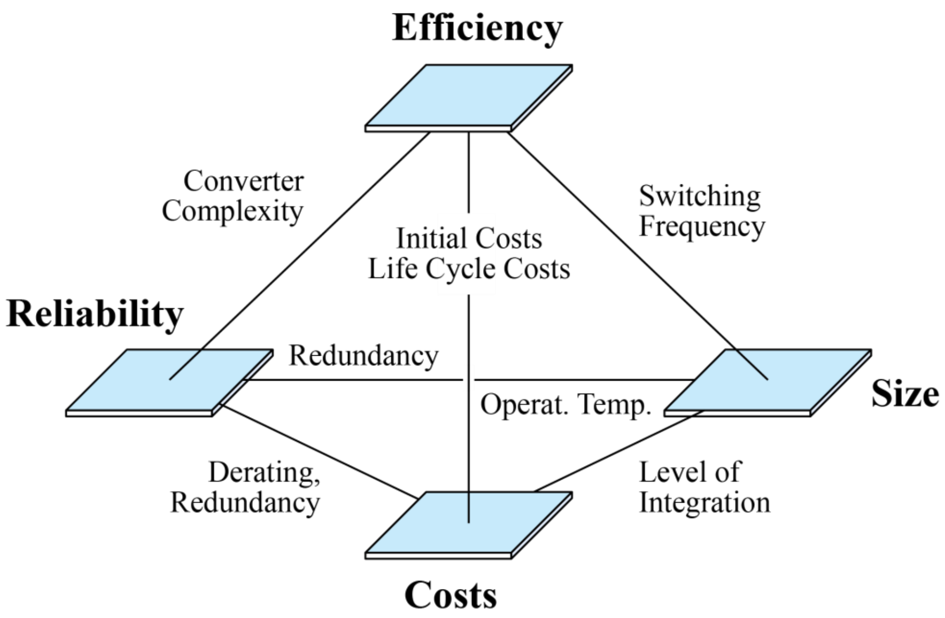
→ **Modulations / Control Schemes**

- Basic Concepts Extremely Well Known - Mature
- Digital Power – All Diff. Kinds of Functions
- PWM might be Merged with Model Pred. Control
- More "Heuristic" Control Schemes
- Model-Based Max. Utilization of Load/Line/Source
- Challenge to Guarantee Stability (!)
- Challenge of Redundancy / Safety Requirements

Advanced Design

▶ Design Challenge

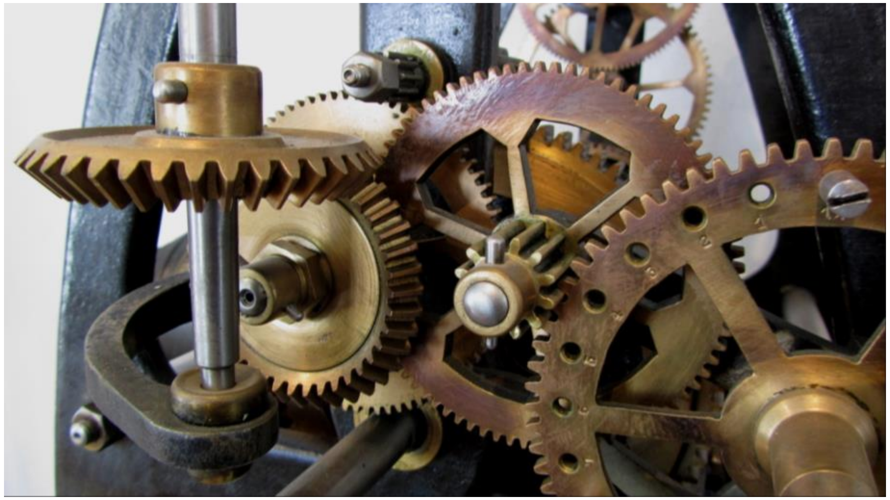
■ **Mutual Couplings of Performance Indices → Trade-Offs**



— **For Optimized System Several Performance Indices Cannot be Improved Simultaneously**

▶ Design Challenge

- Mutual Couplings of Performance Indices → Trade-Offs

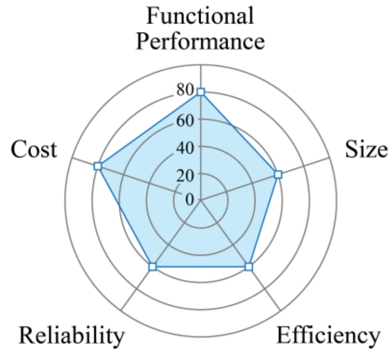


— For Optimized System Several Performance Indices Cannot be Improved Simultaneously

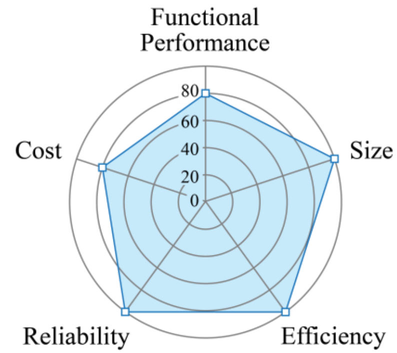
▶ Design Challenge

- **Design for Specific Performance Profiles Requires Advanced CAD Tools**

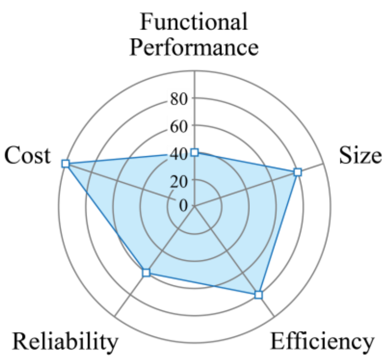
— Avoid Try-and-Error
— Minimize Design Time



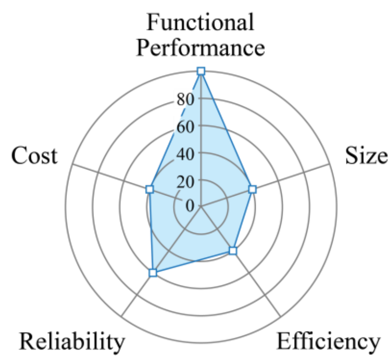
Industry Applications



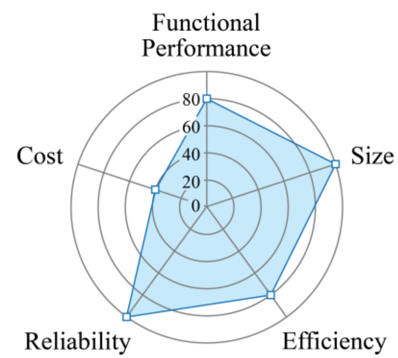
Information & Communication Industry



Domestic Applications



Laboratory Applications

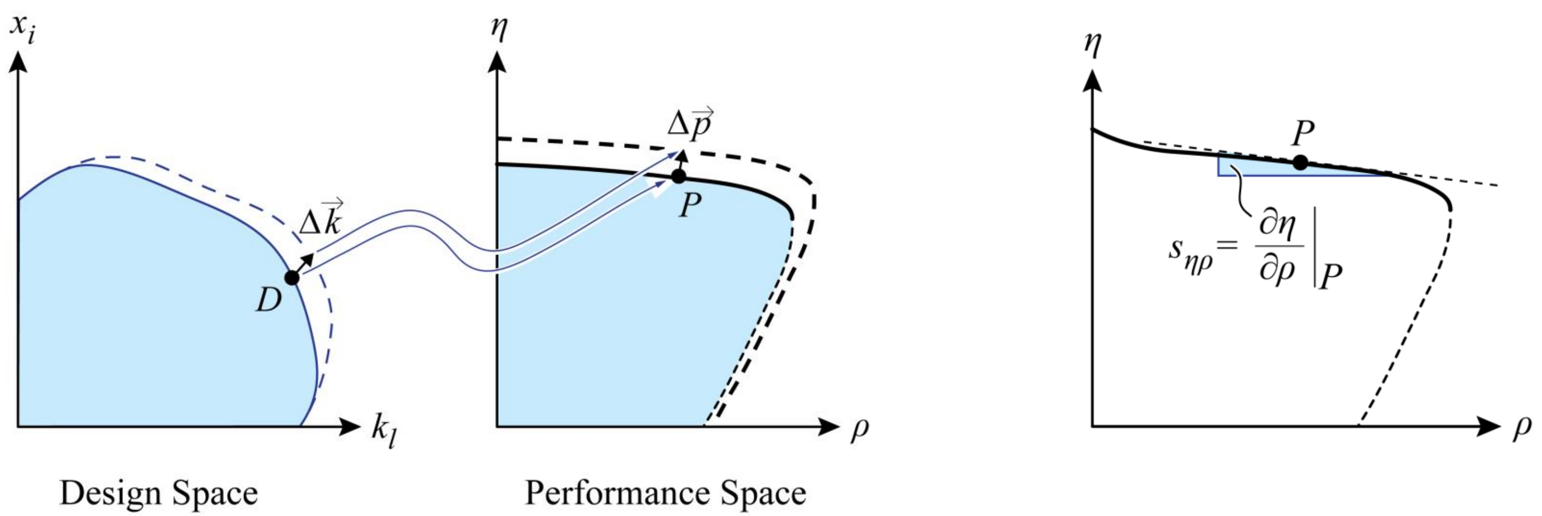


Aerospace Applications

▶ Design Challenge

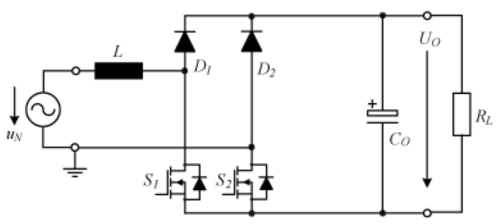
- Advanced Simulations Based Design Allows Multi-Objective Optimization
- Identifies Performance Limits → Pareto Front

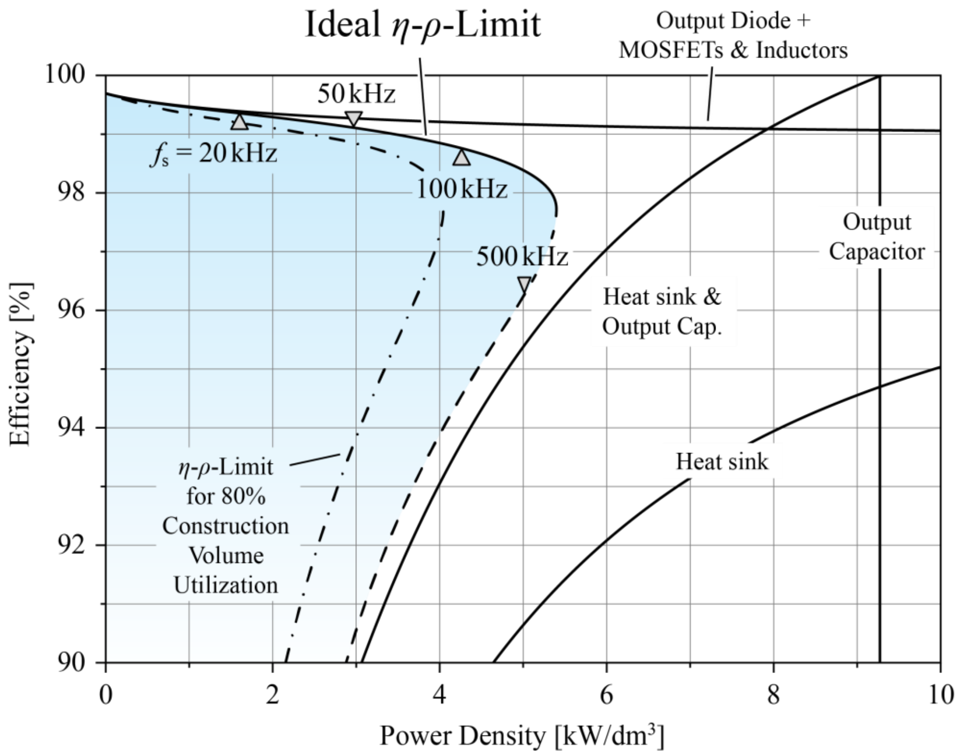
— Sensitivities to Technology Advancements (Example: η-ρ-Pareto Front)
— Trade-off Analysis



► Analysis of Performance Limits → Pareto Front

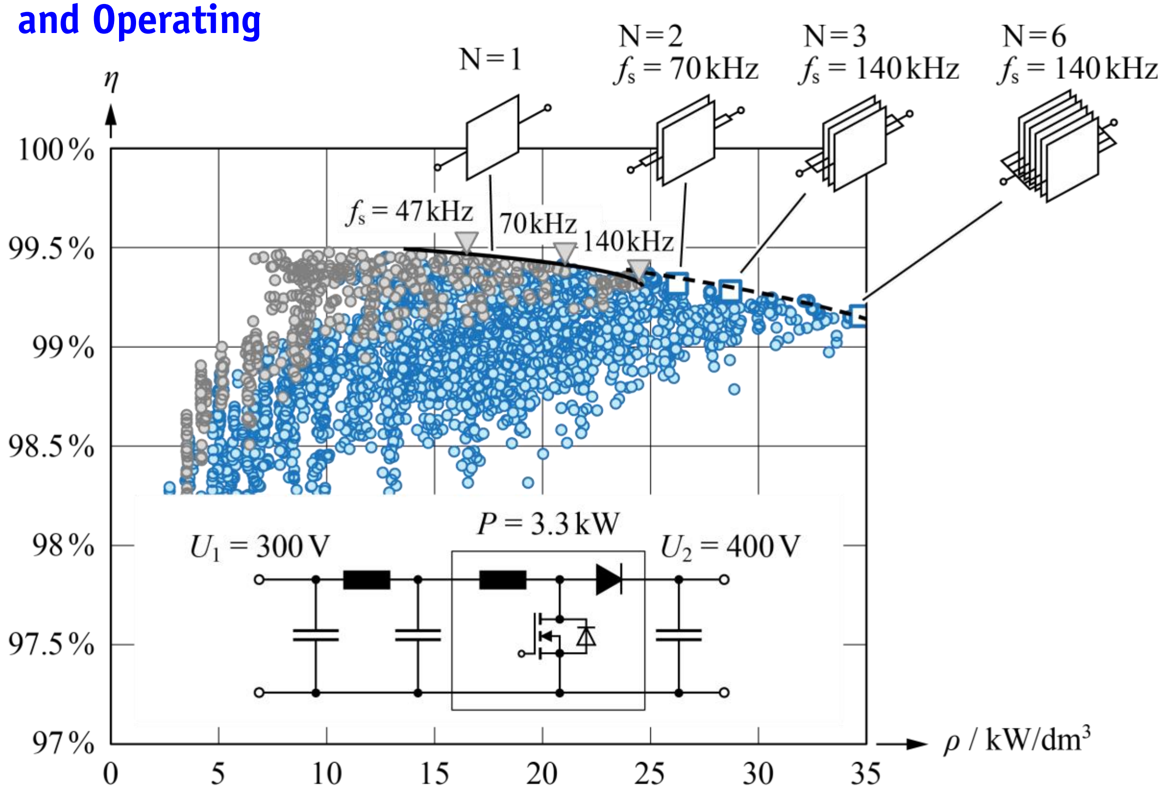
- Clarifies Influence of Main Components and Operating Parameters





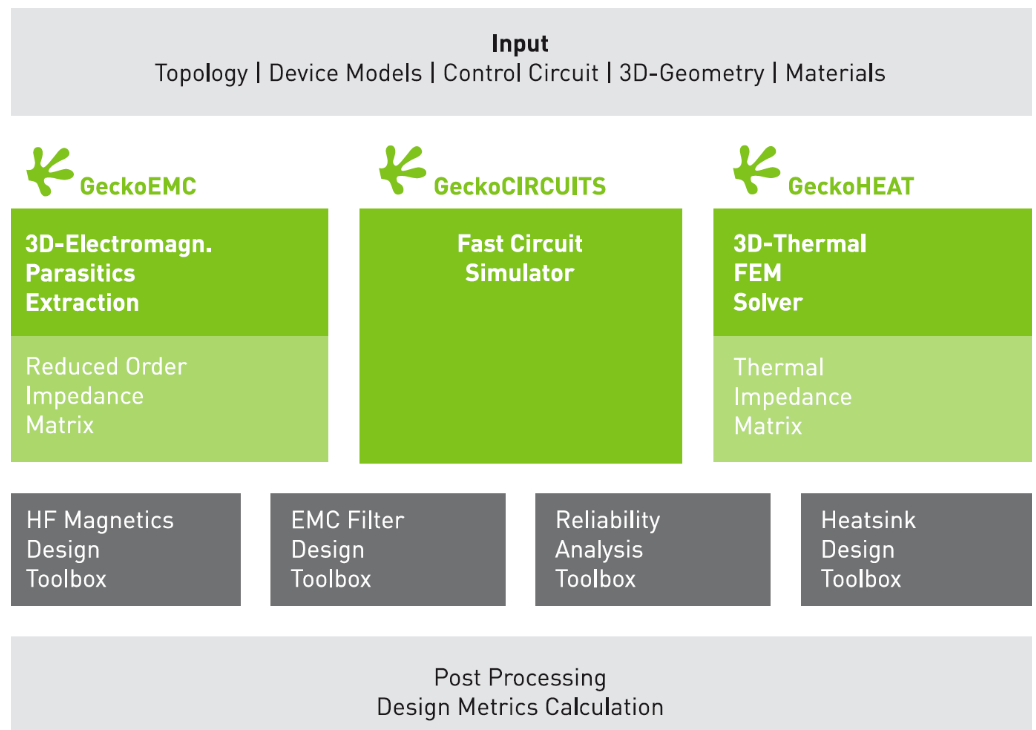
▶ Analysis of Performance Limits → Pareto Front

- Clarifies **Influence of Main Components and Operating Parameters**



▶ Example of Advanced Power Electronics Design Platform

Source: GECKO SIMULATIONS

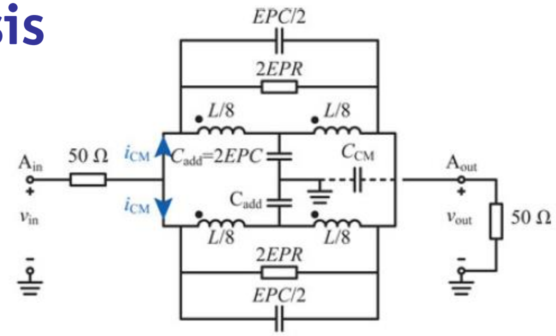


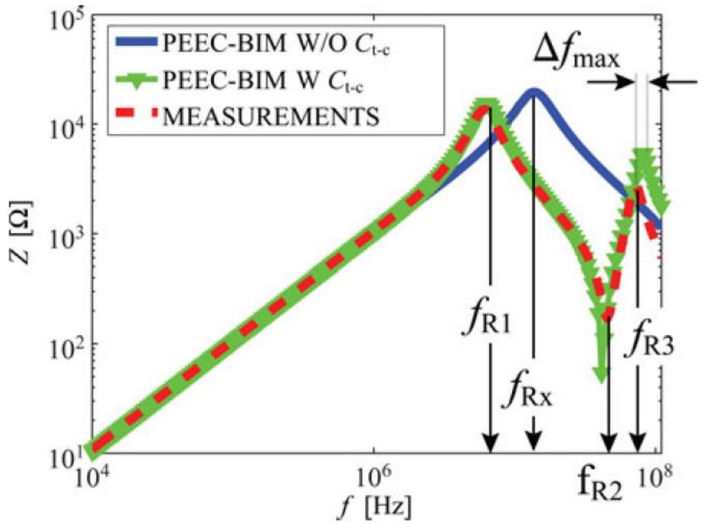
- **Modeling & Design**
  - Circuit Simulation
  - Thermal Simulation
  - EM Simulation

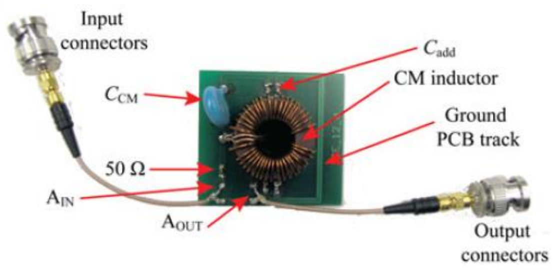
▶ Example – Electromagnetic Analysis

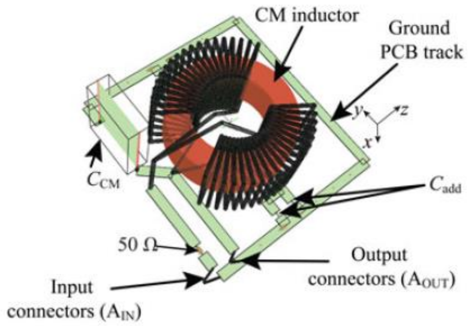
- **GeckoEMC - PEEC Based**

— Analysis of Parasitic Parallel Winding Cap. Cancellation of CM Inductor



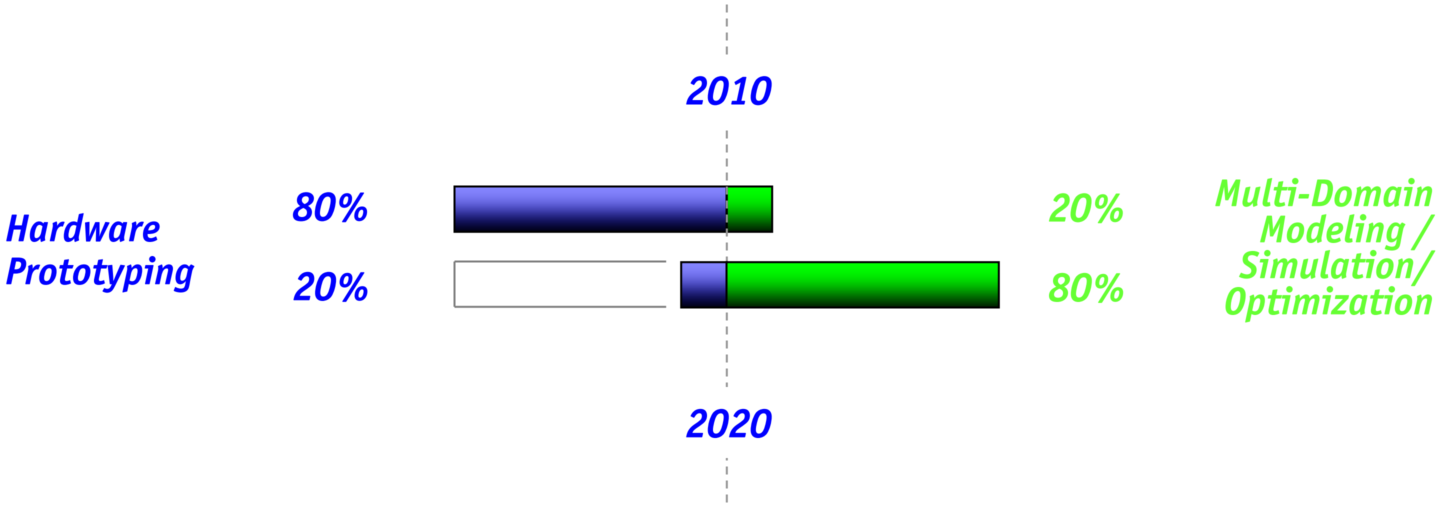






▶ Future Design Process

■ **Challenge: Virtual Prototyping**



- Reduces Time-to-Market
- More Application Specific Solutions (PCB, Power Module, and even Chips)
- Only Way to Understand Mutual Dependencies of Performances / Sensitivities (!)
- Simulate What Cannot Any More be Measured (High Integration Level)

Σ

Virtual Prototyping

→ Remaining Challenges

- Comprehensive Modeling (e.g. EMI, Reliability)
- Model Order Reduction
- Minimization of Simulation Time
- Interactive Features

... will Take a "Few" More Years

“Power Electronics 1.0”

Maturing → Reduce Costs, Ensure Reliability (!)

“New Challenges”

▶ Consider Converters like "ICs"

- If Only Incremental Improvements of Converters Can Be Expected → **Shift to New Paradigm !**

$$p(t) \rightarrow \int_0^t p(t)\,\mathrm{d}t$$

- "Converter" → "Systems" (Microgrid) or "Hybrid Systems" (Autom. / Aircraft)
- "Time" → "Integral over Time"
- "Power" → "Energy"

► Consider Converters like "ICs"

- If Only Incremental Improvements of Converters Can Be Expected → **Shift to New Paradigm !**

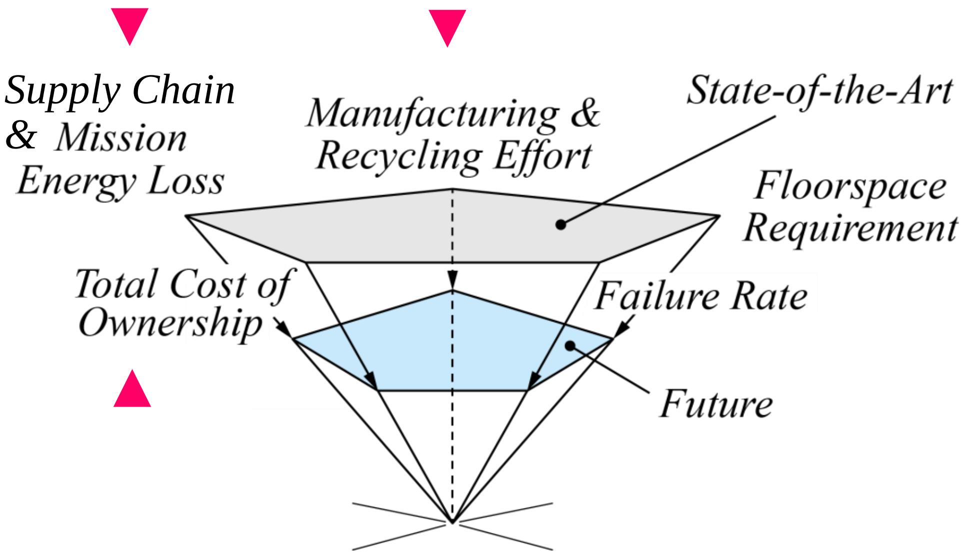
$$p(t) \rightarrow \int_0^t p(t)\,\mathrm{d}t$$

- Power Conversion → Energy Management / Distribution
- Converter Analysis → System Analysis (incl. Interactions Conv. / Conv. or Load or Mains)
- Converter Stability → System Stability (Autonom. Cntrl of Distributed Converters)
- Cap. Filtering → Energy Storage & Demand Side Management
- Costs / Efficiency → Life Cycle Costs / Mission Efficiency / Supply Chain Efficiency
- etc.

► Power Electronics Systems Performance Figures/Trends

■ **Complete Set of New Performance Indices**

- Power Density [kW/m²]
- Environm. Impact [kWs/kW]
- TCO [$/kW]
- Mission Efficiency [%]
- Failure Rate [h⁻¹]



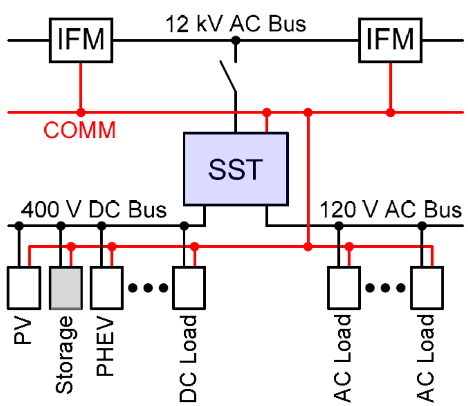
▶ Example: SMART GRID

Future Renewable Electric Energy Delivery & Management Systems (FREEDM)

- Huang et al. (2008)

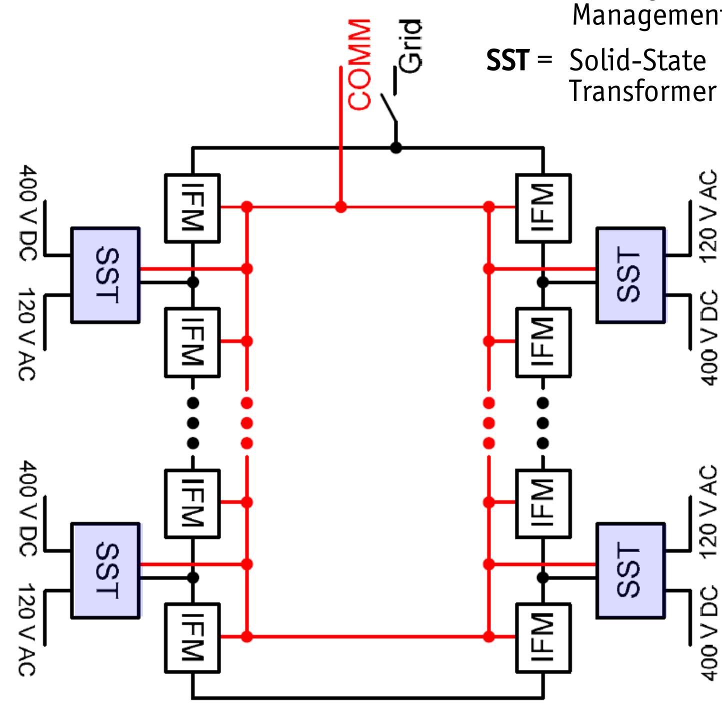
■ **"Energy Internet"**

- Integr. of DER (Distr. Energy Res.)
- Integr. of DES (Distr. E-Storage) + Intellig. Loads
- Enables Distrib. Intellig. through COMM
- Ensure Stability & Opt. Operation
- AC and DC Distribution



IFM = Intellig. Fault Management

SST = Solid-State Transformer



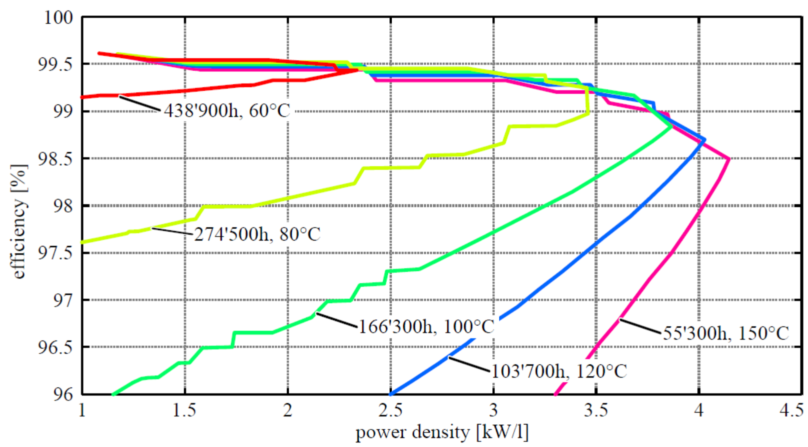
■ **Bidirectional Flow of Power & Information / High Bandw. Comm. → Distrib. / Local Autonomous Cntrl**

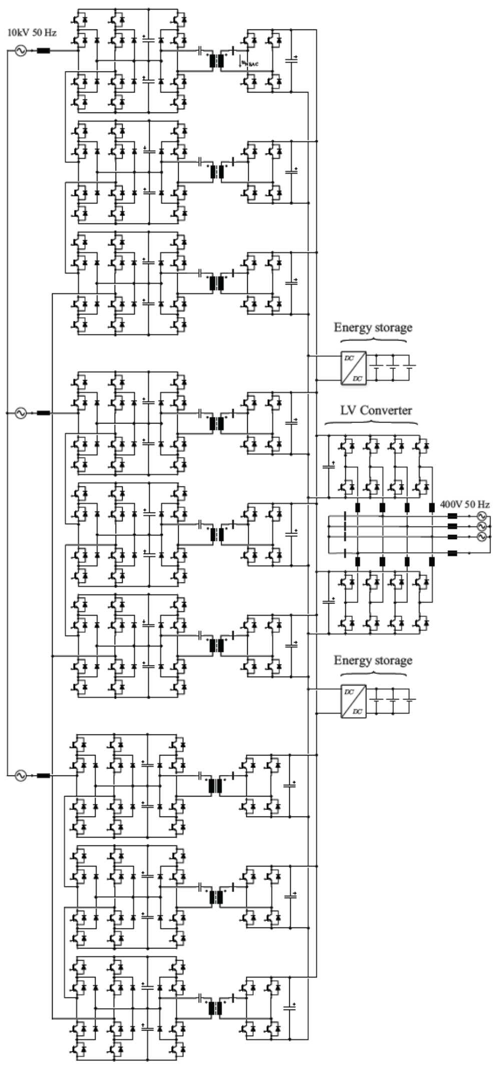
▶ Solid-State Transformer

S_N = 630kVA
U_{LV} = 400 V
U_{MV} = 10kV

■ Trade-Off → Mean-Time-to-Failure vs. Efficiency / Power Density

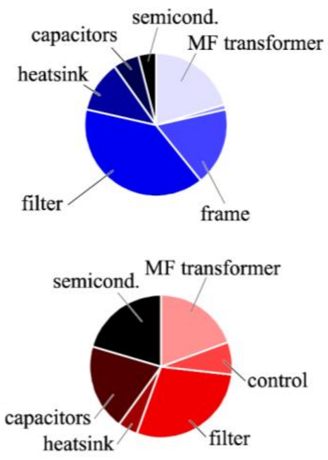
(5 Cascaded H-Bridges, 1700V IGBTs, No Redundancy, FIT-Rate calculated acc. to T_j, 100FIT Base)

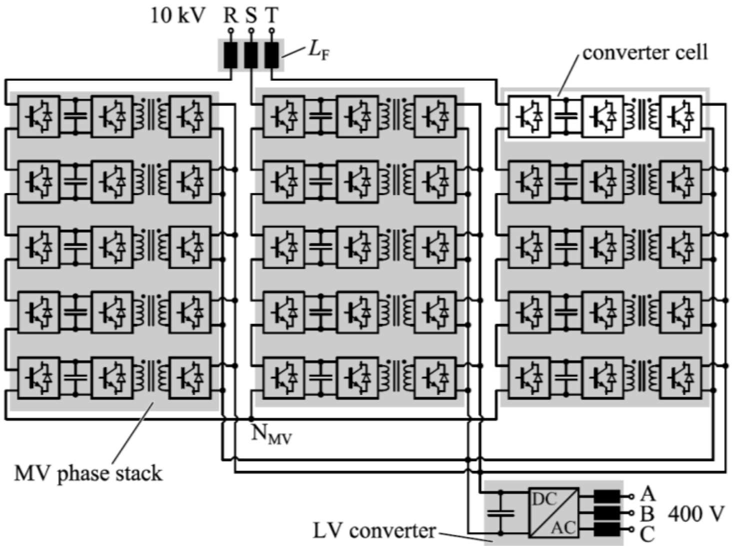




Efficiency Advantage of Direct MV AC – LV DC Conversion

- **Comparison to LF Transformer & Series Connected PFC Rectifier (1MVA)**
  - **MV AC/DC Stage Weight (Top) and Costs (Bottom) Breakdown**





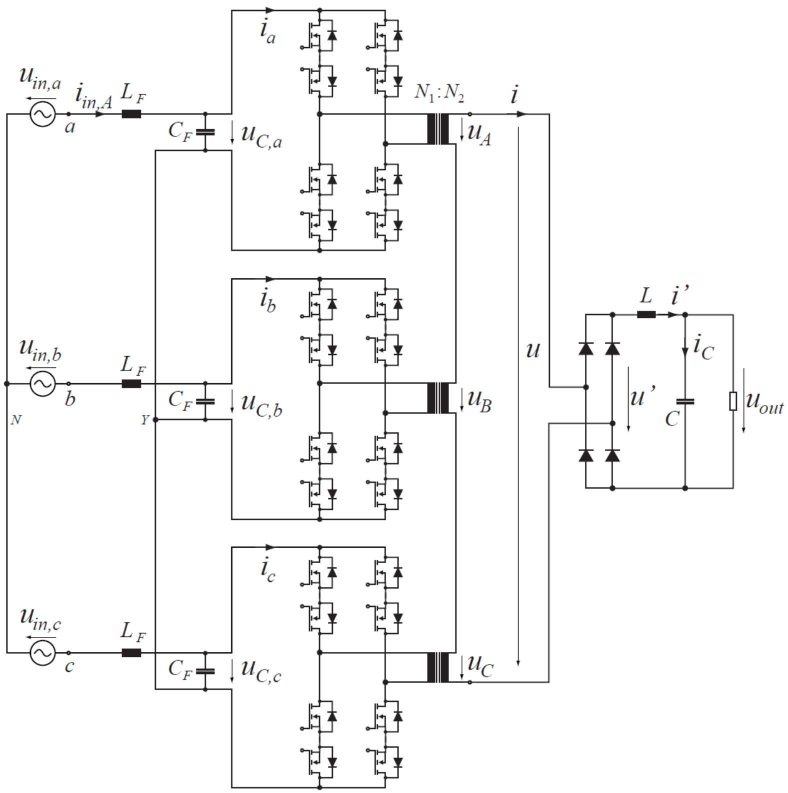
CHARACTERISTIC PERFORMANCE INDICES FOR 1000 kVA LFTS AND SSTS IN AC/AC OR AC/DC APPLICATIONS.

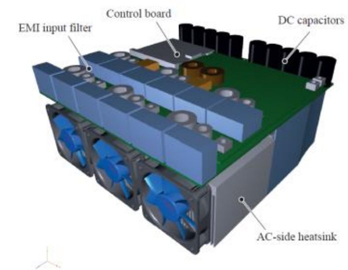
	AC/AC			AC/DC		
	LFT	factor	SST	LFT	factor	SST
losses [W/kVA]	13.0	×2.75	35.7	30.9	×0.58	17.9
costs [USD/kVA]	16.2	×4.75	77.0	43.9	×1.12	49.3
volume [l/kVA]	3.43	×0.57	1.96	3.64	×0.48	1.75
weight [kg/kVA]	2.59	×0.89	2.30	3.63	×0.35	1.26

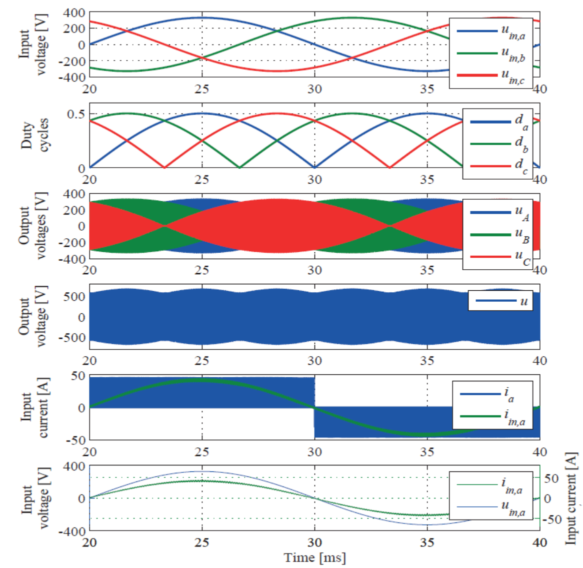
PERFORMANCE CHARACTERISTICS OVERVIEW.

	SST MV	SST LV	SST	LFT
efficiency	98.2 %	98.2 %	96.5 %	98.7 %
volume	1.751 m^3	0.211 m^3	1.962 m^3	3.427 m^3
weight	1262 kg	1036 kg	2298 kg	2591 kg
cost	49.3 kUSD	27.7 kUSD	77.0 kUSD	16 kUSD

▶ 3-ph. BUCK-Type Interfaces for DC Distribution Systems







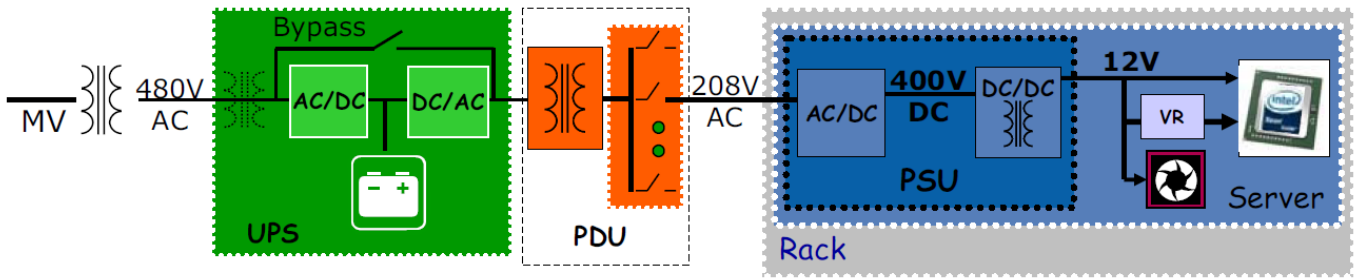
■ Comp. Evaluation of 1-Stage vs. 2-Stage (Boost + DC/DC) Conv. Approach Required

▶ AC vs. Facility-Level DC Systems for Datacenters

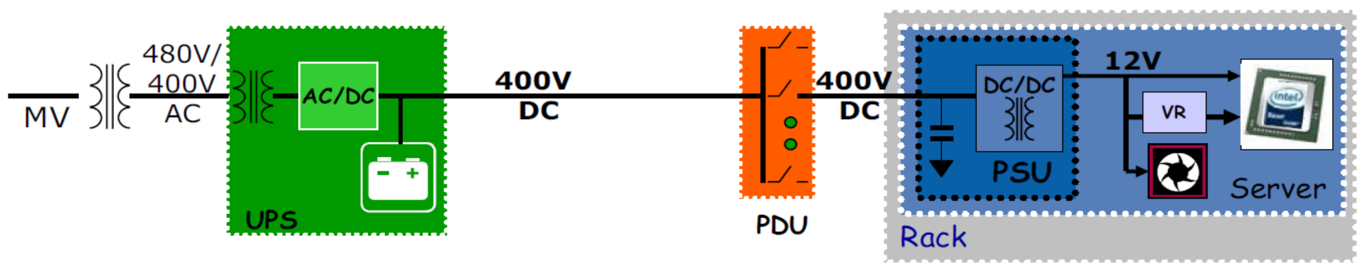
- **Reduces Losses & Footprint**
- **Improves Reliability & Power Quality**

— **Conventional US 480V_{AC} Distribution**

Source: intel 2007



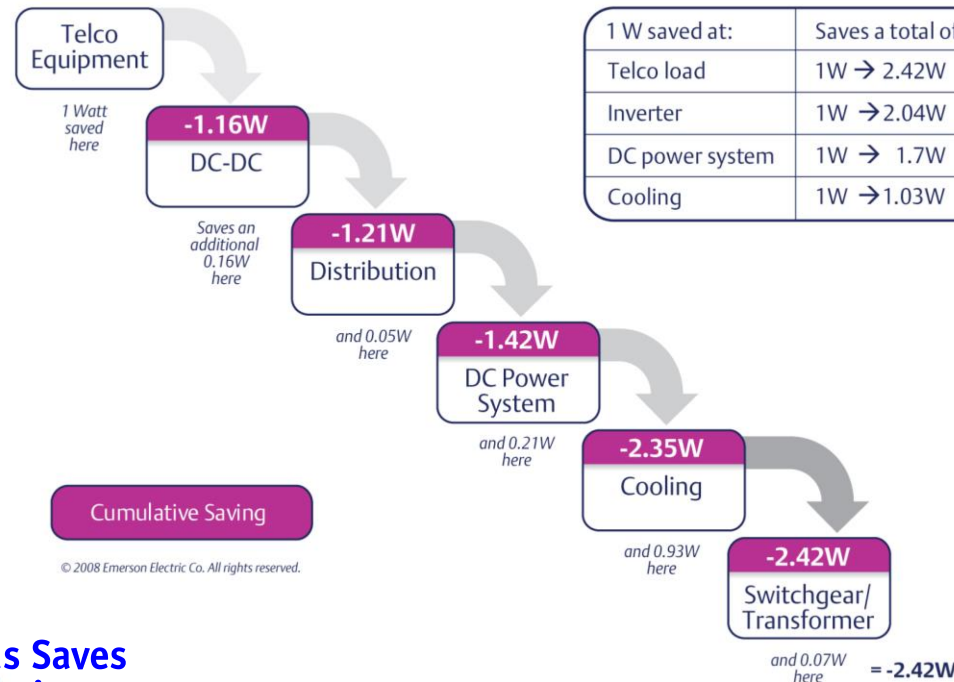
— **Facility-Level 400 V_{DC} Distribution**



- **Proposal for Public +380V_{DC}/-380V_{DC} Systems by Philips, EMerge ALLIANCE, etc.**

System Oriented Analysis

Cascading Effect

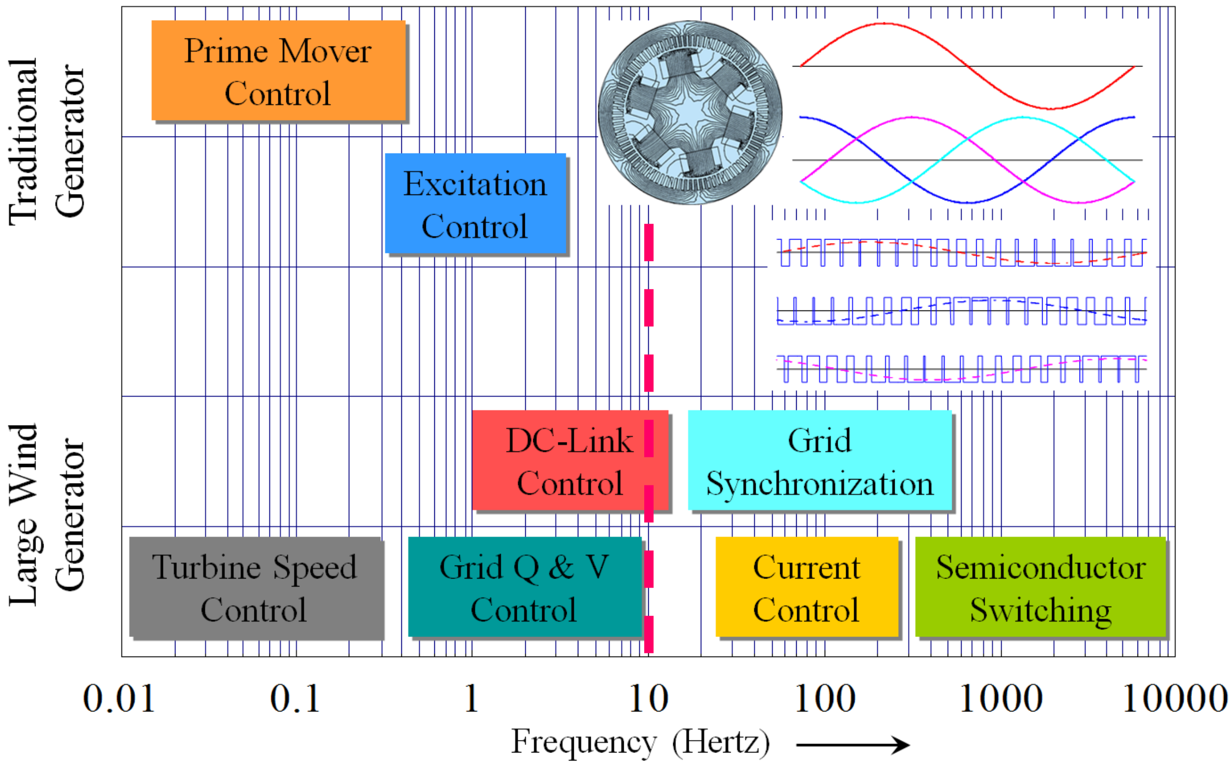


1 W saved at:	Saves a total of:
Telco load	1W → 2.42W
Inverter	1W → 2.04W
DC power system	1W → 1.7W
Cooling	1W → 1.03W

- **1W Saved at Telco Loads Saves 2.42W of Total consumption**

▶ Smart Grid Control Challenge

Source: J. Sun, EPRI-PSMA Workshop 2013



■ Dynamics → from Transient Balance by Kin. Storage (No Cntrl) to ms-Active Power Flow Control

Σ System-Oriented Analysis

→ Challenges

- Get to Know the Details of Power Systems
- Theory of Stability of Converter Clusters
- Autonomous Control
- Design Tools
- Standardization

Remarks on University Research

▶ University Research Orientation

■ General Observations

— Gap between Univ. Research and Industry Needs
— In Some Areas Industry Is Leading the Field

▶ University Research Orientation

■ Gap between Univ. Research and Industry Needs

— Industry Priorities

1. Costs
2. Costs
3. Costs

- Multiple Objectives ...
- Low Complexity
- Modularity / Scalability
- Robustness
- Ease of Integration into System

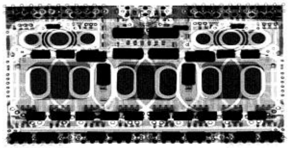
→

— **Basic Discrepancy !**

Most Important Industry Variable, but Unknown Quantity to Universities

▶ University Research Orientation

- In Some Areas **Industry Is Leading the Field !**



— Industry Low-Power Power Electronics (below 1kW) Heavily Integrated –
PCB Based Demonstrators Do Not Provide Too Much Information (!)
Future: "Fab-Less" Research

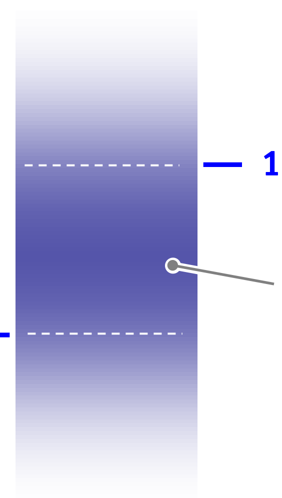
— Same Situation above 100kW (Costs, Mech. Efforts, Safety Issues with Testing etc.)
— Talk AND Build Megawatt Converters (!)

▶ University Research Orientation

MEGA Power Electronics

(Medium Voltage, Medium Frequency)

— 1 MW



"Largely" Standard Solutions

Micro Power Electronics

10W —

(Microelectronics Technology Based, Power Supply on Chip)

+ System Applications

- **Bridge to Power Systems**
- **Establish (Closer) University / Industry (Technology) Partnerships**
- **Establish Cost Models, Consider Reliability as Performance**

▶ University Education Orientation

- **Need to Insist on High Standards for Education**

  * Introduce New Media
  * Show Latest State of the Art (requires New Textbooks)
  * Teach Converter Design (Synthesis not Analysis)
  * Interdisciplinarity
  * Introduce New Media (Animation)
  * Lab Courses!

→ **The Only Way to Finally Cross the Borders (Barriers) to Neighboring Disciplines !**

Finally, ...

Power Electronics 2.0

▶ Technology S-Curve

...after Switches and Topologies

"Passives" & Advanced Design

THE Main Challenges of the Next Decade

+ Costs
+ Systems

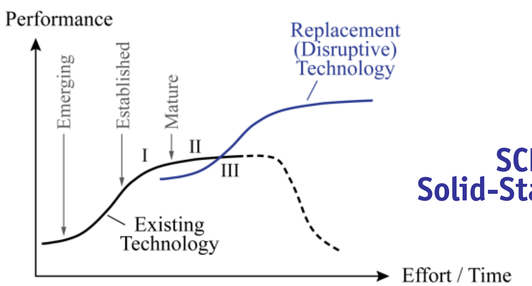
▶ Super-Junct. Techn. / WBG
▶ Digital Power
Modeling & Simulation

▶ Power MOSFETs/IGBTs
▶ Microelectronics
Circuit Topologies
Modulation Concepts
Control Concepts

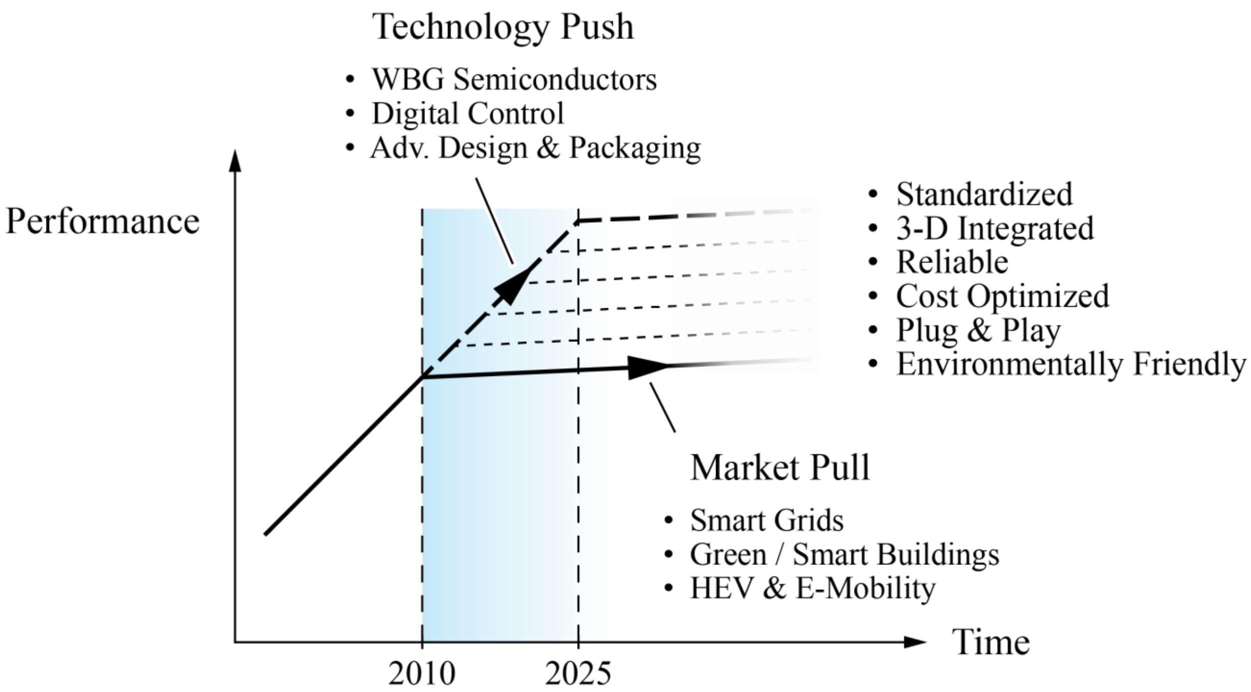
SCRs / Diodes
Solid-State Devices

Paradigm Shift

2014 — 2025



Future Developments



- WBG Semiconductors + Next Level of Integration
- New Applications Could Establish Mass Markets solving the WBG Chicken-and-Egg Problem

Power Electronics 2.0

New Application Areas

- Smart XXX (Integration of Energy/Power & ICT)
- Micro-Power Electronics (VHF, Link to Microelectronics)
- MEGA-Power Electronics (MV, MF)

Paradigm Shift

- From “Converters” to “Systems”
- From “Inner Function” to “Interaction” Analysis
- From “Power” to “Energy” (incl. Economical Aspects)

Enablers / Topics

- New (WBG) Power Semiconductors (and Drivers)
- Adv. Digital Signal Processing (on all Levels – Switch to System)
- PEBBs / Cells & Automated (+ Application Specific) Manufaturing
- Multi-Cell Power Conversion
- Multi-Domain Modeling / Multi-Objective Optim. / CAD
- Cybersecurity Strategies

But, to get there we must …

"Bridge the Gaps"

- Univ. / Ind. Technology Partnerships
- Power Electronics + Power Systems
- Vertical Competence Integration (Multi-Domain)
- Comprehensive Virtual Prototyping (Multi-Objective)
- Multi-Disciplinary / Domain Education

Thank You !

Questions ?