Thermoelectric Cooling for Power Density Maximisation of Power Electronic Converters

J. Biela, and J. W. Kolar
ETH Zurich, Power Electronic Systems Laboratory
Email: biela@lem.ee.ethz.ch; www.pes.ee.ethz.ch

***Abstract*—In many application areas the power density of power electronic converter system is an important design criteria, which is often limited by the passive components and the cooling system. In order to decrease the size of the cooling system, a thermoelectric cooler (TEC) could be inserted between the semiconductor and the heat sink. With the TEC, the temperature drop across the heat sink could be increased so that the volume of the heat sink decreases. In case the ambient temperature is relatively close to the maximum admissible junction temperature, this volume reduction of the heat sink is larger than the additional volume required for the TEC and its power supply as will be shown in this paper. Furthermore, the influence of the TEC on the system efficiency is investigated and using the TEC for actively damping the junction temperature swing in systems with varying losses is discussed.**

I. Introduction

In the last decades, power density of power electronic converter systems has been an important design criteria in many application areas, as mounting space/volume is expensive and in some systems also limited by the application as for example in aircraft or hybrid electric vehicles. By optimally selecting the design variables as for example the operating frequency, the geometry and the turns number of magnetic components or the chip area of the semiconductors, the power density has been pushed to its technological limits, which can not be overcome except with new technologies.

In these optimised systems, the cooling as well as the passive components often consume the largest share of the system volume. The volume of the passive devices could be decreased by an optimal geometrical and electrical design and/or by direct cooling methods, which enable a better heat extraction than free convection or forced air cooling [1], [2].

On the other hand, the volume of the cooling system for the power semiconductor is limited by the thermal conductivity of the heat sink material and the power consumption of the fan. Both are limited due to physical constraints, which results in a minimal volume barrier for the cooling system [3]. This is especially true for systems, where the maximal allowed junction temperature is close to the ambient temperature, so that the possible temperature drop ΔT_{HS} across the heat sink is relatively small and the heat sink volume V_{HS} increases significantly as could be calculated with

$$V_{HS} = \frac{1}{\frac{\Delta T_{HS}}{P_L} CSPI} \tag{1}$$

based on the cooling system performance index (CSPI) [3] and the losses of the semiconductors P_L. Such a condition typically could be found in hybrid electric vehicles, where the ambient temperature is high due to the internal combustion engine and the maximal chip temperature is limited due to the silicon material and packaging issues.

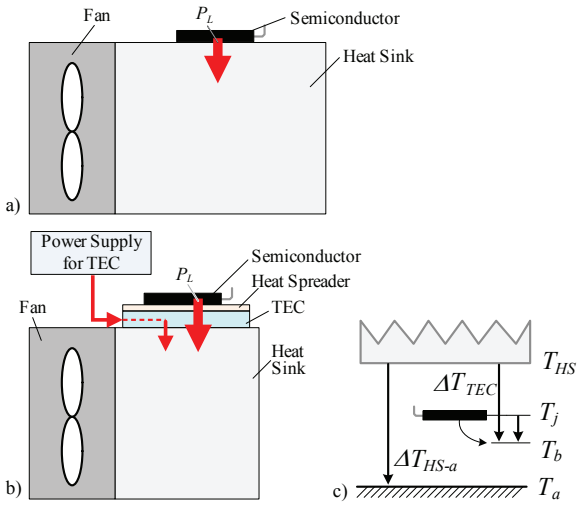

Fig. 1. a) Conventional forced air cooling system and b) high power density cooling system with thermoelectric cooler (TEC) for high ambient temperatures and limited junction temperatures. c) Temperature distribution for the cooling system with TEC. There, T_{HS} is the heat sink temperature, T_j the junction temperature, T_b the base plate temperature of the module/semiconductor housing and T_a the ambient temperature.

Under these conditions, the limitation of the power density due to the cooling system could be overcome by using a thermoelectric cooler (TEC) as shown in Fig. 1a) and b), which allows to increase the temperature drop between the base plate of the semiconductor and the heat sink. Consequently, the heat sink temperature could be increased by the additional temperature difference ΔT_{TEC} generated by the TEC as shown in Fig. 1c), where the heat sink temperature T_{HS} is higher than the junction temperature T_j and the base plate temperature T_b. For simplicity additional thermal contact resistances for example between the TEC and the heat sink are not shown.

As mentioned, with the TEC the heat sink base temperature could be increased, but it is important to note, that the power required by the TEC to generate the temperature difference must also be dissipated via the heat sink of the semiconductors, so that approximately

$$V'_{HS} = \frac{1}{\frac{\Delta T_{HS-a}+\Delta T_{TEC}}{P_L+P_{L,TEC}} CSPI}. \tag{2}$$

is given. At lower ambient temperatures, where the temperature drop of the heat sink could be higher, this fact usually results in a reduction of the power density in case a TEC is applied.

The power loss density in the semiconductors could reach high values up to 100W/cm^2 at the base plate in extreme situations and is usually in the order of a few 10W/cm^2 for air cooled systems. However, the heat transfer capability of a TEC is limited to some Watts per cm^2 (usually $\sim$5W/cm^2). Consequently, between the base plate of the power semiconductor and the TEC a heat spreader must be employed as shown in Fig. 1b) and the mounting surface of the heat sink must be large enough to accommodate the TEC. In compact designs, this could lead to heat sinks which have to be rather flat, what limits the applicability of the concept to systems which have semiconductors with low to medium power loss density.

In this paper the benefits of TEC in systems with high ambient temperatures close to the maximal allowed junction temperatures, as for example hybrid electric vehicles, are evaluated in section III, where also a calculation procedure for minimising the cooling system volume is presented. Before, an analytical model of the TEC is shortly derived in section II. Finally, the influence of the TEC and its power consumption on the system efficiency is evaluated in section IV.

II. Model of the thermoelectric cooler (TEC)

Thermoelectric coolers (and also generators) are devices composed of thermoelectric couples, i.e. *n*- and *p*-type semiconductor pairs of legs (junctions), that are usually connected electrically in series and thermally in parallel [4]. In such a setup several physical phenomena have to be considered, which are shortly discussed in the following in order to derive an electrical model of the TEC.

The Peltier effect is the most important physical phenomena in the considered application. Due to this effect, heat is absorbed at the cold side and emitted at the hot side, when a current flows through the junction. The amount of heat $Q_{P,c}$ absorbed at the cold side is

$$Q_{P,c} = \alpha_{TEC} T_c I_{TEC} \tag{3}$$

and the one emitted at the hot side is

$$Q_{P,h} = \alpha_{TEC} T_h I_{TEC}. \tag{4}$$

With the heat transfer a temperature difference between the two sides results, which is utilised in the considered application for improving the cooling conditions of a power semiconductor. There, α_{TEC} is the Seebeck coefficient (in Volt per Kelvin), T_h is the temperature of the hot side and T_c the temperature of the cold side and I_{TEC} is the current flowing through the TEC, i.e. the junctions.

Due to the flowing current, ohmic losses (Joule heating) are generated in the TEC, what is the second effect. These additional losses and/or the corresponding heat also must be dissipated via the heat sink, so that the size of the heat sink increases compared to a system where just the heat of the converter must be dissipated at the same temperature levels. The ohmic losses Q_J can be calculated by

$$Q_J = R_{el,TEC} I_{TEC}^2, \tag{5}$$

where $R_{el,TEC}$ is the electrical resistance of the TEC.

The power for the ohmic losses must be provided by the power supply of the TEC. Additionally, due to the Seebeck effect, used for example in thermocouples for temperature measurement, a voltage drop at the junction of the two dissimilar materials is generated, which has a value of

$$V_{S,TEC} = \alpha_{TEC} \left(T_h - T_c \right). \tag{6}$$

Consequently, the input voltage of the TEC is given by

$$V_{TEC} = R_{el,TEC} I_{TEC} + \alpha_{TEC} \left(T_h - T_c \right) \tag{7}$$

resulting in an total electric power consumption of

$$P_{el,TEC} = V_{TEC} I_{TEC}. \tag{8}$$

This power must be provided by the auxiliary power supply supplying the TEC.

Based on these effects, the equivalent circuit shown in Fig. 2 and the equations

$$Q_c = \frac{\Delta T_{TEC}}{R_{th,TEC}} + \alpha_{TEC} T_c I_{TEC} - \frac{R_{el,TEC} I_{TEC}^2}{2} \tag{9}$$

$$Q_h = \frac{\Delta T_{TEC}}{R_{th,TEC}} + \alpha_{TEC} T_h I_{TEC} + \frac{R_{el,TEC} I_{TEC}^2}{2} \tag{10}$$

for the thermal behaviour can be derived [5], [6], where with the first term the thermal conduction (Fourier process) is modelled.

These equations describe the steady state behaviour and use a lumped model of the actually distributed effects as for example the ohmic losses. For modelling also transient effects, thermal capacitances must be included as described for example in [6]. However, in the considered application only the steady state operation is considered in a first step, which enables a size reduction of the cooling system. In [6] further information on the difference between lumped and distributed models could be found.

The free parameters in the model are the Seebeck coefficient α_{TEC} as well as the electrical resistance $R_{el,TEC}$ and the thermal $R_{th,TEC}$ resistance of the TEC. In order to determine these parameters, the following equations are derived by setting $Q_c = 0$ in (9) and maximising ΔT_{TEC}:

$$\alpha_{TEC} = \frac{V_{max}}{T_h} \tag{11}$$

$$R_{el,TEC} = \frac{V_{max} \left(T_h - \Delta T_{max} \right)}{I_{max} T_h} \tag{12}$$

$$R_{th,TEC} = \frac{2 T_h \Delta T_{max}}{I_{max} V_{max} \left(T_h - \Delta T_{max} \right)}. \tag{13}$$

There V_{max} is the maximal TEC input voltage at the considered hot side temperature T_h, ΔT_{max} is the maximal temperature difference of the TEC, when no external heat is transported from the cold to the hot side, i.e. $Q_c = 0$. For achieving the maximal temperature difference, current I_{max}

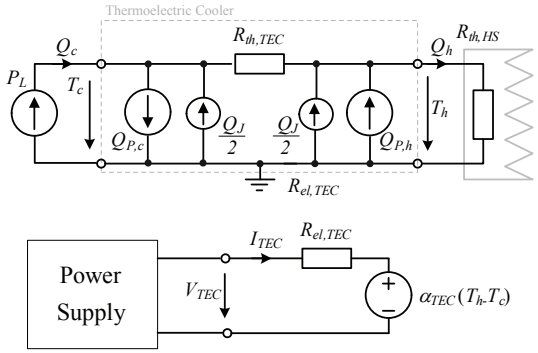

Fig. 2. Top: Electrical equivalent circuit describing the thermal behaviour of the TEC. There the heat/losses P_L injected at the cold side are transferred to the hot side, where the heat is dissipated by the heat sink. Bottom: Electric model of the TEC with auxiliary power supply.

must be provided to the TEC. The three parameters V_{max}, ΔT_{max} and I_{max} are usually given in the data sheets of the TEC and can be used to configure the model.

For summing up above derived equations, an electrical equivalent circuit describing the thermal behaviour of a cooling setup with TEC is given at the top of Fig. 2 and the electrical behaviour of the TEC is modelled by the equivalent circuit shown at the bottom.

On the left hand side of the thermal model in Fig. 2 a current source is shown, which represents the losses P_L of the semiconductor(s). These losses have to be dissipated via the heat sink with the thermal resistance $R_{th,HS}$ shown on the right hand side. In between there is the model of the TEC for the thermal behaviour. This consists of the thermal resistance of the TEC and two current sources $Q_{P,c}$ and $Q_{P,h}$ describing the Peltier effect. Since the distributed effect of the Joule heating is modelled with lumped sources, there are two additional current sources having an amplitude of $\frac{1}{2}Q_J$.

The electrical model at the bottom of Fig. 2 simply consists of the electrical resistance and a voltage source for the Seebeck effect.

III. Optimal Power Density

Based on the model for a TEC presented in the previous section, in the following the power density of converter cooling systems is optimised for converters which must operate at high ambient temperatures close to the maximal allowed junction temperature. First, the calculation procedure is presented and thereafter the optimisations results are shown.

A. Optimisation Model

By applying a TEC, the volume of the heat sink could be reduced as the allowed temperature drop across the heat sink is increased. However, the volume of the TEC and the volume of the power supply for the TEC partly compensate the volume reduction of the heat sink. Additionally, the power consumed by the TEC also must be dissipated via the heat sink, what limits the heat sink volume reduction. Consequently, a power density increase by applying TECs is only given in special situations and requires an optimal choice of the parameters in order to fully utilise the TEC.

TABLE I
Parameters of the HT8-7-30 by Melchor [7].

Q_{max}	49W
I_{max}	8.3A
V_{max}	11.4V
ΔT_{max}	89K
V_{TEC}	6.08cm^3

For maximising the power density, the volume of the cooling system including the TEC and the auxiliary components must be given as function of the free parameters. Assuming that the operating conditions of the semiconductors, i.e. mainly the junction temperature, are the same for the systems with and without TEC, the losses in the semiconductors do not change by adding a TEC to the system. Consequently, only the design parameters of the TEC, i.e. the size A_{TEC} and the operating point (ΔT_{TEC}) can be varied during the optimisation process. The size of the heat sink is fixed by choosing ΔT_{TEC} for a given T_j and T_a.

For deriving the volume of the cooling system as function of the size and the temperature difference $V_{Cool,TEC} = f(A_{TEC}, \Delta T_{TEC})$, first the total heat, which must be dissipated by the heat sink, is determined with (10). There, the parameters α_{TEC}, $R_{el,TEC}$ and $R_{th,TEC}$ are calculated with (11)-(13) based on data sheet values for V_{max}, ΔT_{max} and I_{max}, so that

$$Q_h = \frac{V_{max}}{2T_h \Delta T_{max} I_{max}} \Big(-I_{TEC}^2 \Delta T_{max}^2 - I_{max}^2 \Delta T T_h + \left(I_{max}^2 \Delta T + 2 I_{TEC} I_{max} T_h + I_{TEC}^2 T_h \right) \Delta T_{max} \Big) \quad (14)$$

results for the total losses. For these data sheet values, the high temperature thermoelectric cooler HT8-7-30 by Melchor [7] is used as example in the following, when numerical values are given.

In order to scale the size of the TEC, it is assumed, that for a larger TEC simply more junctions are thermally connected in parallel, i.e. the cooling capability of the TEC scales linearly with the area A_{TEC} of the TEC. Depending on the electrical interconnection, the input current and/or the voltage of the TEC change with the number of junctions. Here, it is assumed that the operating voltage depends linearly on A_{TEC}, i.e. also the power consumption of the TEC scales linearly with A_{TEC}. Thus, in (14) and in (11)-(13) the maximal voltage V_{max} must be replaced by $V_{max} A_{TEC}$.

The total heat Q_h in (14) depends now on ΔT, A_{TEC} and the current I_m through the TEC. By equating the heat Q_c flowing into the TEC at the cold side with the losses P_L of the semiconductor, I_m could be calculated as

$$I_m = \frac{R_{th,TEC} \alpha_{TEC} (T_h - \Delta T) - k_1}{R_{el,TEC} R_{th,TEC}} \quad (15)$$

with

$$k_1 = \sqrt{R_{th,TEC}} \cdot \sqrt{\left((\Delta T - T_h)^2 \alpha_{TEC}^2 - 2 R_{el,TEC} P_L \right) R_{th,TEC} - 2 R_{el,TEC} \Delta T}.$$

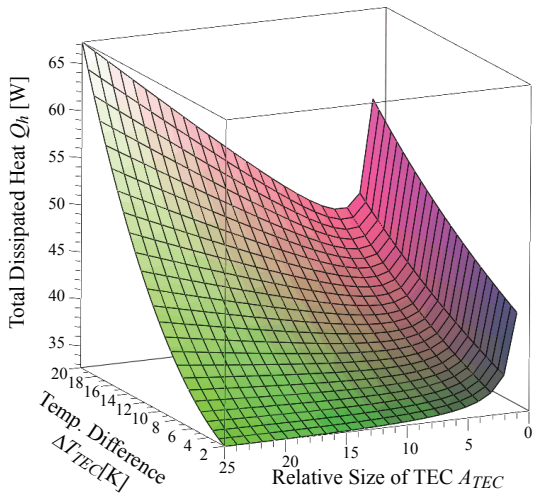

Fig. 3. Total losses $P_{tot,HS}$, which must be dissipated by the heat sink, for semiconductor losses of $P_L = 31.5$W @ $T_j = 140°$C are shown as function of the relative size of the TEC, where a size of 100% (A_{TEC}=1) is defined by the size of the HT8-7-30, and as function of the temperature difference ΔT. There, it is important to note, that a large size requires a large mounting area on the heat sink.

This equation is used to eliminate I_m in (14) resulting in $P_{tot,HS}$ ($= Q_h$), which is not presented here for the sake of brevity. In Fig. 3 a plot of the total losses $P_{tot,HS}$, which must be dissipated by the heat sink, is shown as function of the temperature difference and the size of the TEC for semiconductor losses of $P_L = 31.5$W. With decreasing size of the TEC, i.e. $A_{TEC} \to 0$, the consumed power of the TEC increases rapidly, since the TEC requires more and more power to pump the heat and when the area becomes to small, the TEC cannot pump the heat any more.

The total losses $P_{tot,HS}$ must be dissipated via the heat sink, so that the required maximal allowed thermal resistance of the heat sink is

$$R_{th,HS} = \frac{T_{j,max} + \Delta T_{TEC} - T_a}{P_{tot,HS}} - R_{th,j-s} = f(\Delta T, A_{TEC}), \quad (16)$$

where $R_{th,j-s}$ is the thermal resistance between junction and TEC including any interface materials between semiconductor and TEC. For simplicity in $R_{th,j-s}$ also thermal resistances between TEC and heat sink are included. With $R_{th,HS}$ and the CSPI the volume of the heat sink could be determined using (1).

In addition to the heat sink volume and the volume of the TEC, also the volume of the TEC power supply must be considered for evaluating the power density. The total power consumption of the TEC is given by (8), where I_{TEC} must be replaced by (15) resulting in

$$P_{L,TEC} = \frac{(k_1 - \alpha_{TEC} R_{th,TEC} T_h)}{R_{el,TEC} R_{th,TEC}^2} \cdot (k_1 + \alpha_{TEC} R_{th,TEC} (\Delta T - T_h)) . \quad (17)$$

Assuming a power density of $\rho_{PS,TEC}$ and an efficiency of $\eta_{PS,TEC}$ for the TEC power supply, the volume is $V_{PS,TEC} =$

TABLE II
APPLIED PARAMETERS FOR CALCULATING THE COOLING SYSTEM VOLUME.

Semiconductor Losses P_L	31.5W
$CSPI$	15W/K/dm^3
Ambient Temp. T_a	120°C
Max. Junction Temp. T_j	140°C
Junction to Sink $R_{th,j-s}$	0.5K/W
Power Density $\rho_{PS,TEC}$	7.5kW/dm^3
Efficiency $\eta_{PS,TEC}$	85%

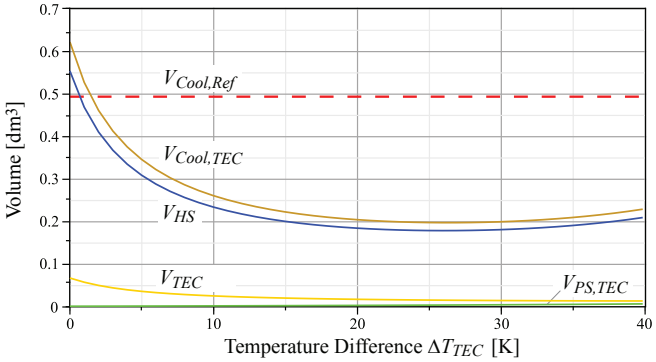

Fig. 4. Volume $V_{Cool,TEC}$ of the cooling system with TEC and component volume as well as the volume of the conventional cooling system without TEC $V_{Cool,Ref}$ as function of the temperature difference ΔT_{TEC}.

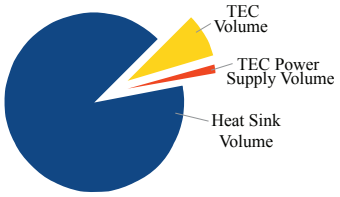

Fig. 5. Volume distribution of the cooling system with TEC for the optimal operating point ΔT_{TEC}=27K according to Fig. 4.

$\rho_{PS,TEC}/(P_{L,TEC}/\eta_{PS,TEC})$ and the total volume of the cooling system including the TEC and the TEC power supply could be calculated as function of A_{TEC} and ΔT_{TEC} resulting in $V_{HS} + V_{TEC} + V_{PS,TEC}$.

B. Optimisation Results

With the above discussed equations, the volume of a cooling system with TEC for a simple power MOSFET is minimised based on the data given in Table II and for the TEC with the data given in Table I. During the optimisation, the junction temperature is kept constant at T_j=140°C, i.e. the size of the heat sink is adapted to the losses and the TEC, and the thermal resistance between the junction and the TEC plus the thermal resistance between TEC and heat sink is assumed to be 0.5K/W.

In Fig. 4 the contributions to the overall volume of the cooling system, $V_{Cool,TEC}$, i.e. the heat sink volume V_{HS}, the TEC volume V_{TEC} and the volume $V_{PS,TEC}$ of the TEC power supply are shown as function of the temperature difference ΔT_{TEC} across the TEC. Additionally, the volume

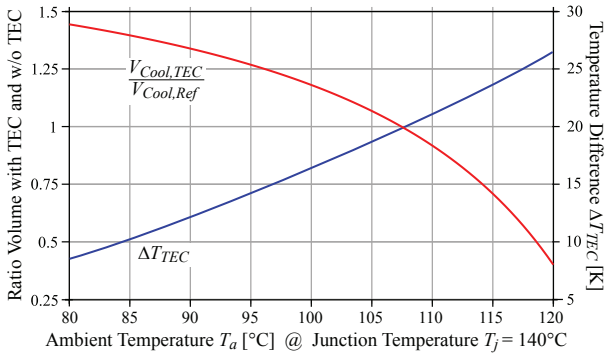

Fig. 6. Temperature difference ΔT_{TEC} of the TEC and volume ratio between the cooling system with TEC ($V_{Cool,TEC}$) and without TEC ($V_{Cool,Ref}$) as function of the difference between maximal junction and ambient temperature.

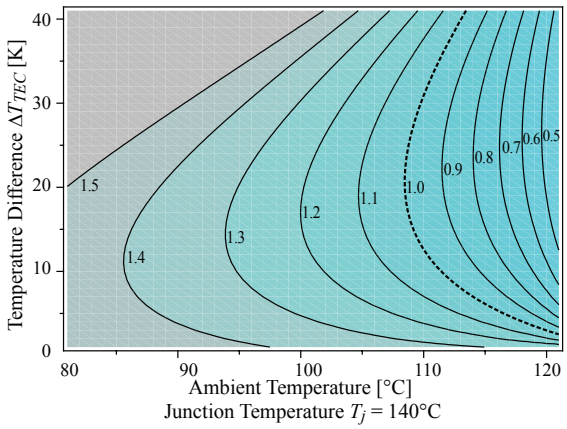

Fig. 7. Contour plot of the ratio between $V_{Cool,TEC}$ and $V_{Cool,Ref}$ as function of the TEC temperature difference ΔT_{TEC} and the ambient temperature T_a. There, a fixed junction temperature of T_j=140°C is assumed.

for a cooling system $V_{Cool,Ref}$ without TEC is shown as reference.

For small values of ΔT_{TEC} the cooling system with TEC is worse than the conventional cooling system, since the TEC adds additional volume and an additional thermal resistance. Due to the small ΔT_{TEC} the volume reduction of the heat sink is too small, so that the total volume is larger than the one of a conventional cooling system. For $\Delta T_{TEC} = 0$ the heat sink of the cooling system with TEC must be larger than the heat sink of the system without TEC, since the TEC inserts an thermal resistance between junction and ambient, by which the thermal resistance of the heat sink must be reduced at $\Delta T_{TEC} = 0$ in order to keep the junction temperature constant. Consequently, for $\Delta T_{TEC} = 0$ it is better to omit the TEC.

This fact also leads to an increase of the area of the TEC A_{TEC} for decreasing ΔT_{TEC}, since the benefit of the heat sink volume reduction is small and the additional penalty due to the thermal resistance is kept as small as possible by the optimiser, i.e. the optimiser tries to increase the area of the TEC.

Considering Fig. 4 a minimal cooling system volume of only 40% of the size of the conventional system results with ΔT_{TEC} values in the range between 20K. . .30K. Such a large volume reduction is only achieved for a small temperature difference T_j-T_a, where an additional ΔT_{TEC} increases the allowed temperature drop across the heat sink significantly.

This could be also seen in Fig. 6, where the temperature difference of the TEC and the volume ratio of the cooling system with and without TEC is shown for different ambient temperatures. There, it could be seen that a TEC only results in a smaller cooling system when the ambient temperature is close to the maximal junction temperature. In the considered case T_a must be higher than approximately 108°C for achieving a volume reduction. In Fig. 7 the same ratio is given as contour plot as function of the temperature difference and the ambient temperature. In both cases the junction temperature is assumed to be 140°C.

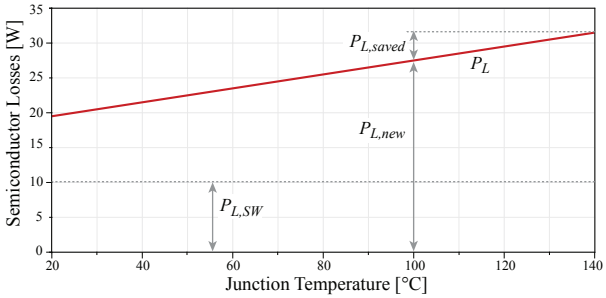

Fig. 8. MOSFET losses P_L as function of the junction temperature. By for example decreasing the junction temperature from 140°C to 100°C, losses in the amount of $P_{L,saved}$ can be saved and only $P_{L,new}$ must be dissipated via the heat sink and pumped by the TEC. For simplification it is assumed that the switching losses $P_{L,SW}$ are independent of temperature.

IV. Efficiency of TEC Cooling Systems

For power semiconductors the conduction and/or the switching losses are dependent on the junction temperature. A well known example is the on-resistance of power MOSFETs, which increases with increasing junction temperature.

By applying a TEC in combination with a heat sink, not only the volume of the heat sink could be decreased as described in the previous section, but also the junction temperature could be decreased while keeping the heat sink volume approximately constant. With the decreasing junction temperature the semiconductor losses decrease as has been experimentally verified in [8]. However, additional losses are generated in the TEC and the power supply of the TEC. Consequently, the question arises, whether it is possible to increase the system efficiency with a TEC.

In Fig. 8 the losses in a power MOSFET are shown as function of the junction temperature as example. The starting point of the considerations is a junction temperature of 140°C, which could be decreased for example to 100°C by a TEC. With T_j=100°C the losses decrease and $P_{L,saved}$ losses can be saved and the heat sink must only dissipate $P_{L,new}$. These, $P_{L,new}$ must be pumped by the TEC, what generates addi-

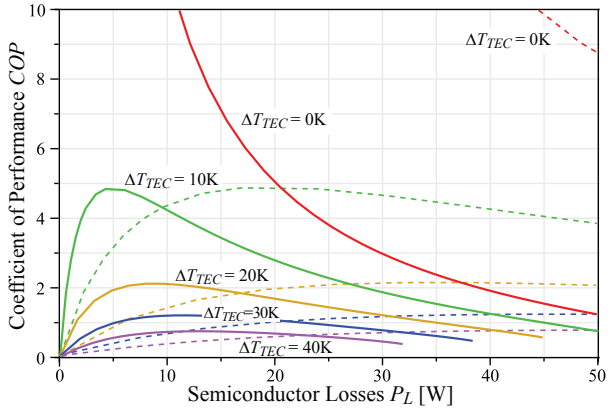

Fig. 9. Coefficient of performance COP for the TEC with the data given in Fig. I as function of the semiconductor losses for different temperature differences ΔT_{TEC}. The solid line is for the original size of the HT8-7-30 and the dashed lines for a version scaled by a factor of 4 in size ($A_{TEC} = 4$).

tional losses. Consequently, the system efficiency increases only if these additional losses are smaller than $P_{L,saved}$.

With the coefficient of performance $COP = P_L/P_{TEC}$, i.e. pumped heat divided by additional losses due to the TEC, which characterises the TEC, the relation

$$COP > \frac{P_{L,new}}{P_{L,saved}} \frac{1}{\eta_{PS,TEC}} \tag{18}$$

could be set up for determining, whether an increase of the system efficiency is possible or not.

In the considered case with the data given in Table II, the losses are reduced by 4W (T_j= 140°C → 100°C), so that the COP must be larger than 8 at a ΔT_{TEC}=40K and a pumped heat of 27.5W. Looking at Fig. 9, where the coefficient of performance is given for the TEC with the data in Table I for two different sizes, it becomes obvious, that an efficiency improvement in the considered case is not possible. Only for zero temperature drop ΔT_{TEC} the TEC reaches COP values larger than 8. For a ΔT_{TEC}=40K, the COP is below 1, even if the size of the TEC is significantly increased.

Consequently, an improvement of the system efficiency, including the TEC and the power supply of the TEC, is only possible if the dependency of the losses P_L is very strong, i.e. a large loss reduction is possible even for a relatively small ΔT_{TEC}. With a COP in the range of 1 for a ΔT_{TEC} = 30K. . .40K, a loss reduction by a factor of 2 must be achieved for a reduction of the junction temperature by 30K. . .40K. Such conditions are usually not given for common power semiconductors.

V. Conclusion

By combining a heat sink and a TEC, the volume of the cooling system including the TEC and the TEC power supply could be significantly reduced in case the difference between the maximal junction temperature and the ambient temperature is relatively small and air cooling is applied. In the considered case a volume reduction of approximately 60% has been achieved at the optimal operating point. In order to determine the optimal operating point an optimisation procedure are

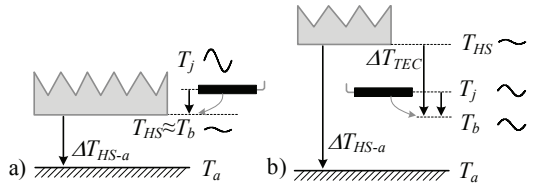

Fig. 10. a) Cooling system without TEC, where a relatively fast variation of the semiconductor losses results in a large temperature swing of the junction. b) With a TEC the temperature swing could be actively damped by distributing the amplitudes between the TEC and the junction.

presented in this paper and results for a prototype system are discussed.

Furthermore, the influence of the TEC on the system efficiency has been evaluated. There, usually a reduction of the efficiency results with the TEC, even if the TEC reduces the operating temperature of the semiconductors, so that lower losses in the semiconductor are generated. This is caused by the ratio of heat pumped by the TEC to the power consumed by the TEC, which is usually too small too achieve an efficiency increase.

In cooling systems with a TEC and varying losses in the semiconductors, the TEC could be used to actively damp the temperature swing in the semiconductor as shown in Fig. 10. Due to the thermal capacitance of the heat sink, the varying losses result in a relatively large temperature swing of the junction in the system without TEC. With a TEC this temperature swing could be actively reduced by varying the temperature drop across the TEC, so that the temperature swing is distributed between the TEC and the junction. This distribution could be optimised for maximal reliability of both the semiconductor and the TEC as will be discussed in a future publication. There, also mobile converter systems with TEC, which only operate for a relatively short time, and which are applied in systems, where a weight reduction results in an increase of the overall system efficiency due to reduced fuel consumption as for example aircraft, are investigated.

References

[1] J. Biela and J. W. Kolar, "Cooling concepts for high power density magnetic devices," in *Proc. of the Power Conversion Conference - Nagoya (PCC)*, 2007, pp. 1–8.

[2] J. Biela, U. Badstuebner, and J. W. Kolar, "Design of a 5-kW, 1-U, 10-kW/dm^3 resonant dc-dc converter for telecom applications," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1701–1710, 2009.

[3] U. Drofenik, G. Laimer, and J. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proceedings of the International PCIM Europe Conference*, June 2005, pp. 608–619.

[4] G. Gromov, "Thermoelectric cooing modules," RMT Ltd. (www.rmtltd.ru), Tech. Rep., 2009.

[5] D. Mitrani, J. Tomé, J. Salzar, A. Turó, M. Garciá, and J. Chávez, "Methodology for extracting thermoelectric module parameters," in *IEEE Transactions on Instrumentation and Measurement*, vol. 54, no. 4, August 2005, pp. 1548–1552.

[6] S. Lineykin and S. Ben-Yaakov, "Modeling and analysis of thermoelectric modules," in *IEEE Transactions on Industry Applications*, vol. 43, no. 2, March/April 2007.

[7] H. Melchor. (2010). [Online]. Available: http://www.melcor.com/tec.html

[8] J. Wang, K.Zou, and J. Friend, "Minimum power loss control - thermoelectric technology in power electronics cooling," in *IEEE Energy Conversion Congress & Expo, San Jose, California*, 2009.