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Closed-Loop $\mathrm{d}i/\mathrm{d}t$ and $\mathrm{d}v/\mathrm{d}t$ IGBT Gate Driver

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***Abstract*—This paper proposes a new concept for attaining a defined switching behavior of IGBTs at inductive load (hard) switching, which is a key prerequisite for optimizing the switching behavior in terms of switching losses and electromagnetic interference (EMI).**

First, state of the art gate driver concepts which enable a control of the IGBT's switching transients are reviewed. Thereafter, a highly dynamic closed-loop IGBT gate driver using simple passive $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ feedbacks and employing a single analog PI-controller is proposed. Contrary to conventional passive gate drivers, this concept enables an individual control of the current and voltage slopes largely independent of the specific parameters or nonlinearities of the IGBT. Accordingly, a means for optimizing the trade-off between switching losses, switching delay times, reverse recovery current of the freewheeling diode, turn-off overvoltage and EMI is gained. The operating principle of the new gate driver is described and based on derived control oriented models of the IGBT a stability analysis of the closed-loop control is carried out for different IGBT modules. Finally, the proposed concept is experimentally verified for different IGBT modules and compared to a conventional resistive gate driver.

***Index Terms*—Insulated gate bipolar transistors (IGBTs), switching circuits, driver circuits, closed loop systems, feedback circuits.**

I. Introduction

IGBT power semiconductors with anti-parallel freewheeling diodes are employed in a wide variety of clamped inductive load (hard) switching voltage source power electronic converters, e.g. in solid state transformers (SST), uninterruptible power supplies (UPS) or in variable speed drive systems. In order to supply the gate current for turning-on and turning-off the IGBTs and to provide the typically needed galvanic isolation for the power and the control signals, gate drivers are employed.

The challenging task of the gate driver is to switch the IGBT at defined rates of $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ independent of the load current level, the DC-link voltage or the junction temperature and to limit its current and voltage to the safe operating area (SOA) by means of an overvoltage and overcurrent protection. Furthermore, the gate driver should be immune against high common-mode (CM) $\mathrm{d}v/\mathrm{d}t$ transients of the IGBT source potential. In addition, the pulse width of the control signal should be maintained at the power terminals of the IGBT with minimum delay, in order to achieve the lowest possible distortion of the output voltage. A reliable overall converter operation is achieved by status feedback from the gate driver to the PWM controller, e.g. by means of a simple fault-signal or an IGBT health status indicator. With respect to a robust and low cost implementation the part count and the complexity should be as low as possible.

This paper focuses on achieving a defined switching behavior, i.e. an individual control of the current and voltage slopes for all operating conditions, in order to gain a means for optimizing the switching trajectories with respect to switching losses, reverse recovery current of the freewheeling diode, turn-off overvoltage, switching delay times and electromagnetic interference (EMI). In Section II state of the art concepts of controlling the IGBT's switching trajectories are reviewed first. Thereafter, in Section III a closed-loop IGBT gate driver with highly dynamic $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control is proposed, which enables an active shaping of the IGBT's switching trajectories largely independent of the nonlinearities and parameter variations of the IGBT. Subsequently, a stability and performance analysis based on control-oriented models of the IGBT and the gate driver is performed for different IGBT modules in Section IV. The hardware implementation and a prototype of the closed-loop gate driver are thereafter presented Section V. An experimental verification of the proposed concept including a comparison to a resistive gate driver and a performance comparison for different IGBT modules is presented in Section VI. The paper concludes with a summary and an outlook on subjects of future research in Section VII.

II. State of the Art IGBT Switching Trajectory Control

State of the art IGBT gate driver concepts, which enable a control of the current and voltage switching trajectories at hard switching, are discussed in the following. A schematic classification, which classifies these concepts into passive, open-loop and closed-loop types, is depicted in Fig. 1.

The resistive push-pull gate driver, cf. Fig. 2, which consists of a switchable voltage source v_G and turn-on / off gate resistors $R_\mathrm{G,on/off}$, is a very simple and thus a widely used approach. Corresponding current and voltage waveforms at hard switching are depicted in Fig. 3 for low (1) and high (2) values of the gate resistors. The use of low-ohmic gate resistors leads to high absolute values of the gate current i_G, which results in fast switching transients, i.e. high absolute values of the current and voltage time derivatives [1]. Fast switching is on the one hand beneficial in terms of short turn-on / off delay times t_d [2]and low switching losses $E_\mathrm{on/off}$ [3], cf. Fig. 3. On the other hand EMI is increased, as the conducted CM EMI depends on $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ [4] and the radiated EMI depends

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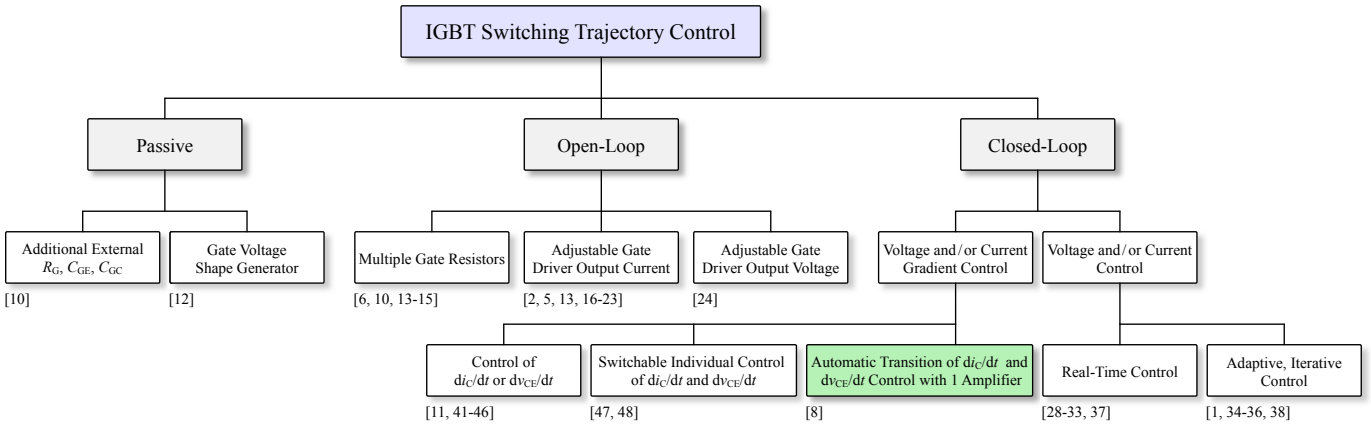

Fig. 1: Classification of gate driver concepts enabling a shaping of the IGBT's switching trajectories subdivided into passive, open-loop and closed-loop types. The proposed closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control concept, which employs a single amplifier and features a seamless automatic transition from $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ to $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control (turn-on) and vice versa (turn-off), is highlighted.

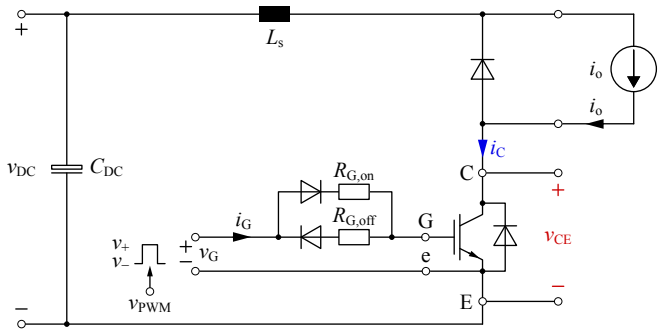

Fig. 2: Equivalent circuit for the inductive load (hard) switching by means of a push-pull gate driver. L_s represents the sum of the DC-link, busbar and IGBT module internal parasitic inductances, i.e. the commutation loop inductance.

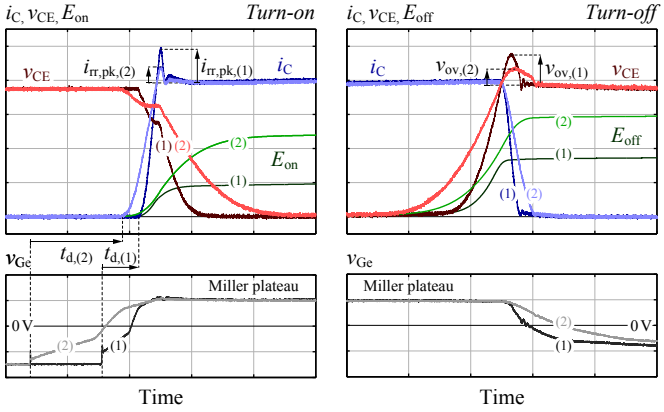

Fig. 3: Typical current and voltage waveforms at hard switching by means of a push-pull gate driver during turn-on and turn-off using small (1) or large (2) gate resistors $R_{\mathrm{G,on/off}}$.

on $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ [5, 6]; thereby the second corner frequency in the noise spectrum is shifted to higher frequencies [7]. In addition, also a higher semiconductor stress occurs, i.e. a high $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ leads to larger overvoltage v_ov at turn-off due to the stray inductance L_s of the commutation loop and to larger peak reverse recovery current $i_\mathrm{rr,pk}$ [8] as well as diode snap-off overvoltage at turn-on [9].

It is apparent, that the controllability of the switching waveforms is very limited with this simple approach, i.e. it is not possible to individually control the current and voltage slopes as well as the delay times, which would be needed for an overall optimization of the switching operation. In the following, different gate driver concepts that enable an independent and more accurate control of the switching trajectories are discussed.

A. Passive Feed-Forward Control Concepts

An individual adjustability of the current and voltage slopes can be achieved by extending the basic push-pull gate driver circuit of Fig. 2 with an additional external gate capacitance C_GE and/or a Miller capacitance C_GC. The insertion of an extra Miller capacitance mainly reduces the absolute value of $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ and an added gate capacitance slows down the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ [10]. This approach typically causes increased switching delay times as well as gate driver losses due to the larger IGBT capacitances and increases the risk of a cross conduction fault in bridge leg applications for larger Miller capacitances [11].

A solution to avoid these disadvantages is the feed-forward gate-voltage shape generator presented in [12], whereas $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ at turn-on is defined by the passively generated gate voltage slope applied to the IGBT. During $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ the gate current is increased due to the Miller-plateau of the gate-emitter voltage. With this approach the controllability of the voltage slope is limited.

B. Open-Loop Control Concepts

An individual control of the gate current and thus of the IGBT can also be achieved through the gate driver, i.e. via employing switchable or adjustable gate resistors [6, 10, 13–15], gate current sources/sinks [2, 5, 13, 16–23] or gate voltages [24]. A schematic overview of such gate driver concepts is depicted in Fig. 4. The basic idea thereby is to subdivide the switching transients into delay, current slope and voltage slope intervals, whereby a specific gate resistor/current/voltage is selected for each interval, in order to independently control the IGBT in these intervals. For all topologies the control of the

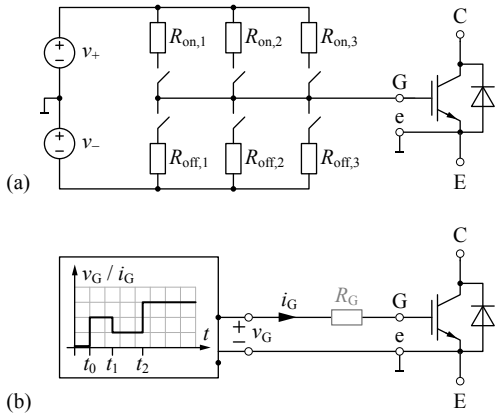

Fig. 4: Gate driver with an adjustable output stage by (a) switchable gate resistors and (b) switchable gate voltage or gate current source featuring discrete resistances / voltage / current levels.

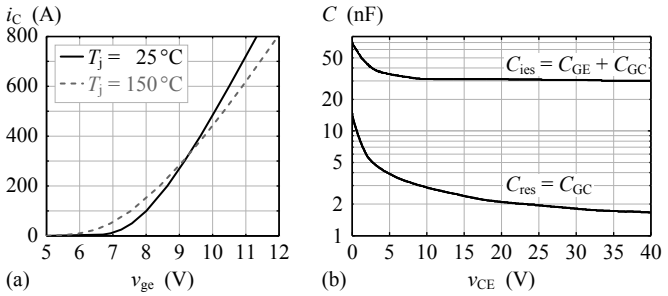

Fig. 5: Typical (a) nonlinear IGBT transconductance g_m (Infineon FF450R12KE4) in dependency of the junction temperature T_j and (b) differential (small-signal) capacitances C_{res} and C_{ies} (Semikron SKM 500 GA 123 D) depending on v_{CE} at $v_{Ge} = 0\,V$ and $f = 1\,MHz$.

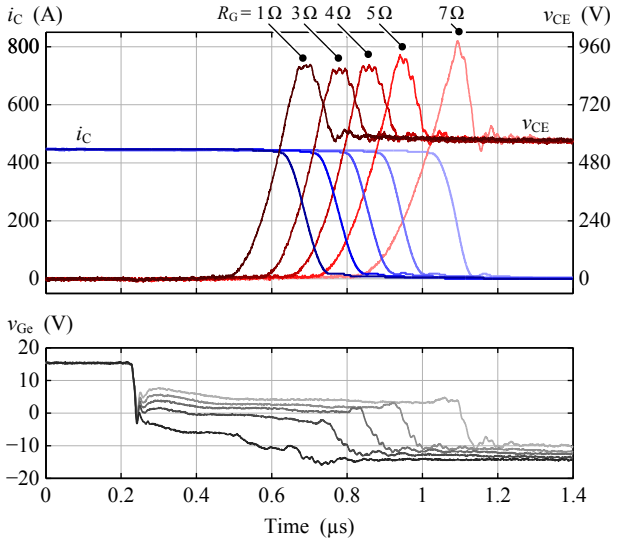

Fig. 6: Measured turn-off waveforms of a trench-gate field-stop IGBT module (Infineon FF450R12KE4) at hard switching for different values of the gate resistor $R_G \approx \{1\,\Omega, 3\,\Omega, 4\,\Omega, 5\,\Omega, 7\,\Omega\}$.

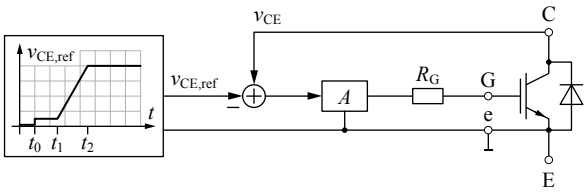

Fig. 7: Simplified analog closed-loop v_{CE} control with a reference voltage $v_{CE,ref}$ profile.

output stage can either be based on a fixed profile [13, 20], an operating point dependent action [6, 14, 23] or an event feedback of the switching transients [2, 6, 15–18, 21, 24].

The practical implementation has to ensure an operation of the IGBT in the SOA, i.e. has to limit $\mathrm{d}i_C/\mathrm{d}t$ and $\mathrm{d}v_{CE}/\mathrm{d}t$ values, for all operating conditions such as varying junction temperature T_j, load current i_o or DC-link voltage v_{DC}, and is thus tuned for the worst case. In particular, $\mathrm{d}i_C/\mathrm{d}t$ is highest at low values of T_j and large values of i_C due to the larger transconductance g_m, cf. Fig. 5 (a). At nominal operating conditions, i.e. high values of T_j and values of i_C below nominal current, a lower absolute value of $\mathrm{d}i_C/\mathrm{d}t$ results and thus the IGBT is switching slower than actually permissible. This in turn leads to higher switching losses than desired. The absolute value of $\mathrm{d}v_{CE}/\mathrm{d}t$ increases with v_{CE} due to the decreasing value of the Miller capacitance C_{GC}, cf. Fig. 5 (b), and thus the gate driver is tuned for the maximum value of v_{DC}. As long as v_{CE} is below this value, i.e. most of the time, the IGBT switches slower than allowed; accordingly, the switching losses and delay times are larger than requested.

In addition to these dependencies of the switching trajectories on the operating conditions, the $\mathrm{d}i_C/\mathrm{d}t$ at turn-off of trench-gate field-stop IGBTs is sensitive to a desaturation of the semiconductor [25–27]. Lower gate currents and / or higher gate resistances result in a slower voltage slope at turn-off. Thereby, the stored charge in the drift region of the IGBT is partly extracted and thus the $\mathrm{d}i_C/\mathrm{d}t$ is increased. This is unexpected and typically unwanted, as it is causing higher overvoltage (cf. Fig. 6, $R_G = 7\,\Omega$), and makes it extremely difficult for an open-loop gate driver to switch the IGBT along a desired switching trajectory.

Missing compensation of the IGBT's nonlinearities and / or remaining dependencies on the load and temperature conditions are a main drawback of all these passive and open-loop control concepts. With an open-loop approach, accurately defined and constant current and voltage slopes in all operating points can thus hardly be obtained. For that reason, closed-loop concepts with negative feedback are applied to achieve a more precise control.

C. Closed-Loop Control Concepts

Compensation of the IGBT's nonlinearities and operating point and temperature dependencies is advantageously achieved by closed-loop control.

A sophisticated closed-loop analog v_{CE} control topology as schematically shown in Fig. 7 was proposed, investigated and gradually developed further in [28–33]. A similar approach could also be followed for an i_C control. If a combination of voltage and current control is needed, the generation of both reference signals by analog circuits will be involved and hardly feasible due to their mutual dependency and the dependency on the operating point, e.g. the temporal variation of the state transition (current- / voltage slope) or the value of the load current.

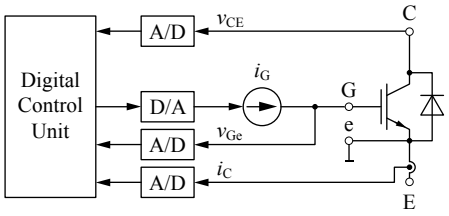

Fig. 8: Digital gate driver unit comprising a microcontroller (e.g. FPGA), A/D converters for measuring the IGBT's state variables and a D/A converter providing the reference signal for the controlled gate current source.

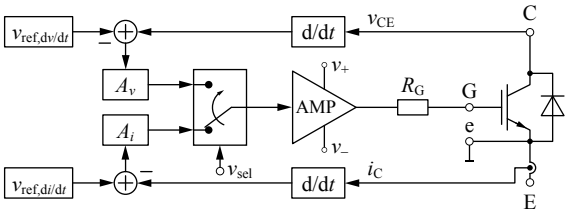

Fig. 9: Schematic analog closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control concept where the transition between the current and the voltage slope control has to be actively detected and triggered via v_sel.

The handling of a combined i_C and v_CE control becomes only feasible by means of a digital approach as developed in [1, 34–38] and schematically pictured in Fig. 8. In doing so, all main state variables (i_C, v_CE and v_Ge) are sampled and processed in a digital control unit that controls the gate current in order to attain the desired switching trajectories. Due to the relatively large delay times of the D/A- and A/D-conversion of 55 nanoseconds [37] or even 100 to 200 nanoseconds [1] in the signal paths, a real-time approach is only promising for IGBT switching transients not faster than ca. 2 microseconds. Iterative, adaptive and system parameter dependent approaches are therefore typically applied to overcome this problem [1, 34–36]. Their main downside is the lack of accurate control in case of a significant change in the system state between subsequent switching operations. In addition, the limited bandwidth of current sensors, and the highly dynamic reference and feedback signals are limiting the performance and accuracy of any i_C and v_CE control concept. The cost of high-speed D/A- and A/D-converters is high, too.

Best performance with regard to analog control bandwidth is achieved by means of analog closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control concepts [39, 40] (cf. Fig. 9) due to constant reference value(s), simple control amplifier stages and passive measurement circuits providing high analog control bandwidth. Different implementations of only $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ control [11, 41–43], $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ control at turn-on [44, 45] and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control at turn-off [45], or individual solutions for current or voltage slope control during turn-on or turn-off [46] have been shown. A complete solution of turn-on and turn-off $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control was presented in [47, 48]. However, due to the implementation with a large number of bipolar transistors and the need for detection and selection of the respectively active control loop (cf. Fig. 9), the performance was limited to $200\,\mathrm{A}/\mu\mathrm{s}$ and $1\,\mathrm{kV}/\mu\mathrm{s}$ respectively.

In the next section, a highly dynamic analog closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ gate driver concept without a dedicated activation of the respective control loop is proposed.

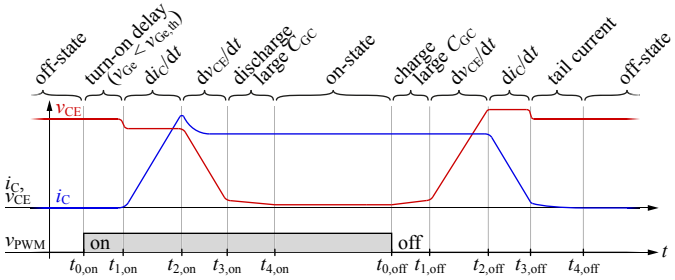

Fig. 10: Schematic current (i_C(and voltage (v_CE) waveforms at hard switching during turn-on and turn-off subdivided into characteristic intervals. v_PWM corresponds the PWM control command input.

III. Proposed Closed-Loop Gate Driver

A. Conceptual Description and Operating Principle

In order to explain the basic idea of the proposed closed-loop gate driver, first the hard switching of an IGBT is briefly reviewed. The typical current and voltage waveforms for inductive load switching are shown in Fig. 10. Thereby, the intervals with current and voltage changes always appear in direct sequence and / or without overlap at both turn-on and turn-off. As a consequence, ideally, $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ is zero during the collector current change and $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ is zero during the collector-emitter voltage change. This fact permits the utilization of a combined $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ closed-loop control, i.e. both control loops are closed simultaneously via a single PI-controller, where in contrast to [47, 48] no active selection of the control loop is required. Therefore, an automatic and extremely fast transition from the current to the voltage slope control and vice versa occurs, and the PI-controller controls that variable which is changing.

However, a single exception must be considered. In the turn-on interval $t_{2,\mathrm{on}} \ldots t_{3,\mathrm{on}}$, where i_C is reduced after the diode's peak reverse recovery current, cf. Fig. 10, $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ is not zero during the voltage slope, different to the original assumption. For that reason, a clipping circuit preventing this unwanted negative $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ feedback during the turn-on voltage slope will be presented in Section V-D.

The block diagram for the proposed combined closed-loop current and voltage slope control is depicted in Fig. 11. There, the input reference signal $v_{\mathrm{ref,d}/\mathrm{d}t}$, that is set once at the beginning of every switching operation, is kept at a constant value for the complete switching process and defines in combination with the positive feedback gains k_I and k_V the set-points for both control variables,

$$\left(\frac{\mathrm{d}i_\mathrm{C}}{\mathrm{d}t}\right)_\mathrm{ref} = \frac{v_{\mathrm{ref,d}/\mathrm{d}t}}{k_I}, \tag{1}$$

$$\left(\frac{\mathrm{d}v_\mathrm{CE}}{\mathrm{d}t}\right)_\mathrm{ref} = -\frac{v_{\mathrm{ref,d}/\mathrm{d}t}}{k_V}. \tag{2}$$

Accordingly, a turn-on, at which $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ is positive and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ negative, is initiated by setting $v_{\mathrm{ref,d}/\mathrm{d}t}$ to a constant positive value which is amplified and integrated by the PI-controller to charge the IGBT's gate. Applying a negative value at $v_{\mathrm{ref,d}/\mathrm{d}t}$ initiates a turn-off. To be able to adjust the current and voltage slopes individually for turn-on and turn-off, the absolute values of the reference voltage $v_{\mathrm{ref,d}/\mathrm{d}t}$ and

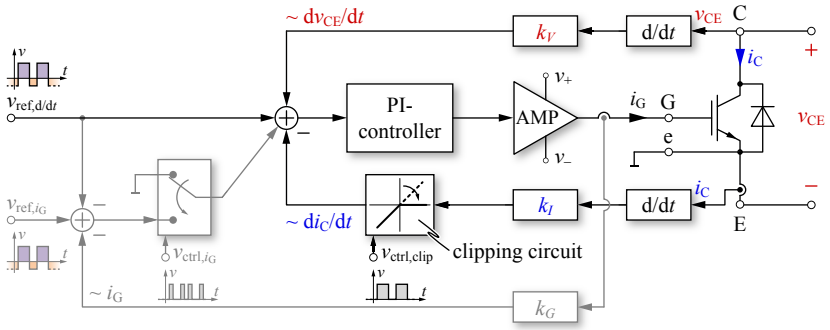

Fig. 11: Block diagram of the proposed combined closed-loop current slope and voltage slope control (dark-colored) extended by an additional gate current control (light-colored) that is used to define the gate current during the turn-on and turn-off delay intervals as described in section III-B. Signal $v_{\mathrm{ref,d/dt}}$: reference value for the current and voltage slope control; $v_{\mathrm{ctrl,clip}}$: control command for the clipping circuit; $v_{\mathrm{ref},i_\mathrm{G}}$: reference value for the gate current control; $v_{\mathrm{ctrl},i_\mathrm{G}}$: control command for the gate current control.

also the feedback gains k_I and k_V may be selected differently for turn-on and turn-off.

Since the dynamic feedbacks of $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ only provide information of the system during the current and voltage slopes, the PI-controller is not able to control the IGBT during the turn-on and turn-off delay intervals $t_{0,\mathrm{on/off}} \dots t_{1,\mathrm{on/off}}$, cf. Fig. 10. This missing feedback typically results in too high absolute values of the gate current at the interval transition point t_1 and thus leads to an overshoot in the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ at turn-on and the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ at turn-off. A solution acting prior to a current or voltage slope feedback is hence presented in the following.

B. Extension by Gate Current Control

If the gate current, that mainly defines the current and voltage slopes [1], is actively controlled in the turn-on and turn-off delay intervals, the aforementioned overshoots can be prevented. Such a gate current control can be implemented into the proposed closed-loop gate driver concept without changing the current and voltage slope control part as depicted in Fig. 11.

The corresponding sequence diagram for the reference and control signals of the combined i_G, $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control is shown in Fig. 12. A switching operation is initiated by setting the reference signals for the current and voltage slopes $v_{\mathrm{ref,d/dt}}$ and for the gate current $v_{\mathrm{ref},i_\mathrm{G}}$ to the desired values and by activating the gate current control via the control signal of the multiplexer $v_{\mathrm{ctrl},i_\mathrm{G}}$ simultaneously. Subsequently, the gate current control must be deactivated by means of toggling the multiplexer at the beginning of the current rise at turn-on or at the voltage rise at turn-off. This point in time can be assumed to occur with a defined time delay after the initiation of the switching operation, or can be derived from reaching a predefined gate-emitter voltage level or at latest at the point of active current or voltage slope feedback.

In addition, it's even possible to employ a 2-step gate current reference at turn-on and turn-off, whereas first a high gate current is selected to minimize the switching delay times and then a lower gate current is programmed to avoid the aforementioned overshoots.

The circuit diagram and a realized prototype of the proposed closed-loop gate driver will be shown in Section V. However,

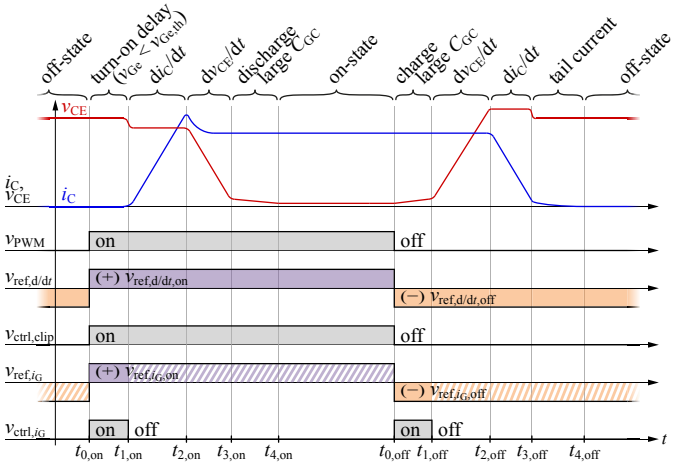

Fig. 12: Sequence diagram for the closed-loop control of i_G, $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ during turn-on and turn-off according to Fig. 11. v_PWM corresponds the PWM control command input.

first the stability and robustness of the proposed closed-loop switching trajectory control are verified with respect to different IGBT modules in the next section. This allows to predict the control performance and to analyze the stability and robustness of the concept.

IV. Control Oriented Modeling and Stability Analysis

Key issue of any closed-loop control is system stability. Based on models of the proposed gate driver and the IGBT, which are described and/or derived in this section, the stability and robustness analysis of the closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ switching trajectory control will be performed.

A. Model of the Closed-Loop Gate Driver

The PI-controller of the proposed gate driver, cf. Fig. 11, is implemented using a high-bandwidth operational amplifier (cf. Section V). Its transfer function is given by

$$G_\mathrm{OP}(s) = \frac{A_\mathrm{DC,OP}}{s\frac{A_\mathrm{DC,OP}}{2\pi f_\mathrm{T,OP}} + 1}, \tag{3}$$

where $A_\mathrm{DC,OP}$ denominates the DC-gain of the amplifier and $f_\mathrm{T,OP}$ the transit frequency. Since the operational amplifier is

Parameter	*Value*
$A_{\mathrm{DC,OP}}$	100 dB
$f_{\mathrm{T,OP}}$	350 MHz
$f_{\mathrm{c,AMP}}$	100 MHz
k_V	1 ns
k_I	1 nH

TABLE I: Parameter values of the closed-loop gate driver circuit.

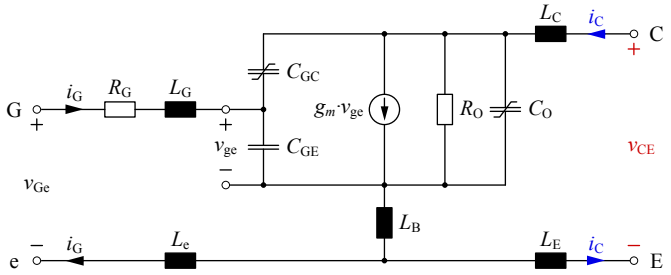

Fig. 13: Simplified IGBT model valid in the active region including parasitic inductances of the bond wires and / or the electrical terminals.

used in a non-inverting configuration, the transfer function of the PI-controller is given by

$$G_{\mathrm{PI}}(s) = \frac{G_{\mathrm{OP}}(sK_{\mathrm{P}} + K_{\mathrm{I}})}{s(G_{\mathrm{OP}} + K_{\mathrm{P}}) + K_{\mathrm{I}}}, \tag{4}$$

where K_{P} denominates the proportional gain and K_{I} defines the integral part $K_{\mathrm{I}}s^{-1}$. The output amplifier, that is used to provide the needed output current, can be modeled as low-pass filter with a corner frequency at $f_{\mathrm{c,AMP}}$, i.e.

$$G_{\mathrm{AMP}}(s) = \frac{1}{s\frac{1}{2\pi f_{\mathrm{c,AMP}}} + 1}. \tag{5}$$

Positive $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback is needed since the IGBT shows an inverting characteristic for the voltage slope. This is provided by means of an RC-high-pass filter,

$$H_{V,\mathrm{HP}}(s) = k_V \frac{s}{sk_V + 1}, \tag{6}$$

where the time constant equals the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ feedback gain k_V and specifies the corner frequency $f_{\mathrm{c},V} = \frac{1}{2\pi k_V}$ of the high-pass filter. The voltage drop across a parasitic inductance in the current path is utilized for generating a $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ proportional feedback signal,

$$H_{I,\mathrm{HP}}(s) = k_I s. \tag{7}$$

The corresponding parameters of the amplifiers and feedback signals, which are used for the hardware implementation in Section V, are summarized in Table I.

B. Control-Oriented IGBT Model

For the IGBT a small-signal model valid in the active operating region as used in [30, 31, 43, 49–53] and shown in Fig. 13 can be employed as a basis for the investigation of the closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ switching trajectory control.

On the basis of this IGBT model, the transfer functions from the gate voltage $V_{\mathrm{Ge}}(s)$ to the collector-emitter voltage $V_{\mathrm{CE}}(s)$ and to the collector current $I_{\mathrm{C}}(s)$ can be derived. However, these derivations depend on the operating conditions given by the external circuitry, which in this case is the equivalent circuit for the inductive load switching, cf. Fig. 2. Since the operating conditions for the voltage and the current slope are different, the IGBT's transfer functions for both slopes are derived separately in the following.

1) Interval of $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ Control: In this interval, i.e. for the voltage slope, i_{C} is impressed by the inductive load, cf. Fig. 2, and is therefore assumed to be constant. Accordingly, the transfer function from the gate voltage to the collector-emitter voltage can be calculated based on Fig. 13 as [30, 31]

$$G_V(s) = \frac{V_{\mathrm{CE}}(s)}{V_{\mathrm{Ge}}(s)} = \frac{a_3s^3 + a_2s^2 + a_1s + a_0}{b_3s^3 + b_2s^2 + b_1s + b_0}, \tag{8}$$

with the coefficients

$$\begin{aligned}
a_0 &= -g_m R_{\mathrm{O}} \\
a_1 &= R_{\mathrm{O}} C_{\mathrm{GC}} \\
a_2 &= L_{\mathrm{B}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
a_3 &= L_{\mathrm{B}} R_{\mathrm{O}} C_{\mathrm{t}} \\
b_0 &= 1 \\
b_1 &= R_{\mathrm{O}}(C_{\mathrm{GC}} + C_{\mathrm{O}}) + R_{\mathrm{G}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
b_2 &= R_{\mathrm{O}} R_{\mathrm{G}} C_{\mathrm{t}} + (L_{\mathrm{Ge}} + L_{\mathrm{B}})(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
b_3 &= R_{\mathrm{O}} C_{\mathrm{t}}(L_{\mathrm{Ge}} + L_{\mathrm{B}}) \\
C_{\mathrm{t}} &= C_{\mathrm{GE}} C_{\mathrm{GC}} + C_{\mathrm{GE}} C_{\mathrm{O}} + C_{\mathrm{GC}} C_{\mathrm{O}},
\end{aligned} \tag{9}$$

which is in accordance with [30, 31] and is given here for the sake of completeness and easier reference. The inductances in the gate path can be joined according to $L_{\mathrm{Ge}} = L_{\mathrm{G}} + L_{\mathrm{e}}$.

2) Interval of $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ Control: In this interval, i.e. for the current slope, v_{CE} is clamped by the diode to the DC-link, cf. Fig. 2, and is thus assumed to be constant. Accordingly, the transfer function from the gate voltage to the collector current can be derived based on Fig. 13 as

$$G_I(s) = \frac{I_{\mathrm{C}}(s)}{V_{\mathrm{Ge}}(s)} = \frac{c_3s^3 + c_2s^2 + c_1s + c_0}{d_4s^4 + d_3s^3 + d_2s^2 + d_1s + d_0}, \tag{10}$$

with the coefficients

$$\begin{aligned}
c_0 &= g_m R_{\mathrm{O}} \\
c_1 &= -R_{\mathrm{O}} C_{\mathrm{GC}} \\
c_2 &= -L_{\mathrm{B}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
c_3 &= -L_{\mathrm{B}} R_{\mathrm{O}} C_{\mathrm{t}} \\
d_0 &= R_{\mathrm{O}} \\
d_1 &= L_{\mathrm{CE}} + L_{\mathrm{B}}(1 + g_m R_{\mathrm{O}}) + R_{\mathrm{G}} R_{\mathrm{O}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}) \\
d_2 &= R_{\mathrm{G}}(L_{\mathrm{CE}} + L_{\mathrm{B}})(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
&\quad + R_{\mathrm{O}}(C_{\mathrm{GE}}(L_{\mathrm{B}} + L_{\mathrm{Ge}}) + C_{\mathrm{GC}}(L_{\mathrm{CE}} + L_{\mathrm{Ge}}) \\
&\quad + C_{\mathrm{CE}}(L_{\mathrm{CE}} + L_{\mathrm{B}})) \\
d_3 &= R_{\mathrm{G}} R_{\mathrm{O}} C_{\mathrm{t}}(L_{\mathrm{CE}} + L_{\mathrm{B}}) \\
&\quad + L_{\mathrm{t}}(C_{\mathrm{GE}} + C_{\mathrm{GC}}(1 + g_m R_{\mathrm{O}})) \\
d_4 &= L_{\mathrm{t}} R_{\mathrm{O}} C_{\mathrm{t}} \\
C_{\mathrm{t}} &= C_{\mathrm{GE}} C_{\mathrm{GC}} + C_{\mathrm{GE}} C_{\mathrm{O}} + C_{\mathrm{GC}} C_{\mathrm{O}} \\
L_{\mathrm{t}} &= L_{\mathrm{CE}} L_{\mathrm{Ge}} + L_{\mathrm{CE}} L_{\mathrm{B}} + L_{\mathrm{Ge}} L_{\mathrm{B}},
\end{aligned} \tag{11}$$

where the inductances in the power- and gate paths can be joined according to $L_{\mathrm{CE}} = L_{\mathrm{C}} + L_{\mathrm{E}}$ and $L_{\mathrm{Ge}} = L_{\mathrm{G}} + L_{\mathrm{e}}$.

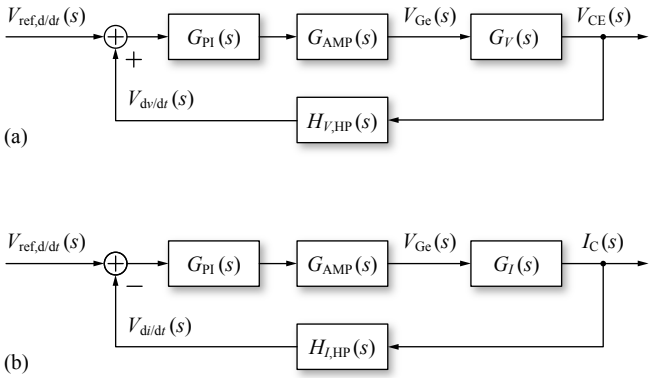

Fig. 14: Block diagram representation of the closed-loop (a) voltage- and (b) current slope control. $G_{\mathrm{PI}}(s)$ corresponds to the PI-controller, $G_{\mathrm{AMP}}(s)$ to the output amplifier, $G_V(s)$ and $G_I(s)$ are the small-signal transfer functions of the IGBT and finally $H_{V,\mathrm{HP}}(s)$ and $H_{I,\mathrm{HP}}(s)$ represent the high-pass feedbacks according to equations (3) to (11).

C. Closed-Loop Transfer Functions

The derived transfer functions for the gate driver and the IGBT are defining the block diagrams representing the voltage- and current slope control depicted in Fig. 14. Accordingly, the open-loop transfer functions from the reference signal $V_{\mathrm{d/dt,ref}}$ to the voltage and current time derivative values are given by

$$G_{V,\mathrm{OL}}(s) = \frac{V_{\mathrm{d}v/\mathrm{d}t}(s)}{V_{\mathrm{ref,d/dt}}(s)} = G_{\mathrm{PI}}(s) \cdot G_{\mathrm{AMP}}(s) \cdot G_V(s) \cdot H_{V,\mathrm{HP}}(s), \tag{12}$$

$$G_{I,\mathrm{OL}}(s) = \frac{V_{\mathrm{d}i/\mathrm{d}t}(s)}{V_{\mathrm{ref,d/dt}}(s)} = G_{\mathrm{PI}}(s) \cdot G_{\mathrm{AMP}}(s) \cdot G_I(s) \cdot H_{I,\mathrm{HP}}(s). \tag{13}$$

Finally, the corresponding closed-loop transfer functions for the voltage and current slope control based on positive $V_{\mathrm{d}v/\mathrm{d}t}$ and negative $V_{\mathrm{d}i/\mathrm{d}t}$ feedback can be derived,

$$G_{V,\mathrm{CL}}(s) = \frac{G_{V,\mathrm{OL}}(s)}{1 - G_{V,\mathrm{OL}}(s)}, \tag{14}$$

$$G_{I,\mathrm{CL}}(s) = \frac{G_{I,\mathrm{OL}}(s)}{1 + G_{I,\mathrm{OL}}(s)}. \tag{15}$$

D. Stability Analysis

A fundamental property of the proposed closed-loop gate driver is the common PI-control amplifier for the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control loops, that is controlling the current and voltage slopes subsequently, since they appear in direct sequence without overlap at hard switching. This temporal separation allows to independently investigate the closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control, i.e. $G_{V,\mathrm{CL}}(s)$ and $G_{I,\mathrm{CL}}(s)$, under the condition of identical PI-controller parameters for both control loops.

1) Closed-Loop Transfer Functions: In order to determine the closed-loop transfer functions (14) and (15), the parasitic inductances and the small-signal IGBT model parameters related to Fig. 13 must be known. In appendix A a detailed derivation of these model parameters is given for three IGBT modules from different manufacturers. All these IGBTs feature a blocking ability of $1.2\,\mathrm{kV}$ and a current rating of $400-450\,\mathrm{A}$. As will be shown, the parasitic inductances of an IGBT module are key parameters regarding the closed-loop controllability.

	K_{P}	K_{I}
IGBT (A)	3.75	$12.9 \cdot 10^7$
IGBT (B)*	1.34	$8.57 \cdot 10^7$
IGBT (C)	5.93	$14.5 \cdot 10^7$

TABLE II: PI-controller parameters for the closed-loop control of the IGBT modules' (A), (B)* and (C) high-side IGBT.

a) $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control: By means of the IGBT parameters, the closed-loop transfer functions (14) and (15) can be evaluated in dependency of the controller parameters. In a first step, the PI-controller was adjusted individually for each of the three IGBT modules in order to achieve a $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control without overshoot in the step response. The controller gains K_{P} and K_{I} for the different modules are given in Table II and the corresponding Bode diagrams and step responses of the closed-loop $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control are depicted in Fig. 15 (a,b).

As can be observed, the control of the IGBT modules with larger gate loop inductance $L_{\mathrm{gl,HS}} = L_{\mathrm{G}} + L_{\mathrm{e}}$, cf. Fig. 27, demands for higher K_{P} and K_{I} values of the controller, in order to achieve the desired step response, and exhibits a lower closed-loop control bandwidth, f_{c}. This behavior results due to the implementation of the PI-controller by means of an operational amplifier with limited gain-bandwidth product. A higher controller gain, that is needed at larger gate loop inductance, reduces the control bandwidth, and in addition leads to an increased applied gate voltage amplitude. Since in practice the output voltages of the operational amplifier and the output amplifier are limited to the supply voltages, v_+ and v_-, i.e. $\pm 15\,\mathrm{V}$, another (non-linear) reduction of the control dynamics may occur. For the sake of simplicity, this effect is not considered here.

b) $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control: As the proposed gate driver concept employs only a single control amplifier, the PI-controller for the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control must be the same as for the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control, however the control loops are different in both cases. On the basis of the optimized $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control, the closed-loop transfer functions for the current slope control, $G_{I,\mathrm{CL}}$, can be evaluated. The corresponding Bode diagrams and step responses of the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control are depicted in Fig. 15 (c,d).

Since the controller is optimized for the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control, an unsatisfying performance of the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control results, that is close to or even beyond the limit of stability as can be seen in Fig. 15 (c,d). In the following, two different solutions to overcome the problem of having only one PI-controller, that is used to implement two different control tasks, are presented. On the one hand, the controller can be optimized for the more sensitive, i.e. less stable, control loop. In the present case, this would mean to adjust the PI-controller for the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ loop. Therewith, an optimal current slope control could be achieved with the drawback that the control bandwidth of the voltage slope control would be below it's optimal value. On the other hand, a degree of freedom is to add an external

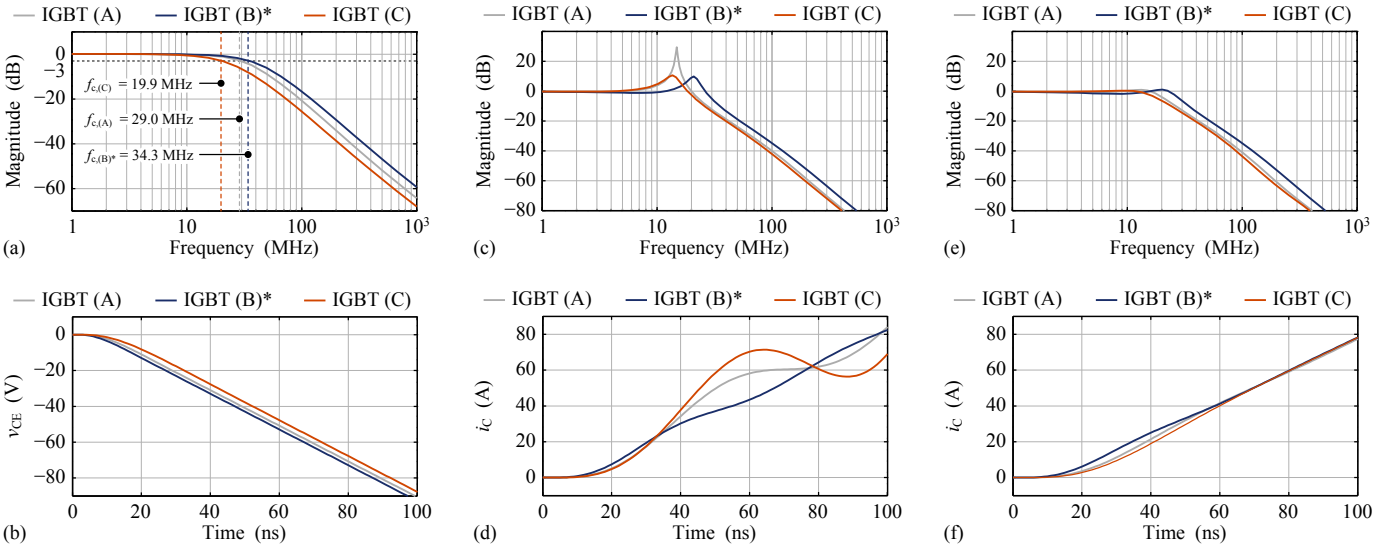

Fig. 15: (a) Bode diagram of the closed-loop $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control and (b) step response of v_{CE} for a $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ reference value step from 0 to $-1\,\mathrm{kV}/\mu\mathrm{s}$ with the PI parameters given in Table II and the IGBT parameters of Table III. (c,e) Bode diagrams of the closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control and (d,f) step responses of i_{C} for a $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ reference value step from 0 to $1\,\mathrm{kA}/\mu\mathrm{s}$ with the same PI-controller optimized for the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control. (c-d) without and (e-f) with increased gate-emitter capacitance, i.e. $C_{\mathrm{GE,(A),ext.}} = 143\,\mathrm{nF}$, $C_{\mathrm{GE,(B)*,ext.}} = 38\,\mathrm{nF}$ and $C_{\mathrm{GE,(C),ext.}} = 230\,\mathrm{nF}$.

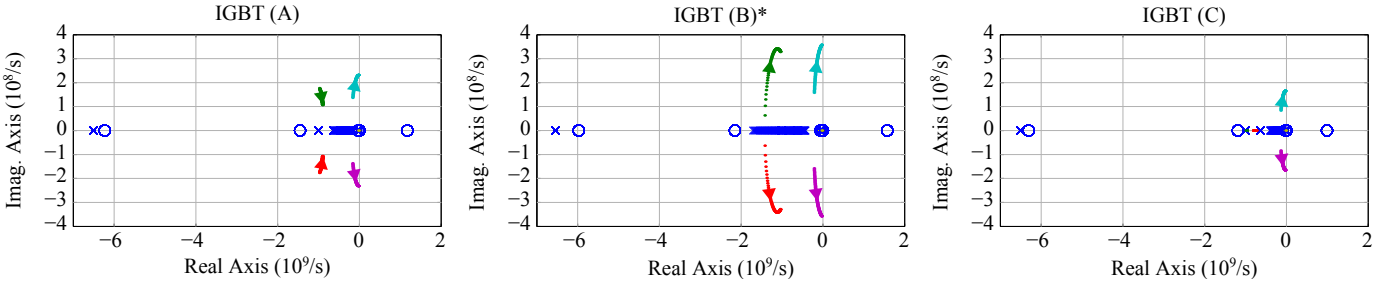

Fig. 16: Root locus plots for an increase of the PI-controller's proportional gain (K_{P}) from nominal value to 4-times the nominal value.

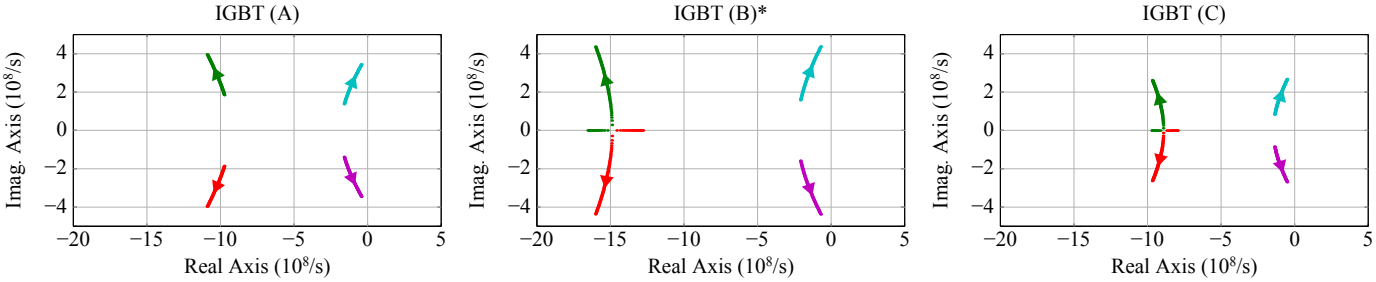

Fig. 17: Root locus plots (poles only) of the $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control related to Fig. 15 for a decrease of the IGBT's Miller capacitance C_{GC} from nominal value, cf. Table III, down to 25 % of the nominal value.

gate- or Miller capacitance close to the IGBT chip, whereby the effective values for C_{GE} and C_{GC} are then defined by the sum of the IGBT's internal and the external capacitance values. Since i_{C} is controlled via the gate voltage and v_{CE} depends on the Miller capacitance's voltage, adding additional capacitance acts as low-pass filter for the corresponding loop. In the present case, the PI-controller could be adjusted for a fast $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control and the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control loop could be adapted by means of additional gate capacitance to get a desired control behavior.

The performance of the closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ control with additional gate capacitances, which have been tuned by means of evaluating / optimizing the closed-loop transfer functions, is depicted in Fig. 15 (e,f). Since the two control loops are subsequently active for inductive switching, adding gate capacitance does not directly impact the voltage slope control. The disadvantages of this solution are the increased gate drive charge and the difficulty to insert a capacitor close to the chip in practice.

2) Parameter Variations: A verification of the control's robustness can be performed by investigating the impact of IGBT and controller parameter variations. According to Nyquist's stability criterion, the stability of a closed-loop system is given, if all poles of the corresponding open-loop transfer function are located in the open-left s-half plane.

To investigate the sensitivity of the controller, the root-

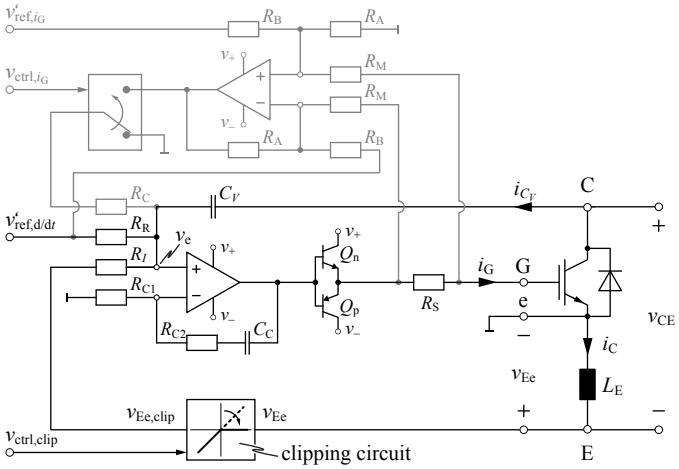

Fig. 18: Circuit diagram of the proposed closed-loop $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ gate driver (shown in black) with a clipping circuit to block a negative $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ feedback at turn-on as proposed in Section V-D including the gate current control (shown in gray).

locus plots of the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ loop for an increase of the PI-controllers' proportional gain (K_P) up to 4-times the nominal value are depicted in Fig. 16. It can be seen for all IGBT modules, that the control gets very close to the stability limits for the maximum value of K_P. From the controller's side, there should accordingly not be a concern regarding stability, since in practice the PI-controller's gain is properly adjusted initially and then kept constant.

For the robustness analysis of the control with respect to the IGBT's parameters, root-locus plots of the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ loop for reduced Miller capacitance, cf. Fig. 17, are evaluated. Reducing the Miller capacitance down to $25\,\%$ of the nominal value as worst case assumption for high values of v_CE leads to a shifting of the pivotal poles of the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control towards the right s-half plane, but the system is still stable. A similar analysis can be performed for the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ loop in terms of increased transconductance g_m. There, the dominant poles are also shifted towards the right s-half plane for an increase of g_m by a factor of 4, and therewith the system gets close to instability. Since this high value of g_m exceeds the specified values in the data sheets by far, no stability issues need to be expected in practice.

V. Hardware Implementation

According to Fig. 11, the implementation of the proposed closed-loop gate driver relies on $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$, $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ and i_G feedback signals, the determination of the control error, a PI-controller and a highly dynamic and powerful output amplifier stage. The circuit schematic of the proposed gate driver with constant feedback gains is presented in Fig. 18 and will be discussed in the following.

A. Measurement Circuits

The measurement of the time derivative signals $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ features a duality. Feedback proportional to $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ is derived as voltage drop across an inductance in the load current path, e.g. the emitter's parasitic bond wire inductance L_E as shown in Fig. 18. The current of a capacitor connected in parallel to the voltage path, i.e. to the IGBT collector terminal, is used as feedback signal proportional to $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$. In practice, depending on the accuracy needs of the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ control, the tolerances of this parasitic inductance could either be taken into account by selecting a slightly lower $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ set-point or be compensated by means of measurement and calibration of the sensing circuitry.

Neglecting any parasitic inductance in the auxiliary emitter connection and assuming a (+)-input voltage v_e of the operational amplifier being comparably small with regard to v_CE, the two feedback signals can be expressed as

$$v_\mathrm{Ee} \approx -L_\mathrm{E} \cdot \mathrm{d}i_\mathrm{C}/\mathrm{d}t, \tag{16}$$

$$i_{C_V} \approx C_V \cdot \mathrm{d}v_\mathrm{CE}/\mathrm{d}t. \tag{17}$$

The gate current i_G can be measured as voltage drop across a very small, e.g. $100\,\mathrm{m}\Omega$, shunt resistor in the gate path.

B. Control Error

For the determination of the control error v_e, i.e. for summing up the reference and the negative feedback signals, a passive network consisting of R_C, R_R, R_I and C_V can be employed as depicted in Fig. 18. Thereby, the capacitor C_V of the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ feedback path acts as a low-pass filter for the reference, the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and the gate current control signals. If this time constant, which in practice is typically in the nanosecond range, would be too high for a particular case, a buffer amplifier could be inserted to decouple the capacitor of the voltage slope feedback. For the determination of the gate current control error, an operational amplifier wired as multi-port subtractor can be employed, cf. Fig. 18 (shown in gray).

1) Interval of Current and Voltage Slope Control: During the control of the current and voltage slopes the gate current control is turned-off via setting $v_{\mathrm{ctrl},i_\mathrm{G}}$ to logic low. In order to make the practical implementation of the control error signal generation as easy as possible, $R_\mathrm{C} = R_\mathrm{R}$ can be selected without giving up a significant degree of freedom. In that case the control error signal becomes

$$\begin{aligned} v_\mathrm{e} \approx \underbrace{v'_{\mathrm{ref},\mathrm{d}/\mathrm{d}t} \cdot \frac{R_I}{R_\mathrm{R}+2R_I}}_{v_{\mathrm{ref},\mathrm{d}/\mathrm{d}t}} - \underbrace{L_\mathrm{E} \cdot \frac{R_\mathrm{R}}{R_\mathrm{R}+2R_I}}_{k_I} \cdot \mathrm{d}i_\mathrm{C}/\mathrm{d}t \\ + \underbrace{C_V \cdot \frac{R_\mathrm{R} \cdot R_I}{R_\mathrm{R}+2R_I}}_{k_V} \cdot \mathrm{d}v_\mathrm{CE}/\mathrm{d}t. \end{aligned} \tag{18}$$

This is in accordance with Fig. 11, i.e. the control error equals the sum of the control reference signal and the current and voltage slope feedbacks with individual feedback gains.

2) Interval of Gate Current Control: In the interval of the gate current control, the $\mathrm{d}/\mathrm{d}t$-control reference signal $v'_{\mathrm{ref},\mathrm{d}/\mathrm{d}t}$ must be cancelled out. This is achieved by setting $R_\mathrm{A}/R_\mathrm{B} = R_\mathrm{C}/R_\mathrm{R}$. Since the gate current control is only active in the turn-on and turn-off delay intervals, the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ feedbacks are assumed to be zero. Under the

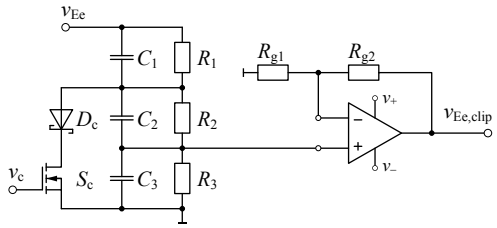

Fig. 19: Schematic of the clipping circuit to restrict negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback during turn-on, at which S_{c} has to be closed permanently.

consistent assumption of $R_{\mathrm{C}} = R_{\mathrm{R}}$ the control error signal during the gate current control becomes

$$v_{\mathrm{e}} \approx \underbrace{v'_{\mathrm{ref},i_{\mathrm{G}}} \cdot \frac{R_I}{R_{\mathrm{R}}+2R_I}}_{v_{\mathrm{ref},i_{\mathrm{G}}}} - \underbrace{\frac{R_{\mathrm{S}} \cdot R_{\mathrm{A}}}{R_{\mathrm{M}}} \cdot \frac{R_I}{R_{\mathrm{R}}+2R_I}}_{k_{\mathrm{G}}} \cdot i_{\mathrm{G}} \tag{19}$$

and is also in accordance with Fig. 11.

C. Control Amplifier and Buffer Stage

The PI-controller can be implemented by means of a fast operational amplifier as shown in Fig. 18, where the gains result as

$$K_{\mathrm{P}} = 1 + R_{\mathrm{C2}}/R_{\mathrm{C1}}, \tag{20}$$
$$K_{\mathrm{I}} = 1/(R_{\mathrm{C1}} \cdot C_{\mathrm{C}}). \tag{21}$$

As output buffer amplifier, a push-pull emitter-follower (Q_{n}, Q_{p}) can be used to provide the high analog bandwidth and the needed current gain. In doing so, the parallel connection of lower current rated bipolar transistors is beneficial compared to single devices in terms of current gain (typ. $h_{\mathrm{FE}} > 100$) and analog bandwidth ($f_{\mathrm{T}} > 100\,\mathrm{MHz}$). In addition, the operational amplifier must be able to operate at $\pm 15\,\mathrm{V}$, featuring a high bandwidth and provide comparably high current source and sink capabilities.

D. Clipping of Negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ Feedback at Turn-On

Ideally, the time intervals with current and voltage slopes at hard switching are not overlapping as illustrated in section III-A, which enables the proposed combined and subsequently active $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control. However, at turn-on the collector current i_{C} is reduced after the diode's peak reverse recovery current i_{rr}, i.e. during the voltage slope. To achieve an optimal control of $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$, the negative $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback, at which the feedback voltage v_{Ee} is positive, must be prevented or at least strongly attenuated at turn-on. This can be achieved by inserting the proposed clipping circuit shown in Fig. 19 into the $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ feedback path. In doing so, the switch S_{c} must be closed during the entire turn-on transients as shown in Fig. 12. The positive voltage of v_{Ee} at current fall will thus be restricted to the forward voltage of diode D_{c} multiplied by the dividing ratio of the compensated voltage divider ($R_2||C_2$, $R_3||C_3$). In contrast, the negative voltage of v_{Ee} during current rise is not clipped since D_{c} blocks in this case. At turn-off, S_{c} is open and no clipping takes place.

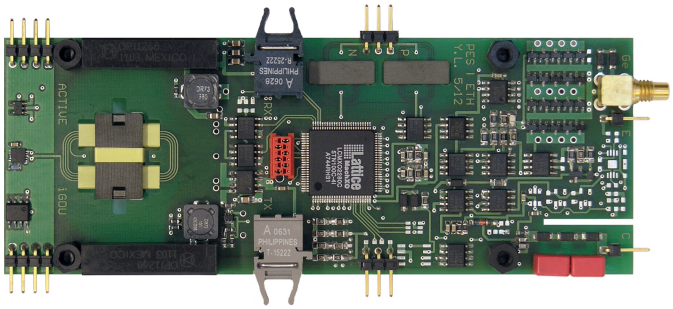

Fig. 20: Developed prototype of the proposed closed-loop gate driver; dimensions of the PCB: 50 mm x 133.3 mm and / or 1.97 in x 5.25 in.

E. Hardware Prototype

A prototype of the proposed closed-loop gate driver was developed, cf. Fig. 20, that contains all described measurement and control circuits, in order to experimentally verify the concept. The setting of the control reference signals and the multiplexers are triggered by a finite state machine running at 100 MHz implemented in a complex programmable logic device (CPLD) on the gate driver.

VI. Experimental Verification

In the following, experimental measurement results using the developed gate driver prototype, cf. Fig. 20, are presented in order to verify the closed-loop $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control concept proposed in this paper. All subsequent measurements are based on double-pulse tests by means of an experimental test setup consisting of a DC link capacitor, a half-bridge IGBT module and an air-core inductor as inductive load.

A. Independent Control of $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$

Fig. 21 shows the independent control of the current and voltage slopes at the turn-on and turn-off transients for IGBT module (B)*, cf. appendix A. Setting the different individual references of $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ was carried out by adjusting the feedback gains k_I and k_V, cf. Fig. 11, and (1) or (2), respectively. Based on these measurements, the independent $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ and $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ control of the proposed closed-loop gate driver could experimentally be approved. In practice, this enables a defined switching behavior of the IGBT in the SOA and a desired trade-off between switching losses and EMI.

B. Comparison to Resistive Gate Driver

In order to comprehensively illustrate the benefits of the proposed closed-loop gate driver regarding switching losses, a comparison to a passive, i.e. resistive, gate driver is provided in the following. For the experimental analysis the low-side switch of a 300 A, 1.2 kV IGBT half-bridge module (Infineon FF300R12MS4) in EconoDUAL housing has been selected, in order to additionally verify the gate driver for a different type of semiconductor and / or housing.

The passive gate driver's resistors for turn-on and turn-off were adjusted for a maximum $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ of ca. $\mp 1\,\mathrm{kA}/\mu\mathrm{s}$. Thereby, a $\mathrm{d}v_{\mathrm{CE}}/\mathrm{d}t$ of roughly $\pm 0.5\,\mathrm{kV}/\mu\mathrm{s}$ results, cf. Fig. 22 (a). The same $\mathrm{d}i_{\mathrm{C}}/\mathrm{d}t$ was set with the closed-loop

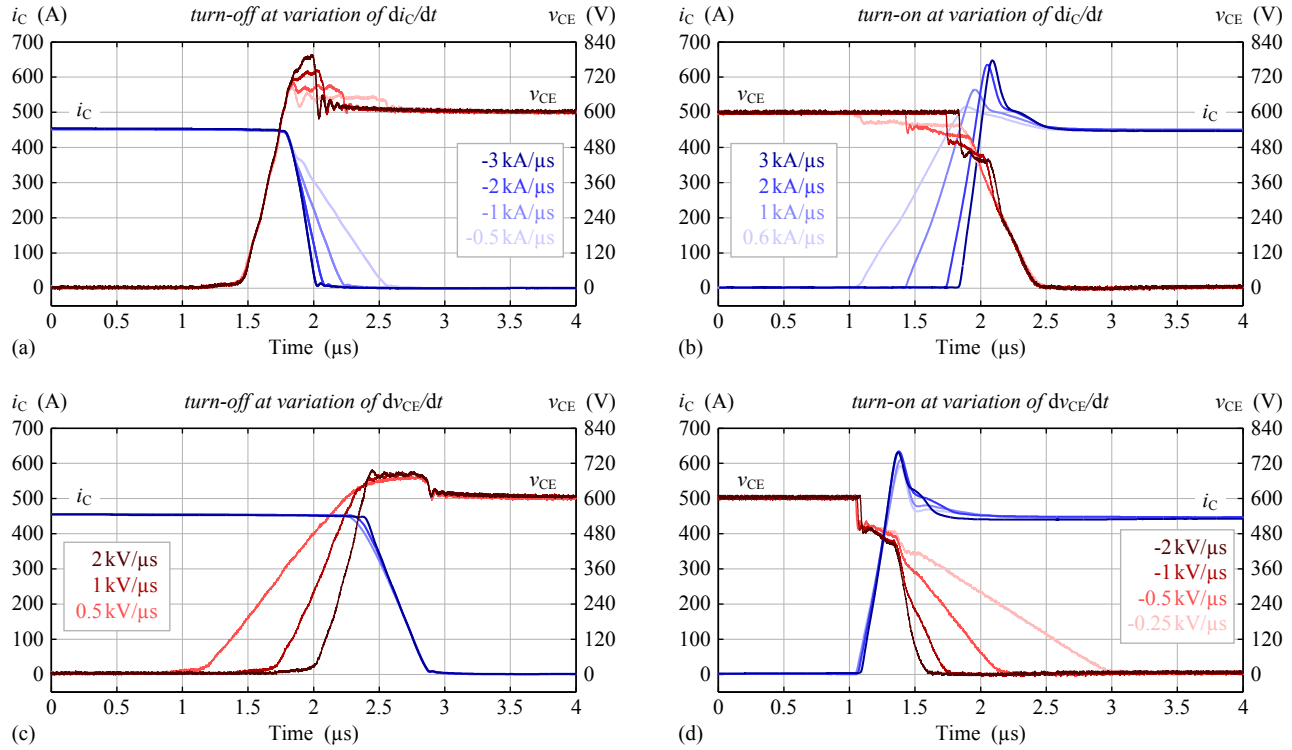

Fig. 21: Measurement results at closed-loop switching of IGBT (B)* for different $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and/or $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ reference values. Variation of $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ at (a) turn-off with $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t_\mathrm{ref} = 2\,\mathrm{kV}/\mu\mathrm{s}$ and (b) turn-on with $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t_\mathrm{ref} = -1\,\mathrm{kV}/\mu\mathrm{s}$. Variation of $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ at (c) turn-off with $\mathrm{d}i_\mathrm{C}/\mathrm{d}t_\mathrm{ref} = -1\,\mathrm{kA}/\mu\mathrm{s}$ and (d) turn-on with $\mathrm{d}i_\mathrm{C}/\mathrm{d}t_\mathrm{ref} = 2\,\mathrm{kA}/\mu\mathrm{s}$.

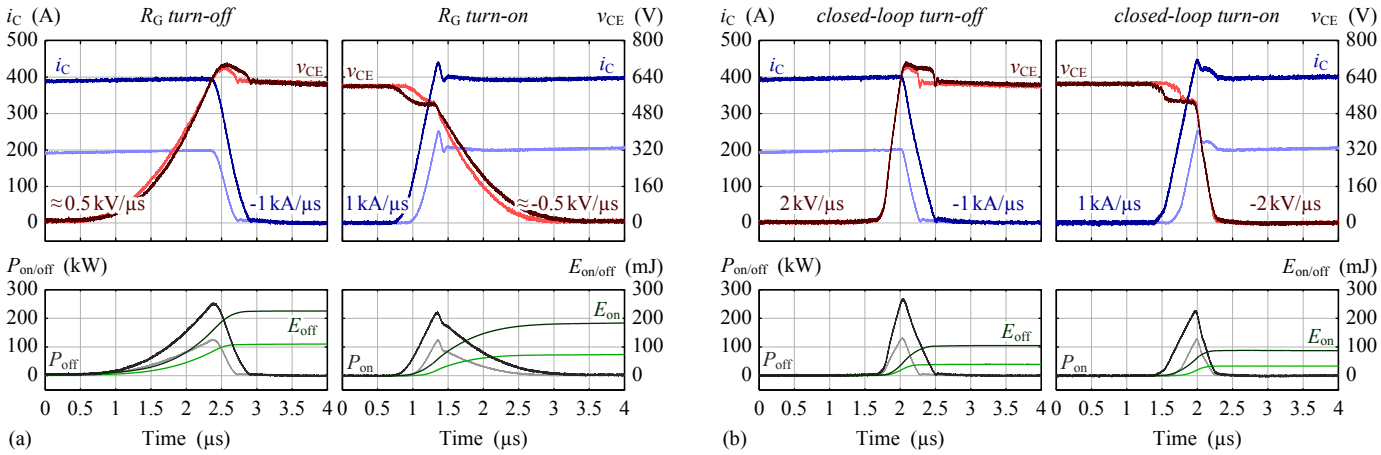

Fig. 22: Experimental comparison of the turn-off and turn-on switching trajectories and switching losses at employing (a) a resistive gate driver and (b) the proposed closed-loop gate driver.

gate driver, however, contrary to the resistive gate driver, the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ can be selected independent of the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and has been set to $\pm 2\,\mathrm{kV}/\mu\mathrm{s}$ in this case, cf. Fig. 22 (b). For both gate drivers, similar current slopes and accordingly similar diode peak reverse recovery currents and turn-off overvoltages result. However, due to the faster voltage slope, the switching losses of the closed-loop gate driver are about halved in comparison to the resistive gate driver. The ability of setting $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ individually from each other enables to significantly reduce the switching losses in cases, where the gate resistors of a passive gate driver cannot be reduced due to restrictions of SOA operation or EMI.

C. Comparison of Different IGBT Modules

Fig. 23 shows the closed-loop control of IGBT modules (A), (B)*, and (C), cf. appendix A, at turn-on for a variation of the load current i_o. In accordance with the stability analysis of Section IV and Fig. 15, IGBT module (B)* shows the most accurately controlled current and voltage values. Slight oscillations are observable for module (A) and the controllability of module (C) is most demanding due to the high gate loop inductance. This result is in accordance with the expected behavior, i.e. for larger gate loop inductance L_gl a high PI-controller gain must be selected to achieve a fast control, which in turn causes a less accurate and/or less stable control.

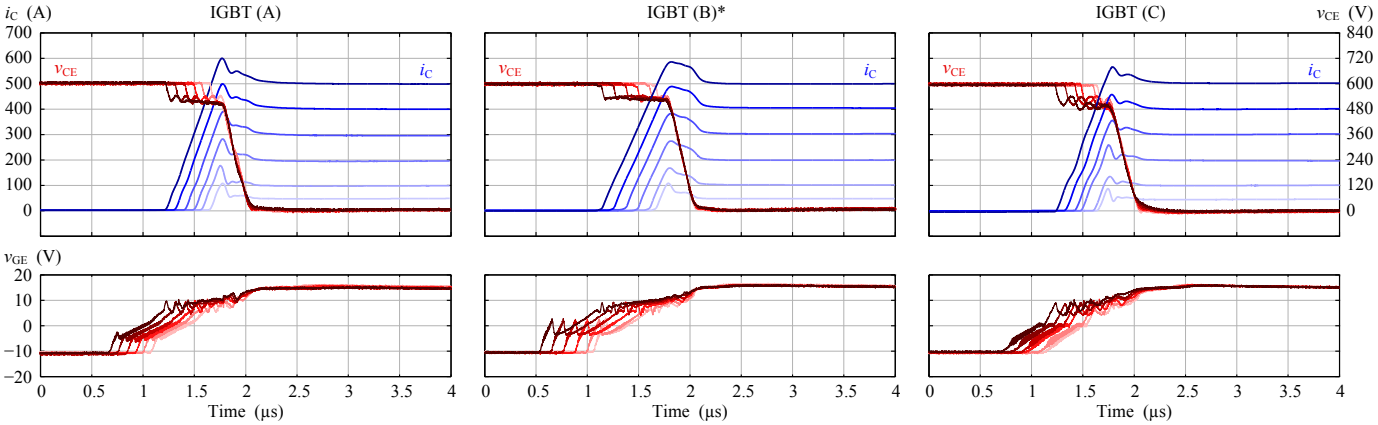

Fig. 23: Measured closed-loop controlled turn-on waveforms at $1\,\mathrm{kA}/\mu\mathrm{s}$, $-2\,\mathrm{kV}/\mu\mathrm{s}$ of the IGBT modules (A), (B)* and (C).

In addition, Fig. 23 depicts the natural transition from the $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ to the $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control. Independent of the level of the load current i_o, the gate driver first controls the current slope. As soon as the diode reverse recovery current peak is reached, which takes longer for larger values of i_o, the gate voltage v_Ge is controlled according to the voltage slope reference.

D. Closed-Loop Control Using SiC Diodes

The gate driver was also tested in combination with the low-side switch of a $1.2\,\mathrm{kV}$, $300\,\mathrm{A}$ IGBT half-bridge module containing SiC-diodes (Infineon FF300R12MS4F_ENG), and compared to an IGBT half-bridge module comprising conventional Si-diodes (Infineon FF300R12MS4). The corresponding comparative measurements are shown in Fig. 24. It can be summarized, that the control is accurate and stable for the conventional module as well as for the module with SiC-diodes. As expected, the SiC diode does not show any reverse recovery effect, but its abrupt blocking excites a small ringing between the stray inductance and the parasitic capacitance of the diode.

VII. Conclusion

In this paper, a highly dynamic closed-loop IGBT gate driver providing independent $\mathrm{d}i_\mathrm{C}/\mathrm{d}t$ and $\mathrm{d}v_\mathrm{CE}/\mathrm{d}t$ control is presented and investigated. It permits to adjust the current and voltage slopes according to set-point values largely independent of nonlinearities or parameter variations of the IGBT. Therewith, a degree of freedom for the converter design is gained, which allows to ensure an operation in the SOA and a defined trade-off between switching losses and EMI independent of the load current level, the DC-link voltage or the junction temperature of the employed IGBTs.

By means of using only simple passive measurements for the generation of the feedback signals and a single operational amplifier as PI-controller, high analog control bandwidth is achieved enabling the application of a closed-loop gate driver even for switching times in the sub-microsecond range.

Furthermore, the closed-loop gate control allows combining IGBTs from different manufacturers for the realization of a converter system without requirement of tuning gate resistors etc. as typically required for conventional gate driver circuits.

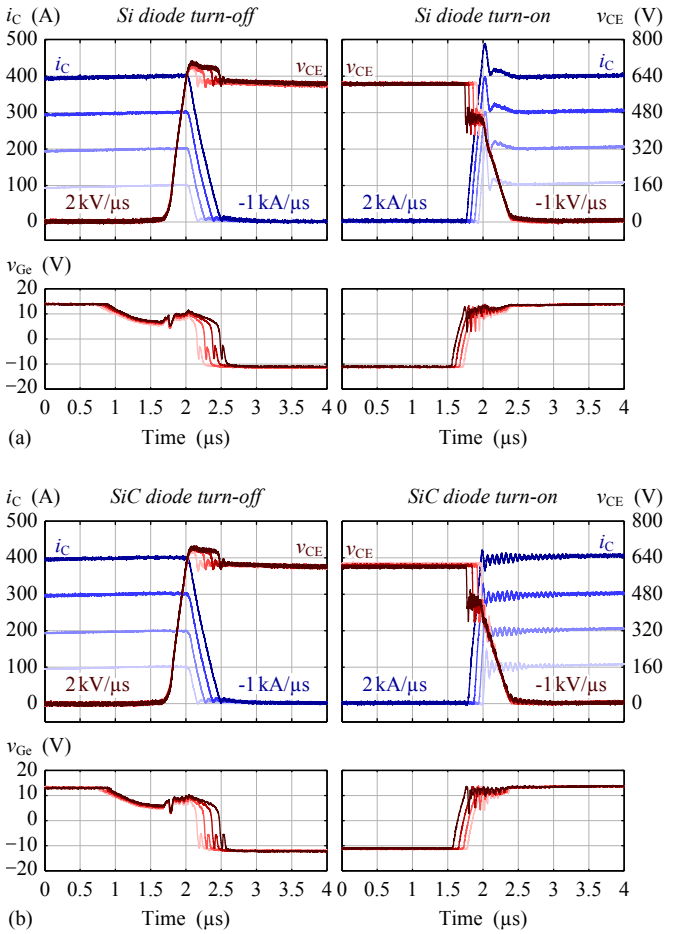

Fig. 24: Measurement results for the (a) conventional Si-diode Si-IGBT module and (b) SiC-diode Si-IGBT module. Turn-off at $-1\,\mathrm{kA}/\mu\mathrm{s}$, $2\,\mathrm{kV}/\mu\mathrm{s}$ and turn-on at $2\,\mathrm{kA}/\mu\mathrm{s}$, $-1\,\mathrm{kV}/\mu\mathrm{s}$.

Accordingly, the proposed gate driver concept facilitates a minimization of production and maintenance costs and therefore could support a widespread application of power electronic converters in industry and renewable energy systems.

Future research will address the application of the gate driver concept in bridge leg configurations with a focus on the safe operation in nominal and failure case and a minimum distortion of the output voltage.

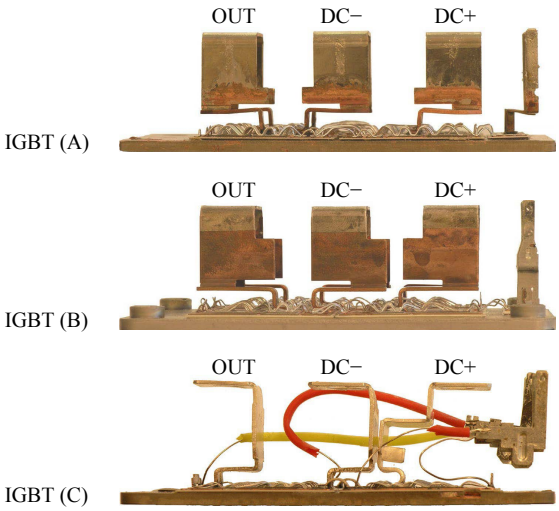

Fig. 25: Side view with visible construction of the screw terminals for the power connections of the disassembled half-bridge IGBT modules of manufacturers (A) - (C).

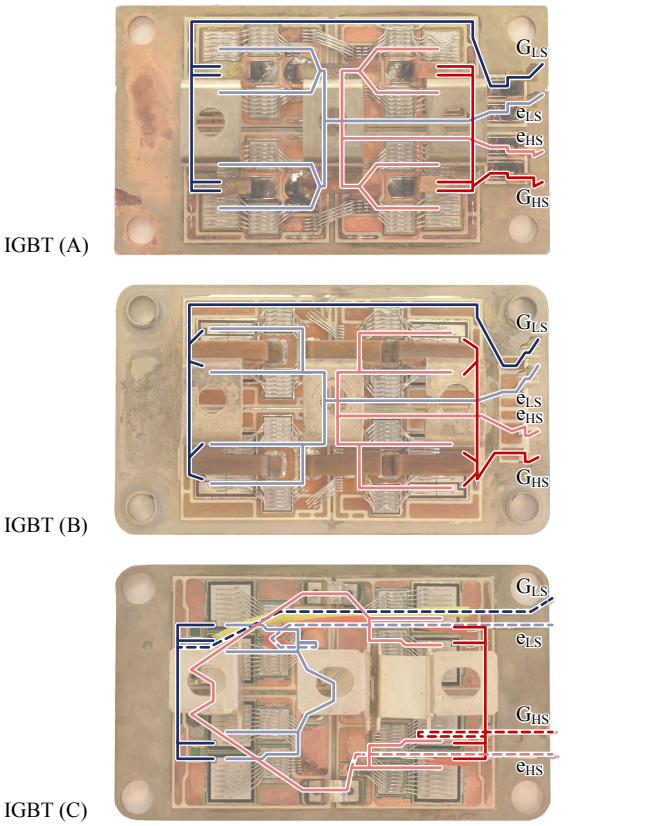

Fig. 26: Top view of the IGBT modules (A) - (C) with highlighted gate- and auxiliary emitter connections (solid: bond wire connections; dashed: silicon insulated cabling).

APPENDIX A
IGBT MODULE PARASITICS AND MODEL PARAMETERS

In order to perform a stability analysis of the proposed closed-loop gate driver, the parameters of the small-signal IGBT model, cf. Fig. 13, and their variations must be known. For that reason, in this section the parasitic inductances of three IGBT modules from different manufacturers are investigated. The remaining model parameters of these modules are subsequently extracted from the IGBTs' datasheets.

A. Parasitic Inductances

Parasitic inductances of an IGBT module are in general undesired. On the one hand, the total inductance in the power path L_{pp} contributes to the parasitic inductance L_{s} of the commutation path, which is causing an overvoltage at the IGBT's turn-off transients, cf. Fig. 3. On the other hand, as shown in this paper, the inductance in the gate loop L_{gl} is negatively affecting the achievable control bandwidth of the closed-loop IGBT gate driver, cf. Fig. 15.

Source of the IGBT module's parasitic inductances is the mechanical setup, which is consisting of the screw terminals for the power connections, the gate driver terminals and the internal wiring, e.g. via bond wires. Three IGBT half-bridge modules from different manufacturers in the $1.2\,\mathrm{kV}$ class with current ratings of 400-450 A (all in $62\,\mathrm{mm}$ housing) have been disassembled, in order to illustrate and compare their mechanical setups and parasitic inductances.

Fig. 25 depicts the construction of the IGBT module's power terminals, which are a main reason for the parasitic inductance L_{pp}. It's apparent that the DC+ and DC− terminals of modules (A) and (B) are located side by side, whereas a coplanar, i.e. low-inductive, layout is employed for module (C). According to the measured inductance values depicted in Fig. 27, module (C) exhibits the lowest value of L_{pp} as a result of it's coplanar layout and module (A) shows the largest value of L_{pp} due to the parallel layout with large geometric distance. The module's internal gate and auxiliary emitter wirings are highlighted in Fig. 26, to compare the different manufacturing approaches. Bond wires are employed for modules (A) and (B) to interconnect the gate driver terminals and the IGBT chips resulting in similar values of the gate loop inductances, cf. Fig. 27. Module (C) uses, in addition to the bond wires, silicon insulated cables for the connection from the module terminals to the baseplate, what results in additional wiring loops and thus increased gate loop inductances.

Since the gate driver terminals are located next to the high-side IGBT and diode chips, the gate loop of the low-side IGBT is considerably larger than the one for the high-side device as depicted in Fig. 26. Accordingly, larger values result for the measured low-side gate loop inductance $L_{\mathrm{gl,LS}}$ than for the high-side inductance $L_{\mathrm{gl,HS}}$ as shown in Fig. 27. In order to investigate and experimentally verify the impact of reduced parasitic gate loop inductance on the closed-loop control, the high-side gate driver terminals of module (B) have been bypassed by a low-inductive coaxial connection. Therewith, $L_{\mathrm{gl,HS}}$ of module (B) was reduced by $26\,\mathrm{nH}$ and / or $46\,\%$ as illustrated in Fig. 27. This modified module is denominated as module (B)* in this paper ($L_{\mathrm{gl,LS}}$ is not modified, as only the high-side switch is operated and only the freewheeling diode of the low-side switch is utilized).

B. Small-Signal IGBT Model Parameters

The remaining parameters of the IGBT model are derived from the IGBT's data sheets and are summarized in Table III.

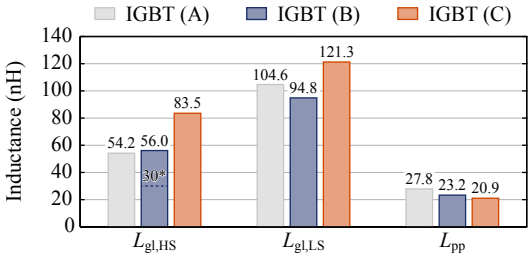

Fig. 27: Measured gate loop and power path inductances of the three IGBT modules (A), (B) and (C) shown in Fig. 25 and Fig. 26. The gate loop inductance is measured between the gate terminal and auxiliary emitter terminal of the high-side ($L_{\mathrm{gl,HS}}$) and the low-side ($L_{\mathrm{gl,LS}}$) IGBT. The total inductance in the power path L_{pp} is measured from the DC+ to the DC- connector with a straight connection of both terminals for closing the measurement loop. In case a low-inductance coaxial connection to the foot ends of the gate driving terminals, i.e. a direct connection to the corresponding pads of the DBC would be used, the parasitic gate loop inductance $L_{\mathrm{gl,HS}}$ of module (B) could be reduced from 56 nH to 30 nH. The corresponding module is denominated as (B)*.

	IGBT (A)	*IGBT (B)**	*IGBT (C)*
g_m (S)	200	200	200
R_{G} (Ω)	2	2.05	1.62
L_{B} (nH)	1	1	1
L_{E} (nH)	2.1	3.85	3.2
L_{C} (nH)	11	6.75	6.25
L_{G} (nH)	27.1	15	41.7
L_{e} (nH)	27.1	15	41.7
C_{GE} (nF)	34.9	26.9	23
C_{GC} (nF)	0.61	0.32	0.87
C_{O} (nF)	0.06	0.03	0.09
R_{O} (Ω)	50	50	50

TABLE III: Parameter values of the high-side IGBTs (A), (B)* and (C). Operating point: $v_{\mathrm{CE}} = 300\,\mathrm{V}$, $i_{\mathrm{C}} = 200\,\mathrm{A}$.

The values for the transconductance g_m at a current $i_{\mathrm{C}} = 200\,\mathrm{A}$, the gate capacitance

$$C_{\mathrm{GE}} = C_{\mathrm{ies}} - C_{\mathrm{res}} \tag{22}$$

and the Miller capacitance

$$C_{\mathrm{GC}}(v_{\mathrm{CE}}) \approx C_{\mathrm{GC,ref}} \sqrt{\frac{v_{\mathrm{CE,ref}}}{v_{\mathrm{CE}}}} \tag{23}$$

at a voltage $v_{\mathrm{CE}} = 300\,\mathrm{V}$ can directly be extracted and calculated. The output capacitance

$$C_{\mathrm{O}} = C_{\mathrm{oes}} - C_{\mathrm{res}} \tag{24}$$

is assumed to be smaller by a factor of 10 than C_{GC}. R_{O} is typically not specified in the data sheet, thus a typical value for an 1.2 kV, 400 A IGBT [49] is used. R_{G} and L_{E} have been measured with an impedance analyzer. The measured gate loop inductance, $L_{\mathrm{gl,HS}}$, cf. Fig. 27, is assumed to be equally split to L_{G} and L_{e}. L_{B} in modules with auxiliary emitter terminal is typically very small, can hardly be measured and was thus estimated. Assuming that the inductance of the power path is split into two equal parts for the high and the low side IGBT,

$$L_{\mathrm{C}} \approx L_{\mathrm{pp}}/2 - L_{\mathrm{B}} - L_{\mathrm{E}}. \tag{25}$$

is used to calculate L_{C}.

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