Letters to the Editor

Comparison of 3-Phase Wide Output Voltage Range PWM Rectifiers

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***Abstract*—A three-phase buck + boost pulsewidth modulation (PWM) rectifier with a three-switch buck-type rectifier input stage and an integrated dc/dc boost converter output stage, and a three-phase boost + buck PWM rectifier system formed by series connection of a boost-type rectifier input stage (Vienna Rectifier) and a dc/dc buck converter output stage are presented and comparatively evaluated. Both systems are characterized by sinusoidal input current and wide output voltage control range. The comparison is for 6 kW rated output power at 400 Vrms line-to-line input and variable output voltage 200 V, . . . , 600 V and identifies the buck + boost approach as significantly superior regarding the overall efficiency, the volume and weight of the passive power components, and the overall system complexity.**

***Index Terms*—System efficiency, three phase pulsewidth modulation (PWM) rectifiers, wide output voltage range.**

I. Introduction

For industrial applications like variable speed six-step inverter drives or power supplies for plasma technology, a variable dc voltage has to be provided. Aiming for unity power factor mains operation, this dc voltage can be generated using a buck + boost converter concept (cf., Fig. 1), formed by the integration of a three-phase three-switch buck-type input stage [1] and a boost-type dc/dc output stage [2]. Alternatively, a three-phase three-switch three-level boost-type pulsewidth modulation (PWM) (Vienna) rectifier [3] with series connected three-level buck-type dc/dc output stage (cf., Fig. 2) could be employed.

In this paper, both converter concepts are compared for a 6 kW plasma power supply application with 400 Vrms three-phase line-to-line input and a dc output voltage range of $U_0 = 200\ \mathrm{V}, \ldots, 600\ \mathrm{V}$. The comparison is focused on three aspects, namely: 1) the system efficiency, where results of switching loss measurements [4], [5] are utilized; 2) the volume and weight of both systems; and 3) system aspects like complexity and realization effort. For performing a fair comparison for both systems, latest semiconductor technology is assumed to be employed and switching frequencies have been selected, which guarantee a good compromise between efficiency and power density.

In the following, the topology shown in Fig. 1 is denominated as buck + boost rectifier and the topology in Fig. 2 as boost + buck rectifier.

II. Comparative Evaluation of the Systems

In the following, the buck + boost and the boost + buck systems are compared concerning:

1) overall efficiency;
2) volume and weight;
3) system aspects.

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The comparison in this paper is based on the separate design of the buck + boost and the boost + buck topology, where each design aims for a good balance between system efficiency and power density. In the case at hand, the voltage stresses on the power semiconductors of the input stages are different, wherefore also the utilized semiconductor technologies and the appropriate switching frequencies have to be selected differently.

In [4] it was shown that for the buck + boost system (comprising a 1200 V insulated gate bipolar transistor (IGBT) input stage and a 600 V power MOSFET in the boost output stage) $f_{\mathrm{S,BuBo}} = 25$ kHz is a good selection, and for the boost + buck system, where all turn-off power semiconductors are realized by power MOSFETs, $f_{\mathrm{S,BoBu}} = 50$ kHz can be chosen. As a detailed analysis shows, the switching frequency has to be chosen much higher for the boost + buck topology as compared to the buck + boost topology in order to achieve a high power density as it is given for the buck + boost topology already for low switching frequencies. If a lower switching frequency for the boost + buck system were chosen, a considerably higher volume and weight of the passive components would result as will be shown in Section II. The components of both systems are selected in [4] and are compiled in Table I.

A. Overall Efficiency

The dependence of the efficiency of the buck + boost and the boost + buck rectifier on the output voltage is depicted in Fig. 3. For $U_0 = 200$ V the boost + buck topology shows slightly lower losses than the buck + boost converter, where an IGBT is lying in each input phase current path. Due to the relatively high conduction losses (originating from the high output current I at low U_0) and the fast reverse recovery behavior of the power diodes in combination with the low switching frequency ($f_{\mathrm{S}} = 25$ kHz), switching losses are not taking significant influence on the efficiency although devices with 1200 V blocking capability are employed.

For $U_0 = 400\ \mathrm{V}, \ldots, 600$ V the buck + boost topology exhibits the highest efficiency. There, both power transistors of the buck output stage of the boost + buck system are switching half the rectifier stage output voltage, i.e., $u_{\mathrm{sw}} = U/2$, therefore, the total buck-stage switching losses are proportional to the full dc link voltage, $P_{\mathrm{sw}} \sim U = 800$ V.

In contrast, the switching losses of the buck input stage of the buck + boost system are approximately proportional to the average value of the highest mains line-to-line voltage over every $\pi/3$ mains interval, therefore $P_{\mathrm{sw}} \sim \hat{U}_{N,l-l,\mathrm{avg},\pi/3'} = 3/\pi \cdot \sqrt{2} \cdot 400\ \mathrm{V} = 540\ \mathrm{V}$.

Remark: This approximation shall only show a main characteristic, the dependence of the switching losses on square terms of voltage and current according to (1) in [4] is not considered here. Furthermore, there are only conduction losses in the diode of the buck + boost converter boost stage as the boost power transistor is activated only for $U_0 > 490$ V, while the input (boost) stage of the boost + buck rectifier is operating continuously in order to maintain the PFC function of the system. Therefore, for $U_0 > 270$ V the buck + boost topology exhibits a significantly higher efficiency than the boost + buck system.

As shown in [6], the system efficiency serves as the main indicator for the operation costs of a converter. In the case at hand, the higher efficiency of 0.7% for the buck + boost topology (at $U_0 = 400$ V) would result in an energy economization of 368 kW · h per year for continuous operation at 6 kW. Assuming an energy prize of \$0.13 U.S. per kW · h (average energy cost for industry and

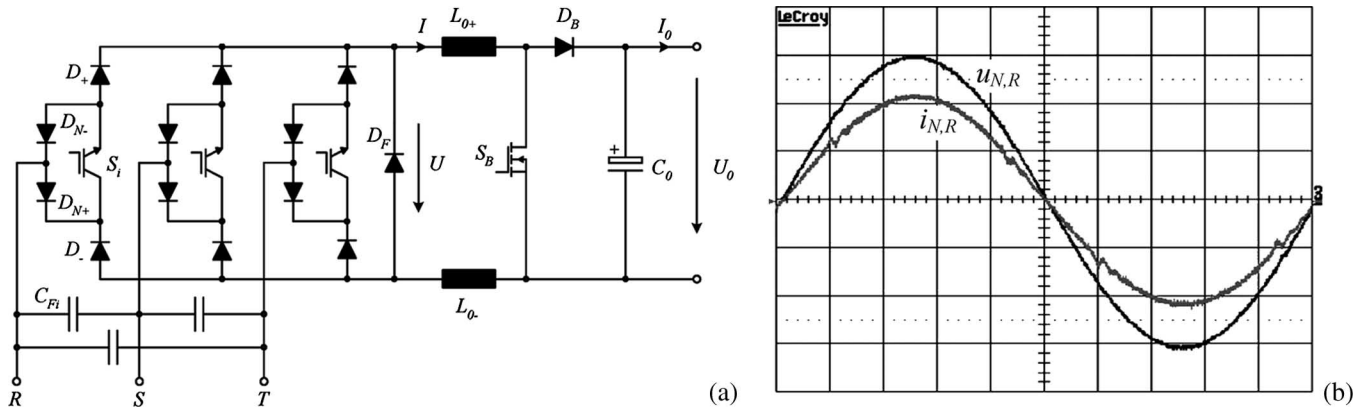

Fig. 1. (a) Three-phase/switch buck-type PWM rectifier with integrated dc/dc boost-type output stage and (b) measured mains phase voltage and mains phase current waveforms (voltage scale 100 V/div, current scale 5 A/div). For the measurement of the mains current a two-stage EMC input filter has been included that is not shown in (a).

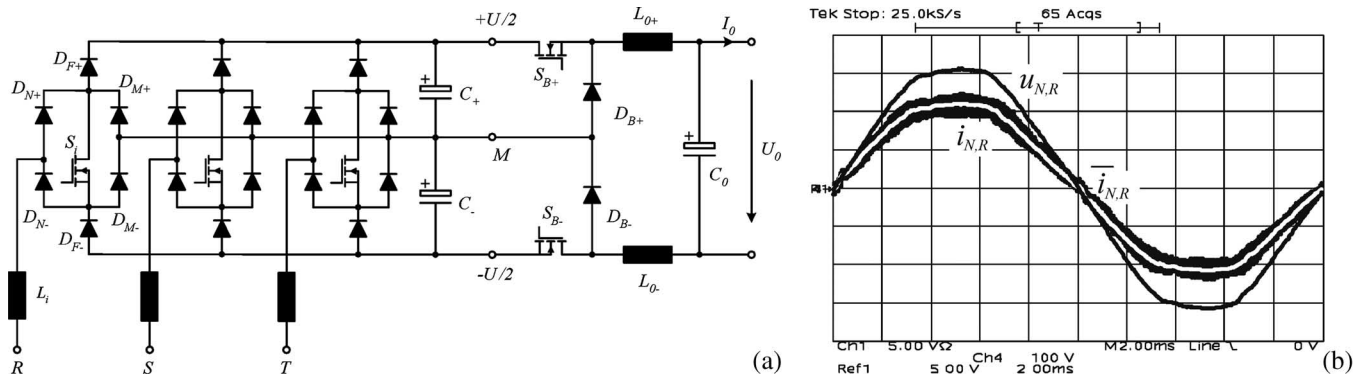

Fig. 2. (a) Three-phase/level/switch-boost-type PWM (Vienna) rectifier with three-level buck-type output stage and (b) measured voltage and current waveforms (voltage scale 100 V/div, current scale 5 A/div). For the measurement of the mains current a two-stage EMC input filter has been employed which is not shown in (a). Remark: Due to the deviation of the mains phase voltage, being present at the time of measurement, the current does not show a perfectly sinusoidal shape. In case the system would be supplied by a power amplifier providing a perfectly sinusoidal voltage, the input current quality would be identical to Fig. 1(b).

households in industrialized countries according to the International Energy Agency [7]) this results in a cost reduction of $565 U.S. per rectifier unit over a time period of ten years for an estimated interest rate of 3% per year.

B. Volume and Weight

The volumes and weights of the rectifier systems are mainly determined by the passive components and the heat sinks. Since the power losses are comparable for both topologies (cf., Fig. 3), volume and size of the required heat sink will show little difference. Assuming an ambient temperature of $T_\mathrm{a} = 45\ ^\circ\mathrm{C}$ and considering a maximum heat sink temperature of $T_\mathrm{h} = 95\ ^\circ\mathrm{C}$ being sufficiently lower than the maximum admissible power semiconductor junction temperatures, we have for the thermal resistance of the heat sink

$$R_{\mathrm{th,h}} = \frac{T_\mathrm{h} - T_\mathrm{a}}{(1-\eta)\cdot P_\mathrm{in}} = 0.1\ \mathrm{K/W} \tag{1}$$

(η denotes the overall efficiency) resulting in a heat sink volume of $V_\mathrm{hs} = 2.1\ \mathrm{dm}^3$ and/or a heat sink weight of $m_\mathrm{hs} = 2.5$ kg assuming a commercially available product [8] with forced cooling by a 24 Vdc fan. For a heat sink with optimized airflow $V_\mathrm{hs} = 0.37\ \mathrm{dm}^3$ could be achieved [9], and for water-cooled systems even $V_\mathrm{hs} = 0.04\ \mathrm{dm}^3$ [10] (without heat exchanger, pump, and pipes).

In order to highlight the differences of both topologies the heat sink is not included in the comparison depicted in Fig. 3. Furthermore, the electromagnetic compatibility (EMC) input filter, which is somehow comparable for the two systems (the EMC filter of the buck + boost system has a volume of $V_\mathrm{EMC} = 0.4$ l and a weight of $m_\mathrm{EMC} = 0.95$ kg [11]), is not considered in Fig. 3. The buck + boost topology is advantageous over the boost + buck system concerning weight and volume of the passive power components. This is due to the larger number of inductors required for the boost + buck system, where the input inductors despite the higher switching frequency already show a volume comparable to the output inductors L_{0+}, L_{0-} of the buck + boost system. Furthermore, a relatively large dc link capacitor is required for the boost + buck topology in order to accommodate the rms current stress originating from the discontinuous boost stage output and buck stage input currents (advantageously, the switching of both stages is synchronized for minimizing the capacitor current stress). In comparison, the input filter capacitors of the buck + boost rectifier are showing a considerably lower volume.

If the same switching frequencies $f_\mathrm{S,BuBo} = f_\mathrm{S,BoBu} = 25$ kHz were selected for the two systems in order to achieve similar overall efficiencies (at $U_0 = 400$ V) the volume and weight of the passive components of the boost + buck topology would approximately double, if the same ripple values shall be maintained. Compared to the buck + boost system, the size and the weight of the passive components would therefore in total nearly be four times larger, resulting in a very poor power density of the boost + buck system.

C. System Aspects

Besides, efficiency, weight, and volume, also system aspects like the behavior in case of an output short-circuit or mains voltage

TABLE I
SPECIFICATIONS OF THE UTILIZED COMPONENTS FOR THE BUCK + BOOST AND FOR THE BOOST + BUCK TOPOLOGY

	Component	Specification		
Buck+Boost	*IGBTs* S_i	SGH20N120RUF, 1200 V, 20 A, U_{CE0} = 1.28 V , r_{CE} = 35 mΩ,	$k_{1,on}$ = 42 µJ/A, $k_{1,off}$ = 66 µJ/A,	
	Diodes D_i, *FW Diode* D_F	RHRP30120, 1200V, 30A U_F = 0.97 V , r_D = 24 mΩ,	$k_{1,rr}$ = 5 µJ/A	
	S_B	SPW47N60C3, 600V, 47A $R_{DS,ON}$ = 70 mΩ,	$k_{1,on}$ = 39 µJ/A, $k_{1,off}$ = 8.3 µJ/A	
	D_B	30EPH06, 600V, 30A U_F = 0.67 V , r_D = 15 mΩ,	$k_{1,rr}$ = 3.2 µJ/A	
	$C_{F,i}$	PHE840M	$C_{F,i}$ = 4.7 µF @ 280 Vac	ESR = 23 mΩ
	C_0	B43501	C_0 = 2x 470 µF @ 420 Vdc	ESR = 140 mΩ
	L_{0+}, L_{0-}	METGLAS	$L_{0+} = L_{0-}$ = 450 µH @ 30 A	AMCC16B, N = 58
Boost+Buck	*MOSFETs* S_i	SPW47N60C3, 600 V, 47 A, $R_{DS,ON}$ = 70 mΩ,	$k_{1,on}$ = 28.5 µJ/A, $k_{1,off}$ = 8.3 µJ/A	
	FW Diodes D_{Fi}	HFA25PB60, 600V, 25A U_F = 0.95 V , r_D = 24 mΩ,	$k_{1,rr}$ = 3.2 µJ/A	
	Discrete Diodes D_{Mi},D_{Ni}	GBPC2506, 600V, 25A U_F = 0.75 V , r_D = 12 mΩ,		
	S_{B+}, S_{B-}	IXKN 75N60C, 600V,75A $r_{DS,ON}$ = 70 mΩ,	$k_{1,on}$ = 39 µJ/A, $k_{1,off}$ = 8.3 µJ/A	
	D_{B+}, D_{B-}	DSEP 2x91-06A, 600V, 91A U_F = 1 V , r_D = 11 mΩ,	$k_{1,rr}$ = 3.2 µJ/A	
	L_i	METGLAS	L_i = 350 µH @ 20 A	AMCC10, N = 45
	C_+, C_-	B43501	$C_+ = C_-$ = 4x 470 µF @ 420 Vdc	ESR = 140 mΩ
	L_{0+}, L_{0-}	METGLAS	$L_{0+} = L_{0-}$ = 130 µH @ 30 A	AMCC8, N = 32
	C_0	B43501	C_0 = 1x 470 µF @ 420 Vdc	ESR = 140mΩ

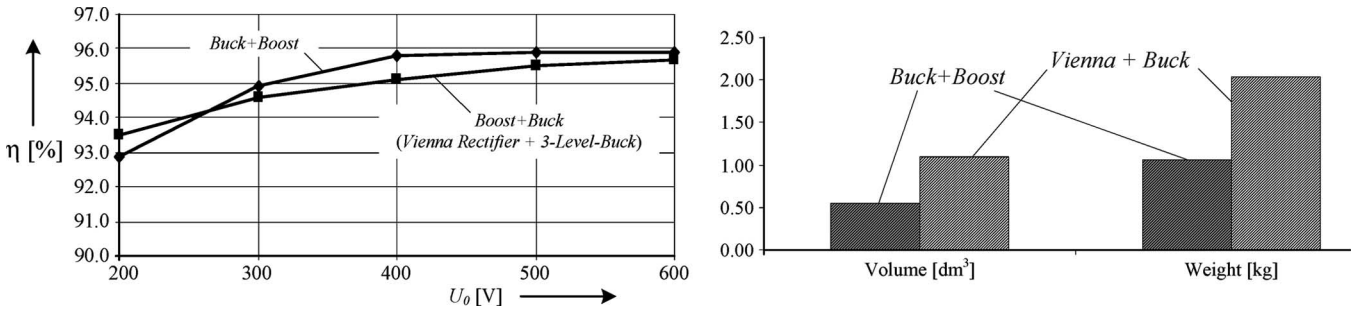

Fig. 3. Comparison of the overall efficiencies of the two topologies for different output voltages (left) and comparison of volume and weight of the passive components of the two topologies (right) (heat sink, cooling fans, power semiconductors, auxiliary supply, etc., are not included).

unbalance have to be included in the system evaluation. Furthermore, complexity/reliability and manufacturing effort constitute important aspects.

As can be seen directly from comparing Figs. 1 and 2, the buck + boost system shows a considerably lower realization effort/complexity of the power circuit than the boost + buck topology, e.g., lower number of active and passive components. Furthermore, for the control of the buck + boost system only one dc-sided current sensor is required, while for the control of the boost + buck system three current sensors have to be employed. Finally, the buck + boost topology does allow a direct system start-up and/or does not rely on a precharging of a dc link capacitor.

Both systems can be operated in current limiting mode in case of an output short circuit and can maintain unity power factor input behavior also in case of heavily unbalanced mains and/or loss of a mains phase [12], [13].

An aspect which has to be given attention in case of mains voltage distortions and operation of multiple systems in parallel is the proper damping of the input filter of the buck + boost system, which should be implemented using passive and active (control) means [11].

III. CONCLUSION

Two three-phase unidirectional unity power factor PWM rectifier topologies, i.e., a buck + boost and a boost + buck system are comparatively evaluated concerning efficiency, volume, weight and system aspects. Both systems are designed for 6 kW rated power, 400 Vrms line-to-line input and wide output voltage range from 200 to 600 V, where a realization of the input stages based on latest discrete power semiconductors is considered.

The three-phase buck + boost rectifier shows a slightly higher overall efficiency in a main part of the operating range which effects

lower operating costs and is characterized by lower weight and volume of the passive power components. This is also given for including the input filter inductors required for the buck + boost system into the considerations. Reducing the switching frequency of the boost + buck system from 50 to 25 kHz would reduce the system losses but would also further increase the weight and volume drawback.

A further advantage of the buck + boost converter over the boost + buck concept is the lower complexity of the power circuit and the lower sensing effort and the soft-start capability. Both concepts allow an active current limitation in case of an output short circuit and could continue in operation also for heavily unbalanced mains and/or loss of a mains phase (two-phase operation).

With reference to the aforementioned advantages the buck + boost rectifier system is also a promising topology for applications in future More Electric Aircrafts [14], which are characterized by high reliability requirements, 115 Vrms rated mains voltage, 400 Hz, . . . , 800 Hz mains frequency, and extreme peak to average load ratios. There, the switching frequency would have to be raised to, e.g., 75 kHz due to the high mains frequency. However, this should not significantly impair the system efficiency if SiC devices are employed for the freewheeling diode and the upper and lower diodes of the input buck stage.

REFERENCES

[1] T. Nussbaumer, M. Baumann, and J. W. Kolar, "Comprehensive design of a three-phase three-switch buck-type PWM rectifier," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 551–562, Mar. 2007.

[2] M. Baumann, U. Drofenik, and J. W. Kolar, "New wide input range three-phase unity power factor rectifier formed by integration of a three-switch buck-derived front-end and a DC/DC boost converter output stage," in *Proc. 22nd IEEE Int. Telecommun. Energy Conf.*, Phoenix, AZ, Sep. 10–14, 2000, pp. 461–470.

[3] J. W. Kolar and F. C. Zach, "A novel three-phase three switch three-level unity power factor rectifier," in *Proc. 28th Int. Power Conversion Conf.*, Nuremberg, Germany, Jun. 28–30, 1994, pp. 125–138.

[4] T. Nussbaumer, K. Mino, and J. W. Kolar, "Design and comparative evaluation of three-phase buck boost and boost buck unity power factor PWM rectifier systems for supplying variable DC voltage link converters," in *Proc. 10th Eur. Power Quality Conf. (PCIM)*, Nuremberg, Germany, May 25–27, 2004, vol. 1, pp. 126–135.

[5] J. W. Kolar and F. C. Zach, "Design and experimental investigation of a three-phase high power density high efficiency unity power factor PMW (VIENNA) rectifier employing a novel integrated power semiconductor module," in *Proc. 11th IEEE Appl. Power Electron. Conf.*, San Jose, CA, Mar. 3–7, 1996, vol. 2, pp. 514–523.

[6] P. A. Walther, "A new rectifier system high efficient, high dense, modular, quick to install, and superior for service," in *Proc. 15th INTELEC*, Paris, France, Sep. 27–30, 1993, vol. 2, pp. 247–250.

[7] International Energy Agency, *Key World Energy Statistics 2007*. [Online]. Available: http://www.iea.org/textbase/nppdf/free/2007/key_stats_2007.pdf

[8] Fischer Elektronik, *Hohlrippen-Lüfteraggregate mit Vorkammer LA V 9 250 24*. [Online]. Available: www.fischerelektronik.de

[9] U. Drofenik, G. Laimer, and J.W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proc. Int. PCIM Eur. Conf.*, Nuremberg, Germany, Jun. 7–9, 2005, pp. 608–619.

[10] U. Drofenik, G. Laimer, and J. W. Kolar, "Pump characteristic based optimization of a direct water cooling system for a 10 kW/500 kHz Vienna rectifier," *IEEE Trans. Power Electron.*, vol. 20, no. 3, pp. 704–714, May 2005.

[11] T. Nussbaumer, M. L. Heldwein, and J. W. Kolar, "Differential mode input filter design for a three-phase buck-type PWM rectifier based on modeling of the EMC test receiver," *IEEE Trans. Ind. Electron.*, vol. 53, no. 5, pp. 1649–1661, Oct. 2006.

[12] J. Miniböck and J. W. Kolar, "A novel concept for mains voltage proportional input current shaping of a VIENNA rectifier eliminating controller multipliers," *IEEE Trans. Ind. Electron.*, vol. 52, no. 1, pp. 162–170, Feb. 2005.

[13] M. Baumann and J. W. Kolar, "A novel control concept for reliable operation of a three-phase three-switch buck-type unity-power-factor rectifier with integrated boost output stage under heavily unbalanced mains condition," *IEEE Trans. Ind. Electron.*, vol. 52, no. 2, pp. 399–409, Apr. 2005.

[14] K. Emadi and M. Ehsani, "Aircraft power systems: Technology, state of the art, and future trends," *IEEE Aerosp. Electron. Syst. Mag.*, vol. 15, no. 1, pp. 28–32, Jan. 2000.

Asymmetric Resonant Poles Sustainer for Plasma Display Panel

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***Abstract*—A new plasma display panel (PDP) sustaining driver using asymmetric resonant poles is proposed. Since asymmetric resonant poles are used for inverting the panel voltage, the flexibility in the rising time and the falling time of the panel voltage is increased. Moreover, all sustain switches are turned on with zero-voltage and a voltage notch across the panel is significantly reduced. Since the proposed circuit is implemented with reduced component counts, it features a simple structure and low cost. The operation principle is presented in detail and a 7.5-in ac PDP equipped with the proposed circuit is investigated.**

***Index Terms*—Energy recovery, sustain driver.**

I. INTRODUCTION

The plasma display panel (PDP) has advantages such as light weight, large screen, thinness, wide viewing angle and low radiation. It is expected that the PDP will soon achieve the goal of providing consumers affordable wall-hanging color TVs with large diagonal measurements [1], [2]. Since the sustaining electrodes and scanning electrodes on the front glass substrate and the addressing electrodes on the rear glass substrate are covered with a dielectric layer in a surface-discharge-type ac PDP, an intrinsic panel capacitance $C_{\rm p}$ exists [3]. During the charging/discharging of the panel capacitance, excessive surge currents are generated without an energy recovery circuit. Therefore, considerable amounts of energy stored in the panel are consumed across the nonideal resistance of the circuit and PDP. Furthermore, the charging/discharging surge current could cause serious resonance and electromagnetic interference (EMI) noise.

To solve these problems, several energy-recovery sustain drivers have been proposed. Among them, a widely used sustain driver in [4] is shown in Fig. 1. Since the circuit utilizes the series resonance between the panel capacitance $C_{\rm p}$ and the inductance of the external inductor, most of the lost energy is recovered. However, it still has several drawbacks. The panel voltage cannot rise perfectly from zero to a sustain voltage $V_{\rm s}$ and vice versa because the inevitable conduction losses that occur in the semiconductors, the wires, and other parasitic components lead to a damped oscillation in the circuit. Moreover, when plasma discharge occurs, a large discharge current flowing through the sustain switches causes a voltage notch that reduces the accumulated amount of the wall charge [5]. The rising time and the

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