A Constant Output Current Three-Phase Diode Bridge Rectifier Employing a Novel "Electronic Smoothing Inductor"

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***Abstract*—This paper presents an improvement of the well-known conventional three-phase diode bridge rectifier with dc output capacitor. The proposed circuit increases the power factor (PF) at the ac input and reduces the ripple current stress on the smoothing capacitor. The basic concept is the arrangement of an active voltage source between the output of the diode bridge and the smoothing capacitor which is controlled in a way that it emulates an ideal smoothing inductor. With this the input currents of the diode bridge which usually show high peak amplitudes are converted into a 120° rectangular shape which ideally results in a total PF of 0.955. The active voltage source mentioned before is realized by a low-voltage switch-mode converter stage of small power rating as compared to the output power of the rectifier.**

Starting with a brief discussion of basic three-phase rectifier techniques and of the drawbacks of three-phase diode bridge rectifiers with capacitive smoothing, the concept of the proposed active smoothing is described and the stationary operation is analyzed. Furthermore, control concepts as well as design considerations and analyses of the dynamic systems behavior are given. Finally, measurements taken from a laboratory model are presented.

***Index Terms*—Active rectifier, dc-link supply, three-phase power factor correction.**

I. Introduction

POWER converters based on a dc voltage link are widely used for drives, for the power supply of data managing systems and of telecommunication equipment, for medical purposes, as well as for industrial process techniques. The supply of the dc link of these converters, in general, is performed by a rectifier unit connected to the low-voltage three-phase mains. A multitude of circuit topologies exists for the realization of the rectifier unit (see survey publications [1]–[5]) starting from a simple three-phase diode bridge and ending up with an active unit showing features close to the idealized three-phase ac/dc converter. The most frequently applied systems shall be listed briefly on the basis of the number of active switches. There, pure passive rectifiers with improved mains behavior using current injection techniques [6]–[9], resonant circuits [10], [11], and magnetic phase-shifting devices [12]–[14] shall be not considered in the following lineup due to the low specific power density (W/kg) of those systems.

1) *Three-Phase B6 Diode Rectifier*
   + simple, robust, efficient, low cost;
   – high total harmonic distortion (THD) and low power factor (PF);
2) *Single-Switch Three-Phase Power-Factor Corrector (PFC)*
   • continuous-mode boost converter [15];
   • discontinuous-mode "dither" boost rectifier [16], [17];
   • discontinuous-mode buck-type rectifier [18];
   + regulated dc output voltage, improved THD, good PF;
3) *Dual-Switch Three-Phase PFC*
   • dual boost converter "Minnesota" rectifier [1], [19];
   • dual buck converter with wave shaping [20];
   + regulated dc output voltage, sinusoidal input currents;
   – triple mains frequency injection transformer;
4) *Three-Switch Three-Phase PFC*
   • three-level boost "VIENNA" rectifier [21], [22]
   • three-switch buck rectifier [23], [24];
   + regulated dc output voltage, sinusoidal input currents;
   + no line-frequency filtering elements;
5) *Six-Switch Three-Phase PFC* [25]–[27]
   + regulated dc output voltage, sinusoidal input currents;
   + bidirectional power flow (feedback of power into the mains possible);
   + var generation on ac side possible;
   – high realization effort.

A common property of all active topologies 2)–5) mentioned is that the turn-off power electronic devices in total have to be chosen regarding the half or full dc output voltage and the rated mains input current. This is also true for the simplest active circuit, the continuous-mode boost converter of 2). Although the switching devices of this circuit show a very good silicon utilization [4], they have to be selected considering the full power rating of the system.

The PFC method described in this paper is characterized by the fact that the rating of its active switches is only a fraction of the rectifier output power. The new system has been called an

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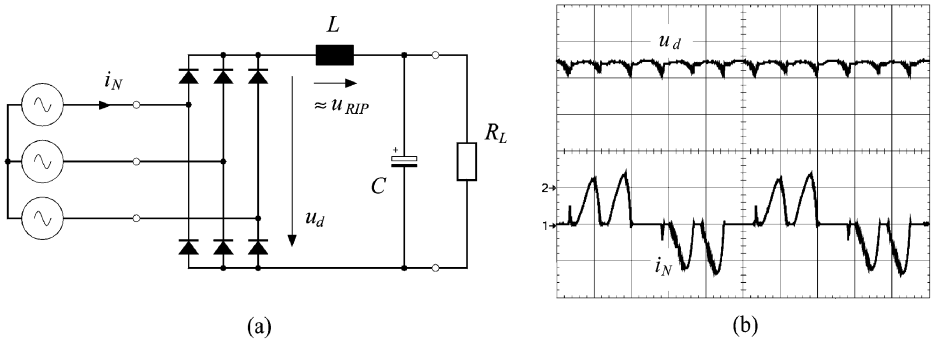

Fig. 1. Mains current and output voltage time behavior of a three-phase diode bridge rectifier. (a) Power circuit. (b) Mains current i_N (ch1: 20 A/div) and output voltage u_d (ch2: 150 V/div), measured PF $= 0.75$; parameters: mains voltage 400 V (rms, line-to-line), $L \approx 1.5$ mH, $P \approx 5$ kW, 4 ms/div.

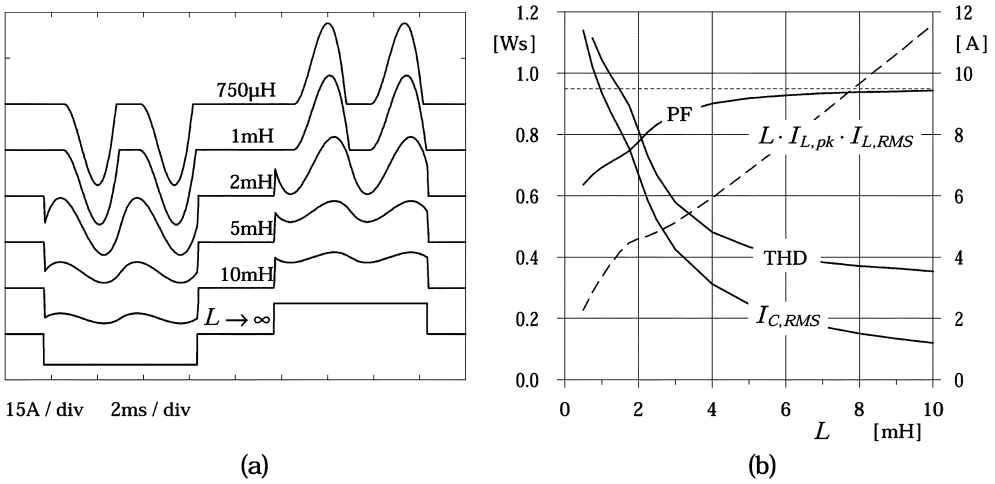

Fig. 2. (a) Mains current wave shapes for different values of the smoothing inductance L. (b) Total PF, THD, and rms current stress $I_{C,\mathrm{RMS}}$ of the smoothing capacitor in dependency on L. Furthermore, the product $L \cdot I_{L,pk} \cdot I_{L,\mathrm{RMS}}$ which corresponds to the rated power and size of the smoothing inductor is shown; parameters: mains voltage 400 V (rms, line-to-line), $P \approx 5$ kW.

Electronic Smoothing Inductor (ESI) because it emulates the behavior of a large-size passive smoothing inductor as described in the following. According to the line-up given above ESI has to be located between items 1) and 2). The poor mains current behavior of the simple three-phase diode rectifier 1) is improved to the behavior of the continuous-mode boost PFC of item 2) avoiding a switch-mode converter operating at full dc output voltage level. The ESI concept, however, does not allow the regulation of the dc output voltage as this can be achieved with all other systems described in items 2)–5). Although a constant voltage level of the dc link independent of the varying mains voltage would simplify the design of the load-side converter, this is not required in each case. (A pulsewidth-modulation (PWM) converter driving an induction machine, e.g., very often compensates a dynamically varying dc-link voltage level inherently by its output current controllers.)

The concept of the electronic smoothing inductor originally has been introduced by the authors in [28]. Afterwards, also, a circuit extension to obtain sinusoidal mains currents as well as advantageous applications for parallel arranged diode rectifiers has been reported [29]. Due to the recent advances in the area of low- and medium-voltage power MOSFETs, the system has gained attractiveness also for rectifiers at higher power levels [30].

II. Background—Diode Bridge Rectifier

To give the background and the motivation of the development of the ESI concept, the characteristic behavior of the widely applied three-phase diode bridge rectifier with a single smoothing inductor L located at the dc side as shown in Fig. 1(a) shall be discussed briefly. The essential drawback of this very cost-effective and reliable rectifier is the significant total harmonic distortion (THD) of the mains currents due to their largely nonsinusoidal wave shape [Fig. 1(b)]. This results also in a poor total PF despite the relatively good displacement factor $\cos\varphi_1$ due to the operation without phase control. Furthermore, the current harmonics also lead to a significant ripple current stress on the dc-link capacitor located at the rectifier output.

As demonstrated by Fig. 2 the drawbacks mentioned before can be reduced by increasing the smoothing inductance. The higher impedance gives an improved attenuation of the rectifier output ripple u_{RIP} and a reduced ripple current appears. For $L \to \infty$ (i.e., pure 120° rectangular input current shape) we get $\mathrm{PF} = 3/\pi = 0.955$, $\mathrm{THD} = 0.31$ and $I_{C,rms} = 0$. However, a large value of L would significantly impair the power density of the rectifier due to the bulky and weighty smoothing inductor. Furthermore, the increased L also worsens the dynamic behavior of the dc-link voltage because the characteristic

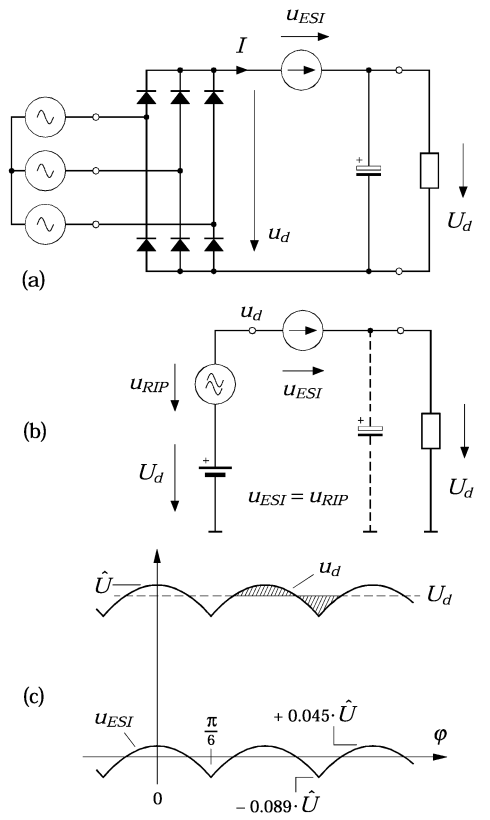

Fig. 3. (a) Replacement of the passive smoothing inductor of Fig. 1 by an active voltage source $u_{\rm ESI}$ which compensates the output ripple $u_{\rm RIP}$ of the diode rectifier. (b) Equivalent circuit diagram and (c) rectifier output voltage $u_d = U_d + u_{\rm RIP}$ and compensation voltage $u_{\rm ESI}$.

impedance $Z^2 = L/C$ is increased as compared to the load resistance R_L which reduces the damping of the LC smoothing filter. This problem is additionally intensified in case of the supply of nonlinear loads, e.g., constant power loads showing a negative small-signal input impedance.

III. Active Smoothing—Basic Operating Principle

The basic approach of the system presented by this paper is the functional replacement of the passive smoothing inductor L of Fig. 1 by a small power electronic unit whose output voltage $u_{\rm ESI}$ in the stationary case according to Fig. 3 compensates the voltage ripple $u_{\rm RIP}$ of the diode bridge and guarantees a well damped dynamic behavior by proper control. Contrary to the PFCs 2)–5) of Section I the power circuit of the ESI only has to be designed regarding the voltage *ripple* of the diode rectifier and not with respect to the *total* dc output voltage U_d. Hence, the switch-mode power converter generating $u_{\rm ESI}$ for practical realizations typically shows a rated power of only $\approx 10\%$ of the output power. Furthermore, due to the reduced voltage level majority carrier based power semiconductors (modern low-voltage high-current MOSFETs and Schottky diodes) are applicable for the ESI stage which allow switching frequencies $f_S \geq 100$ kHz. In connection with the reduced voltage level the switching-frequency filter for the switch-mode stage can be chosen comparatively small (filter inductance typically $100 \ldots 200$ μH for a 5-kW rectifier). This and the reduced losses of modern power semiconductors (e.g., $R_{DS,on} \approx 10$ mΩ for a 100-V/TO220-MOSFET and very low switching losses because Schottky diodes are used) leads to a very compact system with high power density.

As a consequence of the unidirectional current flow defined by the rectifier diodes only a two-quadrant power stage is required for the converter. Thus, the well-known basic 4Q-H-bridge topology can be reduced to an asymmetric half-bridge stage [Fig. 4(a)] consisting of only two power MOSFETs T_1, T_2, two freewheeling diodes D_1, D_2, and a low-voltage dc-link capacitor C_C.

In the ideal case there would be a pure ac power flow across the ESI stage showing frequency components of $6f_N$ ($f_N \ldots$ mains frequency) with zero average value. This results from the ideally pure dc current I (which is guaranteed by a suitable current control loop as described in Section IV) in connection with the pure ac voltage $u_{\rm ESI}$. Therefore, neglecting the losses the dc-link voltage U_C of the switch-mode stage can be provided by a capacitor and no auxiliary power supply would be necessary. This can be compared to a passive smoothing inductor which is, if its losses are neglected, also a pure energy storage element. The proposed active system realizes the energy storage characteristic required for smoothing by the dc-link capacitor of the switch-mode stage. Electrolytic capacitors, however, being usually applied for this reason show a very high specific energy storage density as compared to the magnetic energy storage capability of coils.

As seen by the mains, a diode rectifier enhanced by an ESI stage behaves very much like the continuous-mode boost PFC of Fig. 4(b). In both cases the constant converter current I results in mains currents of 120° rectangular shape leading to PF $= 3/\pi = 0.955$; however, the power stage of the boost PFC has to be designed for the total dc output voltage. For three-phase PFCs connected to the 400-V mains (line-to-line rms voltage) dc-link voltage levels of >600 V have to be used and turn-off devices with a blocking capability of up to 1000 V (typically IGBTs) are required. Due to the fact that the switching frequency of such devices is limited usually to $< 10 \ldots 25$ kHz there remains a substantial higher filtering effort in comparison to the ESI concept which allows the application of power MOSFETs and Schottky diodes with blocking voltages of ≈100 V.

IV. System Control

The elementary control of the ESI converter in a first approximation is analogous to the control of the boost PFC of Fig. 4(b). For such systems usually a two-stage control is applied where the duty-cycle of the switch is determined by an inner current control loop and the, in general, constant dc output voltage is defined by a superimposed voltage control. For the ESI system this voltage control has to be performed such that the output voltage U_O is equal to the dc component U_d of the diode bridge output voltage u_d, i.e., that the global average value $\bar{u}_{\rm ESI}$ (with reference to the fundamental) is controlled to zero. As shown in Fig. 5(a) in the simplest case the current guidance can be achieved using a hysteresis on-off controller whose reference value $i_{\rm REF}$ is gained by the measured rectifier output current i_O plus an additional control term being dependent on $u_{\rm ESI}$.

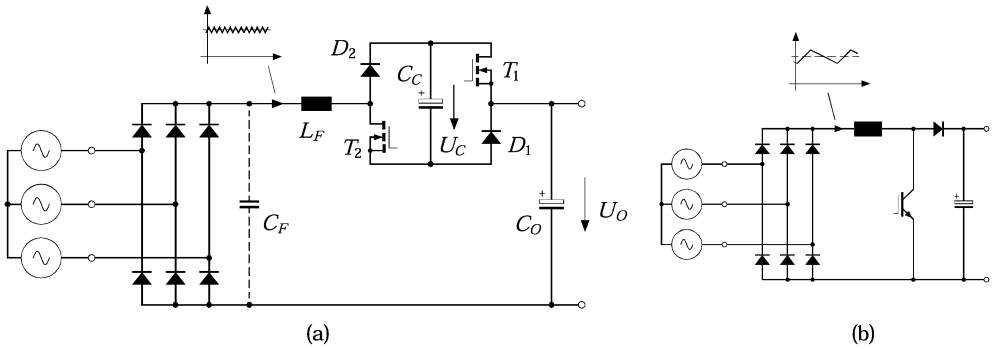

Fig. 4. (a) Power stage of the proposed ESI concept (asymmetrical half-bridge converter). (b) For comparison: conventional three-phase PFC using a single-stage continuous-mode boost converter; both concepts show identical mains current behavior.

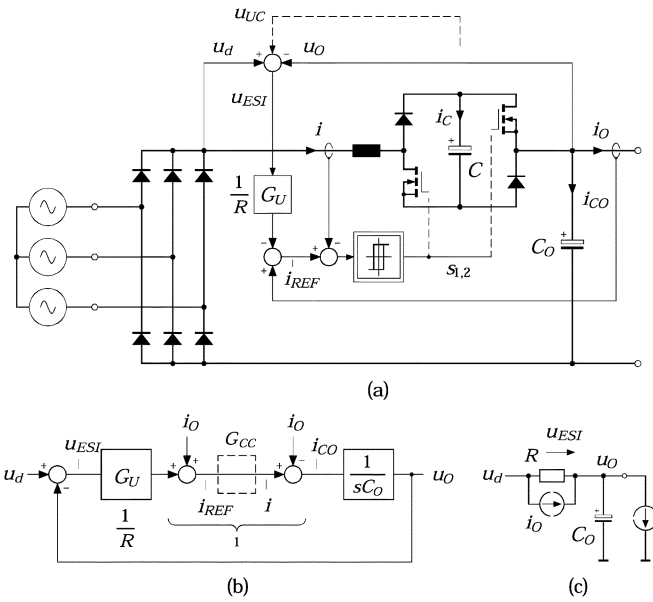

Fig. 5. (a) Basic control concept: two-level hysteresis current control with output current feedforward and superimposed voltage control G_U to achieve $\bar{u}_{\mathrm{ESI}} \approx 0$. (b) Control-oriented equivalent circuit diagram of the voltage loop and (c) equivalent diagram for the system using a P-type voltage controller $G_U = 1/R$.

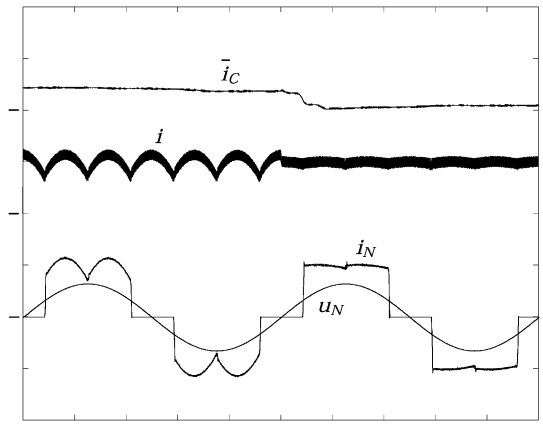

Fig. 6. Current and voltage wave shapes (simulation results) of the ESI concept with two-level hysteresis current control according to Fig. 5(a) for different gain values $R = 20\ \Omega$ (first fundamental period) and $R = 200\ \Omega$ (second period). 500 V/div (u_N), 10 A/div (i_N), 1 A/div ($\bar{i}_C$), 4 ms/div.

According to the control-oriented equivalent diagram of Fig. 5(b) the inclusion of i_O acts as feedforward and, hence, simple P-type voltage control $G_U = k_P = 1/R$ will be sufficient to achieve $\bar{u}_{\mathrm{ESI}} \approx 0$ assuming idealized current control $G_{CC} \approx 1$. The closed-loop system shows a simple PT_1-type structure [Fig. 5(c)] whose response time is defined by $T_1 = RC_O$. Similar to single-phase PFCs an excessive speedup of the voltage control loop is not convenient because this counteracts the energy storage capability of the dc-link capacitor C_O. For the same reason it is of advantage to insert an adequate low-pass filter into the sensing path of i_O if the load converter shows a pulse-shaped input current as this is frequently the case. For a drive system, e.g., the pulsating behavior of i_O is defined by the switching frequency of the PWM inverter usually in the region of a few kilohertz. A fast current controller of the ESI stage would pass this current pulsation via the diode rectifier into the mains which is not desired with respect to the electromagnetic compatibility of the system.

The effort of the application of an extra current sensor for i_O may be seen as a drawback of this control concept. However, on the one hand, for systems in the lower power range the current measurement can be performed easily by a shunt resistor located in the negative current return path giving a low-cost solution for current sensing. (The negative dc-link rail in such systems is used frequently already as the signal ground for the load converter control.) Furthermore, on the other hand, the actual power which gives information on the local average value of i_O very often can be provided by the load converter control without additional effort. Alternatively, the measurement of i_O can also be avoided if a proportional-plus-integral (PI)-type controller is used for G_U. This, however, would worsen the dynamic behavior of the dc-link output voltage in case of rapid load changes.

Fig. 6 shows simulation results for an ESI system with hysteresis current control for the following operating parameters: dc output voltage $U_d = 540$ V (rectified 400 V ac mains), output current $I_O = 10$ A (output power ≈ 5 kW), tolerance band of current controller $\Delta I = 2$ A, smoothing inductor $L_F = 200\ \mu$H, dc-link voltage of ESI power stage $U_C = 70$ V, and maximum switching frequency $f_{S,\max} = 100$ kHz. There, different values of R (gain of the P-type voltage controller) have been used for the two mains periods shown. For the first period a relatively low value $R = 20\ \Omega$ has been chosen resulting in

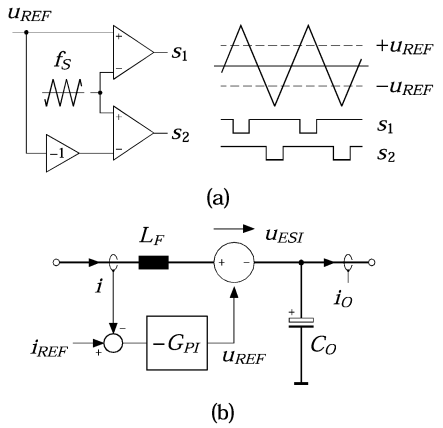

Fig. 7. (a) Generation of phase-shifted gate control signals for three-level control of the power stage. (b) Equivalent diagram of PI-type current control using PWM.

mains currents of similar form as known from feeding a pure resistive load by a three-phase diode bridge. With $R = 200\ \Omega$ being valid for the second period the mains currents are close to the expected 120° rectangular current shape with PF ≈ 0.955. As indicated by the averaged current $\bar{i}_C$ flowing into capacitor C a small net energy flow into the dc link of the ESI stage appears dependent on the value of R which can be used for partially compensating the semiconductor losses of the power stage; for details see Section VI.

The essential drawback of the hysteresis current control as described before is the two-level switching characteristic. The output voltage of the ESI stage here is defined as $+U_C$ or $-U_C$ according to the polarity of the control signal $s_{1,2}$ being common to both transistors. With this simple control no free-wheeling states are used which results in a comparatively high switching frequency for a given width of the control error (tolerance band ΔI). As mentioned in Section V it therefore is of significant advantage to replace the two-level hysteresis stage by three-level control. This can be easily achieved by using a PI-type average current-mode controller $G_{\rm PI}$ whose output signal $u_{\rm REF}$ acts as a control signal for two PWM comparators generating phase-shifted control signals s_1 and s_2 by comparison of $u_{\rm REF}$ with a triangular carrier signal of constant switching frequency f_S (Fig. 7). This actually doubles the effective pulse frequency of the switching stage output voltage which significantly reduces the size of the EMI filter components. The transition from two-level control to three-level control does reduce the voltage ripple at the filter capacitor C_F by a factor of eight with no additional effort to the power stage! The controller gain has to be dimensioned such that the bandwidth of the loop results typically to $f_S/10 \ldots f_S/4$ in order to guarantee the slope condition [31].

V. Stationary Operation—Design Considerations

In order to give guidelines for the dimensioning of the system in the following the voltage and current stress on the active and passive components of the power stage shall be calculated. First, the dc-link voltage U_C has to be chosen. According to Fig. 3(c) U_C has to be at least $\geq 0.089\hat{U} = (3/\pi - \sqrt{3/2}) \cdot \hat{U}$ in order to guarantee controllability. There, $\hat{U}$ represents the peak value of the diode bridge output voltage, i.e., $\hat{U} = 566$ V for 400 V ac mains voltage. Considering a sufficient voltage margin for proper control in a practical realization U_C is set typically to about 10%–15% of $\hat{U}$, i.e., 60–90 V. To compensate the voltage ripple of the diode bridge a voltage across the active smoothing stage of

$$u_{\rm ESI} = u_d - U_d = \hat{U}\left[\cos\varphi_N - \frac{3}{\pi}\right] \tag{1}$$

(valid for interval $\varphi_N = -(\pi/6) \cdots + (\pi/6)$ and using $U_d = \bar{u}_d = (3/\pi)\hat{U}$ and $\varphi_N = \omega_N t, \omega_N \ldots$ mains angular frequency) has to be generated as the local pulse average value within the switching period $T = 1/f_S$ by PWM using the duty cycle $\delta = 0 \ldots 1$ (Fig. 8)

$$u_{10} = U_C \cdot \delta \quad u_{20} = U_C \cdot (1-\delta), \tag{2}$$

$$u_{\rm ESI} = u_{20} - u_{10} = U_C \cdot (1 - 2\delta). \tag{3}$$

Combining (1) and (3) gives the relative turn-on time of the transistors

$$\delta(\varphi_N) = \frac{1}{2} - \frac{1}{2}\frac{\hat{U}}{U_C}\left[\cos\varphi_N - \frac{3}{\pi}\right] \tag{4}$$

and of the diodes

$$1 - \delta(\varphi_N) = \frac{1}{2} + \frac{1}{2}\frac{\hat{U}}{U_C}\left[\cos\varphi_N - \frac{3}{\pi}\right] \tag{5}$$

which are required as weighting functions for the calculation of the average and rms values of the transistor current

$$I_{T,avg} = \frac{3}{\pi}\int_{-\pi/6}^{+\pi/6} I \cdot \delta(\varphi_N) d\varphi_N = \frac{1}{2} I, \tag{6}$$

$$I_{T,rms} = \sqrt{\frac{3}{\pi}\int_{-\pi/6}^{+\pi/6} I^2 \cdot \delta(\varphi_N) d\varphi_N} = \frac{1}{\sqrt{2}} I. \tag{7}$$

These equations show that the average current stress does not depend on the voltage ratio $\hat{U}/U_C$ which can be explained by the fact that due to the pure ac characteristic of $u_{\rm ESI}$ the average duty ratio is equal to 1/2. As a result, the current stress on the diodes becomes equal to the values of the transistors (for the sake of brevity the calculation is omitted): $I_{D,avg} = I_{T,avg}$ and $I_{D,rms} = I_{T,rms}$.

The current ripple of i and the current stress on the dc-link capacitor C depend on the PWM operating mode. If both transistors are gated by the same control signal $s_1 = s_2$ the voltage $u_{\rm ESI}$ is formed by $+U_C$ and $-U_C$ [two-level control, Fig. 8(a)]. In this case the capacitor current results as $I_{C,rms} = I$, not being dependent on $\hat{U}/U_C$ if the current ripple Δi is neglected. In order to reduce the ripple current amplitude it is very advantageous, however, to use three-level control where $+U_C$, 0, and $-U_C$ are used for generating as mentioned in the previous section. Due to the tighter voltage approximation and the doubling of the effective switching frequency the maximum current ripple is reduced to 1/4 as compared to two-level control

$$\text{two-level control}: \Delta I_{\max} = \frac{U_C}{2L_F f_S} \text{ at } \delta = \frac{1}{2} \tag{8}$$

$$\text{three-level control}: \Delta I_{\max} = \frac{U_C}{8L_F f_S} \text{ at } \delta = \frac{1}{4}, \frac{3}{4}. \tag{9}$$

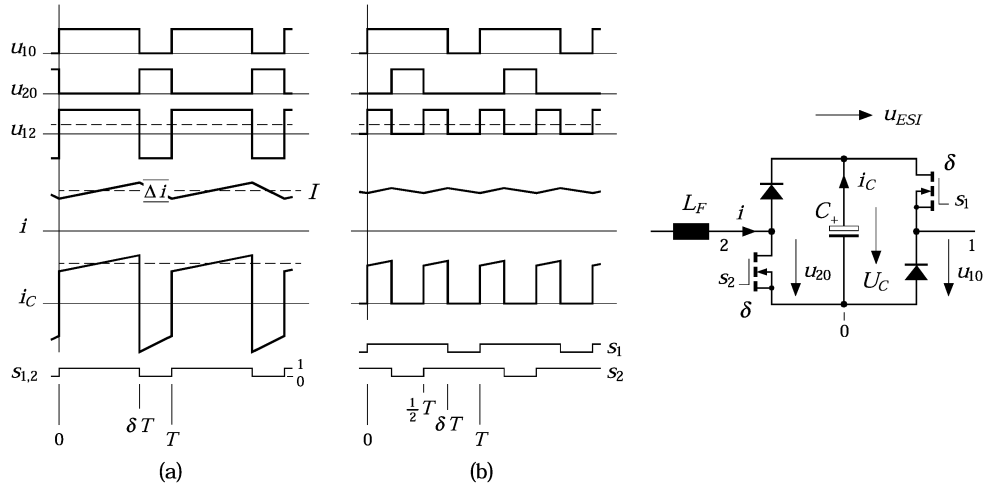

Fig. 8. Voltage and current wave shapes of the switch-mode stage within a pulse interval T for (a) two-level control and (b) three-level control using control signals s_1, s_2 which are phase shifted by $T/2$.

It can be shown, furthermore, that besides the ripple also the current stress on the dc-link capacitor C is reduced by three-level control, but now depends on the ratio $\hat{U}/U_C$. Omitting the detailed calculation for the sake of brevity, the current stress results as

$$I_{C,rms} = I \cdot \sqrt{\frac{\hat{U}}{U_C}} \cdot \sqrt{\frac{36}{\pi^2}\left[\sqrt{\frac{\pi^2}{9}-1} - \arctan\sqrt{\frac{\pi^2}{9}-1}\right]}$$
$$= 0.186 \cdot I \cdot \sqrt{\frac{\hat{U}}{U_C}}. \quad (10)$$

Based on the relations derived before a rough dimensioning and component selection for the 5-kW active smoothing system mentioned in Section IV shall be given for three-level control as follows:

output current	$I_O = 10$ A$(P_O \approx 5.4$ kW$)$;
output voltage	$U_d \approx 540$ V$(\hat{U} = 566$ V$)$;
dc-link voltage	$U_C = 70$ V;
switching frequency	$f_S = 100$ kHz;
smoothing inductor	$L_F = 100$ μH;
ripple current	$\Delta I_{\max} = 0.9$ A$_{pp}$;
trans./diode current	$I_{T,D,avg} = 5$ A;
	$I_{T,D,rms} = 7.1$ A;
dc-link capacitor	$I_{C,rms} = 5.3$ A.

According to the calculated ratings the following components has been chosen for the power circuit: T_1, T_2: IRFB 4710 (TO220 MOSFET, 100 V, $R_{\mathrm{DS,on}} \approx 30$ mΩ at 125 °C); D_1, D_2: 16CTQ100 (100 V/16 A TO220 Schottky diode, $U_{F,TO} \approx 0.47$ V, $r_T \approx 14$ mΩ at 125 °C); C: 3×680 μF/100 V in parallel (Panasonic FC, $\emptyset$18 mm× 40 mm, ESR 36 mΩ, 2.3 A$_{rms}$); L_F: 100 μH/12 A, realized using 42 turns of 1.5-mm^2 wire on 58083 $\emptyset$40 mm× 14.5 mm HighFlux powder core (calculated losses $\approx$ 2.5 W [32]). A rough calculation of the component losses leads to the following:

- T conduction losses: 1.5 W/device;
- D conduction losses: 3 W/device; switching losses: 3 W/leg (estimated);
- L total losses: 2.5 W;
- C ESR losses: 0.5 W;

which sum up to 18 W for the entire power stage. Considering some additional losses for the gate drivers, the control and for sensing, the total losses of the system are estimated to be lower than 30 W which is only 0.6% of the rectifiers rated output power. For a rectifier with pure passive smoothing (Fig. 1) with, e.g., $L = 1$ mH, approximately equal losses would appear in the smoothing inductor. Further, it has to be mentioned that the ESI concept saves losses in the diode rectifier and also in the main dc-link capacitor C_O due to the reduced rms current ratings. For the treated dimensioning example $I_{C,\mathrm{rms}}$ can be lowered according to Fig. 2(b) by ≈ 8 A which would save 13-W losses assuming that C_O is formed by a series connection of two capacitors with ≈ 100 mΩ ESR. Alternatively, it would be also possible to use capacitors of lower current ratings. However, it has to be kept in mind that the dc-link capacitors are strongly influenced also by the requirements of the load-side converter. Measurements taken from a 2-kW laboratory prototype fed by a 230-V (rms line-to-line voltage) three-phase mains are presented in Fig. 9. Here, the loss compensation takes place exclusively by choosing a rather low value of R (cf. also first mains period shown in Fig. 6). No explicit control for U_C is implemented; instead, the dc-link voltage is defined by a limiting circuit. The measured total PF $= 0.95$ is close to the maximum of $3/\pi = 0.955$.

VI. Loss Compensation—Startup

In a first guess the losses of the components of the power circuit as calculated before would have to be covered by an auxiliary power supply arranged in parallel to C. A small positive dc component of u_{ESI} in connection with the constant positive load current I, however, will lead to a net power flow $\overline{u}_{\mathrm{ESI}} \cdot I$ into the dc link of the ESI stage. Furthermore, the control concept as described in Section IV emulates the ohmic impedance R located between u_d and u_O as shown in Fig. 5(c) to achieve a proper transient behavior. Therefore, even if $\overline{u}_{\mathrm{ESI}} = 0$ is true, the ac ripple u_{ESI} appears across R. The power flow given by $U^2_{\mathrm{ESI,rms}}/R$, however, is not dissipated but fed into the dc-link capacitor C. The rms value of u_{ESI} can be calculated to be $\approx$4% of $\hat{U}$, i.e., $\approx$23 V for a rectifier operating at the 400-V mains.

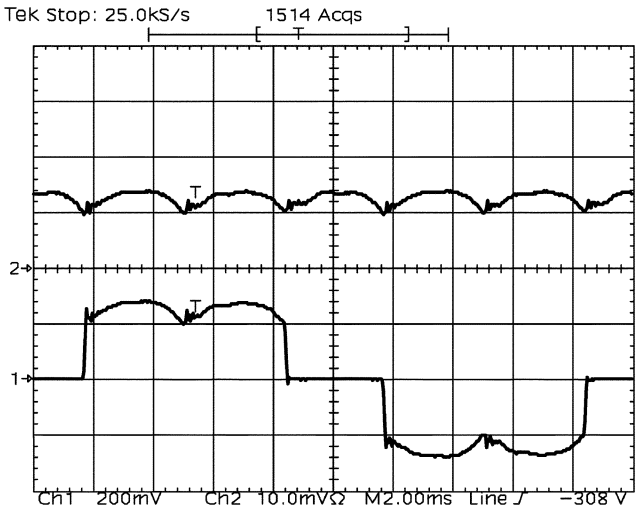

Fig. 9. Current shapes taken from a laboratory model; top (ch2): ESI stage current i; bottom (ch1): mains current i_N; 5 A/div, 2 ms/div; $\mathrm{PF} = 0.95$. Parameters: line-to-line mains rms voltage 230 V ($\hat{U} = 325$ V), $P \approx 2$ kW.

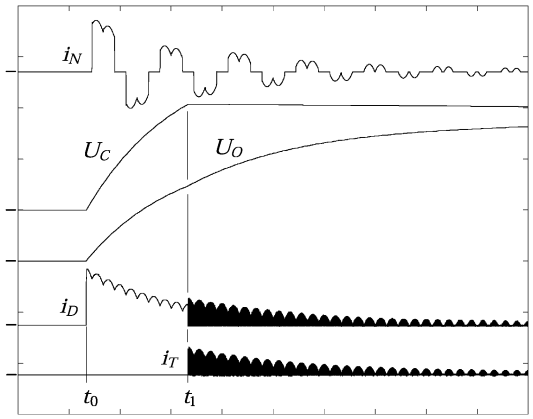

Fig. 10. Simulation of the startup (see text). Scales: 15 A/div; 200 V/div (U_O), 30 V/div (U_C), 15 ms/div.

With this a power flow of 26 W would result in leading to an average current $\bar{i}_C \approx 0.4$ A into C as shown in Fig. 6 which contributes to balance the losses.

To guarantee that the ESI dc-link voltage is kept to the desired level, the basic control of Fig. 5(a) has to be extended by an additional U_C controller. In the simplest case this can be realized by using a P-type controller which senses U_C and generates an additional signal u_{UC} at the $(u_d - u_O)$-subtraction stage as indicated by the dashed line of Fig. 5(a). In order to minimize the realization effort it may be of advantage to use the negative terminal of C as a local ground because this forms the reference point of the U_C-control and, furthermore, allows the easy application of integrated gate driver stages such as IR2110 or similar. In addition, current control concepts based on a shunt resistor inserted between the drain of T_2 and the local ground reducing the effort for sensing i seem of advantage. The switching-frequency common-mode voltage of the signal $u_{\mathrm{ESI}} = u_d - u_O$ (related to the local ground) has to be blocked by a common-mode filter. Alternatively, isolating the sensed u_{ESI} by application of an optocoupler would be possible. The supply of the control circuitry is performed by a small dc/dc converter out of C.

Finally, the startup of the system shall be discussed briefly. As in the case of a conventional diode bridge the proposed concept also requires a startup resistor in order to limit the inrush currents if the rectifier is switched on ($t = t_0$ in Fig. 10). Now, a series connection of the main dc-link capacitor C_O and of the dc-link capacitor C via the diodes $D_{1,2}$ of the ESI stage exists. Due to the capacity of C being typically higher than that of C_O a lower voltage at C appears but would usually exceed the nominal value U_C. To avoid this, the PWM stage has to start operation with $1:1$ duty ratio at $t = t_1$ when U_C reaches its nominal value. Because $\overline{u}_{\mathrm{ESI}} = 0$ then the charging of C stops, C_O is charged to its final value, and the control loops of the ESI stage are activated. The operation of the PWM stage for $t \geq t_1$, however, presumes that the dc/dc converter providing the auxiliary supply of the control circuitry has already started full operation. Furthermore, it has to be mentioned that the ESI system requires a minimum load current i_O for ensuring the described loss compensation function. Considering these items a system without separate auxiliary supply fed by the mains or by the dc output voltage U_O would be realizable.

VII. Conclusion

The proposed ESI concept analyzed in this paper significantly improves the mains behavior of three-phase diode bridge rectifiers based on the replacement of the idealized passive smoothing inductor by an active switch-mode stage. The dimensioning power of this switch-mode converter is small (≈10%) as compared to the total rectifier output power. The applicable semiconductor technology (low-voltage low-loss MOSFETs) leads to a rectifier system of very high total power density and efficiency. Besides the improvement of the total PF to ≈0.95 the active smoothing further results in a lower rms current stress on the dc-link output capacitor and on the rectifier bridge. The losses of the switch-mode stage (typically 0.5%...1% of the total rectifier output power) are of about the same magnitude as for a real smoothing inductor which, however, would give a much lower PF of typically 0.75. The losses of the power components and the auxiliary power being required for the control can be covered by the load current using an appropriate control and starting circuitry. No separate auxiliary supply fed by the mains or by the dc output is required.

By application of low-voltage MOSFETs of very high current rating being available for a short period the proposed active smoothing seems to be attractive even for power levels >100 kW. The main drawback of the system in comparison to pure three-phase active rectifiers is that it does not provide a stabilized dc output voltage. In contrast to those systems the proposed smoothing, however, shows a much lower power rating of the semiconductors.

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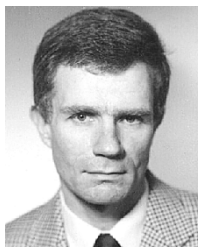

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