Analysis and Control of a Three-Phase, Unity Power Factor Y-Rectifier

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***Abstract*—This paper presents the analysis and operation of a three-phase pulsewidth modulation rectifier system formed by the star-connection of three single-phase boost rectifier modules (Y-Rectifier) without a mains neutral point connection. The current forming operation of the Y-Rectifier is analyzed and it is shown that the phase current has the same high quality and low ripple as the Vienna Rectifier. The isolated star point of Y-Rectifier results in a mutual coupling of the individual phase module outputs and has to be considered for control of the module dc link voltages. An analytical expression for the coupling coefficients of the Y-Rectifier phase modules is derived. Based on this expression, a control concept with reduced calculation effort is designed and it provides symmetric loading of the phase modules and solves the balancing problem of the dc link voltages. The analysis also provides insight that enables the derivation of a control concept for two phase operation, such as in the case of a mains phase failure. The theoretical and simulated results are proved by experimental analysis on a fully digitally controlled, 5.4-kW prototype.**

***Index Terms*—Pulsewidth modulation (PWM).**

I. Introduction

AN IMPORTANT trend in power electronics has been the replacement of the traditional, low frequency offline power supply modules by the high-frequency switched rectifiers. This change is driven by the requirements for high power density, low-harmonic current distortion and a high power factor, and is made possible due to the reducing cost of silicon-based power and control devices. One significant application area for compact, high power factor voltage supplies with galvanic isolation is in providing the power for telecommunication and server facilities. The required power is up to several 100 kW with a dc output voltage of 48 V. The industrial trend to construct these high power systems is to connect, in parallel, multiple three-phase rectifiers, each with a nominal power of 5 to 10 kW, instead of single-phase systems. These modular systems are often an industrial requirement since they have a high reliability due to redundancy and they are hot-pluggable. The modularity also allows for system enlargements and specification changes without expensive or complicated modifications. The input stage of these power supply systems can be realized with either a direct three-phase rectifier topology, where the dc output voltage is common to all phases [e.g., Vienna Rectifier, Fig. 1(a)] or with a modular topology using a star-connection [Y-Rectifier, Fig. 1(b)] or delta-connection (Δ-Rectifier, [1], [2]) of single-phase boost rectifier modules with individual dc output voltages.

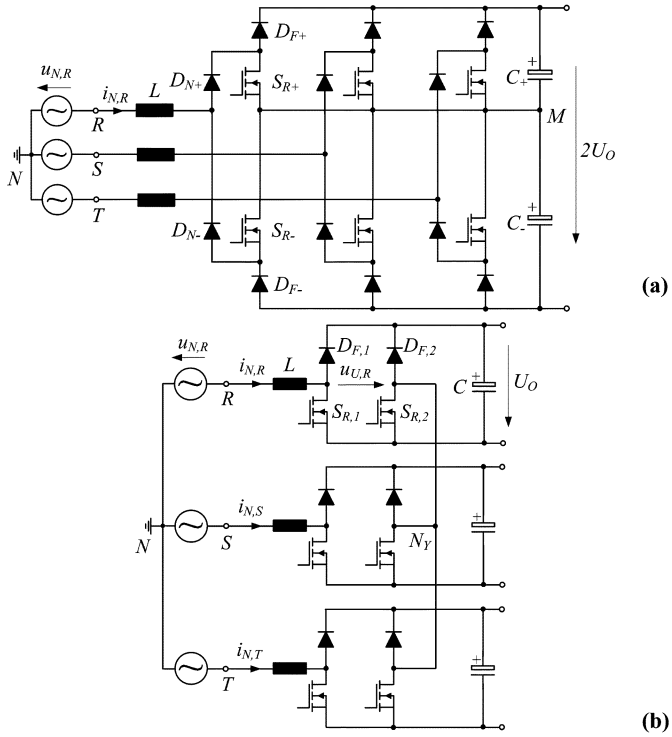

Fig. 1. Direct and modular three-phase PWM rectifier system. (a) Vienna Rectifier using six switches (a three-switch version of the Vienna Rectifier is discussed in [3]). (b) Y-Rectifier, a star-connection of three single-phase two-switch rectifier modules.

The three-level structure of the Vienna Rectifier results in a low blocking voltage stress on the power semiconductors and a small input inductor volume [3]. For a wide line-to-line input voltage range of $320 \ldots 530\mathrm{V_{RMS}}$ the dc output voltage of the input stage has to be set to 800 $\mathrm{V_{dc}}$. This high voltage level is a disadvantage as it is better to realize the isolated dc–dc stage with 600 V power semiconductors so that the converter losses are reduced. Therefore, the dc–dc output stage has to be realized with a series connection of two dc–dc converters (with their outputs parallel connected) and/or a three-level dc–dc converter topology.

With the Δ-Rectifier, the output voltage also has a high voltage level since each single-phase boost rectifier is connected to a line-to-line voltage. However, a significant advantage of the Δ-Rectifier is that the system is able to deliver nominal output power in case of a mains phase loss when a three-phase thyristor bridge is used as the module input rectifier [1].

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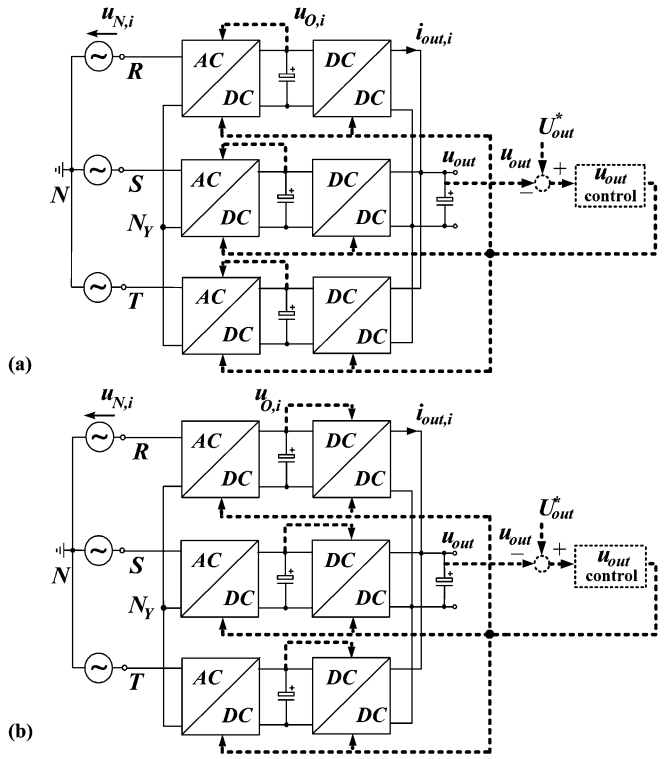

Fig. 2. Control of the dc link voltages $u_{O,i}$ of the phase modules of a Y-Rectifier by (a) changing the power drawn from the mains (input-oriented) or (b) changing the power supplied to the load (output-oriented).

In contrast, the Y-Rectifier has the advantage of a low dc output voltage of only 400 V from each of the phase modules. The dc–dc output stage is created by connecting individual dc–dc converters (built using 600 V power semiconductors) to each of the three rectifier modules and the outputs are then connected in parallel to form a common 48 V output. This leads to a very simple overall structure for the modular three-phase power supply since it is constructed of relatively standard single-phase modules.

Modular Y-configured rectifier systems, which have a neutral line connection to the mains star point N, have been reported in [4], [5]. However, for a standard telecom power supply no neutral wire connection is provided. In the Y-Rectifier, the isolated star point, N_Y, results in a mutual coupling of the individual phase currents and/or module outputs and therefore makes the balancing of the dc link voltages difficult. In [6], to overcome these control difficulties, N_Y was connected to an artificial neutral point formed by three auxiliary transformers. With this approach the modules become decoupled and are operated in a similar way to a system that has a connection between the system star point N_Y and the mains star point N. The disadvantage with this approach is that the system size and cost are significantly increased due to the auxiliary transformers. Therefore, the motivation of the research presented in this paper is to determine whether the decoupling of the modules can be achieved by purely control means rather than by passive components.

There are two different control concepts possible for the Y-Rectifier, as shown in Fig. 2. The first is to control the dc link voltage between the single phase rectifier and the dc–dc converter by changing the power drawn from the mains supply [Fig. 2(a)]. This method is therefore referred to as input-orientated control since the power on the input ac side is regulated. The second concept is an output-orientated control method [Fig. 2(b)], where the dc link voltage is regulated by changing the power supplied to the load through the dc–dc converter.

Unfortunately, very little has been published on the control concepts for the Y-Rectifier. In 1993, an output-orientated control method was briefly presented in [7]. There, the rectifier consisted of a star-connection of three single-phase modules, each containing a power factor correction input stage and a dc–dc resonant converter for the output stage. The control of the dc-link voltages was achieved by changing the power demand of the dc–dc stage. This control concept was proposed without any qualified control-oriented analysis since the concept is straight forward because of the missing mutual interference of the phase control actions. To the knowledge of the authors, no other output-orientated control methods or any input-orientated control methods have been reported in the literature.

The purpose of this paper is to analyze the operation of the Y-Rectifier, based on an analytical analysis of coupled modules, and to determine if a suitable input-oriented control method can implemented. First, in Section II, the basic principle of operation of the system is described by a space vectors analysis of the rectifier input voltages that are available for sinusoidal control of the mains current. From this, the basic performance concerning the mains ripple and inductor realization effort is determined. The analysis shows that the Y-Rectifier exhibits identical space vectors as the Vienna Rectifier, and therefore, in principle, the same high quality mains current is possible. In Section III, the system control of the rectifier system is discussed, firstly looking at the mutual coupling of two series connected modules. By considering the local average values of the system quantities, the module coupling can be formulated in an analytically closed form. This analysis is then generalized to balanced three-phase operation of the Y-Rectifier, where global average values over a mains period are considered. The model clearly shows the coupling of the phase modules caused by the isolated star point N_Y. Based on this, a control concept with reduced calculation effort is designed to ensure constant dc link voltage levels. The proposed control structure is proved by experimental results from a digitally controlled, 5.4 kW prototype.

II. Y-Rectifier

A. Basic Principle of Operation

The modules in a Y-Rectifier can be based on the standard PFC topology, which has an ac-side inductor and a diode full-bridge that is followed by a boost stage. As an alternative, a modified topology with two simultaneously controlled power transistors $S_{i,1}$ and $S_{i,2}$ is employed in each module (see Fig. 1(b) and [8]) in order to reduce the conduction losses and complexity of the input rectifier. Here, the current flows through only two semiconductor devices. The diodes provide the simultaneous functions of rectification and boosting, and therefore must have fast switching and low reverse recovery charge characteristics.

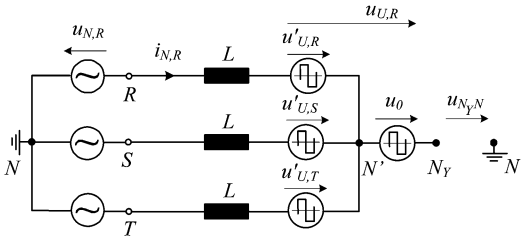

Fig. 3. AC-side equivalent circuit of the Y-Rectifier. N' marks a virtual star-point of the system, which has the same potential as the mains star point N.

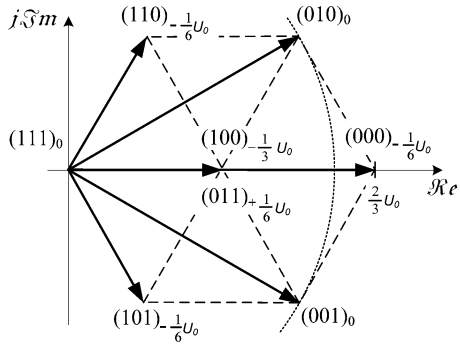

Fig. 4. Space vectors $\underline{u}_U$ of the Y-Rectifier input phase voltages $u'_{U,i}$ available for mains current control in the 60° phase sector defined by $i_{N,R} > 0, i_{N,S} < 0, i_{N,T} < 0$. The switching state and the resulting zero-voltage component mark each space vector.

The principle of operation of the Y-Rectifier is described for a two-level rectifier system (a three-level rectifier implementation is discussed in [9]). The ac side equivalent circuit of a Y-Rectifier is shown in Fig. 3. The current formation in each phase (index $i = R, S, T$) is given by

$$u_{N,i} = L\frac{di_{N,i}}{dt} + u_{U,i} + u_{N_Y N} \tag{1}$$

where the sign of the rectifier input phase voltage, $u_{U,i}$, is determined by the direction of the corresponding phase current, $i_{N,i}$. Since the sum of the three line currents is zero, this results in

$$\frac{di_{N,R}}{dt} + \frac{di_{N,S}}{dt} + \frac{di_{N,T}}{dt} = 0 \tag{2}$$

and, therefore, for a purely sinusoidal symmetric mains voltage system ($\sum u_{N,i} = 0$)

$$u_{N_Y N} = -\frac{1}{3}\sum u_{U,i}. \tag{3}$$

Since the zero sequence component, $u_0 = 1/3(u_{U,R} + u_{U,S} + u_{U,T})$, is contained in the phase voltages $u_{U,i}$, the voltage $u_{N_Y N}$ that appears between the star point N_Y of the phase modules and the mains star point N is equal to $-u_0$. Accordingly, in each phase only the voltage $u'_{U,i} = u_{U,i} - u_0$ is effective for the current formation. Therefore, as shown in Fig. 3,

$$u_{N,i} = L\frac{di_{N,i}}{dt} + u'_{U,i}. \tag{4}$$

Combining the phase quantities $u'_{U,i}$ in a complex space vector given by

$$\underline{u}_U = \frac{2}{3}(u'_{U,R} + \underline{a}u'_{U,S} + \underline{a}^2 u'_{U,T}) \quad \text{where } \underline{a} = e^{j\frac{2\pi}{3}} \tag{5}$$

and introducing equally defined space vectors for the mains phase voltages, $u_{N,i}$, and the mains phase currents, $i_{N,i}$, (4) results in

$$\underline{u}_N = L\frac{d\underline{i}_N}{dt} + \underline{u}_U. \tag{6}$$

The phase quantities $u'_{U,i}$ and $i_{N,i}$ and/or the space vectors $\underline{u}_U$ and $\underline{i}_N$ now can be decomposed into a mains frequency fundamental (index (1)) and a switching frequency ripple component (index (n))

$$\begin{aligned} \underline{u}_U &= \underline{u}_{U,(1)} + \underline{u}_{U,(n)} \\ \underline{i}_N &= \underline{i}_{N,(1)} + \underline{i}_{N,(n)} \end{aligned} \tag{7}$$

and by considering (6), this results in

$$\begin{aligned} \underline{u}_N = \hat{U}_N e^{j\omega_N t} &= L\frac{d\underline{i}_{N,(1)}}{dt} + \underline{u}_{U,(1)} \\ &= j\omega_N L\underline{i}_{N,(1)} + \underline{u}_{U,(1)} \\ L\frac{d\underline{i}_{N,(n)}}{dt} &= \underline{u}_{U,(1)} - \underline{u}_U. \end{aligned} \tag{8}$$

To achieve a sinusoidal mains current shape, a rectifier input voltage $\overline{\underline{u}}_U = \underline{u}_{U,(1)} = U_U e^{j\omega_N t}$ has to be formed, where $\overline{\underline{u}}_U$ denotes averaging over a pulse period. The ripple, $\underline{i}_{N,(n)}$, of the input current, $\underline{i}_N$, is caused by the difference of the applied voltage $\underline{u}_U$ and the ideal voltage $\underline{u}_{U,(1)}$. Therefore, in order to ensure a minimum mains current distortion, the voltage vector $\underline{u}_{U,(1)}$ has to be formed using switching states, which correspond to voltage space vectors in the immediate vicinity of $\underline{u}_{U,(1)}$. Due to the two-level topology of each module, the Y-Rectifier has $2^3 = 8$ possible switching states that are denoted by the combined power transistor switching function

$$s_{RST} = (s_R\, s_S\, s_T) \tag{9}$$

where $s_i = 1$ denotes the turn-on state of the switches $S_{\mathrm{i},1}$ and $S_{\mathrm{i},2}$, and $s_i = 0$ the turn-off state. The two switches $S_{\mathrm{i},1}$ and $S_{\mathrm{i},2}$ in each module operate synchronously, although only one of the switches conducts current in the forward direction, depending on the sign of the input current. The second switch conducts current in the reverse direction through the body diode.

The generated rectifier voltages $u_{U,i}$, which are dependent on the sign of the phase current and the switching state s_i, are defined by

$$u_{U,i} = \mathrm{sgn}(i_{N,i})(1 - s_i)U_O. \tag{10}$$

The voltage space vectors $\underline{u}_U$ corresponding to the different switching states for $i_{N,R} > 0$ and $i_{N,S} < 0, i_{N,T} < 0$ are depicted in Fig. 4. The number and position of the space vectors correspond with those of the Vienna Rectifier for identical signs of the phase currents. Consequently, the same well-known, mains voltage feed-forward signal [10] used to modulate the duty ratio as the Vienna Rectifier can therefore be employed in the Y-Rectifier. With pure sinusoidal feed-forward of the duty

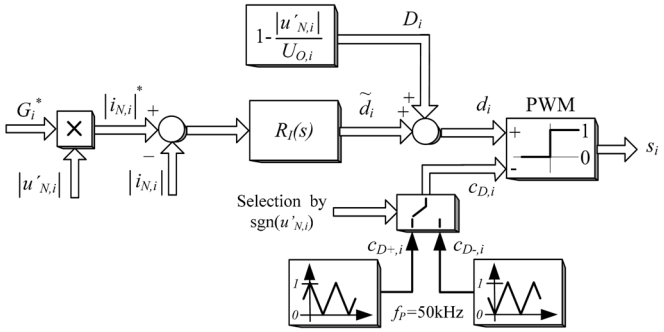

Fig. 5. Average current mode control of the rectifier mains phase currents. Signal paths for all phases are drawn with wide arrows; index $i = R, S, T$.

ratio $D_i = 1 - |u'_{N,i}|/U_O$ the modulation maximum is limited to

$$M = \hat{U}_{N,i}/U_O = 1. \tag{11}$$

The operating limit $M_{\max} = 2/\sqrt{3}$ is only available when a third harmonic is added to the modulation signal.

B. Rectifier Current Control

The Y-Rectifier controller's objective is to regulate the common output voltage of the dc–dc converters and to maintain a constant, equal voltage on the dc link of each of the rectifier modules. Both the input-orientated and output-orientated control approaches require a current controller. To minimize the realization effort of the rectifier's current control, an average current mode (ACM) controller with mains voltage feed-forward is employed in each phase (Fig. 5). The synchronization of the phase modules, to minimize the input current ripple and/or optimize the switching state sequence, is achieved by using the same carrier signals $c_{D+,i}$ and $c_{D-,i}$ for all phases. The difference between these two signals is a time shift of one half period. As is implemented in a Vienna Rectifier, the carrier signals are used alternatively for the PWM generation, with the selection being dependent on the sign of the mains phase voltages. The phase voltages are measured across equal high ohmic resistors in a star arrangement at the system input.

The reference values of the mains phase currents are derived by multiplying the zero sequence free mains phase voltage $u'_{N,i}$ with a reference conductance G_i^* as defined by a combination of superposed voltage control loops (see Section IV). The sinusoidal control of each phase current is implemented in the current controller $R_I\,(s)$. The controller slightly changes the pulse pattern resulting from the duty cycle feed-forward D_i in order to ensure the formation of a voltage $\underline{u}_{L,(1)} = j\omega_N L\hat{I}_N \mathrm{e}^{j\omega N}_t$ [cf. (9)] across the inductors over a pulse period in addition to the mains voltage. As the star point N_Y of the phase modules is not connected to the mains neutral N, the sum of the phase currents is forced to zero, and therefore only two phase currents can be controlled independently. For this reason no integral component of $R_I(s)$ is desired in order to avoid a wind-up of the current controller. However, due to the duty-cycle feed-forward and the low absolute value of $\underline{u}_{L,(1)}$ for high switching frequency operation and/or a low inductance L, a purely P-type controller can ensure a low current control error.

C. Stationary Operating Behavior

Since the rectifier input phase voltage, $u'_{U,R}$, is responsible for the current formation, the changing potential of the system star point N_Y, caused by the switching, leads to the coupling of the modules. The impact of this coupling on the input current ripple is analyzed by simulation of the system in steady-state with balanced mains voltages and compared with a system that is decoupled by connecting the system star point N_Y to the mains star point N. Fig. 6 presents the simulation waveforms and space vector diagram for a two-level Y-Rectifier. For the simulation model, constant module dc link voltages $U_{O,i}$ are impressed in order to omit the superimposed voltage control loop. Fig. 6(d) shows the low ripple contained in the mains phase currents $i_{N,i,(n)}$ (having the same shape as for the Vienna Rectifier) that results from the modular current control concept depicted in Fig. 5. The pulsewidth modulation is optimum, as the current controller employs only voltage space vectors $\underline{u}_U$ in the immediate vicinity of $\underline{u}_{U,(1)} \approx \underline{u}_N$ [Fig. 6(a)]. A small improvement in the remaining input current ripple can be reached by using a third harmonic, such that the switching of the space vectors is optimized. Additionally, Fig. 6(b) shows the time behavior of the current forming rectifier input phase voltage $u'_{U,R}$, and of the local average value $\overline{u}'_{U,R}$, which is approximately equal to the mains voltage feed-forward signal $u'_{N,R}$ due to the low inductance.

Fig. 7 shows the normalized RMS ripple component of the mains phase current for the Y-Rectifier (or Vienna Rectifier) compared to a single-phase module with equal value of the input inductance and/or a modified Y-Rectifier with a neutral connection between N and N_Y. The Y-Rectifier (with no neutral connection) has significantly lower mains current ripple compared to a single-phase module since the third, ninth, 15th,... harmonics are not current forming. The effective line current ripple is reduced by more than 50%. The ripple component can be additionally reduced by approximately 15%–20% through adding a third harmonic (of amplitude 1/6 $\hat{U}_N$) to the mains voltage feed-forward signal.

III. System Control

To develop an input-orientated controller for the Y-Rectifier that is able to provide the required decoupling for each of the modules, an analytical analysis of the mutual coupling of the phase modules is required. In this section, the coupling of two series connected dc–dc converters is first considered in order to aid the understanding of the coupling problem. The analysis is then applied to the series connection of two rectifier modules, which has the same behavior as the Y-Rectifier in case of two-phase operation. A control concept is presented for two-phase operation, which is required during a mains phase loss. The analysis is then extended for the case of three-phase Y-Rectifier operation.

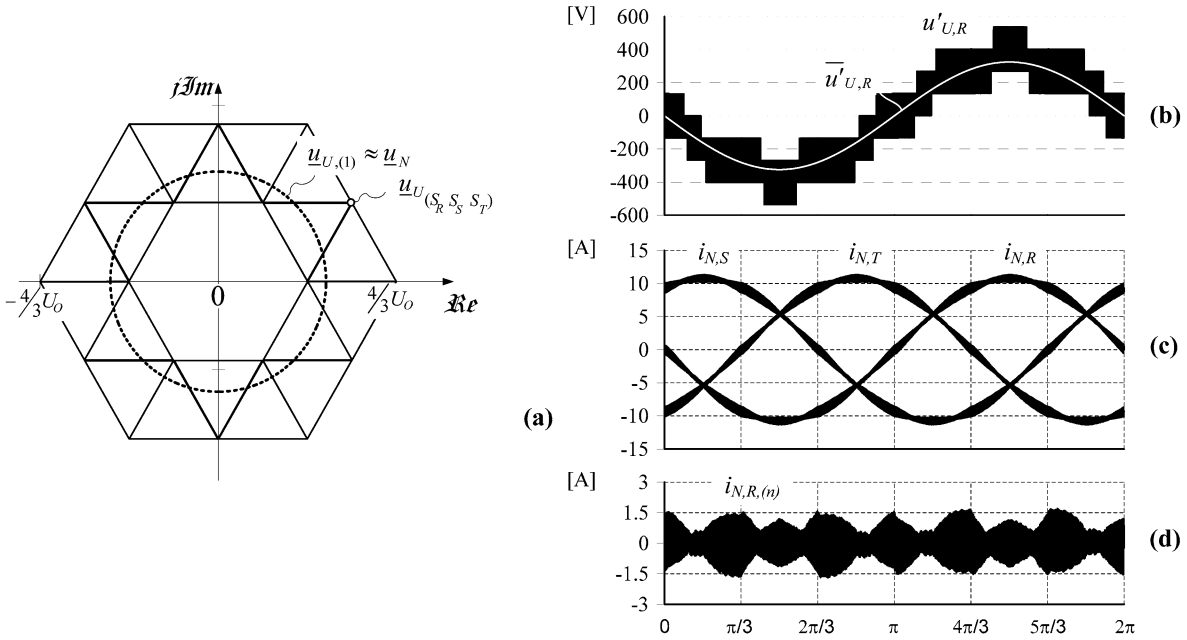

Fig. 6. Digital simulation of the stationary operating behavior of a two-level Y-Rectifier employing average current mode control (Fig. 4). (a) Voltage space vectors $\underline{u}_U$ employed for the formation of $\underline{u}_{U,(1)} \approx \underline{u}_N$ and/or for the sinusoidal control of the mains phase currents. The lines connecting the voltage space vectors are due to the continuous transitions of the real system between the different levels of the rectifier input phase voltages $\underline{u}_{U,i}$. (b) Current forming rectifier input phase voltage and local average $\bar{u}'_{U,R} = \underline{u}_{U,R,(1)} \approx \underline{u}_{N,R}$ of $u'_{U,R}$. (c) Mains phase currents, (d) Ripple component $i_{N,R,(n)}(i_{N,R} = i_{N,R,(1)} + i_{N,R,(n)})$; Simulation parameters: $U_{N,\mathrm{rms}} = 230$ V, $U_{OY} = 400$ V, $L = 560\,\mu$H, $f_P = 25$ kHz, $P_0 = 5.4$ kW, symmetric mains.

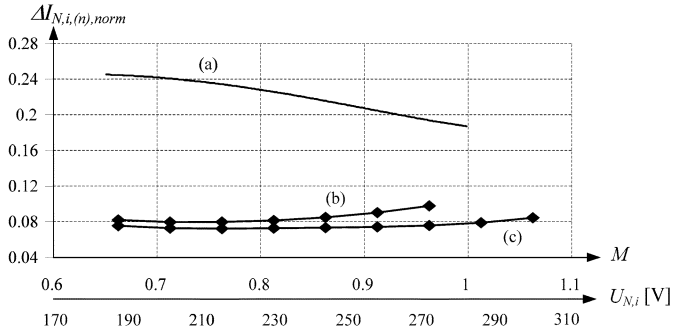

Fig. 7. Normalized RMS ripple component of the phase current for the two-level Y-Rectifier. (a) When N_Y is connected with N, i.e., equivalent to operation of three decoupled single phase modules. (b) Sinusoidal mains voltage feed-forward (cf. Fig. 5), N_Y open. (c) Mains voltage feed-forward with additional third harmonic of amplitude 1/6 $\hat{U}_N$; Normalization base: $i_{\mathrm{norm}} = U_O T_P/8L = 7.1$ A, where T_P denotes the pulse period.

A. Coupling and Control of Two Series Connected DC–DC Boost Converters

In order to gain insight into the coupling of the phase modules of the three-phase system, a series connection of two dc–dc boost converters a, b [Fig. 8(a)] is analyzed as a first step. It is assumed that both converters are operated in continuous conduction mode, the output voltages are constant, and there is an individual proportional current controller for each converter. If there is a change in the input current reference value for converter a by ΔI_a^* this will result in a change $\Delta I_{D,a}$ in the average value of the related output diode current $i_{D,a}$. In order to set a positive change ΔI_a^* the relative turn-on time d_a of power transistor S_a is increased by the current controller. The current controller of converter b now tries to compensate the resulting change of the input current, which is common to both systems, by increasing the relative turn-off time $d'_b = (1 - d_b)$ of S_b. As the output diode current is determined by the product of the input current and the transistor turn-off time, an increase or a decrease $\Delta I_{D,a}$ of $I_{D,a}$ will occur depending on the final increase of the input current $I = I_a = I_b$ and a final decrease of d_a (P-type current control). However, in any case, the output diode current $I_{D,b}$ of system b will be increased by $\Delta I_{D,b}$. Therefore, for a change in a reference current of one module there is an associated change in the output diode current of both modules. This can be mathematically represented as a direct coupling term $H_{ii} = (\Delta I_{D,i})/(\Delta I_i^*)$ and a cross coupling term $H_{ji} = (\Delta I_{D,j})/(\Delta I_i^*)$. The analytical derivation of the coupling terms is presented in [11] for impressed equal output voltages and it is shown, for the considered system parameters, that the cross coupling term is dominant. Therefore, the balancing of the output dc voltages could only rely on the pronounced cross coupling (cf. Fig. 9).

For the series connection of two ac-dc power factor correction phase modules [Fig. 8(b)], a similar analysis can be performed. There, we assume the inner current control to be realized with an ACM controller with duty cycle feed-forward [according to $(u/2)$] as given in Fig. 8(c), and the desired phase current as the current reference signal. In the outer control loop, the reference current for each module is determined by multiplication of the module input voltage with a reference conductance ($i_a^* = G_a^* \cdot u_a, i_b^* = G_b^* \cdot u_b$, where $u_a = u_b = u/2$). If the reference conductivity deviates by ΔG_i^* there is now a change $\Delta \hat{I}_i^*$ in the amplitude $\hat{I}_i^*$ of the related phase current reference value i_i^*. Due to the typically large output capacitance and the slow response of the output voltage control, only the resulting change $\Delta I_{D,a}$ and $\Delta I_{D,b}$ of the diode current global average values (averaged over a mains period) has to be considered. Accordingly, the sinusoidal shape of the input voltage and current does not take direct influence and the system control

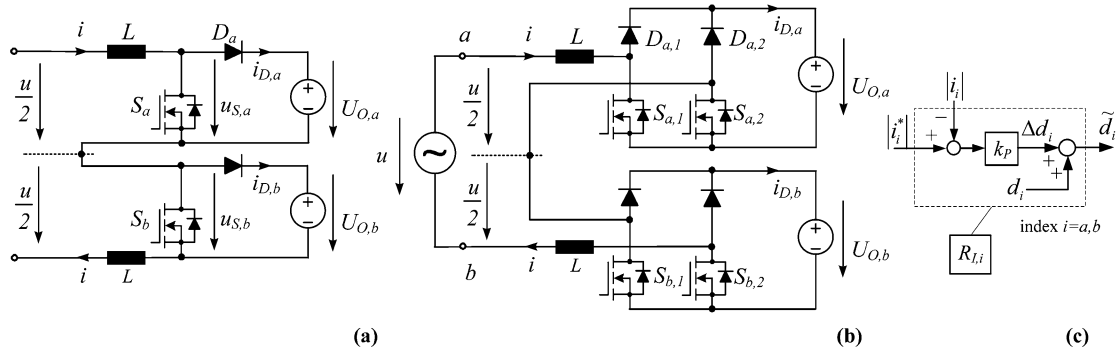

Fig. 8. (a) Series connection of two dc–dc boost converters, (b) series connection of two single-phase boost-type rectifier modules with (c) linear P-type ACM controller which includes input voltage duty cycle feed-forward, d_i, and measured rectified line current $|i_i|$.

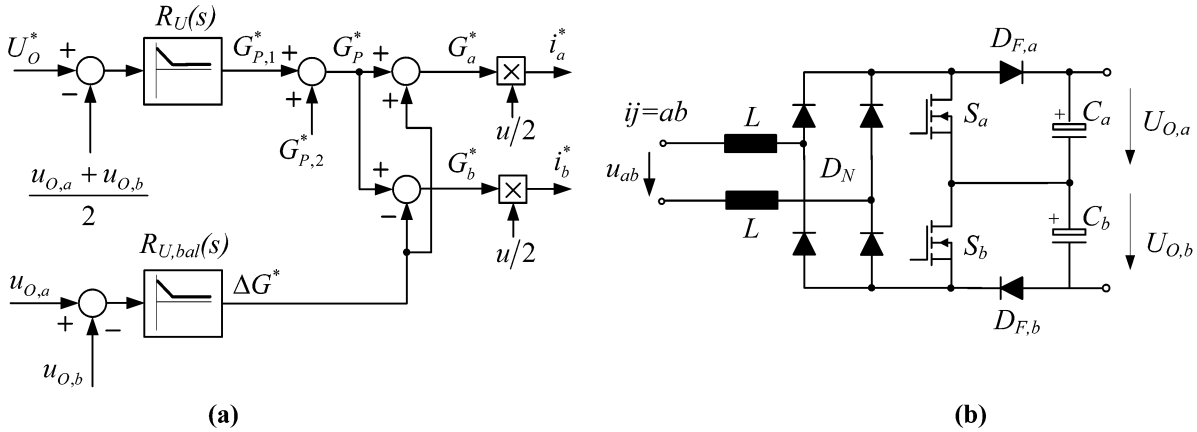

Fig. 9. (a) Voltage controller for the Y-Rectifier with two-phase operation. (b) Three-level topology with equivalent coupling properties as the series connection of two rectifier modules [see Fig. 7(a)].

behavior can be characterized by the coupling coefficient terms $H_{ii} = (\Delta I_{D,i})/(\Delta \hat{I}_i^*)$ and $H_{ji} = (\Delta I_{D,j})/(\Delta \hat{I}_i^*)$. The result of the analytical analysis in [11] shows that the cross coupling term H_{ji}, for the considered system parameters, is dominant compared to the direct coupling H_{ii} term.

A proper control concept for the superposed voltage controller of $U_{O,i}$ is shown in Fig. 9(a). The deviation of the reference output value U_O^* minus the average value of the measured output voltages $(U_{O,a} + U_{O,b})/2$ is amplified by the voltage controller $R_U(s)$. The controller output $G_{P,1}^*$ takes equal influence on the reference value of the inner current controllers. To increase the control dynamics concerning load changes, a feed-forward signal $G_{P,2}^*$, which represents the power being supplied by the dc–dc stage, is added to $G_{P,1}^*$. Additionally, to compensate for any unbalance of $U_{O,a}$ and $U_{O,b}$ the output ΔG^* of the controller $R_{U,\mathrm{bal}}(s)$ is added to or subtracted from the reference current values, based on the dominant cross coupling. This structure of the outer voltage controller could be implemented in the digital controller of the Y-Rectifier for two-phase operation, i.e., in case one mains phase is lost. The duty cycle feed-forward in the inner current controllers $(R_{I,a}(s), R_{I,b}(s))$ is determined by $d_i = 1 - (|u|/2)/(U_O) = 1 - (|u|)/(U_{O,a} + U_{O,b})$.

The voltage controller of Fig. 9(a) utilizes the cross coupling to compensate for any unbalance between the two output voltages. For example, to decrease $U_{O,a}$ the current reference i_a^* is increased through ΔG^*. Switch $S_{a,1}$ is now turned on longer by the proportional current controller, which results in less current flowing into $U_{O,a}$ and more current into $U_{O,b}$.

The series connection of the two two-level modules can be rearranged and simplified into a three-level topology as shown in Fig. 9(b). As can be seen, the same current must flow in each phase and therefore there will be coupling between the upper and lower part of the output circuit. For the three-level rectifier there is an alternative control method, where only one current controller is employed and the voltage on the two output capacitors is balanced by adjusting the duty cycle of each of the switches. This basic control concept could be applied to the converter in Fig. 8(b).

B. Y-Rectifier Operating With Symmetric Three-Phase Mains

In the following, the analytical analysis of the module coupling for a three phase input voltage is derived, followed by the synthesis of a proper concept for the module output voltage control. This is similar to the coupling of series connected single phase modules due to their common input current i; in the case at hand the isolated module star point N_Y forces the sum of the ac-side input currents to zero

$$\sum_i i_i = i_R + i_S + i_T = 0 \tag{12}$$

which results in a coupling of the phase currents and/or of the power flows in the phases. Therefore, a change in the reference input current of one phase module $(\Delta \hat{I}_i^* = \Delta G_i^* \cdot \hat{U}_N |\cos(\omega t - \varphi_i)|)$ will cause a change $\Delta I_{D,i}$ of the global average value of the output diode current of

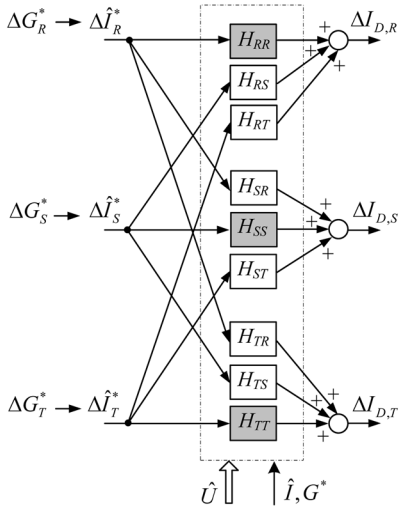

Fig. 10. Block diagram representation of the three-phase Y-Rectifier showing the influence of changes of the amplitudes of input current reference values (for a balanced, sinusoidal three-phase reference current system) on the phase module output diode current average values. For symmetric mains, all cross coupling terms have equal values $H_{ij} = H_{ji}$ (indices $i, j = R, S, T$).

each module. The stationary coupling coefficients are depicted in Fig. 10 by a control-oriented block diagram and represented by the matrix formulation

$$\begin{pmatrix} \Delta I_{D,R} \\ \Delta I_{D,S} \\ \Delta I_{D,T} \end{pmatrix} = \underline{H} \cdot \begin{pmatrix} \Delta \hat{I}_R^* \\ \Delta \hat{I}_S^* \\ \Delta \hat{I}_T^* \end{pmatrix} = \begin{pmatrix} H_{RR} & H_{RS} & H_{RT} \\ H_{SR} & H_{SS} & H_{ST} \\ H_{TR} & H_{TS} & H_{TT} \end{pmatrix} \cdot \begin{pmatrix} \Delta \hat{I}_R^* \\ \Delta \hat{I}_S^* \\ \Delta \hat{I}_T^* \end{pmatrix}. \tag{13}$$

The current controller for each module is implemented, as shown in Fig. 8(b), with feed-forward control of the duty cycle by $d_i = 1 - |u_{N,i}|/U_O$. The analytical calculation of the coupling coefficients is derived for a deviation of an operating condition, where the module dc link voltages have equal values ($U_{O,i} = U_O$) and the entire load P_O is shared equally over the three module outputs.

In the following calculations some expressions for the three-phase system are reduced to a single-phase form with indexes $i, j = R, S, T$ and the index N for mains voltages and currents is omitted. The input voltages are assumed to be purely sinusoidal with a phase shift of 120° as given by

$$\begin{aligned} u_i &= \hat{U}\cos(\omega t - \varphi_i) \\ &= \hat{U}\cos\left(\omega t - n\frac{2\pi}{3}\right) \quad \text{where } n = 0, 1, 2; \end{aligned} \tag{14}$$

for no small signal deviations, the rectified phase currents used in for current control (Fig. 13) have a purely ohmic behavior of

$$i_i = \hat{I}\left|\cos\left(\omega t - n\frac{2\pi}{3}\right)\right|. \tag{15}$$

In case a small signal deviation is introduced by individual changes $\Delta\hat{I}_i^*$ of the phase current reference amplitudes, the reference current becomes $\tilde{i}_i^* = (\hat{I}^* + \Delta\hat{I}_i^*)|\cos(\omega t - n(2\pi)/(3))|$. If it is assumed, at the considered operating point, that the reference and actual current values for no deviation are equal for all phases ($\hat{I}_i^* = \hat{I}^* = \hat{I}_i = \hat{I}$, ideal current control) then the rectified phase current also contains a small signal deviation, given by

$$\tilde{i}_i = (\hat{I} + \Delta\hat{I}_i)\left|\cos\left(\omega t - n\frac{2\pi}{3}\right)\right|. \tag{16}$$

The sum of the ac-side phase currents is zero, which is described by the condition

$$\mathrm{sgn}(u_R)\tilde{i}_R + \mathrm{sgn}(u_S)\tilde{i}_S + \mathrm{sgn}(u_T)\tilde{i}_T = 0. \tag{17}$$

In a similar way as in the case of the series connected dc–dc converters (Section III-A), the change in reference signal will cause a change in the diode current. To establish the coupling in the three-phase case, the change in diode current is determined from the off-time duty cycle and the phase to phase voltage loop equation.

According to Fig. 8(c) the relative turn-off times of the switches S_i are given by

$$\begin{aligned} \tilde{d'}_i &= \frac{1}{U_O}[|u_i| - K_P(\tilde{i}_i^* - \tilde{i}_i)] \\ &= \frac{1}{U_O}[|\hat{U}_i| - K_P(\Delta\hat{I}_i^* - \Delta\hat{I}_i)]\left|\cos\left(\omega t - n\frac{2\pi}{3}\right)\right|. \end{aligned} \tag{18}$$

The phase to phase voltage equation is

$$u_i - u_j = \underbrace{+L\frac{di_i}{dt} - L\frac{di_j}{dt}}_{\approx 0} + U_O(\mathrm{sgn}(u_i)\tilde{d'}_i - \mathrm{sgn}(u_j)\tilde{d'}_j) \tag{19}$$

and the fundamental inductor voltage drop can be neglected for high switching frequency and/or low inductance of the input inductors. This leads to a direct relation of the line-to-line input voltages and the duty cycles

$$(u_i - u_j) = U_O[\mathrm{sgn}(u_i)\tilde{d'}_i - \mathrm{sgn}(u_j)\tilde{d'}_j]. \tag{20}$$

Considering (17) and setting (18) into (20) results in

$$\begin{aligned} &\Delta\hat{I}_R|\cos\omega t| \\ &\quad = +\frac{2}{3}\Delta\hat{I}_R^*|\cos\omega t| + \frac{1}{3}\Delta\hat{I}_S^*\left|\cos\left(\omega t - \frac{2\pi}{3}\right)\right| \\ &\qquad + \frac{1}{3}\Delta\hat{I}_T^*\left|\cos\left(\omega t - \frac{4\pi}{3}\right)\right| \\ &\Delta\hat{I}_S\left|\cos\left(\omega t - \frac{2\pi}{3}\right)\right| \\ &\quad = +\frac{1}{3}\Delta\hat{I}_R^*|\cos\omega t| + \frac{2}{3}\Delta\hat{I}_S^*\left|\cos\left(\omega t - \frac{2\pi}{3}\right)\right| \\ &\qquad - \frac{1}{3}\Delta\hat{I}_T^*\left|\cos\left(\omega t - \frac{4\pi}{3}\right)\right| \\ &\Delta\hat{I}_T\left|\cos\left(\omega t - \frac{4\pi}{3}\right)\right| \\ &\quad = +\frac{1}{3}\Delta\hat{I}_R^*|\cos\omega t| - \frac{1}{3}\Delta\hat{I}_S^*\left|\cos\left(\omega t - \frac{2\pi}{3}\right)\right| \\ &\qquad + \frac{2}{3}\Delta\hat{I}_T^*\left|\cos\left(\omega t - \frac{4\pi}{3}\right)\right| \end{aligned} \tag{21}$$

for the input voltage condition of $u_R > 0$ and $u_S, u_T < 0$. The deviations $\Delta i_{D,i}$ of the output diode currents $i_{D,i}, \tilde{i}_{D,i} = i_{D,i} + \Delta i_{D,i}$, are determined by

$$\begin{aligned}
\Delta i_{D,R} &= d'_R \Delta i_R + \Delta d_R i_R \\
&= \frac{\hat{U}}{U_0} \Delta \hat{I}_R |\cos \omega t|^2 \\
&\quad - \frac{K_P(\Delta \hat{I}_R^* - \Delta \hat{I}_R)}{U_0} \hat{I} |\cos \omega t|^2 \\
\Delta i_{D,S} &= d'_S \Delta i_S + \Delta d_S i_S \\
&= -\frac{\hat{U}}{U_0} \Delta \hat{I}_S \left| \cos\left(\omega t - \frac{2\pi}{3}\right) \right|^2 \\
&\quad - \frac{K_P(\Delta \hat{I}_S^* - \Delta \hat{I}_S)}{U_0} \hat{I} \left| \cos\left(\omega t - \frac{2\pi}{3}\right) \right|^2 \\
\Delta i_{D,T} &= d'_T \Delta i_T + \Delta d_T i_T \\
&= -\frac{\hat{U}}{U_0} \Delta \hat{I}_T \left| \cos\left(\omega t - \frac{4\pi}{3}\right) \right|^2 \\
&\quad - \frac{K_P(\Delta \hat{I}_T^* - \Delta \hat{I}_T)}{U_0} \hat{I} \left| \cos\left(\omega t - \frac{4\pi}{3}\right) \right|^2 .
\end{aligned} \tag{22}$$

Setting (21) into (22) leads to the time-dependent coupling coefficients of

$$\begin{aligned}
h_{ii}(\omega t) &= +\frac{1}{3U_0}(2\hat{U} - K_P \hat{I}) \cos^2(\omega t - \varphi_i) \\
h_{ij}(\omega t) &= -\frac{1}{3U_0}(\hat{U} + K_P \hat{I}) \\
&\quad \times \cos(\omega t - \varphi_i) \cos(\omega t - \varphi_j).
\end{aligned} \tag{23}$$

Using the same proceeding to determine the coupling coefficients for the next 60° phase sector leads to identical expressions. Therefore, over the entire mains period the time-dependent coupling coefficients of (23) are valid and the coupling matrix can be defined with the time-varying elements as

$$\begin{pmatrix} \Delta i_{D,R} \\ \Delta i_{D,S} \\ \Delta i_{D,T} \end{pmatrix} = \begin{pmatrix} h_{RR}(\omega t) & h_{RS}(\omega t) & h_{RT}(\omega t) \\ h_{SR}(\omega t) & h_{\mathrm{SS}}(\omega t) & h_{ST}(\omega t) \\ h_{TR}(\omega t) & h_{TS}(\omega t) & h_{TT}(\omega t) \end{pmatrix} \cdot \begin{pmatrix} \Delta \hat{I}_R^* \\ \Delta \hat{I}_S^* \\ \Delta \hat{I}_T^* \end{pmatrix}. \tag{24}$$

As the voltage control loop dynamics is selected to be significantly lower than the mains frequency, (23) can be integrated over a mains period to produce the global average coupling coefficients

$$\begin{aligned}
H_{ii} &= \frac{1}{2\pi} \int_0^{2\pi} h_{ii}(\omega t)\, d(\omega t) = \frac{1}{3U_0}(\hat{U} - \frac{1}{2} K_P \hat{I}_i) \\
H_{ij} &= \frac{1}{2\pi} \int_0^{2\pi} h_{ij}(\omega t)\, d(\omega t) = \frac{1}{12U_0}(\hat{U} + K_P \hat{I}_i)
\end{aligned} \tag{25}$$

which characterize the system control and coupling properties in matrix form [cf. (13)].

One way to show that this derivation is valid is to consider a simple example where all the three phase reference currents change by the same amount such that they automatically fulfill the current sum condition. For the case of symmetrical mains voltages and by using (13) and (25) the change in the output diode current can be determined from

$$\begin{aligned}
\frac{\Delta I_{D,i}}{\Delta \hat{I}^*} &= \frac{1}{3U_0}\left(\hat{U} - \frac{1}{2} K_P \hat{I}\right) + \frac{2}{12U_0}(\hat{U} + K_P \hat{I}) \\
&= \frac{\hat{U}}{2U_O}.
\end{aligned} \tag{26}$$

Rearranging (26) into $(\hat{U} \Delta \hat{I}^*)/(2) = U_O \Delta I_{D,i}$ shows that the correct power balance of the system is obtained and therefore proves that the derivation is valid.

An alternative confirmation is by comparing calculated coupling coefficients (H_{ii}, H_{ij}) to results from digital simulations. Fig. 11 shows the comparison of the calculated and simulated coefficients for a current controller with a gain of $K_P = 15.2\ \mathrm{VA}^{-1}$ and demonstrates the high accuracy of the modeling approach for the case of nominal operating voltage. The small deviations can be explained by the simplifying assumptions facilitating the simple analytical calculation.

One has to point out that for deriving the system model the small-signal phase current deviations are assumed to show a sinusoidal shape in phase with the according phase current [cf. (16)] as it considerably simplifies the calculations. In practice there is a phase displacement ϕ_{ii*} between the actual and reference currents, however the assumption can be justified by the fact that the influence on the transferred power is only from $\cos \phi_{ii*}$, which has values close to 1 for small values of ϕ_{ii*}.

As shown in Fig. 11 for the fixed current gain K_P, the characteristics of H_{ii} and H_{ij} intersect within the operating range. At these intersection points the matrix $\underline{H}^{-1}$ is characterized by singularity. Dominant direct coupling exists for the low input current operating range and for high input currents the cross coupling term is dominant. In case an adaptive decoupling matrix, $\underline{M}_{\mathrm{DEC}} = \underline{H}^{-1}$, is employed for the system control, the system could only be decoupled for operating points with sufficient distance from the intersection regions. A controller design based on ideal decoupling is presented in [11] and is limited by the following restrictions.

a) For the operating points where all elements of the system matrix $\underline{H}$ have equal values $H_{ii} = H_{ij}$ no decoupling matrix exists because of the singularity of $\underline{H}$ $(\det(\underline{H}) = 0)$.
b) The calculation of the system matrix $\underline{H}$ is based on idealized and simplified assumptions. Therefore, operation with sufficient decoupling is limited to small disturbances around the balanced operation points.
c) Simple expressions for the decoupling matrix $\underline{M}_{\mathrm{DEC}} = \underline{H}^{-1}$ [e.g., (27)] are only possible for symmetric mains voltages (is assumed for the derivation of $\underline{H}$ in the case at hand). For unbalanced mains, the resulting analytical

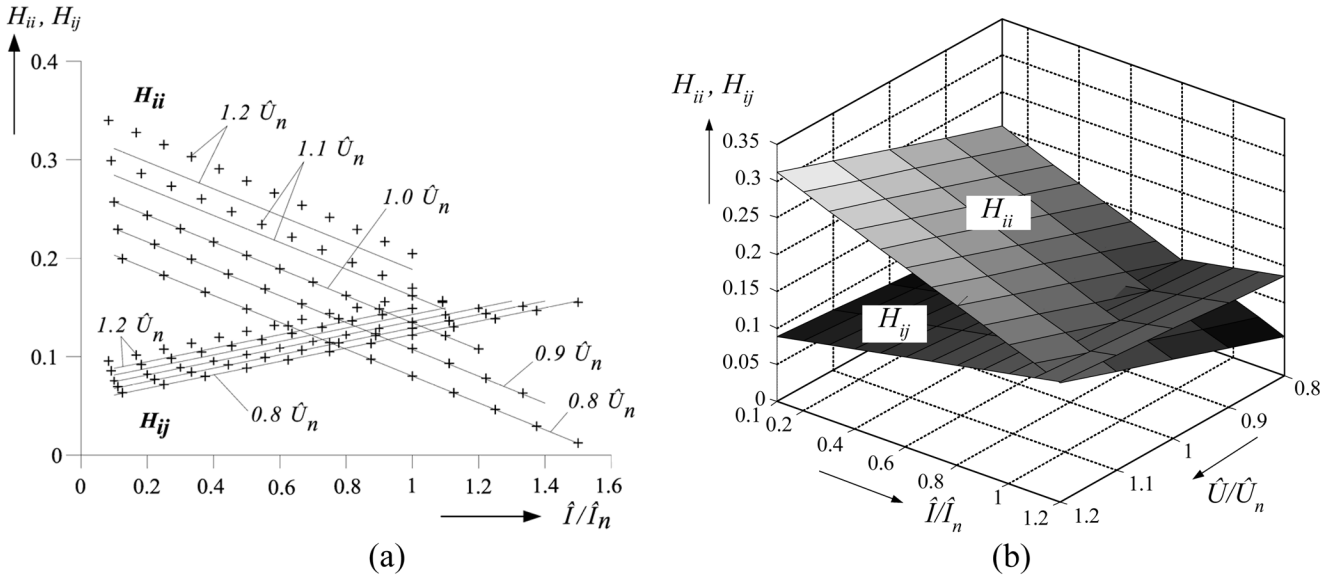

Fig. 11. (a) Comparison of the Y-Rectifier coupling coefficients H_{ii} and H_{ij} from simulation (points "+") and analytical calculation ((25), solid lines and (b) 3-D). Current gain $K_P = 15.2$ VA^{-1}; system parameters: symmetric mains/load condition, $\hat{U}_n = 325$ V and $P_{O,n} = 3500$ W for each phase module.

expressions for the decoupling coefficients are very complex and would cause a very high computational effort to adapt the decoupling matrix to the actual operating point.

$$\underline{M}_{\mathrm{DEC}} = \underline{H}^{-1} = \frac{2U_0/(3\hat{U})}{(\hat{U} - K_P\hat{I})} \times \begin{pmatrix} 5\hat{U} - K_P\hat{I} & -(\hat{U} + K_P\hat{I}) & -(\hat{U} + K_P\hat{I}) \\ -(\hat{U} + K_P\hat{I}) & 5\hat{U} - K_P\hat{I} & -(\hat{U} + K_P\hat{I}) \\ -(\hat{U} + K_P\hat{I}) & -(\hat{U} + K_P\hat{I}) & 5\hat{U} - K_P\hat{I} \end{pmatrix}. \quad (27)$$

In order to avoid the problem of intersections between the cross- and direct-coupling coefficients, the current controller gain K_P has to be reduced so that $H_{ii} > H_{ij}$ is given over the whole operation range. Based on (25) the condition $H_{ii} > H_{ij}$ can be translated into

$$K_P < \frac{\hat{U}_{\min}}{\hat{I}_{\max}} \quad (28)$$

where $\hat{U}_{\min}$ denotes the minimum phase voltage amplitude and $\hat{I}_{\max}$ is the maximum phase current amplitude of the given operating range. A problem of this approach can arise, as in case of wide input voltage and/or power range, where the current controller gain K_P has to be reduced to very low values. Fulfilling (28) automatically fulfils $H_{ii} > 0$ as can easily be proven using (25). Fig. 12(a) shows the stationary coupling coefficients for $K_P = 15.2$ VA^{-1} ($f_D \cong 4.5$ kHz) violating the condition in (28). Setting $K_P = 7.0$ VA^{-1} ($f_D \cong 2.1$ kHz) fulfils (28) [see Fig. 12(b)] and is sufficient for realizing a current controller with low control error and acceptable dynamics over the whole operating range.

By increasing K_P, the point P_S in Fig. 12(a) would shift to the very left-hand side and result in $H_{ii} < H_{ij}$ over a wide operating range. However, it is only in principle that the shifting the singularity to small power levels is of benefit since the singularity is still in the operating range from zero to full current. For example, when the current is close to zero the condition

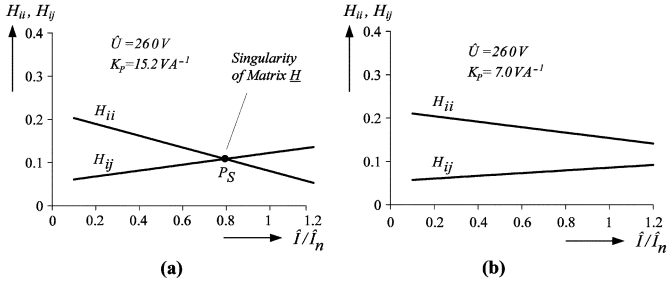

Fig. 12. Stationary coupling coefficients for $\hat{U} = \hat{U}_{\min} = 0.8 \cdot \hat{U}_n = 260$ V and (a) current controller gain $K_P = 15.2$ VA^{-1} and (b) $K_P = 7.0$ VA^{-1} where the singularity is shifted to a high power level outside the operating range.

$H_{ii} > H_{ij}$ will reoccur. Furthermore, increasing K_P results in a low current control phase margin and therefore is of no further practical interest.

IV. Designing a DC-Link Voltage Control

The role of the Y-Rectifier controller is to define the input phase current reference values, according to a symmetric ohmic loading of the mains, and to maintain the output voltages of the individual rectifier phase modules $U_{O,i}$ to a given level U_O^*. The output voltage of the dc–dc converters connected to the Y-Rectifier module outputs are controlled to the reference value U_{out}^*. A control concept that matches these requirements is shown in Fig. 13. The control concept is a computationally simpler implementation than using the decoupling matrix and is based on the fact that the current controllers' gain is set such that the direct-coupling terms are dominant and/or (28) is satisfied. Therefore, any unbalance in dc link voltage of one phase can be compensated by changing the reference current of that phase (direct coupling) and ignoring the smaller influence of the other two phases (cross coupling). The other part of the controller uses the assumption that the Y-Rectifier is operating off symmetric mains supply and that a step change in the output load should cause an equal change in the input current of all of the three modules.

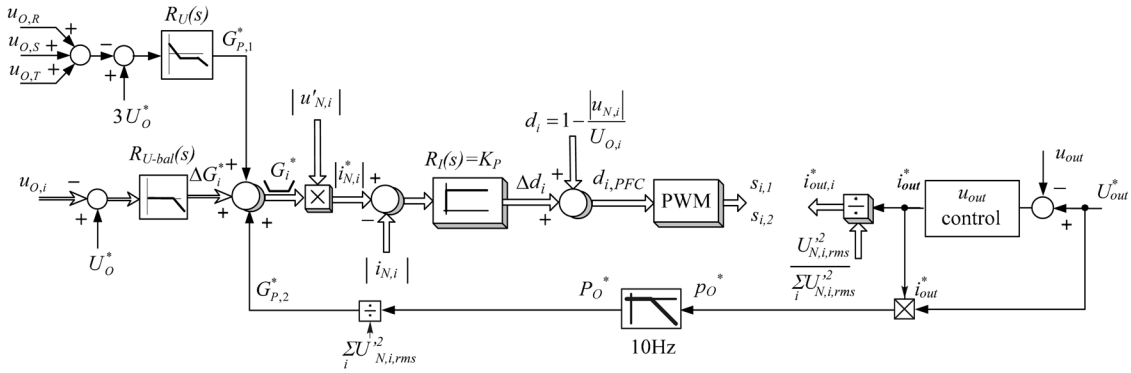

Fig. 13. Control structure of the Y-Rectifier for three-phase balanced mains operation. Signal paths for all phases are drawn with wide arrows. The index N is reintroduced for mains voltages and currents.

The input reference conductance G_i^* is calculated from the sum of the voltage controller ($R_U(\mathrm{s})$) output $G^*_{P,1}$, the output power feed-forward term $G^*_{P,2}$, and the output of the balancing voltage controller, ΔG_i^*. To balance unequal dc link voltages $U_{O,i}$, individual balancing controllers $R_{U-\mathrm{bal},i}(s)$ insert a correction term ΔG_i^* based, as previously described, on the dominant direct coupling of the system within the operation range. The balancing of the dc link voltages operates with lower dynamics compared to the setting of their average value $(\Sigma U_{O,i})/3)$ by $R_U(s)$. The reference value $i^*_{N,i}$ of an input phase current $i_{N,i}$ is then calculated by multiplication of G_i^* with the zero-sequence-free component $u'_{N,i}$ of the corresponding mains phase voltage derived from a star connection of equal resistors. The value G_i^* is limited to ensure that the phase current amplitude does not exceed an admissible maximum value $\hat{I}_{N,\max}$ according to the dimensioning of the system.

The dc–dc output stage is formed by three parallel connected dc–dc converters with a common output and the reference current, $i^*_{\mathrm{out},i}$, for the individual dc–dc output current controllers (not shown) is set according to a symmetric ohmic loading of the mains. The output power of a dc–dc converter stage connected to a rectifier phase module output $U_{O,i}$ is defined to be equal to the module input power by properly selecting $G^*_{P,2}$ and the dc–dc stage output current $i^*_{\mathrm{out},i}$. Therefore, the dc link voltage $U_{O,i}$ ideally should remain at a constant level. However, due to the losses in the real system, control of $U_{O,i}$ has to be provided such that it adapts the reference conductance G_i^* by ΔG_i^*.

V. Experimental Implementation

A 5.4 kW, 400 $\mathrm{V_{RMS}}$ line-to-line Y-Rectifier, with integrated dc–dc converters producing 48 $\mathrm{V_{dc}}$, has been implemented in hardware. The Y-Rectifier prototype has the parameters shown at the bottom of the page.

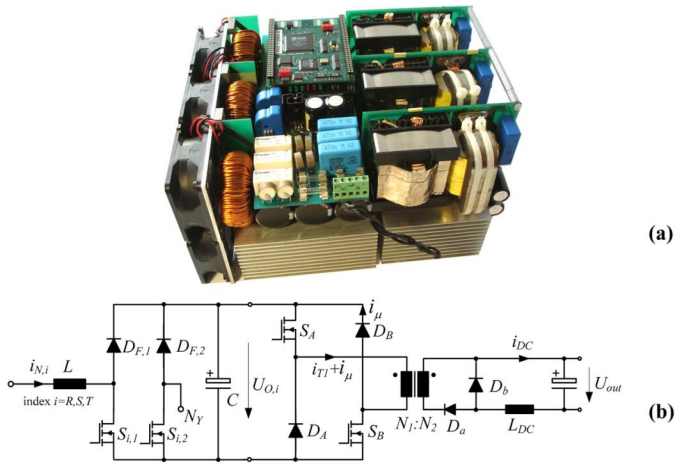

Fig. 14. (a) 5.4-kW prototype of the Y-Rectifier with dimensions of 20 cm × 12 cm × 27 cm, weight of 6.2 kg, and power density of 840 W/dm^3 (13.8 W/in^3). (b) Topology of one of three power modules.

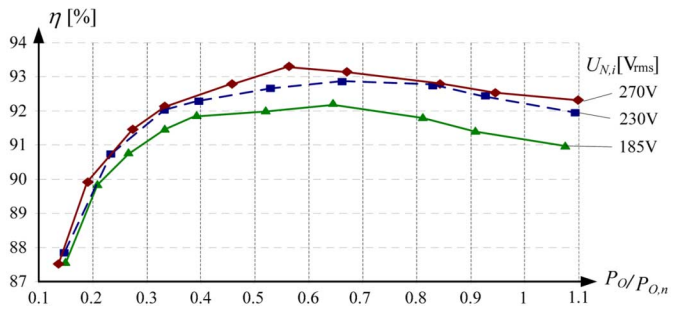

Fig. 15. Measured system efficiency for various symmetrical mains voltages and output powers.

The modular structure of the system can be easily seen from the prototype shown in Fig. 14(a). Each module consists of the

Rated power	$P_{O,n} = 5400$ W $\quad (\rho_{Po/V} = 840$ W/dm$^3 = 13.8$ W/in$^3)$
Input voltage range	$U_{N,l-l} = 320$ V $\ldots 530$ $\mathrm{V_{rms}}$
Module dc link voltage	$U_{O,i} = 400$ $\mathrm{V_{dc}}$
Output voltage	$U_{\mathrm{out}} = 46 \ldots 54$ $\mathrm{V_{dc}}$
Switching frequency	$f_P = 50$ kHz (for PFC rectifier and dc–dc output stage)
Module input inductors	$L = 580$ μH (iron powder cores)

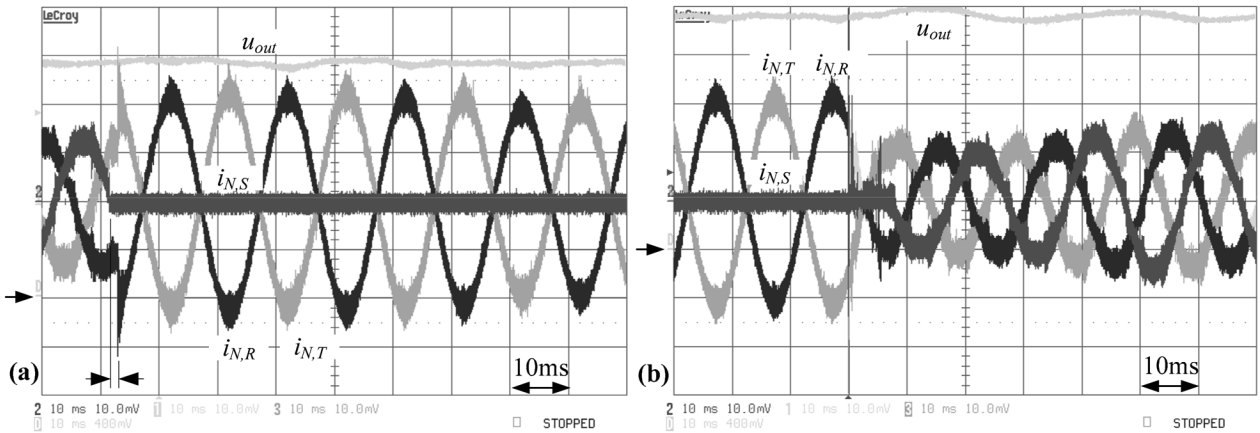

Fig. 16. Experimental phase currents and output dc voltage for a phase loss (a) and reconnection (b) of phase S. Output voltage zero-level marked by the left side arrow. Current range: 5 A/Div, Voltage range: 10 V/Div.

loss-minimized two-level PFC input stage and a two-switch forward converter for the dc–dc output stage [Fig. 14(b)]. A connection PCB links three of these power modules in star-connection to the three phase mains and includes the digital controller, measurement circuits and the housekeeping power supply. The digital controller is implemented with an ADSP-21992 digital signal processor (DSP) and a PLD for generating the PWM signals of the 12 power MOSFETs (four in each phase).

For testing, the complete rectifier system is supplied from a symmetric three-phase voltage system generated by a three-phase high power linear amplifier (Spitzenberger & Spies DM 15000 PAS) and feeds an ohmic load. The overall efficiency, with dependency on the input voltage at constant output voltage $u_{\rm out} = 48$ V, is measured by a power analyzer (Norma Power Analyzer D6100) and shown in Fig. 15. The nominal system efficiency is over 92% and therefore is competitive to direct three phase rectifier systems described in [12]–[15] that show an overall efficiency in the range of 91 to 93.5%.

The measured THD of the phase currents, up to the 50th harmonic, is less than 1.9%. The dynamic behavior for the case of a phase loss and then return of the third phase after two-phase operation are shown in Fig. 16. After detecting a phase loss (marked distance in Fig. 16(a), t <1.5 ms) the DSP system switches from the three-phase control structure shown in Fig. 13 to the two-phase control structure in Fig. 9(a). Once nominal three-phase mains voltages are detected again, the DSP changes from the two-phase control structure back to three-phase control structure. It can be seen that the use of a DSP controller allows the control strategy to successfully switch between the normal three-phase decoupled strategy to the two-phase strategy and visa-versa. Therefore, the system control quickly adjusts the mains currents so that only a low output power and/or output voltage dip occurs. The low frequency distortion on the output dc voltage is caused by the output stage having a single low pass stage with low damping.

VI. Discussion

The isolated star point, formed by the star-connection of the single-phase rectifier modules (Y-Rectifier), results in a mutual coupling of the individual phase rectifier outputs, therefore individual control of each module is not adequate. The overall controller assumes a power sharing of the modules that is characterized by a symmetrical ohmic load. As a consequence, the control of the Y-Rectifier is only reasonable for a parallel connection of the dc–dc outputs and for supplying a simple common load.

Based on derived analytical expression for the mutual coupling, the maximum value for the control gain of the individual current controllers can be determined, such that the cross coupling does not have significant influence on the system for symmetric mains conditions. To manage the different coupling behaviors during three-phase and two-phase operation, the controller switches between two different control concepts once the phase loss or return condition is detected and this has been experimental verified. For two-phase operation the maximum available output power is reduced to 58% of the nominal power available during symmetrical three-phase operation, since the two series connected modules are now operating off the remaining line-to-line voltage with the same maximum operating current.

VII. Conclusion

The Y-Rectifier combines three single-phase unity power factor rectifier modules with isolated dc–dc converter output stages in a three-phase star connection with floating star point N_Y. This is an attractive concept for the realization of high power telecommunication power supply systems. The main advantages of the Y-Rectifier are the low dc output voltage level of the rectifier modules compared to direct three-phase solutions, and that the system has a high degree of modularity. Compared to individual single-phase rectifiers connected to a three phase mains with neutral, there is a large reduction in the input current ripple. However, not having a connection between N_Y and the mains neutral results in a cross coupling of the dc link voltage control loops. An analytical model is derived that reveals the dependency of the cross coupling terms in the system matrix on the operating parameters and the mains current controller gain. Based on this, a control concept is presented and the criteria for the current controller gain is determined, such that the cross coupling has a low influence on the system. In case of a phase loss, the controller is able to switch to a proper control method for the two remaining modules connected in series. The control method has been experimentally verified for two-phase and three-phase operation. In a typical telecommunication power supply application the output orientated control scheme is the most obvious choice. However, this paper has analyzed the

input orientated control scheme for the Y-Rectifier and it has been shown that input orientated control can be successfully used in applications which require the supply of power to three symmetric isolated loads.

REFERENCES

[1] J. W. Kolar, F. Stögerer, and Y. Nishida, "Evaluation of a delta-connection of three single-phase unity power factor rectifier systems (delta-rectifier) in comparison to a direct three-phase rectifier realization. Part I—Modulation schemes and input current ripple," in *Proc. 7th Eur. Power Quality Conference (PCIM)*, Nuremberg, Germany, Jun. 19–21, 2001, pp. 101–108.

[2] J. Miniböck, R. Greul, and J. W. Kolar, "Evaluation of a delta-connection of three single-phase unity power factor rectifier modules (delta-rectifier) in comparison to a direct three-phase rectifier realization, Part II—Components stress evaluation, efficiency, control," in *Proc. 23rd IEEE Int. Telecommunications Energy Conf.*, Edinburgh, U.K., Oct. 14–18, 2001, pp. 446–454.

[3] J. W. Kolar and F. C. Zach, "A novel three-phase utility interface minimizing line current harmonics of high-power telecommunications rectifier modules," *IEEE Trans. Ind. Electron.*, vol. 44, no. 4, pp. 456–467, Aug. 1997.

[4] A. R. Prasad, P. D. Ziogas, and S. Manias, "An active power factor correction technique for three-phase diode rectifiers," *IEEE Trans. Power Electron.*, vol. 6, no. 1, pp. 83–92, Jan. 1991.

[5] G. Spiazzi and F. C. Lee, "Implementation of single-phase boost power-factor-correction circuits in three-phase applications," *IEEE Trans. Ind. Electron.*, vol. 44, no. 3, pp. 365–370, Jun. 1997.

[6] M. Karlsson, C. Thoren, and T. Wolpert, "A novel approach to the design of three-phase ac/dc power converters with unity power factor," in *Proc. 21st IEEE Telecommunications Energy Conf., INTELEC'99*, Copenhagen, Denmark, Jun. 06–09, 1999, vol. 1, p. 5.1.

[7] D. Chapman, D. James, and C. J. Tuck, "A high density 48 V 200 A rectifier with power factor correction—An engineering overview," in *Proc. 15th IEEE Int. Telecommunications Energy Conf.*, Paris, France, Sep. 27–30, 1993, pp. 118–125.

[8] R. Martinez and P. N. Enjeti, "A high-performance single-phase rectifier with input power factor correction," in *IEEE Trans. Power Electron.*, Mar. 1996, vol. 11, no. 2, pp. 311–317.

[9] R. Greul, U. Drofenik, and J. W. Kolar, "Analysis and comparative evaluation of a three-phase unity power factor Y-Rectifier," in *Proc. 25th IEEE Int. Telecommunications Energy Conf.*, Yokohama, Japan, Oct. 19–23, 2003, pp. 421–428.

[10] J. W. Kolar, U. Drofenik, and F. C. Zach, "On the interdependence of ac-side and dc-side optimum control of three-phase neutral-point-clamped (three-level) PWM rectifier systems," in *Proc. 7th Int. Power Electronics & Motion Control Conf.*, Budapest, Hungary, Sep. 2–4, 1996, vol. 1, pp. 40–49.

[11] R. Greul, U. Drofenik, and J. W. Kolar, "A novel concept for balancing of the phase modules of a three-phase unity power factor Y-Rectifier," in *Proc. 35th IEEE Power Electronics Specialists Conf.*, Aachen, Germany, Jun. 20–25, 2004, ISBN: 07803-8400-8.

[12] N. Backman and R. Rojas, "Modern circuit topology enables compact power factor corrected three-phase rectifier module," in *Proc. 24th Int. Telecommunication Energy Conf. (INTELEC)*, 2002, pp. 107–114.

[13] R. Gules, A. S. Martins, and I. Barbi, "A switched-mode three-phase three-level telecommunications rectifier," in *Proc. 21st Int. Telecommunication Energy Conf. (INTELEC)*, Jun. 6–9, 1999, pp. 29–3.

[14] P. Prestifilippo, R. Scibilia, G. Baggione, and G. Caramazza, "A switched-mode three-phase 200 A/48V rectifier with input unity power factor," in *Proc. 18th IEEE Int. Telecommunications Energy Conf., (INTELEC)*, Oct. 6–10, 1996, pp. 543–547.

[15] J. Miniböck, J. W. Kolar, and H. Ertl, "Design and experimental analysis of a 10 kW 800 V/48 V dual interleaved two-transistor dc–dc forward converter system supplied by a Vienna rectifier I," in *Proc. 41st Int. Power Conversion Conf. (PCIM)*, Nuremberg, Germany, Jun. 6–8, 2000, pp. 569–579.

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