Digital Current Controller for a 1 MHz, 10 kW Three-Phase VIENNA Rectifier

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***Abstract*—Active three-phase rectifiers operated at switching frequencies of 500 kHz and above, in order to increase their power density, require high-speed current controllers. If these current controllers are implemented purely digitally, which is well established today for 20–200 kHz converter systems, then very high numerical data processing demands result. In this paper, two different types of field-programmable gate arrays (FPGAs) are evaluated for realizing high-speed converter current control. For the implementation of such controllers, not only the FPGA has to be considered but rather the entire signal chain. Two alternative A/D interfaces (including high-speed low-voltage differential signaling data transmission) that are able to handle data sampling rates up to 25 MSa/s are verified. Subsequently, a digital current controller is designed and it is shown how hardware multiplier blocks of modern FPGAs can be used advantageously. Furthermore, the FPGA implementation of high-resolution pulsewidth modulation providing symmetrical pulse patterns for high switching frequencies is described. Measurements taken from a 10 kW VIENNA rectifier laboratory prototype finally demonstrate the high performance of the proposed control concept and show that a low mains current total harmonic distortion of 1.4% can be achieved for such ultrahigh switching frequency converters.**

***Index Terms*—AC–DC power conversion, current control, digital control, field-programmable gate arrays (FPGAs), power factor correction (PFC).**

I. Introduction

MODERN active rectifiers offer the advantages of unity power factor, high compactness, high efficiency, and sinusoidal input currents. The three-level VIENNA rectifier (VR) topology [1] is an ideal choice for telecom and data server power supplies or rectifiers for aerospace applications [2]. Aerospace applications are challenging for the current controller realization due to the high, variable input frequency of 360–800 Hz and, additionally, a high power density, i.e., a high power to weight ratio is required [3]. An increase in power density requires an increase in switching frequency from today's industry standard of 20 kHz to over 500 kHz. Current control of such high switching frequency three-phase converters poses a challenge. A classical analog average current controller as in [4] shows several problems, especially, the high-speed analog pulsewidth modulator (PWM) suffers from limited accuracy and configurability. Alternatively, three analog power factor correction (PFC) control chips, which are commercially available for single-phase PFCs (e.g., UC3854), could be applied for current control. This would be an easy and relatively cheap approach to overcome the mentioned drawbacks, but these chips typically use a sawtooth-shaped carrier signal and usually cannot be synchronized in an easy manner. A sawtooth-shaped carrier signal results in nonoptimal switching sequences and the three phases are not correlated due to the missing synchronization. Altogether, this leads to higher current ripple in the boost inductances and to significantly higher input current distortion [5].

Using purely digital current control, by application of a modern high-speed digital signal processor (DSP), is a good way to control these rectifiers for medium and high switching frequencies (f_s = 20–200 kHz) [6]. Considerable research into digital control of single-phase PFCs has been performed by several groups [7]–[11] and a good introduction to digital current mode control can be found in [12]. Input voltage feedforward has emerged as a very effective way to improve the input behavior of digitally controlled PFC circuits [13]. For practical realizations, the sampling point of the current measurement becomes very important due to the disturbances of the current measurement signal in the vicinity of any switching instant. This influence can be avoided if the sampling instant is chosen optimally [14].

In all these approaches, the data processing and numerical calculations of the current controller have to be executed within one switching cycle, which limits the switching frequency of the rectifier system. This is even more difficult to achieve in a single DSP solution since the control of three currents have to be performed sequentially for a three-phase rectifier system. One approach to overcome this limitation is to calculate a new duty cycle for only one phase of the three-phase rectifier during a switching period and to hold the duty cycles of the two other phases constant during this time. In the next switching cycle, the second phase is controlled and the two other phases are held constant, whereas in the following switching cycle, the third phase is controlled. This method was used to control a VR system with a switching frequency of 400 kHz, described in [6]. For this realization, the calculation time of the current controller (for one phase) has been reduced to only 1 μs. Unfortunately, the delay time of the A/D converter has to be added to this calculation time. As a consequence, the inductance value/size has to be increased to achieve a small current ripple. Additionally, this approach shows only an improvement by a factor of three in the calculation speed.

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In [15], a digital "offline" control technique has been presented, where the duty cycles of a single-phase boost converter are calculated in advance based on the power balance equation of the converter. This offline calculation is performed for several operating points and a set of duty cycles are stored in a memory. Depending on the operating point of the rectifier, a specific set of duty cycles is selected to control the switches. This control strategy is not directly dependent on the switching frequency of the converter but cannot be used for the desired application because of the very large input current distortion, and hence, its application is limited to a small number of operating points. Another predictive algorithm is presented in [16] that shows several improvements, but this approach is also not applicable in systems with variable ac input frequencies.

The key to overcome the limited processing speed is "parallelization." This could be implemented by using one DSP for each phase of the three-phase system, but the number of instructions executed between the sampling instants is still limited and the cost of realization is high. Another option is to use a field-programmable gate array (FPGA) for current control, which intrinsically offers parallelization. In contrast to the sequential operation of DSPs, all operations can be executed simultaneously within an FPGA and so a substantial increase in processing speed can be achieved. In [17], a digital controller implementation in an FPGA using a switching frequency of 50 kHz is presented. The efficient implementation of proportional–integral–differential controllers in an FPGA is discussed in [18] as well as FPGA predictive algorithms in [19]. All these designs use conventional logic cells for realization of the controller elements and the processing speed of these elements (dependent on the type of the FPGA) is still limited to clock rates of less than 100 MHz. Another limitation is the realization of a digital PWM (DPWM). For a classical symmetrical counter/comparator realization with a resolution of 10 bit, a clock frequency of over 2 GHz would be necessary, which is far too high, even for high-speed FPGAs. Since switching frequencies in the megahertz range are common in low-power dc/dc converters, a lot of work to overcome this limitation has been performed by research groups dealing with these converter types [20]–[22]. Most of the reported solutions are using digital delay lines for PWM generation and are directly implemented into a prototype chip using standard CMOS processes. Unfortunately, these concepts are not directly applicable for an FPGA implementation because the delay lines are sensitive to temperature and voltage changes, which normally cannot be controlled in a commercial FPGA. Several concepts for implementation of a high-speed, high-resolution DPWM in an FPGA have been developed [23]–[26], but all these concepts realize only edge-aligned PWMs. Hence, a new high-speed PWM scheme is proposed in this paper which is able to generate three-phase symmetrical PWM signals.

In this paper, two realizations for a 1 MHz three-phase rectifier are presented (cf., Fig. 1), which use modern high-speed FPGAs. Today's high-speed FPGAs contain DSP blocks including hardware multipliers that can be used to implement the control algorithm. The effort to implement a controller for switching frequencies above 1 MHz increases rapidly. Hence, two implementations using FPGAs from different vendors are presented.

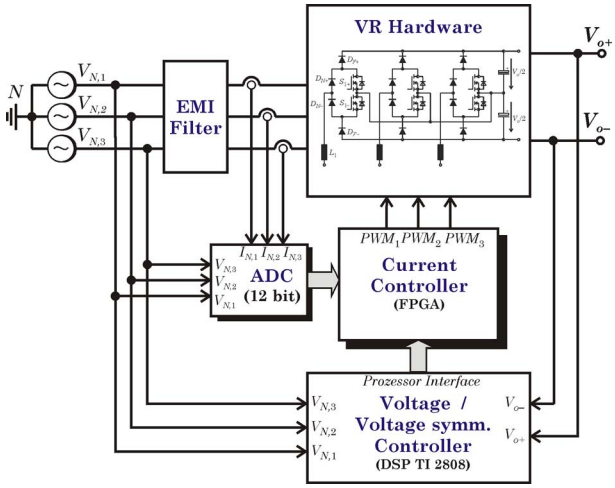

Fig. 1. Structure of the proposed digital current controller for the three-phase six-switch (VIENNA-type) rectifier system.

For the first realization (C1), a maximal switching frequency of 1 MHz is intended and an FPGA from Lattice Corporation (ECP2) is used. The second realization (C2) is for switching frequencies above 1 MHz based on a high-speed FPGA from Xilinx Corporation (VIRTEX4).

An overview of the implemented systems is given in Section II. In Section III, the design of the control loop, considering the whole signal chain, is discussed. The implementation of the current controller in the two different FPGAs including a comparison of performance and chip utilization is the focus of Section IV. In Section V, measurement results taken from laboratory prototypes verify the performance of the different controller realizations.

II. System Overview

In Fig. 1, the basic structure of the proposed control for the three-phase VR system, operating at a switching frequency of 1 MHz, is shown. The digital high-speed current controller is implemented by application of a modern high-speed FPGA. For realization C1, the FPGA ECP2 LFE2-12E-6T144I with a speed grade 6 from Lattice is used. Realization C2, to implement the highest possible switching frequency, uses the VIRTEX4 XC4-VLX25-10FF668 FPGA with a speed grade 10 from Xilinx. There are no analog-to-digital converters (ADCs) included in the FPGAs, which means that an external A/D converter is required. The main limitation for the ADC is its delay time (time between sampling instant and availability of the sampled data), which is also influenced by the interface type of the ADC. Therefore, two different ADCs with different interface types are used for the two realizations.

For the total rectifier system, an output voltage and output voltage symmetry controller are needed. Since the timing requirements for these controllers are not so stringent, a single DSP can be used to control these system parameters. Additionally, the comfortable debugging tools of the DSP can be used for those particular system parts. According to Fig. 1, the internal A/D converters of the DSP with a resolution of 12 bit are used for output voltage measurement. In a typical three-phase

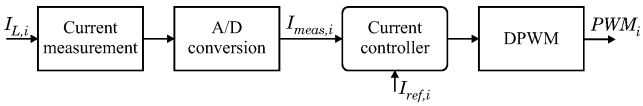

Fig. 2. Single-phase signal chain of the digital current controller for a three-phase current controller.

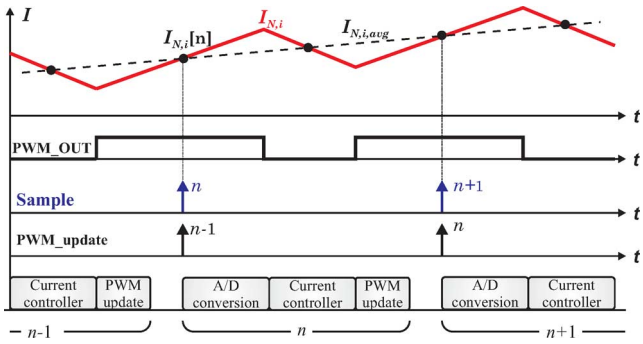

Fig. 3. Timing diagram of the sampling strategy. The current signal is sampled in the middle of the PWM. After the A/D conversion time, the duty cycle d is calculated by the current controller and updated at the start of the next PWM cycle.

rectifier system, an output voltage ripple of 0.1 V_o is required, and therefore, a resolution of 12 bit is sufficient for output voltage measurement. The reduced PWM resolution of the current controller (8 bit) is only of interest for input current quality because the bandwidth of the current controller is much higher than the bandwidth of the output voltage controller. The interface between the DSP (voltage controller) and the FPGA (current controller) can either be realized by a serial or a parallel interface. For the presented realizations, a serial peripheral interface (SPI) is implemented, where the intrinsic DSP functionality can be used.

In order to be able to implement a three-phase rectifier system with a switching frequency of over 1 MHz, each element of the complete signal chain, comprising current measurement, A/D conversion, digital controller, and high-speed DPWM generation, has to be considered in detail (cf., Fig. 2). The realization of a current measurement with a bandwidth of [dc $>$ 1 MHz] poses a challenge, but is not discussed in this paper for the sake of brevity (cf., [27] and [28]).

III. System Design

As a first step, the timing requirements on the system blocks have to be defined. A timing diagram of the sampling strategy (of one-phase current) is shown in Fig. 3. In addition to the average input current $I_{N,i,\mathrm{avg}}$ of the rectifier, a current ripple is present. As is well known, the sample value $I_{N,i}[n]$ is equivalent to the average current value $I_{N,i,\mathrm{avg}}$ if the sampling point is located in the middle of the PWM period. Furthermore, a large amount of ringing occurs in the current measurement signal near the switching instants. The influence of this ringing on the current measurement can be minimized by this sampling strategy. Hence, synchronization between PWM generation and sampling of the currents is very essential. This synchronization can be realized by a center-aligned (symmetrical) PWM

TABLE I
Specifications of the Used A/D Converters

	Controller C1 AD7274	Controller C2 ADS5240
Sampling frequency	1 MSa/s	25 MSa/s
Resolution	12 bit	12 bit
Converters / Package	1	4
Interface	SPI	LVDS
Delay	448 ns	300 ns
Cost (per 1000pcs.)	US$ 6.58	US$ 25.88

generation. Additionally, the center-aligned PWM generation offers the advantage of reduced input current distortions in the intended VR application [5]. Therefore, a center-aligned PWM is used.

After sampling the actual current value $I_{N,i}[n]$, the ADC requires some time to convert the sampled analog value into a digital word. This result is used by the current controller to calculate the new duty cycle of the PWM signal. At the sampling instant $n+1$, the PWM value is updated with the new duty cycle $d[n]$. This sampling strategy is also known as uniformly sampled modulation [29]. Hence, according to Fig. 3, the whole controller calculation, consisting of A/D conversion, calculation of current controller, and update of the PWM, has to be done within a single switching cycle. This delay (deadtime) of one cycle has to be included in the controller design and reduces the phase margin of the controller loop considerably. For lower switching frequencies, a double update of the PWM is possible, which reduces this delay, and therefore, increases the stability of the current controller.

A. A/D Conversion

In a second step, an appropriate ADC has to be chosen. Due to the small amplitude of the ripple current, a high dynamic range of the ADC is needed. Therefore, a converter with a resolution of 12 bit or more may be required. However, the main selection criterion is its delay, because ADCs with high sampling rates usually show a relatively long delay between sampling and availability of the data. A/D-converters with sampling frequencies of 3 MSa/s are commercially available with a simple SPI interface and such a converter is used for the controller realization C1. For higher sampling frequencies, only ADCs with parallel- or LVDS interface [30] are available. Consequently a (pipelined) ADC with a sampling frequency of $f_s = 25$ MHz and an LVDS interface is used for controller realization C2. The main specifications of the used A/D converters are listed in Table I. For comparison purposes, the prices of the two A/D converters are also listed in Table I. In general, the overall system costs should be considered to give a statement on costs. For example, a higher switching frequency results in smaller boost inductors and a smaller electromagnetic interference (EMI) filter, which may reduce the realization costs of these elements. Therefore, overall system costs may get lower at higher switching frequencies even if a more expensive A/D converter is used. The converter ADS5240 used for controller realization C2 has a higher price, but this device already includes four converters

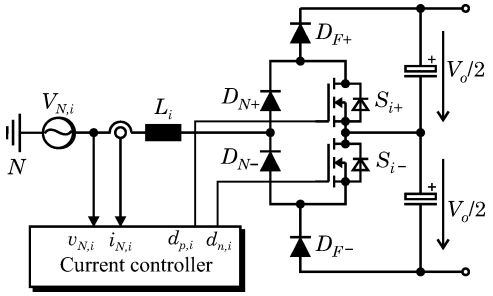

Fig. 4. One phase leg of the three-level six-switch VIENNA-type rectifier.

in a single package, and hence, is a cheaper solution than the device AD7274 used for realization C1 if all four converters are used (the converter AD7274 only includes a single A/D converter). However, the converter ADS5240 offers differential input stages, and therefore, an additional fully differential ADC driver stage is needed that may increase system costs for this realization.

The LVDS interface, in general, is well-suited for power electronic applications because it is based on current drivers and differential signaling. The physical effort of realizing an LVDS interface, however, is much higher than for a simple SPI interface. Indeed, the selected FPGAs, in fact, are able to directly drive the LVDS signals without any additional components, but impedance-controlled and length-matched printed circuit board (PCB) tracks have to be realized. Additionally, as discussed in Section IV, the digital implementation of the LVDS interface in the FPGA is much more complex. However, the serial LVDS interface is the only alternative to a parallel interface if very high switching frequencies of $f_s > 1$ MHz are to be realized.

B. Controller Design

For the design of a digital controller, two different strategies are possible. One strategy is to design an appropriate analog controller and convert it into the digital domain. The other strategy, known as direct digital design, is to directly design the controller in the z-domain. The direct digital design method results in a slightly better controller performance with regard to phase margin and achievable bandwidth [31]. On the other hand, digital redesign offers the capability to use the well-known design methods of the continuous-time implementations. Hence, a digital redesign of an analog controller will be used in this paper. For this purpose, an analog model of the rectifier has to be developed. In this paper, average mode control will be used, which means that all signals are averaged over one switching period. According to Fig. 4, each switch (of the two switches per phase) is only involved for half a period of the mains voltage. Using the duty cycle d_i, the inductor voltage balance results in

$$v_{N,i}(t) - \frac{v_o(t)}{2}(1 - |d_i(t)|) = L\frac{di_{N,i}(t)}{dt}. \tag{1}$$

The output voltage $v_o(t)$ of the rectifier is assumed to be constant $v_o(t) = V_o$, which is accomplished by the output voltage

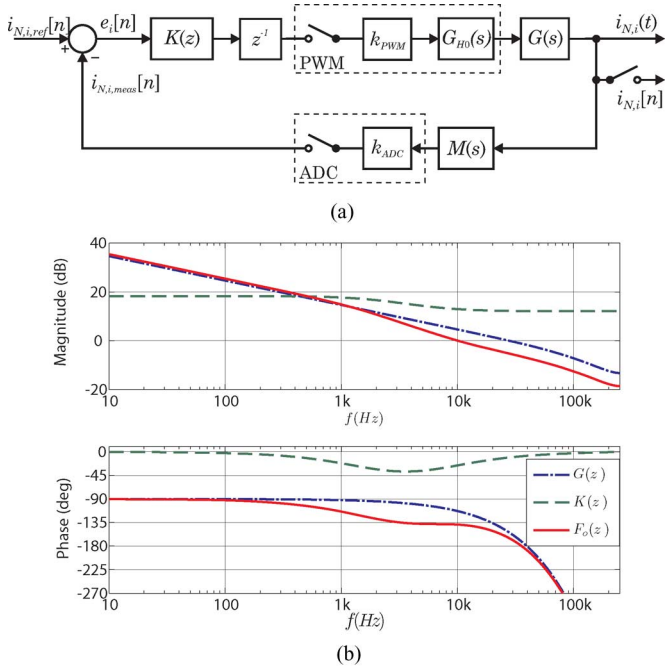

Fig. 5. Design of the digital current controller: (a) control loop and (b) bode plot of the digital current controller. The designed controller shows a phase margin of 45°.

controller. Using the feedforward function

$$d_{\mathrm{res},i} = d_{\mathrm{ff},i} + d_i \qquad d_{\mathrm{ff},i} = 1 - \frac{v_{N,i}(t)}{V_o/2} \tag{2}$$

and by application of the Laplace transform on (1) results in the simple model

$$G(s) = \frac{i_{N,i}(s)}{d_i(s)} = \frac{V_o}{2Ls}. \tag{3}$$

In this model, some details, such as the impedance of the mains, the characteristics of the EMI filter, the delay times of the switches, or the characteristic right-hand-zero of the boost circuit, are not considered for sake of simplicity. Previous work on a 400 kHz VR system [6] showed that a simple P + Lag controller

$$K(s) = K_p\frac{1 + sT_D}{1 + sT_1} \tag{4}$$

in conjunction with the voltage feedforward function of (2) is a good solution. For the design of the analog controller, the delay of the symmetrical PWM $G_{\mathrm{PWM}}(s)$ [32] and the delay caused by the controller calculation $G_{\mathrm{calc}}(s)$, which can be modeled as

$$G_{\mathrm{PWM}}(s) = e^{-sT_s/2} \qquad G_{\mathrm{calc}}(s) = e^{-sT_s} \tag{5}$$

where T_s is one switching period, have to be considered.

For discretization of the analog controller given in (4), the bilinear (Tustin) transformation is used, which results in

$$K(z) = K\frac{1 - k_1 z^{-1}}{1 - k_2 z^{-1}}. \tag{6}$$

The behavior of the designed controller can be verified in the z-domain. A block diagram of the control loop including the digital controller is given in Fig. 5(a). According to [33], the

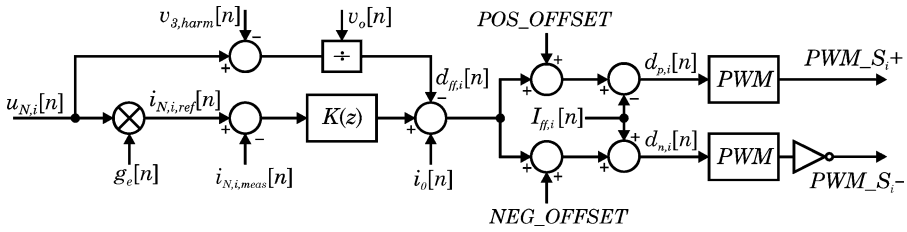

Fig. 6. Structure of the digital current controller for one phase.

symmetrical PWM is modeled by a sample and hold element $G_{H0}(s)$. Additionally, the bandwidth limitation of the current sensor is included in the model by $M(s)$. In Fig. 5(b), a Bode plot of the resulting control loop is depicted, where a phase margin of 45° can be found.

For the final controller implementation, several additional parts have to be added to the current controller. The resulting structure of the digital current controller is shown in Fig. 6. In order to increase the modulation range of the rectifier, a third harmonic signal $v_{3,\mathrm{harm}}$ is added and a zero-sequence current component i_0, generated from the voltage symmetry controller, is used to balance the output voltages [34]. CoolMOS devices are used for realization of the switches. Unfortunately, these devices exhibit, apart from their excellent conduction behavior, a relative large turn-OFF delay at lower current levels [35]. This results in increased current zero-crossing distortions, especially at the intended high switching frequencies [36]. In order to attenuate this effect, a current feedforward signal $i_{\mathrm{ff},i}$ is used to compensate the delay. There are two PWM units necessary to generate the gate signals for the two switches, where the PWM signal of the switch $S_{i\_}$ has to be inverted. The *POS_OFFSET* and *NEG_OFFSET* signals are used to realize the required voltage feedforward signal of (2). These two offsets can also be adapted by a superimposed controller to achieve better performance in DCM [37].

C. PWM Generator

The generation of the symmetrical high-speed PWM signals have to be implemented inside the FPGA since there is no external PWM modulator readily available for such high frequencies. There are several possibilities known in literature to implement a digital high-speed PWM using an FPGA. The performance of a "classical" counter/comparator approach is limited due to the very high clock frequencies required to implement a high-frequency PWM. An FPGA implementation using a hybrid delay line/counter scheme is described in [23]. However, this implementation is only applicable to trailing edge modulators, shows a strong temperature dependence, and is not easy to implement. It has been shown in [24] that the resolution of a counter/comparator approach can be increased by application of phase-shifted clocks. However, this realization is also limited to trailing edge modulators.

In this paper, a novel PWM modulator using two phase-shifted clocks is used (cf., Fig. 7). The modulator consists of two different counters/comparators running with a phase shift of 180°.

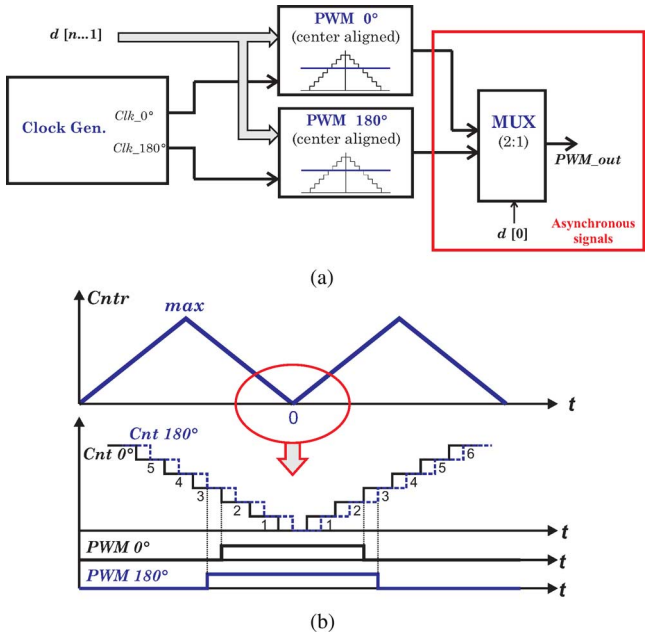

Fig. 7. Proposed digital PWM-concept for a center-aligned PWM modulator: (a) structure of the concept and (b) generation of the PWM patterns for a comparator value of $d = 3$.

TABLE II
COMPARATOR VALUES d FOR THE PROPOSED PWM MODULATOR

	PWM 0∞= 1	PWM 180∞= 1
Count up	*Cntr* < *d*	*Cntr* < *d*
Count down	*Cntr* < *d*	*Cntr* < *d*+1

The least significant bit selects, if either the PWM signal with 180° phase shift or the PWM signal without phase shift is used. A combination of the two signals is used to increase the resolution of the PWM modulator by 1 bit. Only switching between the two phase-shifted PWM signals would result in asymmetrical signals, and therefore, the comparator value d of the 180° phase-shifted modulator has to be adapted. This is done at the two instants, where the counter direction has to be reversed (Cntr = 0, Cntr = max) and the modulator is also updated with the new duty cycle at these instants. Both comparator limits (PWM0 and PWM180) have to be set to d while counting up, whereas the comparator value for the 180° phase-shifted modulator has to be set to $d + 1$ while counting down. The necessary comparator values d are summarized in Table II and the resulting PWM patterns for $d = 3$ are plotted in Fig. 7(b). The

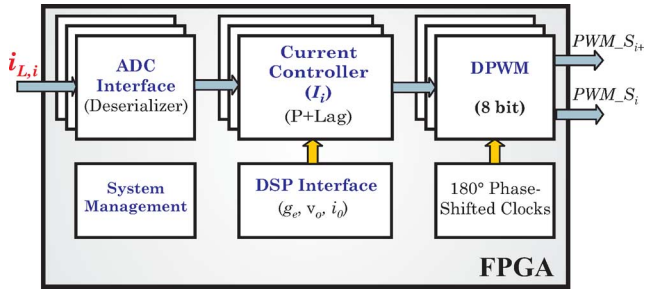

Fig. 8. Overview of the controller implementation in the FPGA.

two phase-shifted signals have to be treated as asynchronous signals in the FPGA. Hence, the multiplexer must be realized by logic cells without a (pipeline) register and operates continuously. The multiplexer output is changed at the same instant when the modulator is updated and the output is set according to the least significant bit of the comparator value $d[0]$. Therefore, timing and routing constraints have to be used in the design implementation. This concept could also be extended to four 90° phase-shifted modulators (modern FPGAs are typically able to generate 90° phase-shifted clocks by an internal delay-locked loop), which would increase the resolution by one more bit. Unfortunately, the more complex adaption of the comparator value d inhibits a high-speed implementation of this extended concept at present.

IV. Implementation of the Systems

In this section, the two implementations of the current controllers using the two FPGAs are discussed. Even though the implementations are adjusted to fit the selected FPGAs in this paper, nearly all other FPGA vendors offer FPGAs with similar functionality, and therefore, could be selected.

An overview of the controller implementation, listing all implemented blocks, is shown in Fig. 8. All three current controllers (one for each phase) are processed in parallel. Additional system parts, like the interface to the DSP, system management, and clock generation for the digital PWM, are also shown. The implementation of the whole system is fully written in very high speed integrated circuit hardware description language (VHDL). To synthesize and fit the implemented controller, the free design tools from the vendors are used (ispLEVER starter for implementation C1 and Xilinx ISE Webpack for the implementation C2). Both implementations are running with an internal system clock of 125 MHz. The data from the superimposed voltage controller g_e and voltage symmetry controller i_0 are sent from the DSP by an SPI interface. This interface is not discussed further here.

A. Implementation of the ADC Interface

According to Section II, the sampling instants have to be synchronized to the PWM generation. Therefore, the PWM module generates the start of conversion signal for the ADC.

1) Implementation C1: The realization of an SPI interface in an FPGA is relatively simple. The serial data stream has

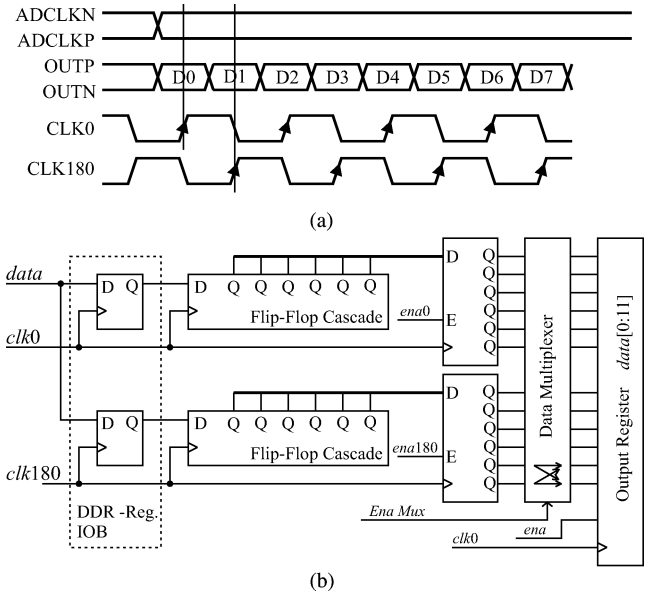

Fig. 9. LVDS interface to the ADCs according to [38]: (a) timing of the interface. The data is sampled at the rising and falling edge of the clock signal and (b) overview of the implementation in the FPGA.

to be deserialized, which can easily be done by a simple shift register. The ADC clock of 31.25 MHz is generated in the FPGA by application of an existing phase-locked loop. In general, there are two possibilities to implement this interface—either the (asynchronous) ADC clock is used as clock signal for the ADC interface in the FPGA or the ADC signals (clock and data) are synchronized to the internal system clock. In general, multiple clock domains should be avoided in FPGAs whenever this is possible; hence, synchronization is the better way. However, several fast clock nets are available in the selected FPGA and so the external ADC clock is used as the clock signal for the realization of the ADC interface, which results in a very easy implementation. Of course, the ADC data has to be synchronized to the system clock after deserialization by application of two D-flip flops.

2) Implementation C2: In contrast to the very easy SPI interface of realization C1, the LVDS interface implementation of realization C2 is much more complex. The ADC interface is implemented according to an application note of Xilinx [38] and it seemed to be straightforward but several issues occurred, which will be discussed in the following. The used Xilinx FPGA offers the capability to drive LVDS signals without any external components. The sampled data is transferred at the rising and falling edge of the differential clock signal [cf., Fig. 9(a)]. To deserialize this serial data stream, the internal DDR input registers (clock signal on positive and negative edges) of the FPGA are used. In this realization, the ADC ADS5240 runs with a sampling frequency of 25 MHz. This high sampling frequency in conjunction with a resolution of 12 bit results in a serial data rate of 300 Mbit/s. To handle such high data rates inside of the FPGA, care has to be taken with the signal timing. Therefore, defined timing and routing constraints are needed for a successful implementation, which requires a detailed knowledge of the FPGA slices. Special attention has to be provided to the

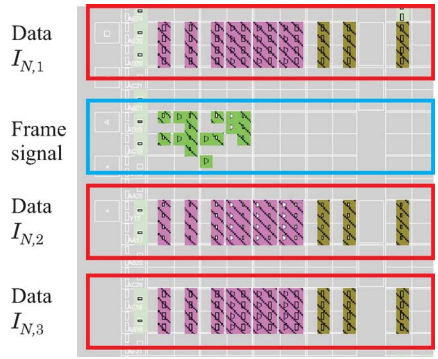

Fig. 10. Resulting placement of the ADC interface (current inputs) in the Xilinx FPGA (implementation C2).

TABLE III
SUMMARY OF THE ADC INTERFACE IMPLEMENTATION IN THE FPGAS

	Slices	$f_{clk,max}$
C1 (ECP2-LFE2-12E)	43	180 MHz
C2 (XC4VLX25)	47	248.16 MHz

generation of the *Ena_Mux* signal, since there, from the FPGAs point of view, the asynchronous signals are matched together to form one data word. The resulting routing of the interface is shown in Fig. 10.

In an FPGA, data and clock inputs show slightly different delays, and therefore, the phase of the clock signal has to be adjusted dynamically. Special clock management blocks are available inside of the FPGA for that purpose. But, unfortunately, it has been found that this clock management block does not work well in the desired frequency range although the frequencies still fulfill the specifications. Therefore, this phase adjustment is not implemented, and as a result, the maximal sampling frequency is limited to 25 MSa/s (although the maximal sampling frequency of the ADC is 40 MSa/s).

Compared to the simple SPI interface, the LVDS implementation requires much more detailed knowledge of the used FPGA but offers very high data rates and a small delay between sampling instant and availability of the data. A summary of the used logic cells and achieved timing is given in Table III.

B. Controller Implementation

The controller given in (1) yields to the control algorithm

$$\begin{aligned} e[n] &= i_{\mathrm{ref}}[n] - i_{\mathrm{meas}}[n] \\ u[n] &= K\left(e[n] - k_1 e[n-1]\right) + k_2 u[n-1] \\ d[n] &= u[n] + d_{\mathrm{ff}}[n] + i_{\mathrm{ff}}[n] \end{aligned} \tag{7}$$

where $d_{\mathrm{ff}}[n]$ and $i_{\mathrm{ff}}[n]$ are the voltage and current feedforward parts. There are several possibilities to realize this control algorithm inside of an FPGA. A realization of a 12×12 bit multiplication using normal logic units of the FPGA is possible, but requires a large number of logic cells and shows a limited timing capability. Alternatively, the multiplications can be avoided by application of shift operators, but then the possibilities of

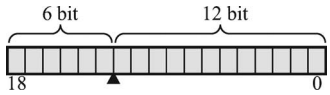

Fig. 11. Fractional number representation of K, k_1, and k_2 in the FPGA.

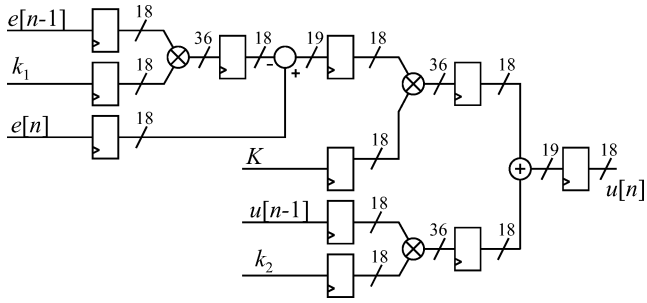

Fig. 12. Implementation of the P + lag current controller for one phase in the FPGAs using the HW multipliers of the FPGA. All the multipliers are pipelined by registers for highest possible throughput.

choosing K, k_1, and k_2 are limited. To overcome this limitation, modern FPGAs offer so-called DSP blocks that include hardware multipliers. These multipliers are able to process an 18×18 bit (signed) multiplication in one cycle and offer additional functionality such as multiplication and addition or multiplication and accumulation. These blocks are typically able to run with clock frequencies of over 300 MHz, if all multiplier stages are pipelined. For the controller implementation, these blocks are used. The DSP blocks can be targeted in a number of ways, where the most promising way is provided by upcoming tools, which allow the system design using MATLAB SIMULINK, and the design is automatically converted into HDL code. Unfortunately, these tools are currently only applicable for low clock frequencies, and therefore, the DSP blocks are directly inferred by VHDL code.

In a first step, after getting the data from the ADC, the data has to be transferred from binary offset to two's complement number representation. This can be made by a simple inversion of the most significant bit of the ADC data word. An 18-bit signed number representation is used in the FPGA because of the required 18 bit numbers for the DSP blocks, but the 12-bit range is not extended to 18 bit. On the one hand, this has the advantage that no overflows can occur. On the other hand. accuracy is given away. For the controller constants K, k_1, and k_2, a fractional number representation, as given in Fig. 11, is used. After the multiplication, the remainder is discarded.

The implementation of the controller in an FPGA differs from an implementation in a DSP, because all calculations are implemented in parallel in the FPGA. However, this does not mean that enable signals have to be generated for every block. As an example, the implementation of the P + Lag current controller of (7) using the HW multipliers is shown in Fig. 12. For a high-frequency implementation, it is very important that all stages are pipelined. According to Fig. 12, the result $u[n]$ is valid after 5 clock cycles and it only has to be ensured that the result is not used for PWM generation before these 5 clock cycles are completed.

TABLE IV
SUMMARY OF THE PWM IMPLEMENTATION IN THE FPGAS

	Slices	$f_{clk,max}$
C1 (ECP2-LFE2-12E)	232	253.16 MHz
C2 (XC4VLX25)	712	255.36 MHz

Since the controller implementation is more or less the same in the two FPGAs, no comparison will be made for this part. The delay of the full current controller is 128 ns for both implementations and is much smaller than the calculation time of a DSP realization (e.g., 1 μs in the realization presented in [6]).

C. PWM Generation

For implementation of the digital PWM of Section III, a clock frequency of 250 MHz is used. A higher clock frequency is not possible even with the high-speed FPGA of implementation C2.

1) Implementation C1: For this implementation, the counter/comparator approach without phase shift is used. Unfortunately, this results in a PWM resolution of only 7 bit at a switching frequency of 1 MHz. For the implementation of the required 7-bit high-speed counters, the VHDL data-type *std_logic_vector* has to be used, because it is much faster than the VHDL data-type *integer*. For each modulator, an own counter is used, which further increases the speed. It has to be said, that a detailed statement about maximal clock frequency of the implementation can only be given if the whole system is fixed by routing constraints; otherwise, the timing is influenced by other system parts. For the realization at hand, only timing constraints are used although the results of the implementation are given in Table IV.

2) Implementation C2: For C2, the resolution is increased to 8 bit by implementation of the proposed PWM concept. The 180° phase-shifted 250 MHz clock is generated by the DCM of the FPGA. Here, the two phase-shifted modulators have to be treated as asynchronous signals in the FPGA so that adding timing and routing constraints to the FPGA design is essential. Special attention has to be paid to the connection of the modulators' output to the multiplexer and further on to the output pin, because the multiplexer has no register. This means that different delays of these signal paths directly result in a phase difference of the two PWM signals. Unfortunately, there exists no timing constraint to define the same routing delay for several signal paths. Therefore, manual placement of the output register and multiplexer has to be opted for instead. With that, delay differences under 50 ps could be achieved. A drawback of the proposed PWM concept is that glitches of the multiplexer can occur. But, in the desired application, several "slow" components (optocoupler, gate driver) would absorb these glitches. For lower switching frequencies (e.g., $f_s = 500$ kHz), the duty cycle can be updated twice a period to minimize the delay of the PWM modulator.

TABLE V
REPORT SUMMARY OF THE CONTROLLER IMPLEMENTATIONS

	C1 (ECP2-LFE2-12E)	**C2** (XC4VLX25)
DSP-block utilization	87 %	68 %
Logic utilization	25 %	10 %
Clock management	50 %	40 %
I/O Pins	41 %	8 %

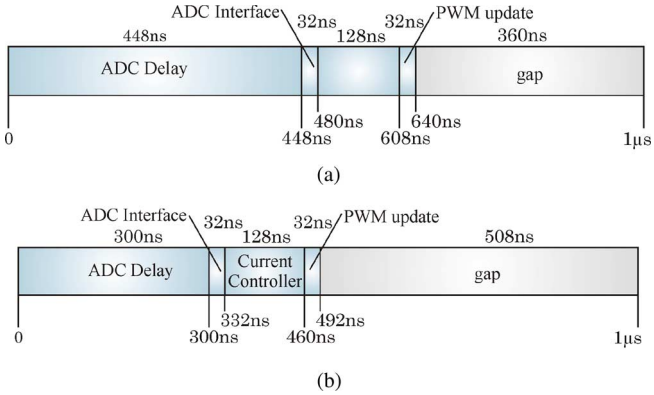

Fig. 13. Resulting timings of (a) current controller implementation C1 and (b) current controller implementation C2 for a switching frequency of 1 MHz.

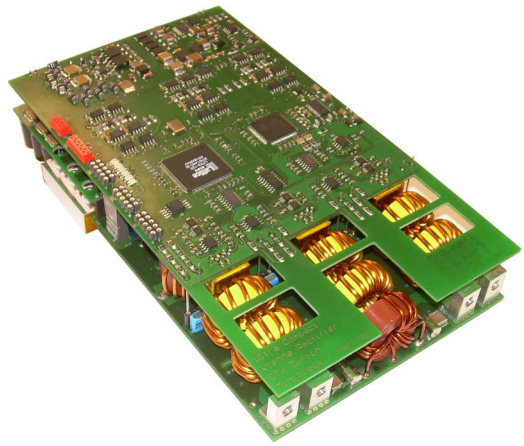

Fig. 14. Picture of the realized VIENNA rectifier prototype designed for a power level of 10 kW with controller implementation C1.

D. Summary of the Implementation

The two designs have been successfully fitted into the two FPGAs. A summary of the report is given in Table V. The utilization of the DSP blocks (one DSP block contains several multipliers) of 68% and 87% means, in practice, nearly a full usage, because there are some mapping limitations of the multipliers into the DSP blocks that inhibit a usage of 100%. In contrast to the utilization of the DSP blocks, only a small amount of the available logic cells and I/O pins are used for the controller implementation. This clearly illustrates that the speed of the FPGA is needed and not its size. The resulting timings of the implementations for a switching frequency of 1 MHz are depicted in Fig. 13. The biggest part of the processing time is the

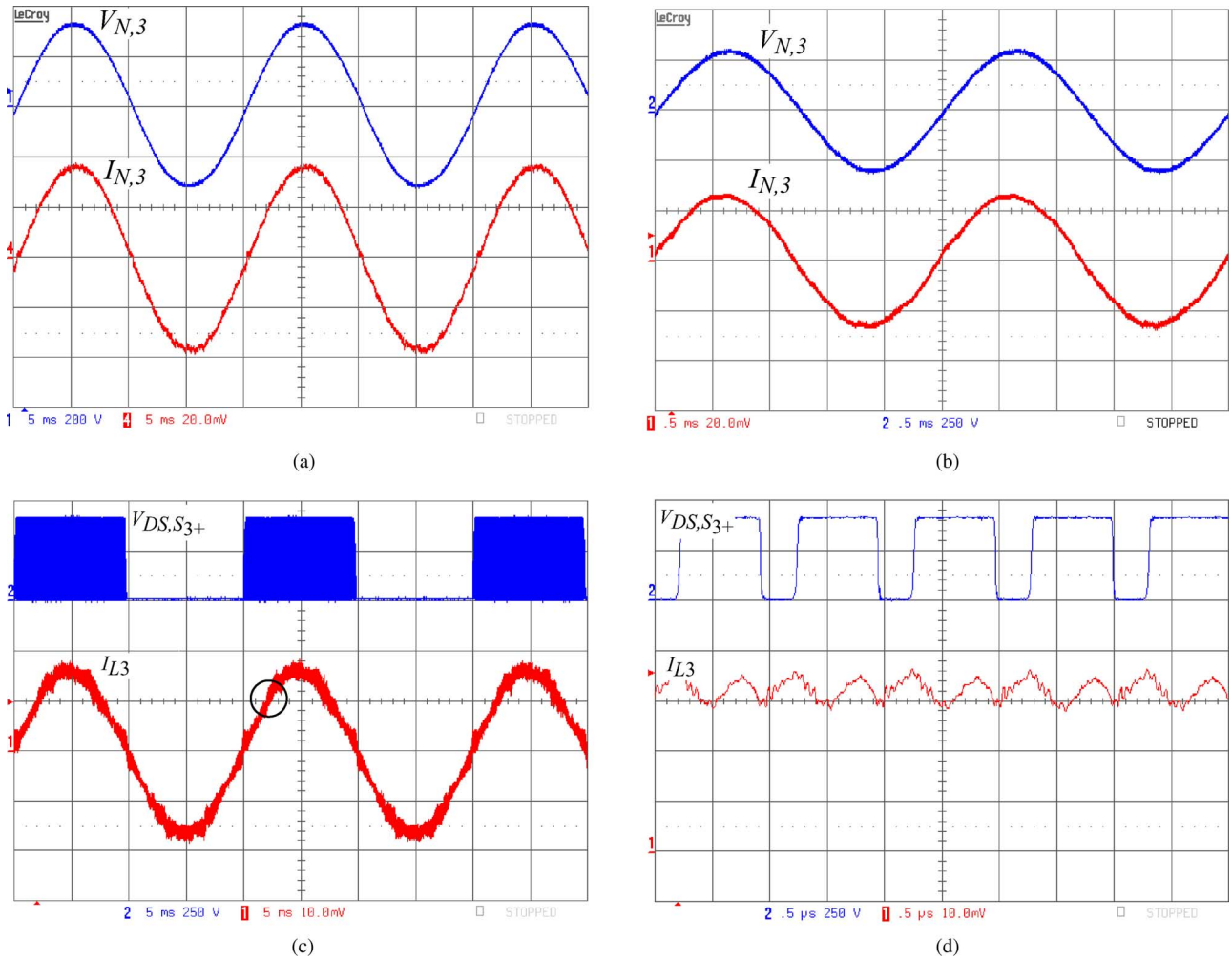

Fig. 15. Measurement results taken from the realized VR laboratory prototype employing controller implementation C1. (a) Input current $I_{N,3}$ at a mains frequency of $f_N = 50$ Hz and an output power level of $P_o = 9.6$ kW. Ch1: 200 V/Div, Ch4: 10 A/Div; timebase: 5 ms/Div. (b) $f_N = 400$ Hz, $P_o = 5.8$ kW. Ch1: 10 A/Div, Ch2: 250 V/Div; timebase: 0.5 ms/Div. (c) Drain–Source voltage $V_{\mathrm{DS,S3+}}$ and corresponding inductor current I_{L3} at $f_N = 50$ Hz and $P_o = 4.2$ kW; Ch1: 5 A/Div, Ch2: 250 V/Div; timebase: 5 ms/Div. (d) Detail of current ripple Ch1: 2 A/Div, Ch2: 250 V/Div; timebase: 500 ns/Div. As typically for three-phase rectifier systems, the current ripple is not only affected by the switching actions of the corresponding phase, but also by the switching actions of the two remaining phases.

ADC delay, even if a pipelined ADC with a sampling frequency of tens of megahertz is used. The second largest part of delay is introduced by the controller implementation caused by pipelining of all the multiplier stages. According to Fig. 13(b), the controller implementation C2 is able to handle switching frequencies of 2 MHz.

V. Experimental Results

To verify the function of the implemented digital current controller, a laboratory prototype of a VR according to the following key specifications has been constructed (cf., Fig. 14):

1) input voltage: $v_{N,i} = 230\ \mathrm{V_{rms}}$;
2) input frequency: $f_{\mathrm{in}} = 50/60$ Hz, 360–800 Hz (different controller gains required);
3) output voltage: $V_o = 800\ \mathrm{V_{dc}}$;
4) output power: $P_o = 10$ kW;
5) switching frequency: $f_s = 1$ MHz;
6) boost inductance: $L = 20\ \mu$H.

Due to the large effort to realize the controller for the three-phase VR prototype, only one controller implementation is realized for the VR prototype. In this prototype, the controller implementation C1 is used for the VR's current controller, which is sufficient for a switching frequency of 1 MHz. Therefore, six external A/D converters are required for input current and input voltage measurement. The system is operated at a switching frequency of 1 MHz and the duty cycle of the PWM is updated once every PWM period. With the control parameter $K = 0.25$, $k_1 = 0.96$, and $k_2 = 0.99$, a phase margin of 45° is achieved for the current controller. In Fig. 15, measurement results taken from the VR prototype at different line frequencies are shown. In Fig. 15(a), the input current $I_{N,3}$ and input voltage $V_{N,3}$ are plotted for a line frequency of $f_N = 50$ Hz and an output power of $P_o = 9.6$ kW ($V_{N,\mathrm{ll}} = 400\ \mathrm{V_{rms}}$, $V_o = 800\ \mathrm{V_{dc}}$). The system exhibits a $\mathrm{THD_I}$ of 1.4 % and power factor of 0.999. Fig. 15(b) shows measurement results at a line frequency of 400 Hz and an output power of $P_o = 5.8$ kW ($V_{N,\mathrm{ll}} = 400\ \mathrm{V_{rms}}$, $V_o = 800\ \mathrm{V_{dc}}$), where a $\mathrm{THD_I}$ of 2.4% can be measured, which

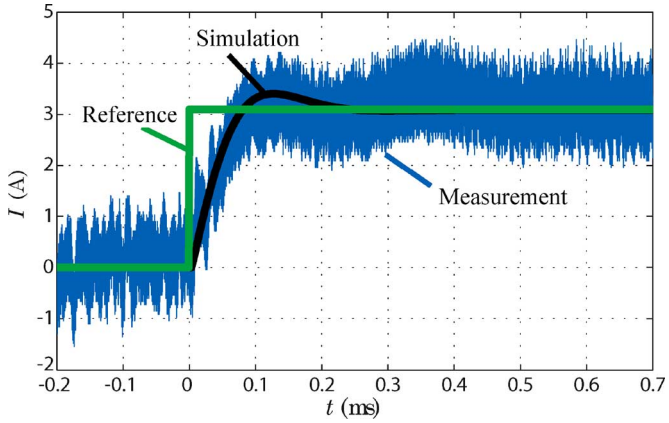

Fig. 16. Measured step response of implementation C1 to a current step of 3 A compared to the simulated step response.

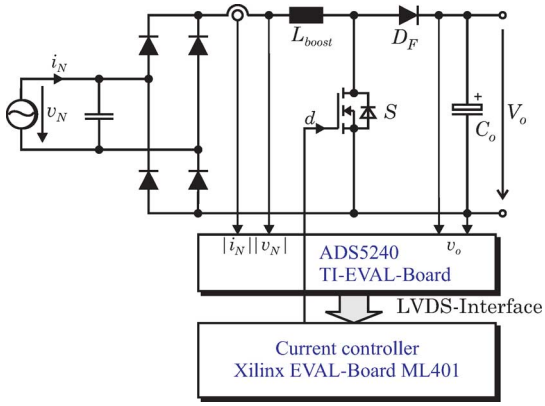

Fig. 17. Structure of the single-phase test system to test the controller implementation C2.

confirms the very good performance of the implemented current controller. As already discussed in Section III, a better input current quality is inhibited by the turn-OFF delays of the MOSFET switches whose influence rises at higher switching frequencies.

Measurements of the inductor current ripple I_{L3} and the drain–source voltage of switch S_{3+} are shown in Fig. 15(c) and (d). The switch S_{3+} is only modulated at positive input currents and is permanently ON at negative input currents. As is typically the case for three-phase rectifier systems, the current ripple is not only affected by the switching actions of the corresponding phase, but also by the switching actions of the two remaining phases. This results in a current ripple with not only primary frequency components at the switching frequency, but also at twice the switching frequency. According to Fig. 15(d), the duty cycle of the switch S_{3+} does not vary significantly, thus confirming the proper operation of the controller. In Fig. 16, the measured inductor current step response to a step of 3 A is shown together with the simulated step response. The current reference of the three-phase current controller signal is created by a step in the conductance g_e, which, in normal operation, is modulated by the much slower output voltage controller. The step responses are in good agreement, but the measured current shows slightly underdamped behavior.

As mentioned earlier, controller implementation C2 was not used for the realization shown in Fig. 14, although in order to be able to test the controller implementation C2, an existing single-phase PFC prototype with the following key specifications was used in combination with the TI-evaluation board ADS5240 (realization of A/D-converter) and the Xilinx evaluation bard ML401 employing the Virtex4 FPGA (cf., Fig. 17):

1) input voltage: $v_{N,i} = 230\ \mathrm{V_{rms}}$;
2) input frequency: $f_{\mathrm{in}} = 50/60$ Hz;
3) output voltage: $V_o = 400\ \mathrm{V_{dc}}$;
4) output power: $P_o = 3$ kW;
5) switching frequency: $f_s = 150$ kHz;
6) boost inductance: $L = 200\ \mu$H.

For that purpose, the controller structure of implementation C2 has not been changed; only, the internal clock frequencies have been reduced to handle the lower operating frequency. According to Section IV, timing analysis of the implementation C2 using the Xilinx design tools verified that an implementation is possible employing the Virtex4 FPGA for switching frequencies up to 2 MHz. However, the implemented system is tested with a switching frequency of 150 kHz. A measurement of the input current at $P_o = 1.5$ kW is plotted in Fig. 18(a). In Fig. 18(b), the measured step response of the current controller is compared to the simulated step response of the designed current controller, where both responses are in good agreement.

The behavior of the proposed DPWM is tested using the evaluation board. The PWM has a frequency of 1 MHz and all three PWM channels are programmed for test purposes to a fixed duty cycle only differing in 1 bit. According to Fig. 19, a PWM value of $d = 50$ results in a pulsewidth of 200 ns for an 8 bit PWM with a maximum countervalue of 125. A PWM value of $d = 51$ results in a pulsewidth of 204 ns, and for $d = 52$, a pulsewidth of 208 ns can be measured. This confirms that a symmetrical PWM with a resolution of 4 ns has been realized.

The question arises if it is really necessary to have the current controller output updated with the switching frequency of 1 MHz, as shown in Fig. 3, or if a current controller operating at 500 kHz combined with a switching frequency of 1 MHz (PWM output updated every second period) would be sufficient. On first considerations, it seems that the controller bandwidth, given in Fig. 5, is more than high enough for a 50 Hz line frequency. However, simulations show that the current ripple would be approximately 10% higher for a 500 kHz current controller, and therefore, the size of the boost inductor and of the EMI filter have to be increased in order to fulfill the given design specifications. From the control side of view, a larger delay time is introduced in the control loop if the PWM modulator is updated every second period. Therefore, the phase margin of the control loop is reduced from 45 to 36°. In order to achieve the same phase margin as the controller with an update rate of 1 MHz, the controller gain has to be reduced approximately by a factor of two. This was tested on the existing prototype at an output power level of 4.1 kW and the $\mathrm{THD_I}$ increased from 2.2% (update rate 1 MHz) to 3.1% when the output was updated with 500 kHz. Hence, one has to be aware, that a combination of a switching frequency of 1 MHz and a controller update of

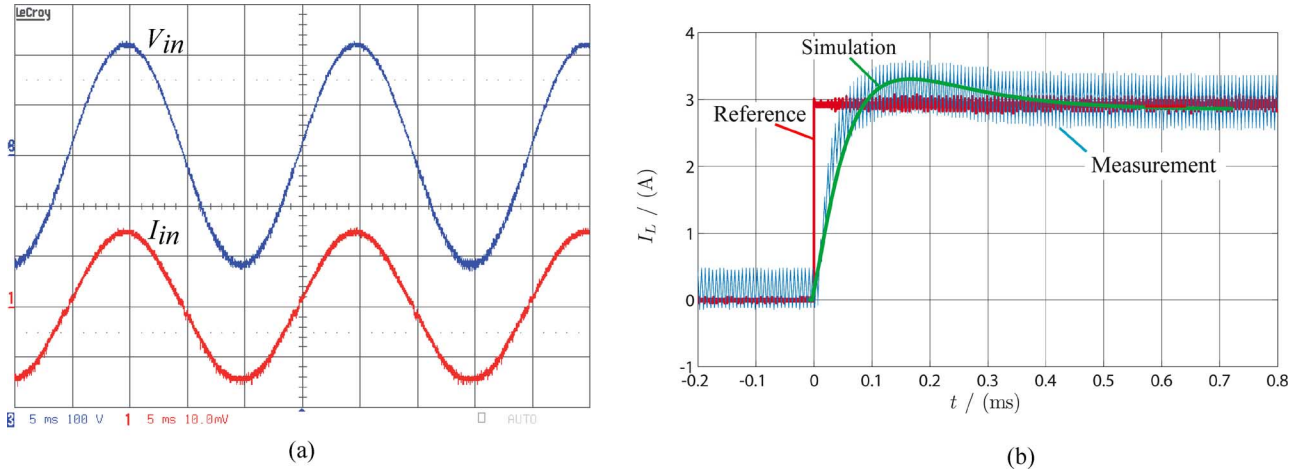

Fig. 18. Measurements taken from the single-phase PFC employing the controller implementation C2. (a) Input current and input voltage at a line frequency of $f_N = 50$ Hz and a power level of $P_o = 1.5$ kW; Ch1: 5 A/Div, Ch3: 100 V/Div; timebase: 5 ms/Div. (b) Measured step response of the inductor current to a step of 3 A compared to the simulated step response of the current controller.

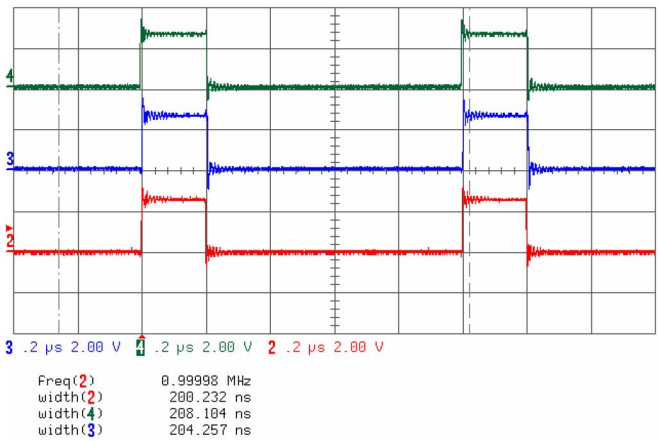

Fig. 19. Measurement result of the proposed PWM concept with a PWM frequency of 1 MHz and the PWM-values: Ch2 (2 V/Div): $d = 50$ (200 ns); Ch3 (2 V/Div): $d = 51$ (204 ns) and Ch4 (2 V/Div): $d = 52$ (208 ns); timebase: 200 ns/Div.

500 kHz results in higher switching losses and a reduced input current quality. If a high switching frequency is to be realized, the current controller should be fast enough to benefit from the high switching frequency.

VI. Conclusion

Two digital current controllers for a three-phase rectifier operating at 1 MHz have been successfully implemented by application of modern high-speed FPGAs. The entire signal chain, starting with the current measurement and ending with the PWM generation has been considered. The way to minimize the delay introduced by the A/D converter has been shown by application of two different high-speed A/D converter implementations. Implementation C1 uses an A/D converter with a sampling frequency of 1 MHz and a well-known SPI interface that results in an effective delay of 448 ns caused by the A/D converter. In contrast, implementation C2 uses a high-speed converter with a sampling frequency of 25 MHz and a high-speed LVDS interface reduces this delay to 300 ns. However, the implementation of this high-speed interface is much more complex and should only be used in cases where the SPI interface is not applicable anymore. A control model of the three-phase rectifier has been developed, which was used to design a digital current controller. All necessary steps to implement the controller in the FPGA have been discussed. For the implementation of the current controllers, DSP blocks of the FPGAs containing hardware multipliers have been used. An increased PWM resolution of 4 ns (8 bit at $f_s = 1$ MHz) with symmetrical pulse patterns has been achieved by application of an enhanced PWM generation, based on a phase-shifted counter/comparator approach. Therefore, timing and routing constraints are needed for a successful implementation in an FPGA, which, in turn, may require detailed knowledge of FPGA design. The good performance of the current controller is verified by measurements taken from a 10 kW rectifier prototype. For an input frequency of 50 Hz and an output power level of 9.6 kW, a $\mathrm{THD_I}$ of the phase currents of 1.4% has been measured, and even at an input frequency of 400 Hz, a $\mathrm{THD_I}$ of 2.4% could be achieved at an output power level of 5.8 kW.

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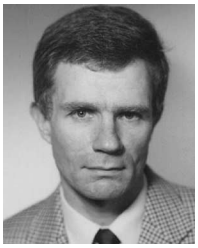

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