High Power Resonant Switched-Capacitor Step-Down Converter

Oliver Keiser*, Peter K. Steimer* and Johann W. Kolar**
*ABB Switzerland Ltd., Turgi, Switzerland
**Swiss Federal Institute of Technology, Zürich, Switzerland

Abstract–**This paper treats a new type of high power Switched-Capacitor-DC-DC-Converter (SCDDC), which is characterized by resonant switching transitions. This drastically reduces switching losses and opens up the possibility to employ thyristors instead of turn-off power semiconductors. At the same time a larger energy can be transferred per switching cycle and/or the application of the SCDDCs can be extended into the megawatt power range. For operation with high switching frequency thyristors are replaced by IGCTs which allow to avoid a turn-off time in reverse-blocking mode. The new converter topology is extensively analyzed using simulations. To gain practical results a small scale prototype is designed and the operation of the proposed converter is experimentally verified including the resonant operation of IGCTs which results in significantly reduced switching losses.**

I Introduction

For several years now, the switched capacitor concept has been applied for DC-DC voltage conversion (SCDCDC). Especially for power supplies of microcontrollers, processors, consumer electronics or mobile devices SCDCDC gained some popularity due to the simple design without inductors, which are still a drawback to have on mass produced printed circuit boards. Switched capacitor voltage converters are even available as an integrated CMOS chip from several manufacturers. A summary of the history of Switched-Capacitor Converters can be found in [1].

The major drawback of the topology used in these switched capacitor converters is the rather low efficiency, which makes the concept unattractive for high power applications. Traditionally, pump capacitors are charged and discharged by parallel connection to the input and output capacitor respectively. For high power applications this concept of course could not be maintained. Controlling the charging current of the switched capacitor by operating the switches in the forward-active region [2] is also not feasible because of resulting high power losses. All high power switches can only be operated in the full turn-on or turn-off state.

In [3] resonant switching has been introduced to increase efficiency of SCDCDC. Topologies were proposed for $\frac{1}{2}$-mode, $\frac{1}{3}$-mode and $\frac{1}{4}$-mode step-down converters as well as the corresponding step-up counterparts. Prototypes have been tested for up to 100 W.

While the former topologies are not controlled and/or the output voltage depends on the input voltage and the load, in [6] a duty ratio control was introduced in order to keep the output voltage stable at a desired level. The proposed method is only able to control the output voltage at one level, defined by the topology, for an input voltage variation of about 20%. This controllability is bought with relatively large switching losses, so ZCS, the main advantage of resonant converters, is not maintained. The concept therefore doesn't seem feasible for high power applications.

Another improvement in switched-capacitor converters has been observed in [7], where a new topology and switching regime lead to lower output ripples and lower current stress of the capacitors, which allows for use of lower capacitance values. This topology is intended for power levels below 1 W.

This paper describes modifications made to the SCDDC, by combining several advantages of the above mentioned topologies, and further development to make the concept suitable for output power levels in the MW range.

II Design

The basic aim of this project was to find a converter topology feasible for high output power with a focus on high current applications, as can be found with chemical processes. Such a converter has to be built with components available on the market today. The switched capacitor converter topology on which the research was based, is depicted in Fig. 1 [7]. There, the

978-1-4244-1668-4/08/$25.00 ©2008 IEEE

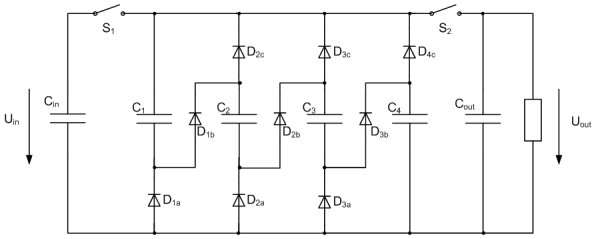


Figure 1: Basic switched capacitor topology

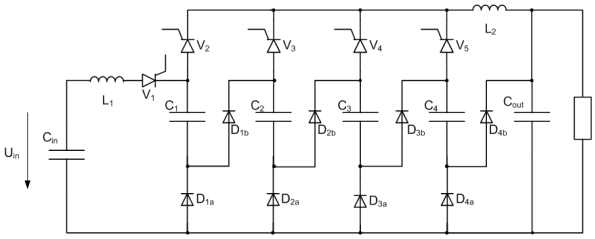


Figure 2: SCDDC with interleaved, resonant dis-/charging

pump capacitors are charged in series and discharged in parallel in order to have a large voltage conversion ratio from input to output. Starting from this topology, the following concepts were added:

- Resonant Switching
- Interleaved Discharge
- Extension of the Charge Pulse.

The resulting new topology is shown in Fig. 2 for the example of four pump capacitors.

Resonant switching is achieved by placing an inductor between capacitors that are connected in parallel. This inductor has a much smaller inductance than that of a comparable buck converter and can be realised with an air core, thereby not adding significant weight or losses. The advantage of resonant switching is, that the pump capacitors are charged and discharged nearly lossless and in a short time interval; furthermore, there are no turn-off switching losses.

Instead of discharging all pump capacitors simultaneously, the capacitors are discharged in interleaved manner. This reduces the current stress on the discharging switches and the output capacitor. Also, the output voltage ripple is significantly reduced. There are several possible discharge strategies which can be used to optimise the operation concerning different criteria.

Because the pump capacitors are alternately connected in series for charging and then discharged individually, individual inductors L_1 and L_2 have to be employed for charging and discharging.

A final improvement is achieved by adding two more diodes, D_{4a} and D_{4b}, to include the output capacitor in the charging path. Consequently there is one extra current pulse on the output capacitor. With this measures all current pulses occurring in steady state operation are equal, as can be seen in Fig. 3. There is one charging pulse and five discharging pulses, one from each pump capacitor, plus the forwarded charging pulse, so the output current is five times larger than the input current. To calculate the input to output voltage conversion ratio it is assumed that the input and output capacitors are large enough to keep the voltages constant. The following variables are used:

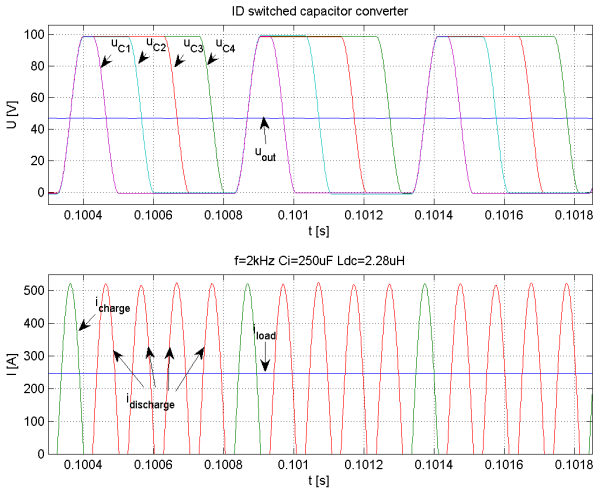


Figure 3: Waveforms of the circuit in Fig. 2

u'_C: voltage of a pump capacitor before charging
u''_C: voltage of a pump capacitor after charging
u'''_C: voltage of a pump capacitor after discharging
C_i: capacitance of a pump capacitor
n: number of pump capacitors
f: switching frequency

The path of the charging current for the example of $n = 4$ is shown in Fig. 4(a). For charging the following holds:

$$n\,u''_C = 2(V_{in} - V_{out}) - n\,u'_C \tag{1}$$

For discharging we have

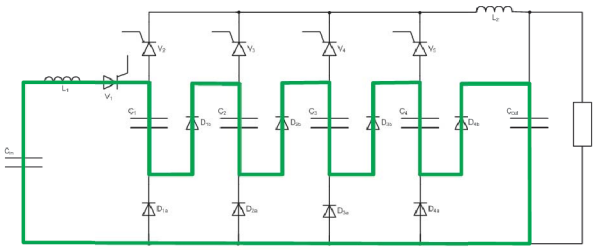
$$u'''_C = 2V_{out} - u''_C \tag{2}$$

In steady-state the initial and the final voltage of the pump capacitors are the same, i.e. $u'''_C = u'_C$. The only solution to these equations is

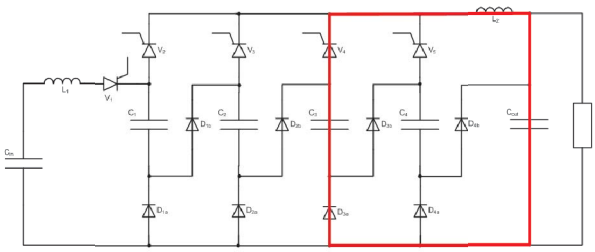
$$V_{out} = \frac{V_{in}}{n+1} \tag{3}$$

A sample discharging path can be seen in Fig. 4(b).

In this example the output voltage is five times smaller than the input voltage. Together with the current ratio the efficiency is theoretically $\eta = 100\%$. For a SCDDC without resonant switching the theoretical efficiency is much lower, e.g. $\eta = 85.7\%$ for a 48 W converter [7]. In practice, there are finite losses resulting

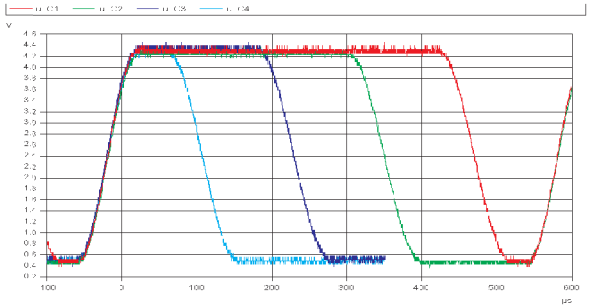


(a) charging

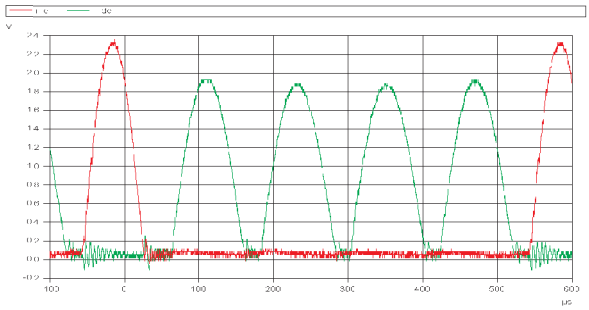


(b) discharging

Figure 4: Current path through the pump capacitors



(a) scale 20:1



(b) 5mV/A

Figure 5: Voltages on pump capacitors and currents in inductors

from forward voltages of the semiconductor and parasitic resistance of capacitors and inductors. However, since the current peaks are much smaller than in a traditional switched capacitor converter, these losses are marginal.

For maximal load of the converter, the pump capacitors are discharged to $u'_C = 0\,\mathrm{V}$. After charging their voltage is $u''_C = 2V_{out}$. The maximum load current therefore is

$$I_{load,max} = 10 V_{out}\, C_i\, f \tag{4}$$

If the load current decreases, there is a transient phase during which u_{out} is increasing for a couple of cycles. Since the voltage of the pump capacitors drops during discharge symmetrical below u_{out}, u'''_C is not zero anymore. In the next charging phase, similarly the voltage increases to $u''_C < 2V_{out}$. During the discharge phase, less energy is transferred to the output capacitor and u'''_C will again be higher than in the previous cycle and so forth. After a couple of cycles u'_C and u''_C will adjust to values supplying the same amount of energy to the output capacitor as the load draws at a constant V_{out}. Accordingly, after the transients the output impedance is $R_{out} = 0\,\Omega$ in quasi steady-state .

III Measurements

A prototype of the topology depicted in Fig. 2 was developed with an output power of 12.5 kW at a maximum load current of 250 A at 50 V (Fig. 7). For the pump capacitors `AVX FFVE` film capacitors with $C = 300\,\mu\mathrm{F}$ are used, whereas the input and output capacitors are electrolyte capacitors with $C_{in} = 16.5\,\mathrm{mF}$ and $C_{out} = 132\,\mathrm{mF}$ respectively. The switches are implemented with fast recovery thyristors (`Eupec TZ335F`) and the inductors are air coils ($L_1 = 8.2\,\mu\mathrm{H}$ and $L_2 = 2.2\,\mu\mathrm{H}$). In Fig. 5 the measured waveforms are shown. The switching frequency in this example is $f = 1.67\,\mathrm{kHz}$. With this setup the switching frequency cannot exceed $f_{max} = 2\,\mathrm{kHz}$ due to the minimum turn-off time required by the thyristors. A resonant pulse lasts $75\,\mu\mathrm{s}$ and the recovery time of a thyristor is $25\,\mu\mathrm{s}$, so for all five pump capacitors $T_{s,min} = 500\,\mu\mathrm{s}$. For higher switching frequencies thyristor 2 would fire before thyristor 1 has regained his forward blocking capability, i.e. thyristor 1 would turn on again, which would cause the input capacitor to fully discharge across L_1, L_2 and the load.

For a high power version, the thyristors therefore are advantageously replaced with IGCTs in order to avoid the recovery delay, which can be up to $600\,\mu\mathrm{s}$ for 6.5 kV thyristors and/or to allow higher switching frequencies.

IV Comparison of a RSCDDC vs. Buck Converters in MW Power Range

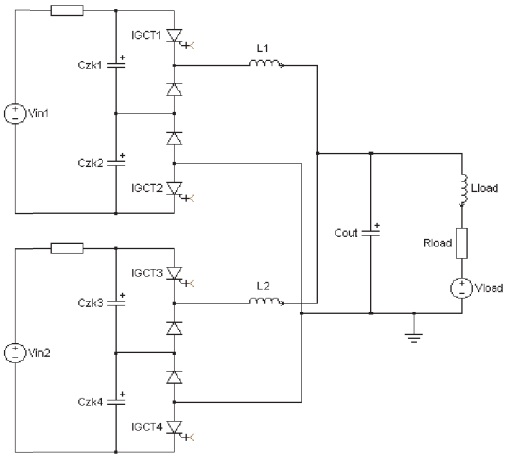
Loss calculations were done for a resonant SCDDC (RSCDDC) with an output power of 2.5 MW at 500 V and 5 kA, based on `ABB 5SHY 35L4512` IGCTs with `DYNEX DSF21545SV` free wheeling diodes. Thanks to resonant switching there are hardly any switching losses and due to using air coils there are no core losses

Element	Variable	Value	Unit
IGCT	$\hat{I}_T$	7.85	kA
	$I_{T,rms}$	2.48	kA
Pump capacitor	C_i	500	μF
	U_{max}	1000	V
	I_{rms}	3.51	kA
	f_1	20	kHz
Inductor	L_1	8.11	μH
	I_{rms}	2.48	kA
	L_2	2.03	μH
	I_{rms}	4.96	kA
DC link capacitor	I_{rms}	2.27	kA
	f_1	2	kHz
Output capacitor	I_{rms}	2.42	kA
	f_1	10	kHz

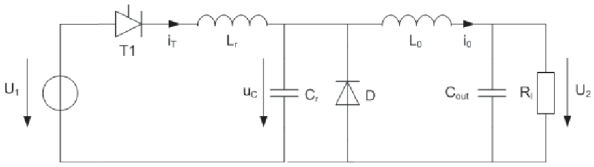
Table 1: Element specification of the RSCDDC

in the inductor. Such inductors with similar inductance and current ratings have been used in another ABB project, and therefore could easily be acquired. Capacitors with the necessary ratings cannot be found in the market as one element, but a solution is to connect several capacitors in parallel. Possible candidates are `AVX TRAFIM` or `Vishay Phao` series.

In Tab. 1 a summary of the calculated element specifications of the RSCDDC is given. Losses are compared



(a) 2cell-3level-buck converter



(b) resonant buck converter

Figure 6: Topology of two buck converters

to a traditional buck converter, with a two cell, three level topology and a resonant buck converter. The circuit topology of the two competitors is shown in Fig. 6. The same IGCTs and Diodes are used in all three converters.

While the 2-cell-3-level-buck converter has lower conducting losses due to lower current peaks, switching and inductor losses are substantially higher. This buck topology uses two inductors with large inductance. Because of the higher inductance coils with iron core are necessary. These inductors contribute a big part to the total weight of the converter, while the weight of the air coils of the RSCDDC is lower by a factor 20 – 40.

The resonant buck converter (RBC) has very few semiconductors, one IGCT and one diode. Because the employed IGCT is asymmetric, another diode has to be added in series. To ensure a fair comparison to the other two topologies, two semiconductors are placed in parallel per logical one. No more than two IGCTs are taken in parallel, because small asymmetries in the semiconductors would see the fastest two conducting a main share of the current. Therefore, a higher number of switches would not reduce the total losses much further and/or is not worth the extra expenses. Due to the function of this converter, a high peak current flows through the IGCT in the resonance phase, as it has to be somewhat larger than two times the output current to ensure ZCS. $\hat{i}_T = 2.5 I_{out}$ can be considered a safe value and also allows for ZCS in transient conditions. Conduction losses in the RBC are smaller than in the other two topologies, but considering the small semiconductor count it is still relatively high. Since the whole output current has to flow through the inductor, large losses are generated there due to the parasitic resistance. No switching losses are occurring in the IGCT and the freewheeling diode, only the diode connected in to the IGCT exhibits reverse recovery losses, as it has to instantly block a reverse voltage after the current zero-crossing.

Losses in the capacitors are not included in these calculations. High power capacitors are usually custom designed and data of the parasitic resistance is not generally available. Furthermore DC-link and output capacitors have a large number of degrees of freedom, only the maximum voltage and ripple are a design requirement. More expensive capacitors usually have a smaller parasitic resistance. Measurements with the medium power experiment showed, that capacitor losses contribute only make up a very small part of the total losses, so it is justified not to include them in the loss calculations for the high power case.

Table 2 shows a summary of the encountered losses.

In the RSCDDC the conducting losses can be further reduced by combining IGCTs and thyristors. Only for the critical transitions between switches there is a need of IGCTs to immediately block forward voltages.

[1] 3 level 2 cell buck converter

Figure 7: Picture of the prototype

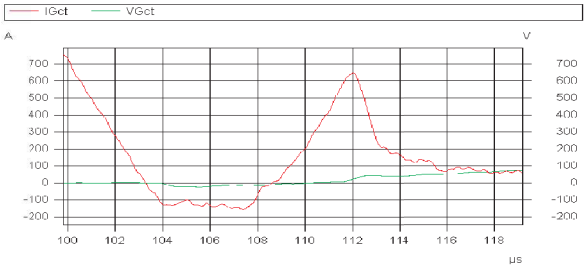
Type of losses	RSCDDC	312cB [1]	RBC
Conducting	37.3 kW	18.9 kW	12.2 kW
Switching	0.24 kW	17.4 kW	0.16 kW
Inductor	7.87 kW	20.5 kW	45.4 kW
Total	45.4 kW	56.8 kW	57.8 kW
Efficiency η	98.22%	97.78%	97.69%

Table 2: Converter losses

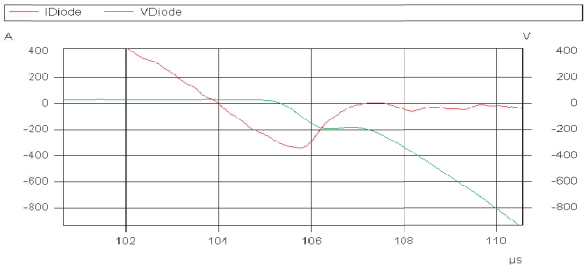
Many transitions are not critical and thyristors can be employed, which have considerably better conducting characteristics.

V Behaviour of IGCTs under Resonant Switching

All semiconductors are operated under resonant switching regime, so theoretically there are no switching losses. In practice the situation is slightly different. An experiment with the same conditions as encountered in the high power RSCDDC was conducted, measurements are shown in Fig. 8. As mentioned before, reverse recovery losses are occurring for the diodes. Asymmetric IGCTs are employed in this design as only this type of devices are showing a large enough current handling capability. This infers that all IGCTs have to be accompanied by diodes. At the current zero-crossing, the diodes are immediately blocking the reverse voltage, so u_{CE} of the IGCT stays at 0 V. Now the excess carriers in the diode are swept out by the reverse voltage and since this current is also flowing through the IGCT, the amount of excess carriers is decreased, but still stays at a high level, since a higher charge is stored in the IGCT than in the diode.



(a) IGCT



(b) Diode

Figure 8: Resonant turn-off of IGCT and series diode

After a delay of about $2.5\,\mu$s from the instant the turn-off signal is sent to the IGCT, the gate-drive circuit starts to sweep out the remaining excess carriers of the lowest p and n region. Within $< 0.5\,\mu$s the cathode pn junction is free of excess carriers and the recovery current has decayed to zero. At this point there is still a positive voltage on the capacitors of the gate circuit and the cathode pn-junction is in blocking state, so no current can flow there. The anode pn-junction is not affected by the gate-drive circuit and stays forward biased the whole time, which slows down the excess carrier recombination. Due to the operation regime, the IGCT has to start blocking as soon as a forward voltage is applied. Since there are still excess carriers present, a forward recovery current pulse can be observed.

This effect puts a limit to the switching frequency. With higher frequencies, the $\frac{\mathrm{d}i}{\mathrm{d}t}$ before turn-off is larger, which implies that more excess carriers are existing at zero-crossing. The forward voltage also appears sooner with higher frequencies, so less excess carriers have recombined, which means that the forward recovery pulse is higher, leading to higher losses.

VI Limitations of the Resonant SCDDC

The RSCDDC is not a universal converter, but adapted for a specific environment. An example for its use are applications, which require high currents in the low voltage region, as can be found in the chemical industry. These applications typically need current regulation, however the RSCDDC cannot do this.

Furthermore, the concept of regulation with a variable duty ratio is not applicable to the RSCDDC. The duration where the source or any of the switched capacitors is transmitting energy is fixed by the resonant frequency. The switching frequency can theoretically be reduced, which would add breaks after each resonant pulse. The only effect of this is that there is a larger voltage ripple on the output capacitor, which in turn leads to larger voltage ripples on the switched capacitors, so each one would transmit more energy per pulse. In the end the average output voltage would still be the same, only with larger ripples. The overall efficiency of the RSCDDC would be reduced in this operation. Because of all this disadvantages, this operating mode is not considered.

VII Conclusion & Outlook

In this paper the topology of SCDCDC converters was modified to create resonant circuits which transfer energy almost lossless due to zero-current-switching (ZCS) in contrast to high losses of conventional SCDCDC systems.
Although this improvement requires to employ inductors in the design, the main element of energy storage is still the pump capacitor. Unlike in a buck converter, where there is always energy stored in the inductor, in the RSCDDC the inductor only stores energy for the transfer between capacitors and within $100\,\mu$s it has completely passed on all its energy. Due to this different application, the inductance is two decades smaller than that of an inductor in a buck converter with the same power rating.

The new topology was tested in simulation and an experimental system of 12.5 kW output power was developed which showed an efficiency of 89%. The majority of the losses of this converter are occurring in the semiconductors due to the forward voltage drop V_{T0} and V_{D0}. Due to the relatively large number of semiconductors in a RSCDDC topology the efficiency is not very high at low voltages. If the voltage is increased, the absolute losses stay constant and therefore relative losses can be reduced.

To verify the feasibility of an application of the new topology in the megawatt range, a comparison between a RSCDDC, a resonant buck converter and a 3-level 2-cell buck converter was performed. Concerning overall efficiency the SCDDC won with 98.22% against the buck converters. The advantage of the RSCDDC is the demand of smaller inductors at the price of more capacitors.

To find out how the employed IGCTs behave during resonant switching, a setup was created for tests under high power conditions. The results showed that there are very low switching losses if the IGCTs are operated under conditions given in the RSCDDC.

A topic of further research is the controllability of the output voltage. A concept that works with the same hardware setup and only requires a change in the control software is the deactivation of some pump capacitors by changing the charging current path. With this measure a selection of discreet output voltage levels becomes available. A possible extension is to dynamically change the number of active capacitors, therefore enabling the output voltage to cover a continuous range.

References

[1] A. Ioinovici, "Switched-capacitor power electronics circuits", Circuits and Systems Magazine, pp. 37–42, Third Quarter 2001.

[2] H. Chung, "Design and analysis of a switched-capacitor-based step-up DC/DC converter with continuous input current", IEEE Transaction on Circuits and Systems, vol. 46, pp. 722–730, June 1999.

[3] Y. P. Benny Yeung, K. W. E. Cheng, S. L. Ho, K. K. Law, D. Sutanto, "Unified analysis of switched-capacitor resonant converters", IEEE Transaction on Industrial Electronics, vol. 51, pp. 864–873, August 2004.

[4] K.K. Law, K.W.E. Cheng, Y.P.B. Yeung, "Design and analysis of switched-capacitor-based step-up resonant converters", IEEE Transactions on Circuits and Systems, vol. 52, pp. 943–948, May 2005

[5] A. Ioinovici, C.K. Tse, H.S.-H. Chung, "Comments on "Design and analysis of switched-capacitor-based step-up resonant converters", IEEE Transactions on Circuits and Systems, vol. 53, p. 1403, June 2006.

[6] D. Qiu, B. Zhang, Ch. Zheng, "Duty ratio control of resonant switched capacitor DC-DC converter", Electrical Machines and Systems, vol. 2, pp. 1138–1141, September 2005.

[7] J. Han, A. v. Jouanne, G. C. Temes, "A New Approach to Reducing Output Ripple in Switched-Capacitor-Based Step-Down DC-DC Converters", IEEE Industry Applications Conference, vol. 2, pp. 1115–1120, October 2004.

[8] F. da Silveira Cavalcante, J. W. Kolar, "Small-signal model of a 5kW high-output voltage capacitive-loaded series-parallel resonant DC-DC converter", IEEE Power Electronics Specialists Conference, pp. 1271–1277, June 2005.

[9] M. Shoyama, T. Naka,T. Ninomiya, "Resonant switched capacitor converter with high efficiency", IEEE Power Electronics Specialists Conference, vol. 5, pp. 3780–3786, June 2004.

[10] Q. Deng, "Comparing regulated charge-pump and inductor-based DC/DC converters", Bodo's Power Systems, pp. 42–44, August 2007.

[11] N. Mohan, T. M. Undeland and W. P. Robbins, *Power electronics: converters, applications and design*, John Wiley & Sons Inc, New York, USA 2003.