

Impact of Power Density Maximization on Efficiency of DC–DC Converter Systems

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Abstract—The demand for decreasing costs and volume leads to a constantly increasing power density of industrial converter systems. In order to improve the power density, further different aspects, like thermal management and electromagnetic effects, must be considered in conjunction with the electrical design. Therefore, a comprehensive optimization procedure based on analytical models for minimizing volume of dc–dc converter systems has been developed at the Power Electronic Systems Laboratory of the Swiss Federal Institute of Technology (ETH Zurich). Based on this procedure, three converter topologies—a phase-shift converter with current doubler and with capacitive output filter and a series–parallel resonant converter—are optimized with respect to power density for a telecom supply (400 V/48 V). There, the characteristic of the power density, the efficiency, and the volume distribution between the components as functions of frequency are discussed. For the operating points with maximal power density, the loss distribution is also presented. Furthermore, the sensitivity of the optimum with respect to junction temperature, cooling, and core material is investigated. The highest power density is achieved by the series–parallel resonant converter. For a 5-kW supply, a density of approximately 12 kW/L and a switching frequency of ca. 130 kHz are obtained.

Index Terms—DC–DC power conversion, optimization, phase-shift converter, power density, resonant converter.

I. INTRODUCTION

THE POWER density of power electronic converters has roughly doubled every ten years since 1970. Propelling this trajectory has been the increase of converter switching frequencies by a factor of 10 every decade, due to the continuous advancement of power semiconductor device technology. This increase in power density has been especially important in the design of telecom power supplies that have to operate in a limited space and have maximum weight requirements.

In the near future, the short-term operating costs of telecom power supplies will outweigh their capital cost. Along with the high operating cost, due to rising energy prices, the negative environmental effects of increasing energy consumption will demand power supplies with the highest possible efficiency. Therefore, an optimization of power supplies with respect to power density and efficiency for future “Green Data Centers” [1], which enables a reduction of cost and cooling effort, is required. The main question that arises is, “to what extent

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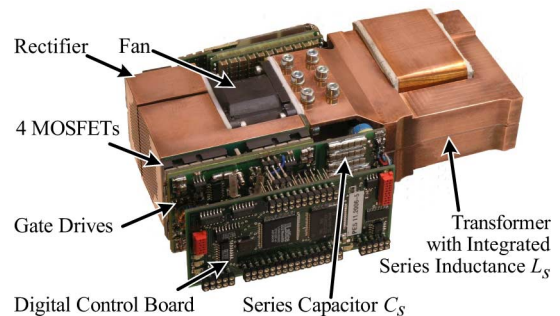


Fig. 1. Prototype of an optimized series–parallel resonant converter for telecom applications with a power density of 10 kW/L and the specification given in Table I.

does a power density optimization influence the efficiency of the converter system?” In order to address this question, an optimization of the converter design is required.

Modern power supply design must consider thermal issues (thermal interfaces, heat distribution, and fluid dynamics) and electromagnetic effects (parasitic elements, electromagnetic coupling, HF-losses, and electromagnetic interference (EMI) filtering) in conjunction with the electrical design since all these areas significantly influence the size and efficiency of the system. Therefore, an automatic optimization procedure is applied in this paper to maximize efficiency and/or power density. With this procedure, the efficiency, the power density, and their mutual influence on two widely used telecom power supply concepts, i.e., a resonant converter and a phase-shift converter with capacitive/inductive output filtering, are investigated.

The optimization procedure is based on analytic approaches with sufficient accuracy but limited calculation effort instead of general finite-element method (FEM)/computational fluid dynamics (CFD) simulations in order to limit the calculation time. Consequently, analytical models and equations, which include the magnetic devices, zero-voltage switching (ZVS)/zero-current switching (ZCS) losses, and HF-losses in the integrated transformer, have been derived and validated for the two converter types. Moreover, thermal models for the transformer/inductor with integrated cooling system and models for the volume of the required cooling system including fan have been developed [2], [3]. The optimization procedure also includes methods for calculating the volume of the resonant and output capacitors.

Based on this procedure, power supplies (cf., Fig. 1) are optimized with respect to power density for the parameters given in Table I. There, the characteristic of the power density, the efficiency, and the volume distribution between the

TABLE I
SPECIFICATIONS OF THE TELECOM POWER SUPPLIES CONSIDERED IN THE OPTIMIZATION PRESENTED IN THIS PAPER

Input voltage	400 V
Input current	13.0 A
Output voltage	54 V
V_{Ripple} at Output	300 mV _{pp}
Output current	92.6 A
Output power	5 kW
Maximum ambient temp.	45 °C

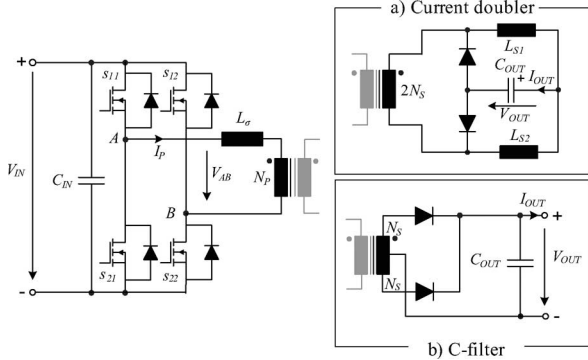


Fig. 2. Schematic of the phase-shift converter with (a) CDR and (b) capacitive output.

components as functions of frequency are discussed. For the operating points with maximal power density, the loss distribution is also presented. Furthermore, the sensitivity of the optimum with respect to junction temperature, cooling, and core material is investigated.

Before the optimization procedure is presented in Section III, the current and voltage waveforms of the three topologies and the main differences are explained in Section II. In Section IV, the models applied in the optimization procedure are briefly described. Thereafter, the results of the optimization and comparison of the topologies are presented in Section V, and the two converter concepts are compared with respect to the maximal achievable power density and efficiency.

II. CONVERTER TOPOLOGIES

In order to find the limits of the achievable power density and efficiency with an optimization procedure, those topologies must be identified first that show the best potential for volume minimization while maintaining high efficiency. In literature, many different topologies have been proposed for telecom applications [4]–[11], which could be basically divided into hard switched, soft switched, and resonant converters. Due to high switching losses, the hard-switched topologies do not allow to reduce the volume of the passive components by increasing the switching frequency and simultaneously having a high efficiency.

In the area of soft-switched converters, phase-shift converters with current doubler (CDR) or with capacitive output filter (CTC) (cf., Fig. 2) [12] are promising representatives, which show low switching losses/high efficiency, a simple control, a

TABLE II
MAIN DIFFERENCE BETWEEN THE THREE CONSIDERED TOPOLOGIES

	Phase Shift		Resonant
	Current-D.	Cap.-Filter	Cap.-Filter
Turns Ratio	2.75:1	5.5:1:1	7:1:1
Rectifier Volt.	$V_{IN}/2.75$	$2 \times V_{OUT}$	$2 \times V_{OUT}$
I_{off} Leg B	medium	high	low/medium
I_{off} Leg A	medium	low	zero
Series Inductance	low	medium	high
Reactive Energy	low	medium	zero/low

For the CDR output, the turns ratio is half the turns ratio of the phase shift full bridge with capacitive output.

low number of components, and the potential for high power density. Therefore, this concept and a series–parallel resonant converter (SPR) are optimized in this paper (cf., Table II). The SPR with capacitive or LC output filter, as shown in Fig. 4, is a promising converter structure since it combines the advantages of the series resonant converter and the parallel resonant converter. On one hand, resonant current decreases with the decrease of the load and the converter can be regulated at no load; on the other hand, good part load efficiency can be achieved [13], [14]. Furthermore, the converter is naturally short-circuit-proof.

A. Phase-Shift Converter

In Fig. 2, a phase-shift converter with the two considered rectifier structures—a CDR and a center-tapped transformer with CTC is shown. The primary side of these converters and also the control of switches are the same for both rectifier topologies. However, the current waveforms (cf., Fig. 3), and the related switching and conduction losses, as well as the transformer design are significantly influenced by the rectifier stage.

With a CDR on the secondary side, a transformer with two standard windings can be applied. There, the turns ratio is $N_P/(2N_S)$ —in the considered case 2.75:1—which leads to a high secondary voltage, which must be blocked by the rectifier diodes (here, worst case $400 \text{ V}/2.75 \approx 145 \text{ V}$). The average current in the output inductors is half of the output current, which is also roughly true for the secondary winding of the transformer. During states 1 and 3 (cf., Fig. 3), the current in the secondary winding is equal to the output inductor current, which rises from $I_{1,CDR}$ to $I_{off,CDR,B}$, which is turned off by a MOSFET of leg B. During states 2 and 4, the current is determined by the leakage inductance of the transformer. There, the current is decreasing relatively slowly down to $I_{off,CDR,A}$, since the voltage across the leakage inductance is approximately equal to the forward voltage drop of the conducting power transistors. The value of the leakage inductance and the current at the switching instant must not be too small in order to guarantee ZVS conditions for all four switches. For determining the power density/efficiency limit, only the operating point with nominal output power is considered. Part load efficiency is neglected, since the aim is to determine the upper achievable limits. Consequently, a relatively low leakage inductance value (here, $\approx 2 \mu\text{H}$) is sufficient for charging/discharging the parasitic output capacitors of the MOSFETs. This inductance is realized by spatial separation of the transformer windings.

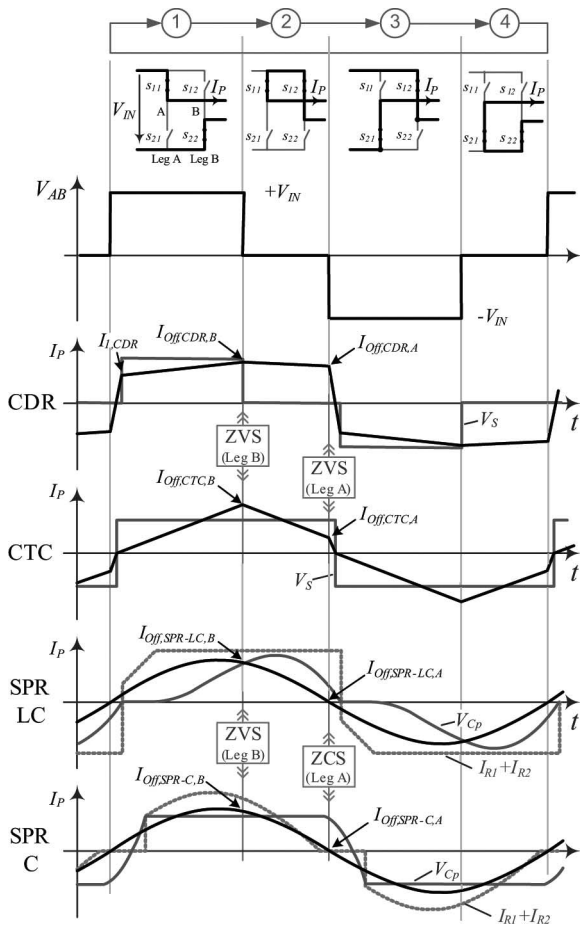


Fig. 3. Switching states and primary currents of the phase-shift converter with (a) CDR, (b) CTC and SPR with (c) LC filter and (d) C filter. Here, a smaller duty cycle has been used than nominal in order to improve the readability of the figure.

In case the full bridge is combined with a center-tapped transformer and a CTC, the series inductance, which is integrated as leakage inductance L_σ into the transformer, must be larger in order to limit the rise of the current I_P (cf., Fig. 3), since two voltage sources are directly connected via the transformer. During states 1 and 3, the voltage across L_σ is $V_{IN} - N_P/N_S V_{OUT}$ and the current rises up to $I_{off,CTC,B}$, which must be turned off by a MOSFET of leg B. In states 2 and 4, the voltage $-N_P/N_S V_{OUT}$ lies across L_σ and the current decreases down to $I_{off,CTC,A}$, which is turned off by a MOSFET of leg A. At the beginning of the following state 3 or 1, the current in the leakage inductance must be decreased first down to zero before it could rise again. During this period, the energy stored in the leakage inductance is fed back to the dc link, which results in a reactive power flow. This reactive power flow is required for obtaining the ZVS condition in leg A. With the CDR, analog behavior could be observed, but the energy is lower since the inductance is smaller.

The required turns ratio of the CTC transformer is $N_P:N_S:N_S$ —in the considered case 5.5:1:1 (assumed maximum duty cycle < 0.85 ; cf., Table V)—resulting in maximal $2V_{OUT}$ across the rectifier diodes during the blocking state if ringing is neglected.

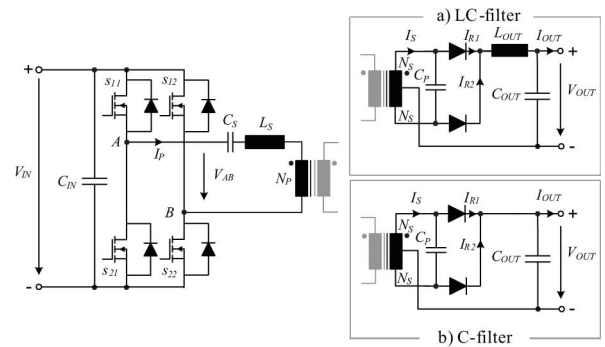


Fig. 4. Schematic of the SPR with (a) LC filter and (b) capacitive output.

B. Series-Parallel Resonant Converter

For the SPR, two different rectifier circuits are considered—a center-tapped transformer with LC output filter and with capacitive filter, as shown in Fig. 4, where, the output filter topology influences the behavior of the dc-dc converter significantly, since the LC filter acts more like a current source at the output and the capacitive filter as voltage source. The current and voltage waveforms are shown in Fig. 3, where besides the resonant current I_P , the voltage across the parallel capacitor V_{C_P} and the current $I_{R1} + I_{R2}$ in the rectifier diodes are also shown.

In case of the LC output filter, the continuous (CCV) and the discontinuous (DCV) capacitor voltage modes must be distinguished [15]. Since the DCV mode usually occurs at heavy load conditions, in Fig. 3, the waveforms for this mode are shown. In the figure, the waveform of the parallel capacitor V_{C_P} is clamped by the output current to zero for a certain period of time, which leads to a discontinuous parallel capacitor voltage V_{C_P} showing a large deviation from the purely sinusoidal shape. At the time when V_{C_P} falls to zero, the resonant current I_S is smaller than I_{OUT} . As long as I_S is smaller, the capacitor voltage V_{C_P} is clamped to zero by the negative difference between I_S and I_{OUT} $[-(I_S - I_{OUT})]$, which flows through the rectifier diodes. In other words, when I_S is larger than I_{OUT} , the positive difference between the currents $(I_S - I_{OUT})$ charges the capacitor C_P .

Due to the sinusoidal resonant current and the output inductor L_{OUT} , the current in the rectifier diodes starts more smoothly resulting in a lower diode turn-on stress. In the secondary winding, however, flows a constant dc current along with an ac component causing higher transformer losses.

With the CTC, the current in the rectifier steps from zero to the value of the output current. This could result in higher diode forward recovery losses, depending on the diode semiconductor technology, and an increased EMI noise level. The transformer secondary rms current, however, is lower, thus resulting in lower losses and a more compact transformer design.

Based on the required output voltage ripple of maximum 300 mV_{pp} and a maximum inductor ripple current of $\pm 7.5\%$ for the LC filter, the component values for the two topologies can be determined (cf., Table III). The ripple current in the filter capacitor in the topology with capacitive filter is much higher than that for the LC filter. Applying electrolytic capacitors, this high ripple current results in a large filter volume due to the

TABLE III
COMPONENT VALUES OF THE LC AND THE CTC SHOWN IN FIG. 4 FOR AN
OUTPUT VOLTAGE RIPPLE OF 300 mV_{pp}

LC-Filter		Capacitive Filter	
C	30 μF	C	470 μF
-		R_{ESR}	50 $\mu\Omega$
L	5 μH	-	
$I_{C,Ripple,RMS}$	4.6 A	$I_{C,Ripple,RMS}$	52 A

TABLE IV
COMPARISON OF LC AND CTC WITH ELECTROLYTIC OR CERAMIC
CAPACITORS

	Electrolytic		Ceramic	
	Cylindrical	Cuboid	SMD-Device	Mounted
$\mu\text{F}/\text{cm}^3$	170	134	111	90
I_{AC}/cm^3	0.25 A	0.19 A	41.6 A	35.1 A
LC-Filter Size in [cm^3]	μF only: 0.22 + 40.9 (L) I_{AC} : 24.2 + 40.9 (L)		0.32 + 40.9 (Inductor) (Max. $I_{AC} < 11.3$ A)	
C-Filter Size in [cm^3]	μF only: 3.7 , $I_{AC} < 1.5$ A I_{AC} : 273 \Rightarrow $C=36$ mF		5.4 (Max. $I_{AC} < 233$ A)	

For electrolytic capacitors, two volumes are given: The first value gives the volume if just the capacitance value is realized—neglecting the ripple current I_{ac} and the current carrying capability of the capacitors. With the second value, the ripple current is also accounted for. The inductor of the LC filter has a volume of 40.9 cm^3 . For the ceramic capacitors also, two volumes are considered: The volume “SMD-device” is the pure volume of the ceramic capacitor and the volume “mounted” also accounts for the volume of the PCB where the capacitors are mounted. There, a double-sided, 1.5-mm-thick board is assumed.

relatively high equivalent series resistance (ESR)/low current carrying capability of electrolytic capacitors. This is shown in the second line of row “LC-Filter Size” in Table IV. The first line represents the volume of the capacitor if just the capacitance value is considered and the ripple current is neglected. With the ripple current, the capacitor volume increases more than by a factor of 10. Both values are based on the cuboid volume of cylindrical electrolytic capacitors.

If the capacitance is realized by ceramic capacitors, the volume decreases down to 0.32 cm^3 including ripple current considerations. In both cases, the volume of the inductor (40.9 cm^3) is based on very compact commercially available inductors, e.g., [16] and [17]. Due to the large inductor volume, the size of the LC filter is relatively large and would consume approximately 10% (including interconnection) of the volume if a power density of 10 kW/L is assumed.

With a capacitive filter and ceramic capacitors, the volume of the filter elements decreases down to 5.4 cm^3 , including the volume of the printed circuit board (PCB) for mounting, and the maximum thermally possible ripple current increases to 233 A. A capacitive filter with electrolytic capacitors would result in a filter volume of 273 cm^3 and a capacitance value of 36 mF if the ripple current is considered. Taking just the required capacitance value into account, this volume decreases to 3.7 cm^3 .

Since with the CTC, the volume of the filter is much smaller and the current in the secondary winding is lower, in the following section, only the resonant converter with CTC is considered in the optimization performed with the optimization procedure.

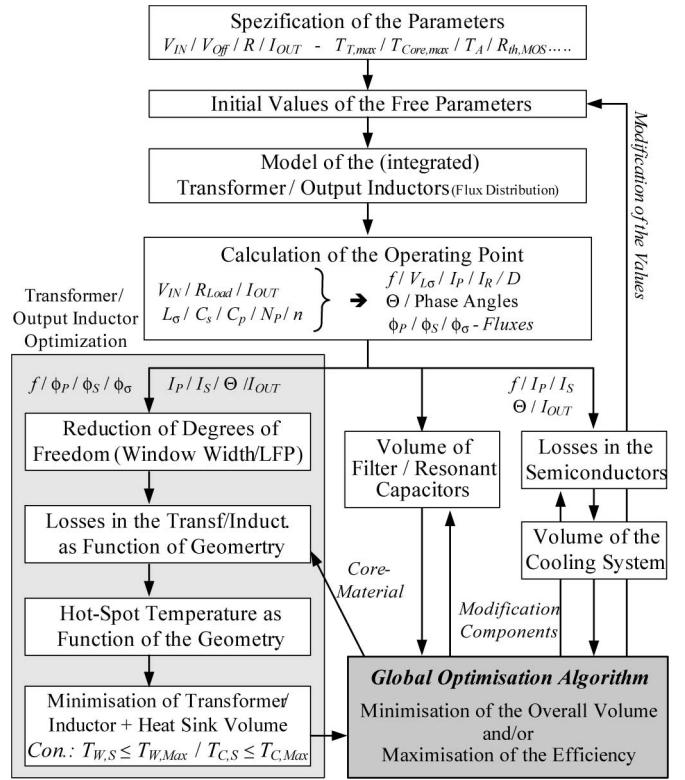


Fig. 5. Automatic procedure for optimizing the volume/efficiency of an SPR while keeping the device temperatures below given limits.

III. OPTIMIZATION PROCEDURE

After identification of the topologies with the best potential for high power density and high efficiency, the components values must be chosen, so that the system volume becomes minimal and/or the efficiency maximal. Since the volume of the single components, which are mainly limited by the respective maximum operation temperature, depend, to some extent, on each other, the optimization of the overall volume/efficiency is a quite involved task with many degrees of freedom.

Therefore, an automatic optimization procedure is applied for determining the optimal component values of the telecom supply.

In Fig. 5, a possible flowchart of such a procedure is given, where the specification of the design parameters, like the input and output voltage, the output power, temperature limits, material characteristics, etc., is the starting point of the procedure. These parameters as well as starting values for the free parameters like N_p , N_s or C_s , C_p , L_s/L_{OUT} must be specified by the user.

Based on the values for the series/leakage, respectively, the output inductance and the turn numbers of the magnetic components are modeled. In case of the phase-shift converter, the models mainly consist of analytic expressions for the flux distribution and the optimal thickness/diameter of the foil/wires for the windings [18]. For the resonant converter, a reluctance model of the transformer with integrated series inductance is calculated. This model is combined with the converter model for calculating the flux distribution in the core [15], [20].

The converter model for the phase-shift converters is based on analytic expressions with which the currents and the voltages as well as the duty cycle and the constraints for ZVS conditions are calculated. For the resonant converter, the operating point of the dc–dc converter is first estimated by an approximated fundamental frequency analysis [21]. With the estimated values, the solution space for the analytic converter model [20] is restricted and the calculation time is reduced. The converter model is based on a set of equations that are derived with the extended fundamental frequency analysis [22] and solved numerically. The solutions are the operating frequency, the voltages, and the currents as well as the flux distribution of the integrated transformer including phase information.

With the currents in the converter, the switching and conduction losses of the MOSFETs and rectifier diodes are determined. These losses, the ambient temperature, and the maximum junction temperatures of the semiconductor devices are used for calculating the volume of the semiconductor heat sink including the fan based on the cooling system performance index (CSPI), which is defined by

$$\text{CSPI}[\text{W/K} \cdot \text{L}] = \frac{G_{\text{th},S-A}[\text{W/K}]}{\text{Vol}_{\text{HS,Magn.}}[\text{L}]} \quad (1)$$

and has been introduced in [3] ($G_{\text{th},S-A}$ is the thermal conductivity of the heat sink). Here, it is important to check the resulting volume of the cooling system, since with the scaling factor CSPI, quite small volume for the heat sink/fan can result, which is difficult to manufacture. A possible solution is to combine heat sinks that are on comparable temperature levels, so that one larger fan could be used for both heat sinks.

Besides the losses in the semiconductors, the volume and losses in the resonant tank capacitors and/or output capacitors are also calculated with the voltages/currents. These losses in the capacitors must be limited to the maximum admissible values.

The volume and shape of the transformer/inductor core and two windings is determined in a second, inner optimization procedure (light-gray-shaded region in Fig. 5). Here, the volume of the transformer/inductor is minimized while keeping the temperatures below the allowed limits. For this purpose, first the geometrical degrees of freedom are reduced to 3 by determining the core window width using the optimal winding thickness and the turns number [21]. In case of transformers with integrated leakage inductance, the width of the leakage path (LFP) is also fixed by setting the flux density in the LEP to the same value as in the middle leg conducting the main flux.

Thereafter, the core and winding losses are calculated as functions of the three remaining geometrical variables [a , b , d ; cf., Fig. 7(a)]. With the losses and the thermal model of the transformer/inductor, the temperature distribution in the core and winding could also be calculated as a function of the variables a , b , and d . The peak temperatures in the windings and the core are, together with the maximum allowed temperatures, the constraints for the following minimization of the volume including the volume of cooling system for the magnetic device [cf., Fig. 7(b)]. Furthermore, the variables a – e , defining the transformer/inductor geometry, can be restricted in order to preserve certain limitations resulting from the manufacturing process.

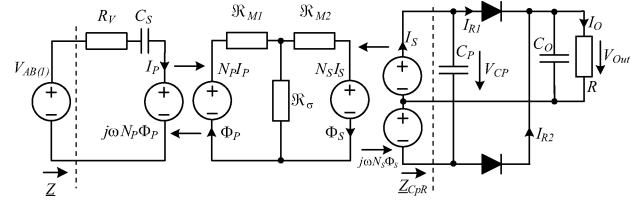


Fig. 6. Equivalent circuit of the SPR with CTC.

In the inner optimization loop, it is also possible to maximize the efficiency of the transformer/inductor, if an upper limit for the volume is given.

Together with the volumes of the capacitors/heat sink, the minimized transformer/inductor volumes are passed to the global optimization algorithm. This algorithm systematically varies the values of the free parameters until a minimal system volume or maximal efficiency is obtained. This procedure is relatively fast/simple for the phase-shift converters since the number of interdependencies is small, but in case of the resonant converter, the models are complex and the calculation/computation effort is huge.

This optimization procedure could also be applied to other problems by extending and/or replacing the utilized models, which are presented in the following section.

IV. MODELS

In the subsequent paragraphs, the different models of the optimization procedure are explained. First, the analytical converter model is derived, and then the equations for the semiconductor losses and the model for the resonant tank capacitor volumes. Finally, the loss equation and the thermal model of the transformer are presented.

A. Analytical Converter Model

With the analytical converter models, the currents and the voltages as well as the operating point (duty cycle, frequency, phase shift, etc.) for the phase shift full bridge with CDR or center-tapped transformer and the series–parallel resonant converter with CTC are calculated.

In case of the SPR [cf., Fig. 4(b)], the models are partly based on the extended fundamental frequency analysis (E-FFA) proposed in [15], [20], and [22], where the currents and voltages are represented by their fundamentals, as shown in Fig. 6. In the model, the control method described in [15] with ZVS condition in one leg and ZCS condition in the other leg as well as control by frequency and duty cycle are also considered in the equations. This control method significantly reduces the switching losses.

For the resonant converter with purely CTC, the E-FFA has been improved so that not only the fundamental component is considered but also the third harmonic, since it significantly influences the behavior of the converter. Thus, both the primary resonant current I_P and the secondary resonant current I_S are sinusoidal with a superimposed third harmonic component. Furthermore, it is assumed that the output voltage is constant and that the components are ideal. The major procedure of the

analysis is to determine the impedance $Z_{C_p R}$ of the parallel connection of C_p and the rectifier at first. With this impedance, the input impedance Z of the resonant circuit, seen by the H-bridge/voltage source V_{AB} (cf., Fig. 6), could be calculated. In the impedance Z , the reluctance model of the transformer is also included.

In the next step, two equations for each harmonic can be set up. The first equation describes the relation between the phase shift of the primary current I_p and the fundamental component of the H-bridge voltage $V_{AB(1)}$, which is determined, on one hand, by the duty cycle D , and on the other hand, by the impedance Z . The second expression relates the input impedance of the resonant tank to the amplitude of the resonant current. These equations are derived in [20] and are solved numerically in the optimization procedure.

B. Semiconductor Losses

For calculating the volume of the heat sink for the semiconductors with (1), the maximum operating temperature and the thermal resistance between junction and heat sink of the semiconductors are required. These values can be derived from the data sheets of the applied semiconductors. Furthermore, the losses in the four MOSFETs including antiparallel diode and two rectifier diodes must be calculated. Based on the currents calculated with the converter models, the rms currents in the MOSFETs and the resulting conduction losses can be calculated. Here, it is assumed that always one MOSFET per leg is turned on, so that the current does not flow via the antiparallel diode but in reverse direction through the MOSFET.

For the rectifier diodes, an approximately constant forward voltage drop is assumed, so that the conduction losses can be calculated with the average currents. The switching losses of the diodes are neglected since it is assumed that Schottky diodes are used.

Due to the ZVS condition, the switching losses cannot be calculated based on the data sheet information. Instead, the measured values, which have been performed with the applied APT50M75 MOSFETs from Microsemi (former Advanced Power Semiconductors) [21], are used in the optimization procedure. Based on these measurements, the losses per MOSFET can be determined by

$$P_{ZVS}[\text{W}] = (1.9e^{-7} I_{\text{off}}^2[\text{A}] - 3.8e^{-6} I_{\text{off}}[\text{A}] + 1.4e^{-5}) f[\text{Hz}]$$

in case the current turned off by the MOSFET is

$$I_{\text{off}} \geq 15 \text{ A} \quad (2)$$

and they are negligible if the current I_{off} is below 15 A.

With the applied control method, one leg of the resonant converter would switch at ZCS condition. However, if the ZCS leg, which should switch at the zero crossing of the resonant current, is switched slightly before the zero crossing, the MOSFET has to turn off a small current. Because of the fast switching and the large output capacitance of the MOSFET, this current does not cause relevant turn-off losses. In case the turned off current is large enough, so that it charges the MOSFET capacitances during the interlocking delay [15], the opposite MOSFET turns

on at zero voltage. Consequently, the switching losses in the ZCS leg are negligible [21].

With the explained approaches, the semiconductor losses can be calculated and the heat sink temperature and volume [cf., (1)] can be determined so that the maximal junction temperature is not exceeded. For the efficiency calculation, the losses in the gate drive circuits, which can be calculated with the gate-charge/capacitance and which increase linearly with frequency, must also be considered.

C. Resonant Tank Capacitors

The capacitors of the resonant tank and the CTC carrying high-frequency currents with a relatively high amplitude. In order to limit the losses and the temperature rise, dielectrics with a low-loss factor $\tan \delta$ are required. There are basically two good choices: either foil capacitors with polypropylene or COG/NP0-type ceramic capacitors. Since the resulting volume with foil capacitors is significantly larger than for ceramics as could be derived from data sheets, the latter are chosen for the considered telecom power supply.

For calculating the volume required for realizing the series and parallel capacitor, a commercial 3.9-nF/800-V COG ceramic capacitor in a 1210 SMD housing from Novacap [23] has been chosen as reference component, since it offers the highest capacitance per volume rating at ac voltages with a high frequency and amplitude. Based on this capacitor, the resulting volume could be calculated by scaling. Here, the volume for mounting the components on a double-sided PCB is also considered in the optimization procedure.

In case of the filter capacitor, a 2.2- μF /100-V X7R ceramic capacitor in a 1210 housing manufactured by muRata [24] is used as reference element. The capacitance value is calculated with the currents based on the maximum allowed ripple voltage of 300 mV_{pp} at the output.

With the currents, the losses in the capacitors can also be determined with the loss factor. These are compared with the maximal allowed values, which can be derived by the loss limit of 0.35 W per 1210 housing at 40 °C ambient temperature and 125 °C maximal dielectric temperature. Here, the decrease of the capacitance with temperature and dc voltage is also considered in the optimization procedure.

D. Transformer Model

In the optimization procedure shown in Fig. 5, the shape of the transformer is also optimized for minimal volume in the inner loop while the hot spot temperatures are kept below the limits. For this inner optimization loop, the volume, the losses, and the temperature distribution in the transformer are needed as function of the geometry. The geometry could be described by five variables, as shown in Fig. 7(a), where the construction of the transformer and the definition of the variables are given. Here, it is assumed that copper foil is used for realizing the primary and secondary windings, since the thermal resistance between the winding layers is lower. Furthermore, per layer, only one turn is realized.

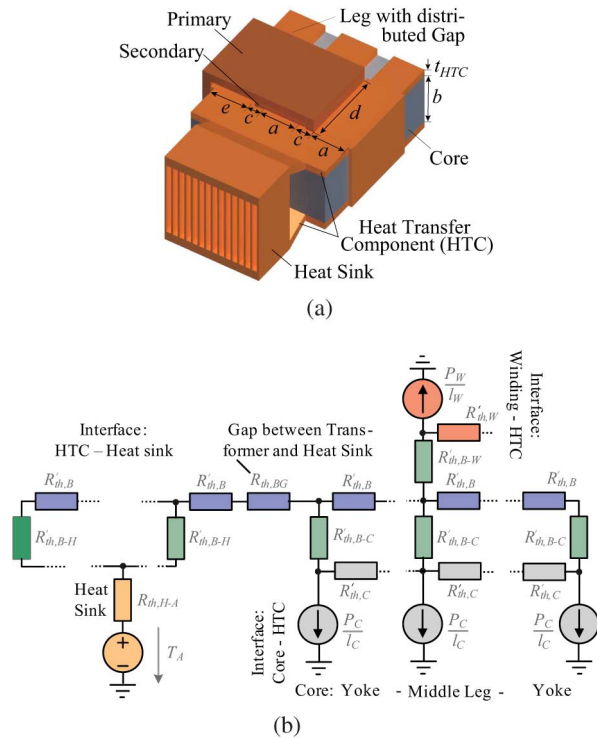


Fig. 7. (a) Geometry of transformer with integrated series inductance and HTC/heat sink for cooling. Parameters a , b , and d are the degrees of freedom in the optimization. (b) Distributed thermal model of the cooling system shown before with the heat sink on the left-hand side, a gap between heat sink bridged by the HTC and transformer, and the transformer with winding on the right-hand side.

In Fig. 7(a), a transformer with integrated leakage inductance is shown [25], where the secondary winding encloses the middle leg and the primary winding the middle and one outer leg, which conducts the leakage flux. This type of transformer is used in the resonant converter and in the phase-shift converter with CTC. In case of the phase-shift converter with CDR, a transformer where both windings enclose only the middle leg is assumed, and the required series inductance is integrated by spatial separation of the windings.

In order to maximize the power density of the transformer, an advanced cooling method as described in [2] has been applied. With this method, the losses in the windings and the core are transferred via a heat transfer component (HTC) to an additional heat sink for the transformer.

For calculating the temperature rise, the losses in the windings and the core are required. The winding losses are calculated by a 1-D approach, which includes skin and proximity effect losses, and the thickness of the foil is optimized as described in [18]. The core losses are calculated by the approach presented in [26], which is based on Steinmetz parameter [27] and the rate of magnetization (dB/dt). The flux density in the core is determined by the optimization algorithm of the transformer, so that a minimal volume results and the flux density is below the maximal allowed one [19].

With the losses, the temperature distribution in the transformer could be calculated based on the thermal model shown in Fig. 7. This model describes the heat flow from the winding/core

via the thermal interfaces and HTC to the heat sink/ambient by distributed thermal resistances (R_{th} per length). The calculation of the temperature profile is based on transmission-line equations, which is described in detail and validated in [2].

For improving the heat flow within the windings made of foil and also from the winding to the HTC, a thermally conductive insulating material is used [28]. Moreover, thermal grease between the core and the HTC and a cover pressing the winding on the HTC are used. This cover is not shown in Figs. 1 and 7(a).

After the volume has been minimized, it is passed to the global optimization algorithm, where it is used for calculating the system volume and varying the parameters systematically.

V. CALCULATION RESULTS

Based on the procedure shown in Fig. 5, the three considered topologies have been optimized for a telecom supply with the specification given in Table I. As already mentioned, during the optimization, only the nominal operating point has been considered—part load efficiency, etc., have not been considered. The results presented are based on the following components/limitations if not stated differently:

- 1) core material: N87 from Epcos ($T_{max} \leq 115^\circ\text{C}$);
- 2) windings: foil windings ($T_{max} \leq 125^\circ\text{C}$);
- 3) center-tapped secondary winding;
- 4) MOSFETs: APT50M75 from Microsemi (former APT);
- 5) rectifier diode: APT100S20 from Microsemi;
- 6) capacitors C_S and C_P : reference 3.9-nF 800-V COG series from Novacap;
- 7) CSPI: 23 (for transformer and semiconductor heat sink);
- 8) maximal junction temperature $T_{j,max} \leq 140^\circ\text{C}$.

A further requirement is the overall height of the supply that should be below $1U$ (≈ 44 mm), which significantly influences the design of the transformer/inductors [especially the height b ; cf., Fig. 7(a)] as well as the cooling system.

In order to obtain the dependency of the power density/efficiency on the operating frequency, the global optimization algorithm (cf., Fig. 5) is replaced by manual parameter variation, which allows to calculate the power density/efficiency for various frequencies. In Fig. 8, the resulting characteristic of the power density and efficiency as functions of frequency are shown. The maximal achievable power density is 19.1 kW/L for the resonant converter and 15/11.7 kW/L for the phase-shift converter with CTC/CDR ($1 \text{ kW/L} = 16.4 \text{ W/in}^3$). Here, only the net volume of the components including PCBs/housings is considered. The volume between the components required for mounting/insulation and due to not fitting housings (e.g., cube type and cylindrical shapes) is not considered, since it depends significantly on the 3-D arrangement of the components and the design of the supply. This volume adds significantly to the total converter volume, so that the resulting power density is lower than the calculated value.

In case of the resonant converter prototype shown in Fig. 1, the calculated power density is 15 kW/L, which is lower than the calculated 19.1 kW/L due to the newer components applied in the presented optimization. The power density of the final

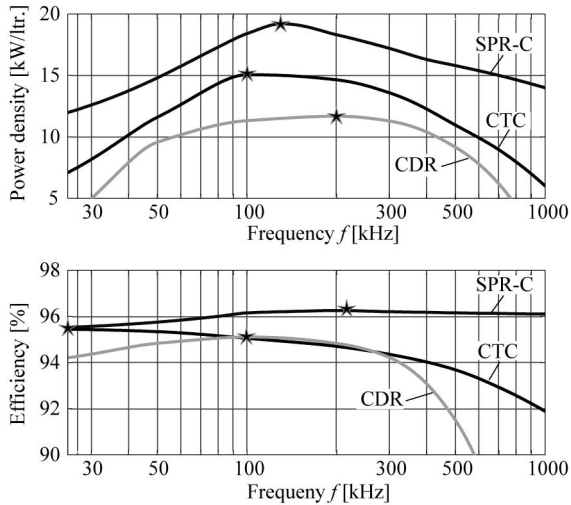


Fig. 8. (a) Power density and (b) efficiency of the phase-shift converter with CTC, CDR, and SPR with C-filter (SPR-C) as a function of switching frequency.

assembled prototype system is 10 kW/L if a similar scaling factor ($2/3\times$) is assumed for the three optimized converter topologies, 12.7 (SPR-C), 10 (CTC), and 7.8 kW/L (CDR). The power density of the CDR could be increased a bit by using integrated magnetics, where the two inductors and the transformer could be realized with only one core [29], [30].

The efficiencies at the operating point with maximal power density are 96.2% for the resonant converter and 95%/94.8% for the CTC/CDR, as shown in Fig. 8(b). At the operating point with minimal losses, an efficiency of 96.3% at a switching frequency of approximately 220 kHz could be reached with the resonant converter. The switching frequency is higher than that at the operating point for maximal power density, since the losses of the passive components reach a minimum at this frequency. Due to the increased volume for the semiconductor heat sink, this operating point results in a power density of only 17.1 kW/L.

In case of the phase-shift converter with CTC, the maximal efficiency is achieved at the lowest considered operating frequency of 25 kHz. Here, the CTC reaches 95.4%. The maximal efficiency for the CDR is 95.1%, which is achieved at 100 kHz.

In Fig. 9, the distributions of the volumes on the magnetic devices (transformer and inductor), the capacitors (resonant tank and output), the heat sink for the semiconductors, and the remaining components like housings, control board, or gate drive for the three topologies are shown. It can be seen that with rising switching frequency, the volume of the semiconductors' heat sink increases due to rising switching losses. The shape of the volume distribution as function of frequency is strongly determined by the passive components, which define a frequency range from approximately 100 to 300 kHz of high power density. Outside this range, the volume of the magnetic devices increases, and at higher frequencies, the volume of the semiconductor heat sink also rises significantly, which limits the achievable power density. At lower frequencies, the volume of the magnetics rises due to increasing volt-seconds and a limited maximum allowed flux density of the core materials. On

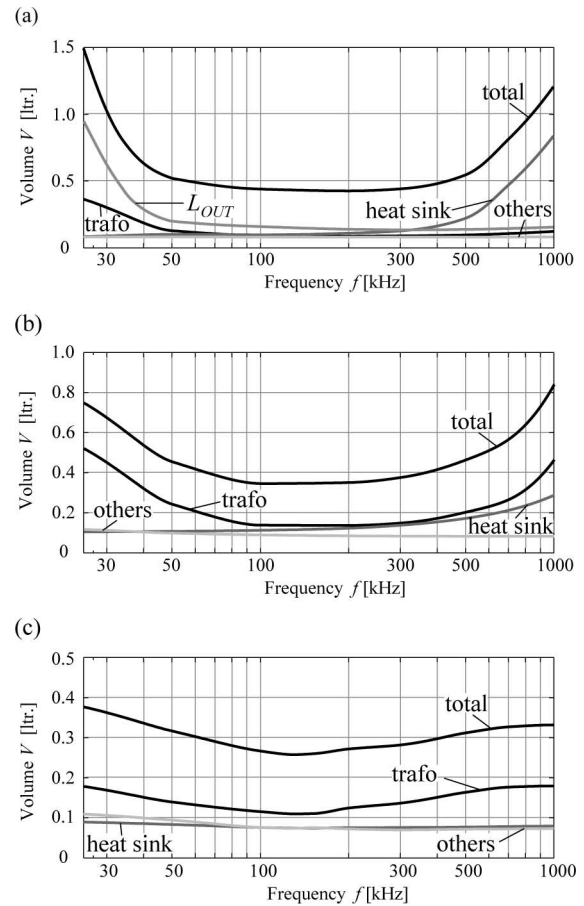


Fig. 9. Volume versus frequency for the phase-shift converter with (a) CDR, (b) CTC, and (c) SPR-C, split in transformer, heat sink, and others, i.e., the volume of the control, the auxiliary, the gate drive, the semiconductor housings, and the dc-link/output capacitor. For the CDR, the volume of both output inductors is shown.

the other hand, rising core and winding losses result in a rising volume for higher operating frequencies.

In case of the CDR, the increase of the inductor volume for lower frequencies is relatively high (cf., Fig. 9(a): 25–50 kHz), so that one output inductor including cooling system becomes larger than the transformer. This is caused by the significantly increasing inductance value of the output inductor, which is required in order to limit the current ripple. For 25 kHz, an inductance value of approximately 50 μH , and for 200 kHz, approximately 6.7 μH are obtained. Due to the high inductance value, the number of turns increases from 5 to 51, so that the losses increase by a factor of 5 between 25 and 200 kHz. With the losses, the volume of the cooling system for the inductors also increases significantly. At the optimal operating frequency of 200 kHz, the volume of one output inductor (71 cm^3) is smaller than the transformer volume (90 cm^3).

Although the series inductance, which is integrated in the transformer, of the resonant converter (26.5 μH) is larger than that of the CTC (12.4 μH), the transformer of the SPR-C (110.8 cm^3) is smaller than that of the CTC (140.9 cm^3). This results from the fact that the volts-seconds on the primary side of the CTC transformer are larger (74 $\mu\text{V}\cdot\text{s}$) than that of the SPR-C

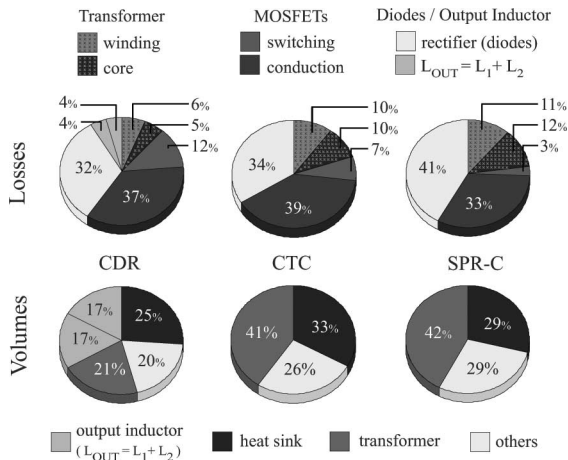


Fig. 10. Distribution of the losses and volumes of the phase-shift converter with CTC/CDR and SPR-C.

(51 $\mu\text{V}\cdot\text{s}$), since the optimal switching frequency is lower (CTC: 100 kHz/SPR-C: 135 kHz), and the voltage waveform (CTC: rectangular/SPR-C: sinusoidal) of the CTC also leads to higher volts-seconds. The higher volt-seconds require a larger core area, which leads to a larger core volume and a larger winding length. The larger winding length and the fact that the turns ratio of the CTC (11:2) is lower than that of the SPR-C (14:2) cause higher winding losses in the primary winding (CTC: $P_{Wdg,P} = 13 \text{ W}/\text{SPR-C } 5.7 \text{ W}$). Since the losses of the primary winding must flow via the secondary winding to the HTC/heat sink (cf., Fig. 7), this causes higher temperature drops in the winding, which requires a better/larger cooling system.

The volume of the other components, i.e., the volume of the control board, the gate drive, the auxiliary supply, the semiconductor housings, the dc-link capacitor (=88 μF), and the output filter capacitor, is relatively constant for all three converter types, since only the volume of the output capacitors, which has only a small share of the other components' volume, is significantly dependent on the operating frequency. This volume decreases with increasing frequency. Since the output capacitor of the CDR is relatively small due to the filter inductors, the volume of the other components is approximately independent of frequency.

A more detailed distribution of the volume as also the losses of the three optimized considered topologies is given in Fig. 10, where, the volume and the losses of the magnetic devices, the capacitors, the semiconductors/heat sink, and the remaining components for the operating point with maximal power density are presented. Further details are shown in Table V.

In Fig. 11, the losses of the transformer, MOSFETs, and rectifiers as functions of the frequency are shown. It can be seen that the shape of the switching loss curve resembles approximately the function volume of the heat sink versus frequency. The conduction losses of the MOSFETs and rectifier diodes are almost constant, since the turns ratio and the duty cycle are approximately constant. This is especially true for the CTC, since there the turns ratio and the duty cycle, which are independent of frequency, directly determine the conduction losses. In case of the resonant converter, the switching losses are very small for

TABLE V
RESULTING SPECIFICATION OF THE OPTIMIZED 5-KW TELECOM SUPPLIES

	Phase Shift		Resonant
	Current-D.	Cap.-Filter	Cap.-Filter
Power Density	11.7 kW/ltr.	14.7 kW/ltr.	19.1 kW/ltr.
(Incl. mounting $\approx \times 2/3$)	7.8 kW/ltr.	10 kW/ltr.	12.7 kW/ltr.
Operating Point			
• Frequency	200 kHz	100 kHz	135(129) kHz
• Duty Cycle	0.81(0.86)	0.82(0.88)	0.78(0.83)
• Efficiency	94.8 %	95 %	96.2 %
Transformer			
• Winding Losses	16 W	24.6 W	21.9 W
• Core Losses	13.8 W	23.7 W	23.5 W
• Turns Ratio	11:4	11:2	14:2
• Winding Temp.	125 °C	124 °C	125 °C
• Core Temp.	107 °C	115 °C	115 °C
• Flux Density	175 mT	240 mT	300 mT
Semiconductors			
• $P_{V,SW,MOS}$	31.2 W	17.8 W	5 W
• $P_{V,Cond,MOS}$	93.7 W	96.8 W	64 W
• Rectifier Losses	83.3 W	83.3 W	83.3 W
• Heat Sink Temp.	125.1 °C	125 °C	130.8 °C
Geometric Trans.			
Middle leg a	13 mm	15 mm	14 mm
Height b	15.1 mm	21 mm	12.2 mm
Window Width c	9.4 mm	7 mm	7 mm
Window Height d	19.3 mm	29.4 mm	31 mm
Leakage Leg e	-	7.4 mm	10.6 mm

The losses in the two inductors of the CDR are $2 \times 10.9 \text{ W}$, the AC flux density is 77 mT, and the inductance is 6.7 μH . The geometry (cf., Fig. 7) of the inductors is: $a = 10 \text{ mm}$, $b = 21 \text{ mm}$, $c = 4.5 \text{ mm}$, $d = 11.3 \text{ mm}$ (in brackets: simulated values including more parasitic elements than considered in the analytic model).

the whole frequency range, since the switched current is close to 15 A [cf., (2)].

For the CDR, the switching losses increase significantly at higher frequencies. This is related to the fact that the CDR at the secondary side causes a short circuit during the freewheeling period, since both rectifier diodes are conducting (cf., Fig. 3/Fig. 2). During this period of time, no energy is transferred to the output and the current in the leakage inductance (here, 2 μH) decreases only slightly due to the voltage drop of the MOSFETs. The current in the leakage inductance at the end of the freewheeling period is required for achieving ZVS condition for leg A. After the freewheeling period, the current in the leakage inductance must be reversed and the amplitude must rise up to the current in the output inductor before one rectifier diode stops conducting. As long as both rectifier diodes are conducting, no energy is transferred, although the input voltage of the transformer is equal to the dc link voltage. At higher frequencies, the time for reversing the current in the leakage inductance takes a larger and larger share of the duty cycle, since this time is fixed by the value of the leakage inductance and dc link voltage. Therefore, the time share for transferring the power becomes smaller and smaller, and the current amplitude

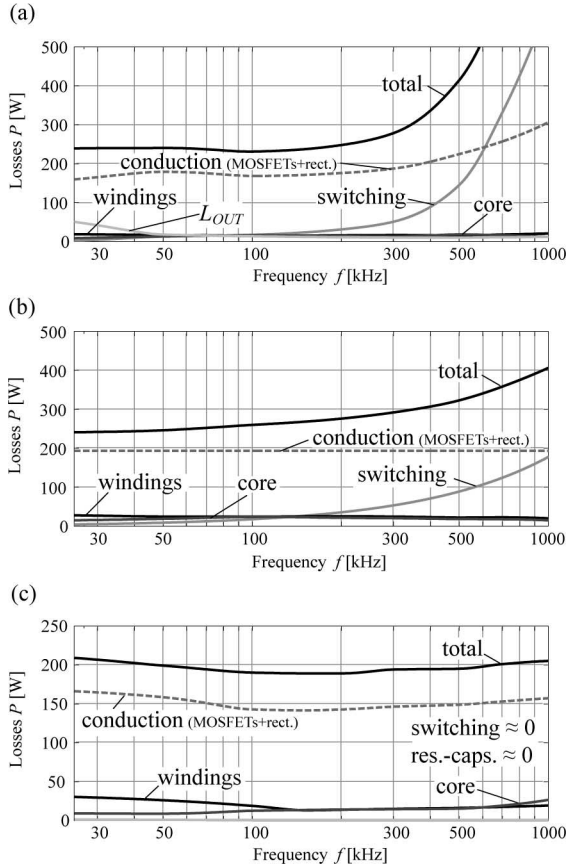


Fig. 11. Losses versus frequency for the phase-shift converter with (a) CDR, (b) CTC, and (c) SPR-C, split in winding, core conduction (MOSFET + rectifier), and switching losses.

must increase, so that the output power is constant. Mainly the peak values $I_{off,CDR,A}$ and $I_{off,CDR,B}$ increase, and the rms values increase only slightly. The increasing peak values lead to higher switching losses [cf., (2)] and also higher conduction losses, since the rms values rise with higher peak currents while the average values are constant due to the shorter conduction time. At higher frequencies, the value of the leakage inductance could be slightly reduced, which would limit the increase of the switching losses at higher frequencies a bit. Since the power density is anyway low at higher frequencies, this has not been considered during the optimization.

The relatively low optimal operating frequency for maximal power density is achieved, since the whole system is considered in the optimization. In case only the transformer for a fixed input voltage/current level would be considered, the optimal operating frequencies for maximal power density of the transformer would be (significantly) higher.

Remark: For the earlier considerations and calculations, it has been assumed that the windings of the transformers/inductors for the three considered systems are made of copper foil. In order to decrease the copper losses a little bit by increasing the cross-sectional area, litz wire could be used instead of the copper foil, which offers more degrees of freedom during the design process. However, the thermal resistance between the single litz wires and an HTC/heat sink is much higher than

TABLE VI
COMPONENTS PARAMETERS OF THE SIMULATION MODELS RESULTING FROM THE OPTIMIZATION PROCEDURE

	Phase Shift		Resonant
	Current-D.	Cap.-Filter	Cap.-Filter
Series Inductance	$2 \mu\text{H}$	$12.4 \mu\text{H}$	$26.5 \mu\text{H}$
Output Inductance	$6.7 \mu\text{H}$	-	-
Series Capacitance	-	-	98.5 nF
Parallel Capacitance	-	-	26 nF
Output Capacitance	$11 \mu\text{F}$	$438 \mu\text{F}$	$254 \mu\text{F}$
Winding Ratio	14:2:2	11:2:2	11:4

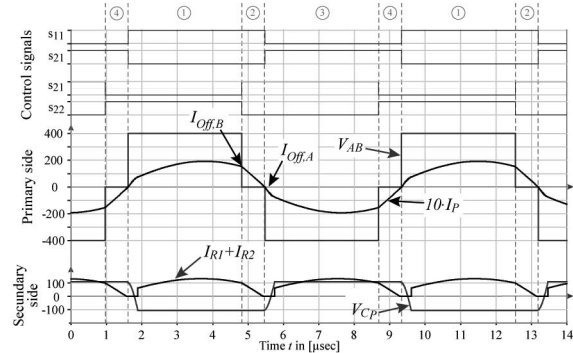


Fig. 12. Simulation results for the SPR with the parameters resulting from the optimization procedure.

TABLE VII
SIMULATION RESULTS FOR THE THREE CONSIDERED CONVERTER TOPOLOGIES

	Phase Shift		Resonant
	Current-D.	Cap.-Filter	Cap.-Filter
Switching Frequency	200 kHz	100 kHz	129.5 kHz
Duty Cycle	0.86	0.88	0.83
Primary Current	17.2 A	19.9 A	15.1 A
Output Voltage	54.0 V	53.9 V	54.0 V
Output Current	92.7 A	92.4 A	92.5 A
Output Power	5.0 kW	5.0 kW	5.0 kW
Turn-off Current Leg A (Calculated)	21.9 A	31.9 A	15.4 A
	22.2 A	32.5 A	15.6 A
Turn-off Current Leg B (Calculated)	21.2 A	10.9	0 A
	21.0 A	11.3 A	$\approx 0 \text{ A}$

with foil, since the contact area is much smaller. Furthermore, the reproducibility of a certain value of the thermal resistance is much more difficult with litz wire than with foil. Therefore, litz wire has been not considered during the comparison.

A. Simulation-Based Results

With the component values and control parameters resulting from the optimization procedure (cf., Table VI), simulation models for each of the three converters have been developed in Simplorer (Ansoft Corporation).

The most important simulated waveforms are given in Fig. 12, and the corresponding values for the SPR are given in Table VII.

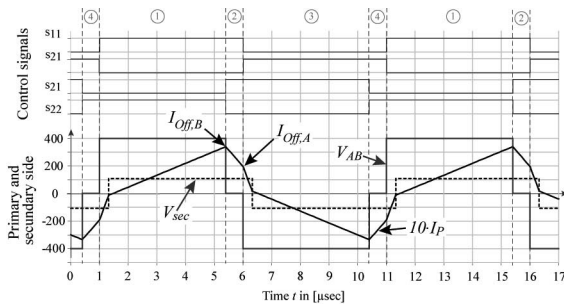


Fig. 13. Simulation results for the phase-shift converter with capacitive output with the parameters resulting from the optimization procedure.

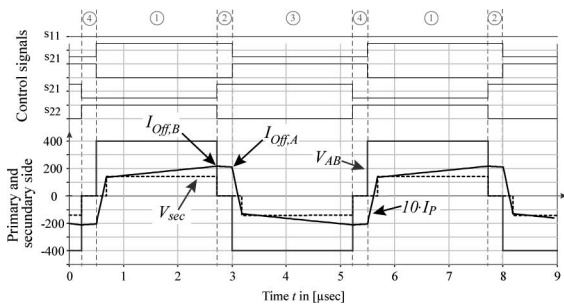


Fig. 14. Simulation results for the phase-shift converter with CDR output with the parameters resulting from the optimization procedure.

For the phase-shift converter with capacitive output and for the phase-shift converter with CDR, the same waveforms are shown in Figs. 13 and 14, respectively. These waveforms correspond very well with the theoretical waveforms presented in Fig. 3. Also, the numerical values in Table VII agree very well with the analytically calculated ones. It can be seen that the simulated values for the duty cycle are larger than the calculated ones, since in the simulation, more “parasitic” effects—like the forward voltage drop of the rectifier diodes and parasitic resistors of the transformer—are considered. In the analytical model, these have been neglected in order to obtain simple, robust, and above all fast calculable equations.

B. Power Density Barriers

In the preceding paragraph, the power density values for available components/technologies have been presented. Now, the influence of different parameters on the achievable power density is investigated. In Table VIII, the achievable power density and efficiency for the phase-shift converter with CTC is shown for different parameter variations. First, it is assumed that the maximal allowed junction temperature is increased from 150 °C to 200 °C (e.g., by applying SiC switches and appropriate packaging)—the remaining parameters (also the $R_{DS,ON}$) are not modified. By this means, the volume of the semiconductor heat sink significantly decreases, so that a power density of 17.1 kW/L (before 14.7 kW/L) can be achieved. It is important to note that with the heat sink, the size of the area for mounting the semiconductors is also shrinking. Consequently, the thermal resistance between the semiconductors and the heat sink increases, so that the gain in power density is very limited.

TABLE VIII

INFLUENCE OF DEVICE PARAMETERS/MAXIMUM ALLOWED TEMPERATURES ON MAXIMAL ACHIEVABLE POWER DENSITY FOR THE PHASE-SHIFT CONVERTER WITH CTC

	Parameter	Old Value	New value	New Density/Eff.
1	Junction Temperature	150 °C	200 °C	17.1 $\frac{\text{kW}}{\text{Lr}}$ 95 %
2	Junction Temp. incl. $R_{DS,on}$	150 °C	200 °C	16.0 $\frac{\text{kW}}{\text{Lr}}$ 95 %
3	$R_{th,MOSFET}$	0.22 $\frac{\text{K}}{\text{mW}}$	0.11 $\frac{\text{K}}{\text{mW}}$	16.1 $\frac{\text{kW}}{\text{Lr}}$ 95 %
	$R_{th,Rectifier}$	0.2 $\frac{\text{K}}{\text{mW}}$	0.1 $\frac{\text{K}}{\text{mW}}$	
4	Winding / Core Temp.	125 °C / 115 °C	150 °C	16.8 $\frac{\text{kW}}{\text{Lr}}$ 94.9 %
5	$P_{Switching}$	P_{SW}	$\frac{1}{2} P_{SW}$	15.9 $\frac{\text{kW}}{\text{Lr}}$ / 95.2 %
6	$V_{F,Rectifier}$	0.9 V	0.45 V	17 $\frac{\text{kW}}{\text{Lr}}$ / 95.8 %
7	1+3+4+5+6	-	-	21.6 $\frac{\text{kW}}{\text{Lr}}$ / 96.3 %

The maximum remains at a switching frequency of approximately 100 kHz, except for case 5, where all improvements are considered at the same time. There the optimal switching frequency rises to approximately 200 kHz.

This effect has not been considered in Table VIII. In the second row, again the achievable power density for an increased power density is shown. But here, the increase of the ON resistance of the MOSFET due to the higher junction temperature has been considered. With the higher ON resistance and the resulting conduction losses, the maximum power density decreases down to 16 kW/L.

In the third row of Table VIII, it has been assumed that the thermal resistance between the chip and the heat sink is decreased. Again, this measure allows to shrink the volume of the semiconductor heat sink, since its temperature can be increased. The power density rises up to 16.1 kW/L. By increasing the operating temperature of the transformer, a value of 16.8 kW/L could be reached. The rising copper losses due to the rising resistivity limit the gain of power density.

Another option would be to decrease the switching losses by 50%. Due to the ZVS condition, this measure results in only small increase of the power density to 15.9 kW/L. A bigger step could be achieved by reducing the forward voltage drop of the rectifier diodes by a factor of 2, which results in a smaller volume of the heat sink. This would lead to a power density of 17 kW/L and an efficiency of 95.8%. A reduction of the conduction losses of the rectifier could be achieved by synchronous rectification. The $R_{DS,ON}$ of the applied MOSFETs, however, must be very low—in the considered case, $\approx 8 \text{ m}\Omega$ at 125 °C for cutting the losses in half. Since the rectifier diodes and their heat sink are already quite small, a synchronous rectifier would not help to improve the power density but only the efficiency.

In case all measures are combined (1+3+4+5+6—not 2), a power density of 21.6 kW/L and an efficiency of 96.3% can be achieved. Similar improvements can be expected for the other systems in case the same measures are taken. A further aspect that could influence the power density is the packaging of the components [31], which is out of the scope of this paper.

Summing up, this leads to two possible ways to improve the power density.

- 1) For components users/supply manufacturers:
 - a) improve the thermal coupling between the semiconductors and the heat sink (e.g., by low-temperature soldering);
 - b) apply advanced cooling methods for the passive components [2].
- 2) For device manufacturers:
 - a) further reduce the conduction losses of the power semiconductors;
 - b) reduce the magnetic materials HF losses;
 - c) decrease the thermal resistance between chip and housing/base plate;
 - d) increase operating temperatures.

Increasing the junction temperature while decreasing the chip size at the same time will not help to improve the power density of the converter significantly, since the ON resistance increases and the area of the heat sink, where the components could be mounted, is often a limiting factor.

VI. CONCLUSION

In this paper, three topologies for telecom supplies—a phase-shift converter with CTC and with CDR and a series–parallel resonant converter with CTC—have been optimized with respect to power density. Here, maximal 12 kW/L (19 kW/L pure component volume) is obtained for SPR. The optimal operating frequency with respect to the power density is approximately 135 kHz. For the phase-shift converter, 10 kW/L is obtained for a CTC and 7.8 kW/L for a CDR. Again, the optimal operating frequencies are relatively low—approximately 100 kHz for the CTC and 200 kHz for the CDR. Here, the efficiencies are 96.2% for the SPR, 95% for the CTC, and 94.8% for the CDR. These values slightly improve ($\approx 0.8\%$) if the converter is optimized for efficiency, but the power density decreases significantly.

The presented optimizations have been performed for operation at nominal output power—part load efficiency, soft switching range, costs or EMI issues, etc., have been neglected. In case these constraints are also considered, the achievable power density will decrease to approximately 6–8 kW/L for the resonant converter. Also, in combination of a PFC converter with a power density of 6–8 kW/L, a system power density of 3–4 kW/L for an air-cooled supply would result.

For increasing the power density, thermal management is especially decisive. Direct cooling of the magnetic components as presented in [2], and improving the thermal resistance between the chip and the heat sink by low-temperature solders, which could replace the thermal grease, are effective measures to reduce the system volume. Semiconductors with reduced losses or improved core materials are other possibilities to increase the power density and efficiency. These approaches, however, can only be followed by device/material manufacturers and are not directly accessible to supply manufacturers.

The largest gain results from optimizing the system parameters for the given specifications. The question which topology

should be applied is important, but does not influence the achievable power density as much as the optimization.

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