PWM Converter Power Density Barriers

Johann Kolar[*]	Member
Uwe Drofenik[*]	Non-member
Juergen Biela[*]	Non-member
Marcelo Heldwein[*]	Non-member
Hans Ertl[**]	Non-member
Thomas Friedli[*]	Non-member
Simon Round[*]	Non-member

Power density of power electronic converters has roughly doubled every 10 years since 1970. Behind this trajectory is the continuous advancement of power semiconductor devices, which has increased the converter switching frequencies by a factor of 10 every decade. However, today's cooling concepts and passive components are major barriers for a continuation of this trend. To identify such technological barriers, this paper investigates the volume of the cooling system and passive components as a function of the switching frequency for power electronic converters and determines the switching frequency that minimizes the total volume. A power density limit of 28kW/dm^3 at 300kHz is calculated for an isolated DC-DC converter, 44kW/dm^3 at 820kHz for a three-phase unity power factor PWM rectifier, and 26kW/dm^3 at 21kHz for a sparse matrix converter. For single-phase AC-DC conversion a general limit of 35kW/dm^3 results from the DC link capacitor. These power density limits highlight the need to broaden the scope of power electronics research to include cooling systems, high frequency electromagnetics, interconnection and packaging technology, and multi-domain modelling and simulation to ensure further advancement along the power density trajectory.

Keywords: Figures of Merit, Power density, Cooling system, Passive components

1. Introduction

The continual development of power electronic converters, for a range of applications, is characterized by the requirements for higher efficiency, lower volume, lower weight and lower production costs (cf. Fig. 1). A high efficiency is usually demanded at the nominal operating point, and in particular for redundant systems operating with partial loads [1], to ensure a good utilization of the energy resources and a low operating cost. The requirement for a reduced converter volume is driven, particularly, by the information technology applications where the rapid progress of integrated circuit technology had led to more compact systems with higher power consumption [2]. A small volume requirement allows a greater design freedom and a lower capital outlay in the building infrastructure [3]. Power electronic converters are increasingly becoming embedded in the final application. This allows a reduction in the installation cost and an improvement in electromagnetic compatibility. When fully integrated within the load, the volume is strongly limited by the main dimensions of the load system, such as variable speed drives for consumer white-goods and low power, point-of-load converters and voltage regulator modules (VRM) [4].

A low converter weight typically means a reduced amount of material is used and for stationary power supplies allows for simple installation, handling and maintenance, which is particularly important for mobile systems such as hybrid vehicles [5] and more electric aircraft [6].
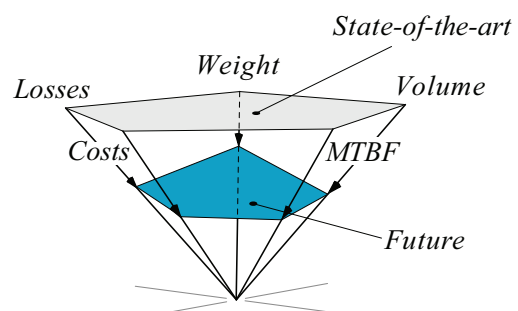
To compare the technological status and performance

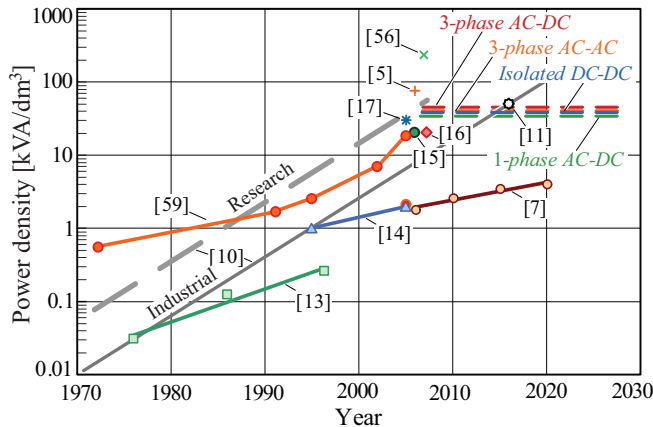Fig. 1. Development trends in converters.

Fig. 2. Power Density trend of industrial and research systems [10] and the Power Density Barriers.

of power electronic converters over a wider power range and with other disciplines, Figures of Merit (FOM) are defined by relating the converter volume, weight, cost and power loss to the output power [7]:

- Power Density, P_O/Vol, $[kW/dm^3]$
- Specific Power, P_O/G, $[kW/kg]$
- Relative Costs, $P_O/\$$, $[kW/\$]$
- Relative Losses, P_V/P_O, $[\%]$

(where P_O and P_V denominate the output power and the power losses, and Vol, G, and $\$$ are the converter volume, weight and cost). The relative loss FOM provides a better measure of the technological advancement for high efficiency systems than just efficiency ($\eta \approx 1 - P_V/P_O$) since an improvement of the efficiency from 95% to 96% appears as a relatively small increase, however it requires a reduction of the losses by around 20%.

To understand what is required for future power electronic developments, the FOMs are typically used in application specific roadmaps (e.g. US Freedom Car initiative [7] and Technology Reports of the Power Supplies Manufacturer Association (PSMA) [8]). There, power density is most frequently utilized to represent and evaluate the progress of the technology.

The trend has been for a large increase in the power density and the dynamic technological development over the last few decades covers the complete cross section of applications and converter types. This trend is shown in a diagram by Ohashi [9] [10] and is summarized in Fig. 2, where the trend line for industrial systems is differentiated from research only systems (since, typically, a period of 10 years is needed for the full introduction of a new concept into industry). In Ref. (10), a power density of $50kW/dm^3$ was emphasized by a special point (see Fig. 2) and indicated by Takahashi as the future power density (time frame>20 years) of inverters utilizing SiC power semiconductors [11].

The power density of 1 to 2 kW/dm^3, shown in Fig. 2 for the year 2000, has been confirmed by a study by the European Center of Power Electronics (ECPE) for industrial AC drive PWM inverters [12]. However in the literature, for individual applications, a less forward reaching development is described. As an example, Ref. (13) shows that for switching power supplies there was an increase in the power density of embedded converters from $0.5W/in^3$ ($30W/dm^3$) in 1976 to $2W/in^3$ in 1986 and it predicted a $4W/in^3$ ($244W/dm^3$) power density for 1996. Similarly, Ref. (14) shows a doubling of the power density of industrial power converters between 1994 and 2004. For automotive converters an increase in power density from the present value of $5kW/dm^3$ to $10kW/dm^3$ is required by 2020 [7]. This demands a doubling of the power density over the next 10 years.

These particular values have already been exceeded by converter systems used in today's hybrid vehicles (e.g. the power control unit of the Toyota Lexus RX400h). Furthermore, in concept studies, water-cooled motor-integrated inverters (with no EMI filter) for hybrid vehicles have reached power densities of $75kVA/dm^3$, e.g. the ECPE demonstrator shown in Fig. 3(a) [5]. Water-cooled, non-isolated, high frequency DC-DC converters presently achieve $25kW/dm^3$ [15] (including a single-stage EMI filter). For a water-cooled, unity power factor, three-phase AC/DC converter, a power density of $10kW/dm^3$ (including EMI filter) is shown in Fig. 3(b) [16]. Furthermore, an air-cooled DC-DC [17] has reached a power density of $30kW/dm^3$ without an EMI filter. The large variation in "state-of-the-art" power densities shows that a single power density value can not be used as a future predictor or target as the converter type and application has a major influence (Fig. 3). In particular, if the converter requires an EMI filter and other passive components then the possible power density is reduced compared to a "all-Si" converter where most of the volume is occupied by the semiconductor power switches.

Accordingly, for the main industrial power electronic applications, a doubling of the power density can be expected in the future. A doubling of power density typically requires an increase in the switching frequency by a factor of approximately 10. This increase in switching frequency can be achieved by using a higher switching frequency in an individual system or, more favorably, by the phase-shifted operation of parallel converters.

An important point to note for the power densities indicated so far is the overall system is frequently not considered and the essential elements, such as the cooling system, EMI filter, filter capacitors, housings and terminals are omitted from the power density calculation. Often, e.g., for power supply modules only the module volume is considered and not the volume needed to transfer the heat to the environment (by air flow or a heat sink) [18]. The same applies to systems with water cooling, where the pump and heat exchanger exhibit a relatively high space requirement [19]. The water effectively represents a transportation medium, like a heat pipe, but finally the heat must be dissipated by conventional radiators to the environment. Therefore, the published high power density figures are only a localized figure and are not representative of the final system power density.
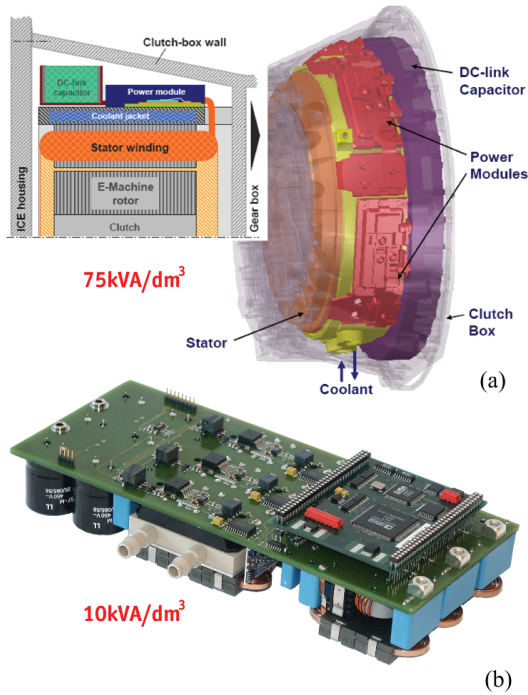
Fig. 3. Two water-cooled, ECPE demonstrators show that power density is strongly application dependent: (a) 75kW/dm^3, 8kHz motor integrated inverter [5], (b) 10kW/dm^3, 400kHz, 3-phase PFC with EMI filter and output capacitors [16].

Fig. 4. Dependency of converter volume on the operating parameters.

A clear overall view of the actual attainable power densities for various converter types, based on today's technology, is missing. However, only the understanding of technological barriers could initiate technological improvements and ensure a further development of the converters along the trend lines shown in Fig. 2.

A power electronic converter is formed from the following main elements:

- Power Semiconductor Modules
- Modulation and Control Circuit / Auxiliaries
- Power Passives (Filter Components/Transformers)
- Cooling System
- Interconnection / Packaging

The power density, ρ, is defined in Eq. (1) as the division of the power output by the total volume, where the total volume is typically a factor of two more than the sum of the partial volumes [12]

$$\rho = \frac{P_O}{Vol} \; < \; \frac{P_O}{\sum Vol_i} \cdots\cdots\cdots\cdots\cdots\cdots (1)$$

The cooling system and the EMI filter exert, in general, a substantial influence on the total volume [20] [16]. An increase in the power density is therefore possible, in principle, with an increase of switching frequency or an increase in the operating temperature of the power semiconductors (Fig. 4).

An increase in switching frequency leads, however, to an increase in the switching losses of the power semiconductors and results in a larger heat sink volume. A
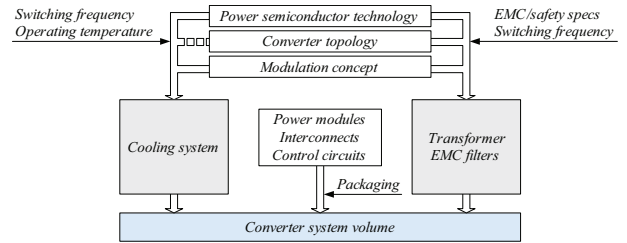
reduction in the relative switching loss increase with switching frequency can be achieved by utilizing soft switching. The switching frequency increase can then be used to decrease the size of the inductive components and thus to decrease the converter's total volume. However, there is an increase in the skin and proximity losses with the frequency increase, which finally leads to a thermal limit since a minimum volume is reached in which no more energy can be dissipated from the surface area. Furthermore, there is not a continuous decrease in the volume of the EMI filter with increasing switching frequency (see Figs. 17 and 18).

A decrease of the heat sink volume can be achieved by increasing the power device's junction temperature, however, this is limited by the maximum permissible operating temperature of the Si power semiconductors (175 to 200°C). Furthermore, a reduced operating temperature is usually set by the thermal stability of the most economical packaging materials and by the reduced life span caused by the increased temperature cycling. Alternatively, the cooling effort can be reduced for a given junction temperature by decreasing the thermal resistance between the junction and the case using, say, double-sided cooling of the power semiconductors [21].

So far the increase in the power density has been achieved by a substantial increase in the switching frequency. New SiC or GaN wide band-gap power semiconductors will make the realization of unipolar power semiconductors with small on-resistances possible for devices with blocking voltages of several kV. For the main industrial applications, this provides the future possibility of extremely low switching losses and a relatively unrestrained ability to optimize the passive components over several decades of switching frequency. Furthermore, since these new semiconductors have higher maximum operating junction temperatures, this will lead to a drastically reduced cooling effort. This is possible because the new power semiconductors have a higher thermal conductivity and small layer thicknesses, however higher operating temperatures depend on developments of appropriate packaging materials and soldering techniques. The availability of power semiconductors with high operating temperatures and extreme switching speeds will therefore move the focus to the passive components since they become the power density limiting components.

This paper analyzes the way the volume of the main passive components and the cooling system changes with switching frequency and, therefore, determines the re-

sulting power density limits. The fundamental types of power electronic converters are considered separately and the volumes of the respective main passive components (indicated in the parentheses) are minimized by properly selecting the operating frequency. The converter types are:

- Isolated DC-DC Converter
  (Transformer and Output Inductors);
- Single-phase unity power factor AC-DC converter
  (Output Capacitors);
- Three-Phase AC-DC Converter
  (EMI Filter and Input Inductors);
- Three-Phase AC-AC Indirect Matrix Converter
  (EMI Filter und Common-Mode Output Inductors).

The considerations are, in each case, for an individual system with a power rating of 5 kW in order to ensure validity of the results in the power range of 1 to 10 kW.

In order to relate the findings to today's semiconductor technology the cooling effort required for today's best available semiconductor combinations is considered in addition to the main passive components. From this a maximum power density results at an optimal operating frequency that clearly identifies today's technological limits and provides a basis for road-mapping activities (ECPE [22], CPES [23], AIST [24]).

In order to guarantee a minimum heat sink volume and/or high power density, section 2 presents how the fin geometry of the heat sink can be adapted so that maximum cooling ability for each unit volume is achieved. This cooling ability then is used to compute the power density limit. In sections 3 to 5 the basic types of power electronic converters are analyzed for power density. This paper concludes with a discussion on the measures needed to increase the power density based on existing technologies.

2. Thermal Management

2.1 Heat Sink Optimization for Forced Convection In order to optimize a heat sink employing forced convection, one has to consider the thermal resistance of the heat sink material, the thermal resistance due to convection, and the temperature increase of the air flowing through the heat sink channels. The following optimization is based on a typical heat sink geometry shown in Fig. 5(a), where the heat generating power devices are placed on a base plate and a number of fins extend out from the opposite side of the base plate.

Generally, the fin geometry provides a pressure drop $\Delta p_{CHANNEL}$ for the air flow through the channels. The air flow is driven by a fan that is characterized by a pressure-flow curve (Fig. 5(b)). Based on the flow and air properties, the convective heat transfer from the fin surface into the air in the channels can be calculated. The heat flow through the heat sink can be described by the thermal equivalent circuit shown in Fig. 6. All these relations can be described employing analytical and empirical equations [25] [19], which allows a systematic optimization of the fin geometry for a given fan.

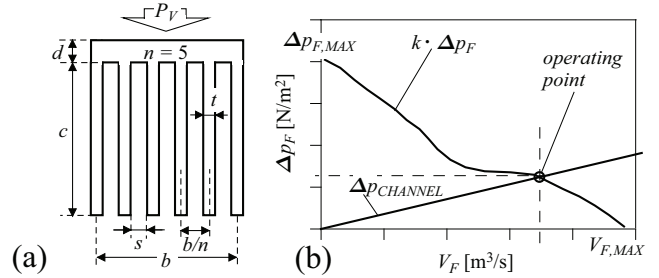A result of a systematic optimization is shown in Fig.

Fig. 5. (a) Heat sink geometry with thermal losses P_V in the area $b \cdot L$, where L is the heat sink length. (b) Fan pressure dependency on air flow V_F. Pressure losses at the channel inlet, Δp_F is multiplied with the fin spacing ratio $k = s/(b/n)$ [19].
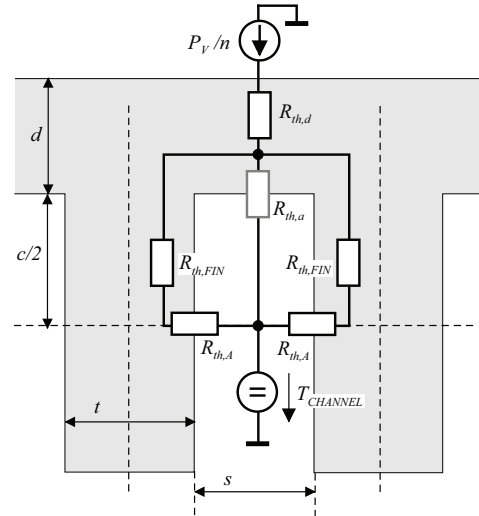

Fig. 6. Thermal equivalent circuit of the heat flow from power module through heat sink base plate and fins into the air flowing through the channel.

7, where the thermal resistance of the heat sink surface to ambient, R_{th}, is given in dependency of the normalized channel width k for different fin numbers [19]. The theoretical optimum design requires 26 fins with fin thickness 0.54mm and channel width 1.0mm, resulting in a thermal resistance of 0.26K/W. Since the optimum is located at a very flat section of the curves, one can select a sub-optimum that may be easier to manufacture but still provides a thermal resistance close to the theoretical minimum.

For comparison of different heat sink designs concerning power density, we calculate the "cooling system performance index $(CSPI)$" [19] as

$$CSPI \left[\tfrac{W}{K \cdot dm^3} \right] = \frac{1}{R_{th} \left[\tfrac{K}{W} \right] \cdot Vol_{CS} [dm^3]} \cdots (2)$$

Experimental prototypes of the optimized heat sinks for typical 5kW converters are shown in Fig. 8. Based on measured R_{th}-values, we obtain $CSPI_{Al} = 17.5 \text{WK}^{-1}\text{dm}^{-3}$ for the aluminum heat sink and $CSPI_{Cu} = 21.6 \text{WK}^{-1}\text{dm}^{-3}$ for the copper heat sink. Both $CSPI$ values are 20% below the theoretical optimum because manufacturing constraints do not allow
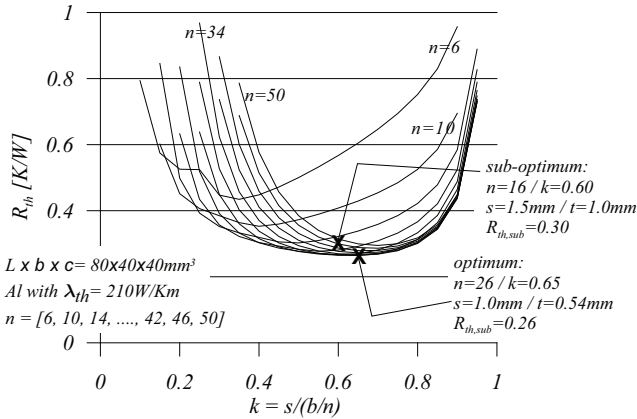
Fig. 7. Sensitivity of thermal resistance, R_{th} for geometric heat sink (Fig. 5) parameter variations. Aluminum heat sink of L=80mm, b=40mm, c=40mm, d=10mm, with SanAce40/50dB fan
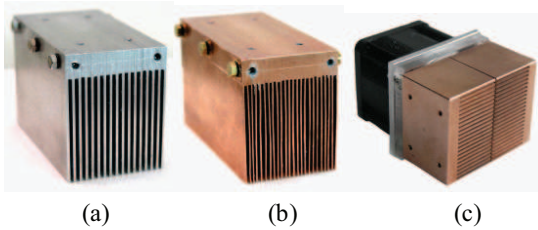

(a) (b) (c)

Fig. 8. Optimized heat sinks for SanAce 40x40 x28mm/50dB fan [26] with A_{CHIP}=32cm², b=c =40mm (a) Al, n=16, s=1.5mm, t=1mm, d=10mm, L=80mm, R_{th}=0.26K/W; (b) Cu, n=23, s=1.3mm, t=0.5mm, d=10mm, L=80mm, R_{th}=0.21K/W; (c) Cu, n=21, s=1mm, t=1mm, d=5mm, L=27mm, R_{th}=0.27K/W.

to fully exploit the theoretical optimum [27]. Fig. 8(c) shows a different heat sink design with two opposite base plates that better utilizes the heat flow through the fins. This results in a higher $CSPI = 30.9\mathrm{WK^{-1}dm^{-3}}$. For a detailed discussion and a comparison with commercially available heat sinks of significantly lower performance, see Refs. (19) and (27).

2.2 Thermal Limits of the Converter Power Density The power density of a converter is limited by the power density of the cooling system by

$$\rho_{SYS} < \rho_{\lim} = \frac{P_O}{Vol_{CS}}[\frac{\mathrm{W}}{\mathrm{dm}^3}]\cdots\cdots\cdots (3)$$

The volume of the cooling system can be expressed based on the definition of the $CSPI$ as

$$Vol_{CS} = \frac{1/R_{th}}{CSPI} = \frac{P_V}{\Delta T_{s-a}}\frac{1}{CSPI}\cdots\cdots (4)$$

with converter thermal losses of

$$P_V = (1 - \eta)\,P_i\cdots\cdots\cdots\cdots\cdots (5)$$

where P_i is the input power and η is the converter efficiency. In this analysis it is assumed that all of the
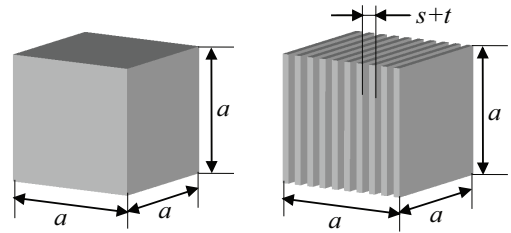

Fig. 9. (a) Surface area of the cube employing natural convection is proportional to the square of the length ($A_{conv} \sim a^2$). (b) 'Internal' surface area consisting of fins is proportional to the third order of the length ($A_{conv} \sim a^2 \cdot a/(s+t) \sim a^3$).

losses are dissipated by the heat sink. The temperature difference ΔT_{s-a} describes the temperature drop from heat sink surface to ambient. Substituting the converter output power by

$$P_O = \eta\,P_i\cdots\cdots\cdots\cdots\cdots\cdots (6)$$

results in a general expression of the power density of the cooling system as

$$\rho_{\lim} = \frac{P_O}{Vol_{CS}} = \frac{\eta}{1 - \eta}\Delta T_{s-a}\,CSPI\,[\frac{\mathrm{W}}{\mathrm{dm}^3}]\cdot\cdot (7)$$

which provides an upper limit for the converter power density. In a first approximation, we assume that the thermal resistance between semiconductors and heat sink surface is small compared to the thermal resistance associated with convection at the heat sink surface.

As shown in Fig. 9(a), the natural convection at the outer surface of a cube-shaped converter is proportional to the square of its base length. If forced convection is employed by realizing part of the converter volume as heat sink plus fan, the effective cooling surface, and, therefore, heat transfer to ambient via forced convection, is proportional to the third order of the base length (Fig. 9(b)). Here, the number of fins $n_{FIN} = a/(s+t)$ is defined by fin thickness t and channel width s. Since the effective cooling surface for employing a heat sink is proportional to the volume, the previously defined $CSPI$, which can be interpreted as 'volumetric thermal conductivity', is verified in Eq. (4).

According to Eq. (7), for a converter system with an efficiency $\eta = 0.97$, employing a cooling system characterized by $CSPI = 20\mathrm{WK^{-1}dm^{-3}}$, and operating in an environment with ambient temperature $T_a = 45°C$, the power density limit is $\rho_{\lim} = 29\mathrm{kW/dm^3}$ for a heat sink temperature of $T_s = 90°C$. A higher heat sink temperature of $T_s = 135°C$ would increase the theoretical limit of the power density to $\rho_{\lim} = 58\mathrm{kW/dm^3}$.

3. Magnetic Devices

Magnetic components, such as transformers and inductors, typically occupy a significant share of the converter volume and are of particular importance in isolated DC-DC converters. In this section, the maximum
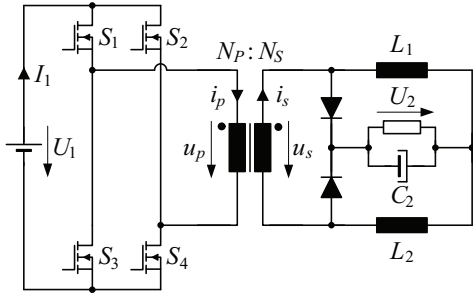
Fig. 10. 5kW DC-DC converter example used to determine the magnetic components power density.
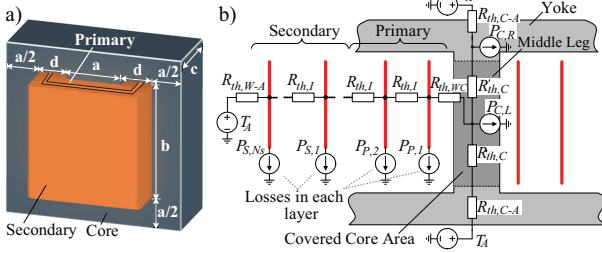

Fig. 11. Transformer (tube type) (a) dimensions with primary and secondary windings, (b) thermal equivalent circuit of the transformer.

power density of transformers and inductors used in DC-DC converter systems is determined. The considerations are based on a DC-DC converter (Fig. 10) used in telecom applications, where a high input voltage (400V) is stepped down to 48V at a power level of 5kW. The method for calculation of the power density is also valid, with a slight adaptation, for other converters.

3.1 Transformer Power Density and Loss Model The calculation of the transformer power density is based on a two-winding transformer with an nearly sinusoidal voltage U_P and current I_P in the primary and U_S and I_S at the secondary. The number of turns is represented by N_P and N_S and since a converter in the range of several kilowatts, with relatively high winding currents, is considered, it is assumed that only one turn per layer of the winding is realized. This could be either a foil winding or several parallel connected solid wires, which can be transformed in an equivalent foil winding [28]. The thickness of the foil (or diameter of the wires) significantly influences the skin- and proximity-effect losses in the winding. In order to minimize these losses, the optimal thickness must be calculated for each operating frequency, f, using, for example [28],

$$d_{Opt,v} = \frac{1}{\sqrt[4]{\frac{5N_v^2 - 1}{15}}} \cdot \frac{\sqrt{2}}{\sqrt{\omega \mu_0 \sigma}} \cdots\cdots\cdots\cdots (8)$$

where N_v denotes the number of layers, σ is the conductivity and $\omega = 2\pi f$. With the thickness of the foils $d_{Opt,v}$, the copper fill factor k_{CU} and the thickness of the bobbin d_{bobbin}, the width of the winding window d (cf. Fig. 11(a)) is

$$d = \frac{1}{k_{CU}} (N_P d_{Opt,P} + N_S d_{opt,S}) + d_{bobbin} \cdots\cdots (9)$$

and the volume of the winding $Vol_{Wdg} = b \cdot d \cdot l_W$ is calculated, where l_w is the length of the winding. By applying the optimal thickness of the layers, the AC losses are 4/3 times the DC losses. Thus, the overall winding losses can be calculated by

$$P_{Wdg} = \frac{N_P l_W}{\sigma b d_{Opt,P}} \frac{4}{3} I_P^2 + \frac{N_S l_W}{\sigma b d_{Opt,S}} \frac{4}{3} I_S^2 \cdots\cdots\cdots (10)$$

With the assumed sinusoidal voltages and currents, a sinusoidal flux density with a peak amplitude of

$$B_P = \frac{\sqrt{2} U_P}{N_P A_{Core} \omega} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (11)$$

results and the core losses in the different core sections can be simply calculated with the Steinmetz equation [29]

$$P_{Core} = C_m f^\alpha B_P^\beta Vol_{Core,\nu} \cdots\cdots\cdots\cdots\cdots (12)$$

where $Vol_{Core,\nu}$ is the volume of the considered section and C_m, α and β are material dependent coefficients. The overall core volume is given by

$$Vol_{Core} = (b + a) \cdot c \cdot 2a + 2d \cdot a \cdot c \cdots\cdots\cdots (13)$$

For a converter with a non-sinusoidal flux density the equations published in Ref. (30) should be applied.

From the core and winding losses, the temperature distribution in the transformer is calculated using a thermal model as shown in Fig. 11(b). It is assumed that the temperature within each layer is approximately uniform and that the heat flows from one layer to the next via the insulation represented by thermal resistance $R_{th,I}$. In the outer layer, the heat is dissipated to the ambient via $R_{th,W-A}$ and at the inner layer it flows via the bobbin $(R_{th,W-C})$ to the core. In the core the heat flows from the middle leg to the yokes where it is dissipated to the ambient via $R_{th,C-A}$. To simplify the calculations it is assumed that the winding losses are uniformly distributed within the winding, which is approximately true since the share of the proximity effect losses on the total losses is relatively small for an optimized layer thickness.

The hottest spots of the transformer are the inner layer of the winding and at the center of the middle leg where the core is covered by the winding and the heat can not be dissipated directly to the ambient.

The thermal resistance between the core/winding surface and the ambient is calculated by

$$R_{th,\nu-A} = \frac{1}{\alpha S_\nu} \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots (14)$$

where α is the heat transfer coefficient for the surface S_ν. This could be calculated by empirical equations for natural convection [31] [33] and forced air cooling [33] [32].

This method has been validated by comparing the results for a 1kW transformer with natural convection [34]
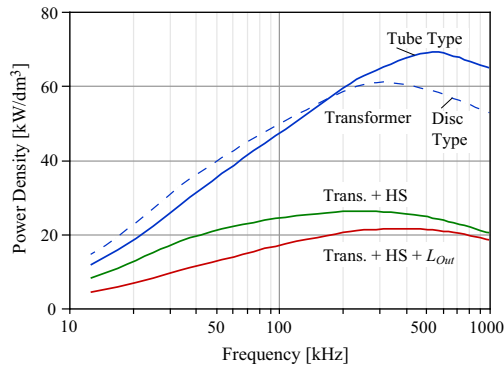
Fig. 12. Power density of the transformer with forced air cooling (top line) including the fan volume. Volume of the semiconductors' heat sink is added (middle line) and the volume of the output inductors is also added (bottom line).

and the results for the calculations in Ref. (35).

In Fig. 12, the power density of the transformer for the 5kW telecom power supply with different operating frequencies is shown. In this case, forced air cooling of the magnetics is considered, where the heat transfer coefficient, Eq. (14), is significantly lower and more heat can be dissipated via the surface than for natural cooling [34]. For calculating the effective power density the volume of the fan and of the air space around the transformer must be considered. The calculation of the fan volume assumes the fan power consumption is limited to 10 W and the channel volume flow is approximately 2/3 of the maximum fan volume flow.

A maximum power density of 69kW/dm^3 could be achieved by the tube type transformer at a switching frequency between 500 and 600kHz. The disc type design reaches 61kW/dm^3 at 300kHz. If the volume of the semiconductors' cooling system, calculated with a $CSPI = 30$WK^{-1}dm^{-3}, is included the maximum power density decreases to approximately 26kW/dm^3 at 250kHz. The conduction and ZVS switching losses of the full bridge and the conduction losses of the output rectifier are based on measurements of APT50M75 MOSFETs and APT100S20B Schottky Diodes. Since the switching losses increase linearly with frequency the optimal operating frequency decreases.

When the volume of the two output inductors is also considered the power density further decreases to 21kW/dm^3 at 400kHz. Since the value of the required output inductance decreases linearly with frequency, the optimal operating frequency increases [34].

3.2 Magnetic Devices plus Heat Sink   In order to increase the power density further an indirect cooling system, as shown in Fig. 13, is applied. Here the transformer losses are dissipated via a Heat Transfer Component (HTC) and an additional heat sink/fan [36].

The thermal model must be adapted to the new cooling method. In order to reduce the temperature drop along the core ($\lambda \approx 4$Km^{-1}W^{-1}) 2mm thick copper foils are connected in parallel to the core. For the results presented here it has been assumed that the thermal conductivity of the HTC is very high (≈ 30000Km^{-1}W^{-1})
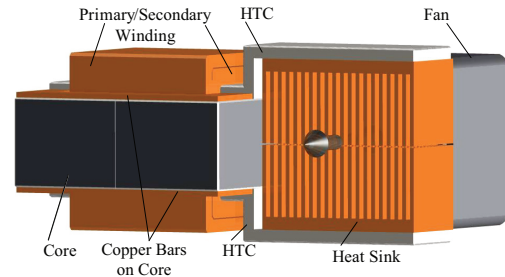

Fig. 13. Transformer with double sided indirect air cooling via a Heat Transfer Component (HTC), a heat sink and a fan.
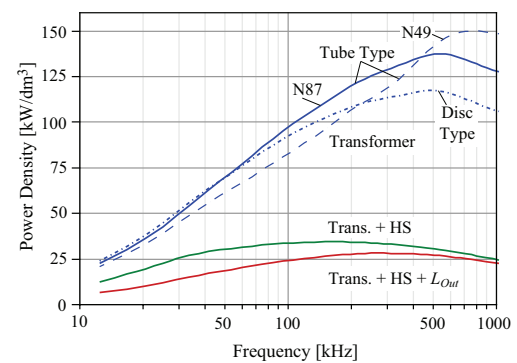

Fig. 14. DC-DC converter power density with indirect air cooling (top) including the transformer's heat sink and fan volume. The volume of the semiconductors' heat sink (middle) and the volume of the output inductors (bottom line) is accounted for.

so that the temperature drop along the HTC is negligible.

The volume of the heat sink and the fan for the transformer can be calculated with the $CSPI$, Eq. (2), where the thermal resistance of the heat sink is required. In order to achieve a minimal total volume the thermal resistance must be included in the optimization of the transformer. In Fig. 14, the resulting power density of the transformer including the volume of the HTC, Cu-bars, heat sink and fan is shown in the upper traces. There, a maximal power density of approximately 138kW/dm^3 for the transformer with ferrite core material of EPCOS N87, including heat sink and fan, is achieved. With the high frequency EPCOS N49 ferrite material even a power density of 150kW/dm^3 at 800kHz could be achieved. Since the N49 material out performs N87 material only at very high frequencies the overall system power density is smaller with N49 than with N87. This is caused by the relatively small share of the transformer volume on the overall system volume and the volume of the semiconductor heat sink increasing with switching frequency. With the disc type transformer a lower power density of 117kW/dm^3 at 500kHz results.

If the heat sink for the semiconductors is also considered the value decreases to 34kW/dm^3. For the system including the output inductors a maximal value of 28kW/dm^3 at 300kHz is achievable. Compared to these values the power density of the complete DC-DC converter, including power switches, controller and capaci-
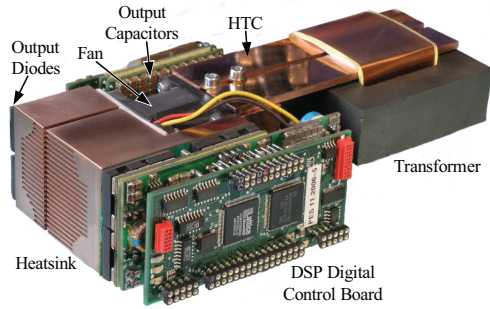
Fig. 15.   5kW, 10kW/dm³ DC/DC Converter.

tors, is lower by a factor of 2.5 to 3. Using this approach a 1U, 5kW, 10kW/dm³ telecom DC-DC converter (Fig. 15) has been developed at ETH Zurich as part of the ECPE demonstrator program.

4.   EMC Filter Impact on Power Density

The EMC filter typically occupies a significant volume of a power converter and therefore influences the power density. The EMI filter volume is dependent on the converter topology and switching frequency. In order to illustrate the influence the EMI filter has on power density, two converter topologies, a three-phase AC-AC Sparse Matrix Converter (SMC) [37] and a three-phase unity power factor Vienna Rectifier (VR) [38], are selected for in-depth analysis. The EMC filter design for these two topologies is performed to obtain minimum filter volumes, based on typical power filter design practices.

4.1   Design of EMC Filters   The total EMC filter is comprised of a combination of multiple high performance differential (DM) and common (CM) mode filter stages, which fulfill the conducted emissions (CE) requirements of CISPR 22-Class B from 150kHz to 30MHz [39]. The limits used in the design procedure are Class B minus 6dB in order to ensure compliance. The design is based on an optimization routine [40], which calculates the filter components values, based on a series of constraints, that lead to minimum filter volumes.

A series of simplifications are performed in order to reduce the calculation effort. The simplifications are:

- the harmonic content of the switched voltages is estimated by using simplified envelopes;
- the three-phases are symmetric;
- the parasitics, inter-component couplings and component tolerances are neglected;
- the capacitor values and core dimensions are available in a continuous range;
- only natural air cooling is used for the inductors.

The starting point of any EMC filter design is the determination of the frequency spectrum for the DM voltages and currents and the CM voltages. These voltages are compared to the desired limits at the frequency of interest, $f = \omega/2\pi$, which is 150kHz for switching frequencies lower than 150kHz or the switching frequency for higher frequencies. This then gives the required attenuation, Att_{req}, at the frequency of interest.
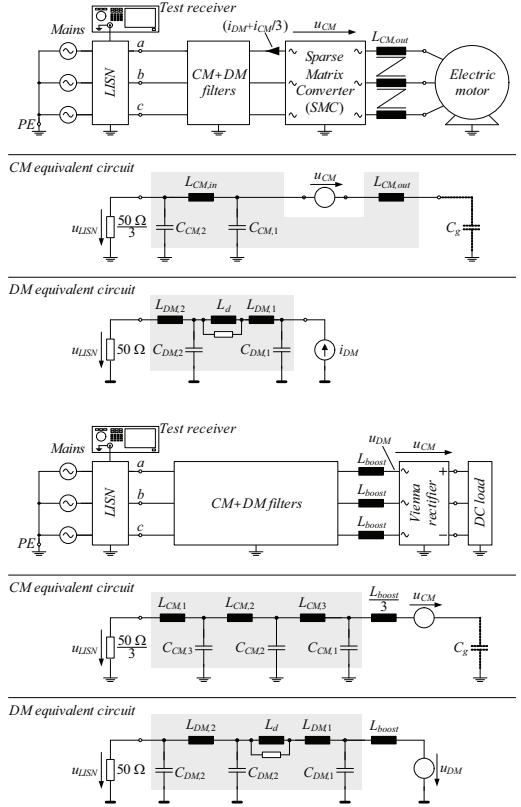

Fig. 16.   Converter and filter topologies with simplified equivalent circuits for (a) Sparse Matrix Converter, and; (b) Vienna Rectifier.

The two power converter systems are presented in Fig. 16, along with the simplified equivalent circuits used for the filter design calculations, where the LISN circuits are replaced for 50Ω resistors representing the input sensing resistance of a test receiver. The choice of a two- or three-stage filter is dependent on the required attenuation, the cost and the volume of the filter [41]. It is shown in Fig. 16(a) that a two-stage filter is considered for the SMC and in Fig. 16(b) a three-stage filter is considered for the VR. With the SMC, an output CM choke is included, since the CM voltage at the input terminals of the electric motor must be limited. The output cable and the machine usually present a high capacitance to protective earth (PE) when compared to the capacitance between the converter's semi-conductors and cooling system. Therefore, for simplicity reasons, this is the only capacitance to PE considered in the design of the SMC filter. The first DM capacitors $C_{DM,1}$ are chosen in order to limit the high frequency ripple of the input voltages of the SMC to 7.5% of the peak input RMS voltage. For the VR, the boost inductors, L_{boost}, are also considered as part of the filters, although their design is based on high performance ferrites and limiting the input peak-to-peak current ripple to 20% of the peak input current.

4.2   Multi-stage DM Filter Volume Minimization   In order to guarantee that the designed filters are of minimal volume, the desired component values can be derived as functions of two equations, namely

the required attenuation at a given frequency and the total volume, which is to be minimized. The main assumptions are; the inductors are designed for their low frequency RMS current, the parasitics of the components do not influence the attenuation at the relevant frequency, and the boost inductor is not included and its value is defined by current ripple requirements.

In order to simplify the problem, the asymptotic approximation of the attenuation for an LC filter is used [41]. It can be proven that for the smallest total inductance, each of the individual inductors must have the same value and the same is valid for the capacitors. Therefore, only one inductance and one capacitance value are left to minimize the volume. Let us consider only the case of a single LC stage, which shows the basic principle of minimizing a filter's volume. The required attenuation, Att_{req}, is

$$Att_{req} = \frac{k_{att}}{L \cdot C}, \text{ where } k_{att} = \frac{1}{\omega^2} \cdots\cdots\cdots\cdots (15)$$

The total volume of the filter is the sum of the volume of the inductor and the volume of the capacitor. It can be assumed that the volume of this type of component is directly related to their stored energy (based on their nominal voltage U_{nom} or current I_{nom}), so that volumetric coefficients for inductors k_L and capacitors k_C are defined as

$$Vol_L = k_L \cdot L \cdot I_{nom}^2 \ \& \ Vol_C = k_C \cdot C \cdot U_{nom}^2 \ (16)$$

These coefficients can be derived based on data sheet information from capacitors and on a series of inductor designs [34]. The total filter volume can be expressed as

$$Vol_{filt} = k_L L I_{nom}^2 + k_C \frac{k_{att}}{L \cdot Att_{req}} U_{nom}^2 \cdots\cdots (17)$$

by using Eqs. (15) and (16). By differentiating (17) with L the minimum volume point can be found and the values for the components are defined by

$$L = \frac{U_{nom}}{\omega \cdot I_{nom}} \sqrt{\frac{k_C}{k_L \cdot Att_{req}}},$$

$$C = \frac{I_{nom}}{\omega \cdot U_{nom}} \sqrt{\frac{k_L}{k_C \cdot Att_{req}}} \cdots\cdots\cdots\cdots (18)$$

The same procedure can be extended to multi-stage filters. Thus, minimal volume filters can be designed based on the ratings of the components and their volumetric coefficients.

4.3 Multi-stage CM Filter Design   For the design of the CM filters, the converters are considered as voltage sources u_{CM} (Fig. 16), which are dependent on modulation, input and output voltages and switching frequencies. The CM filter of the SMC is split into an output CM inductor and a two-stage CM filter at the input. The aim of the output inductor is to keep

the CM RMS voltage at the input terminals of the motor lower than 15V for any switching frequency and any capacitance to ground, C_g, values. The remaining components are responsible for providing the total required attenuation.

Two types of components are considered for the CM filters: ceramic capacitors which are Y2 rated [43] and CM inductors based on toroidal nanocrystalline cores [45], which are "state-of-the-art" in their class. An earth leakage current limitation of 3.5mA is used and this bounds the total capacitance per phase to approximately 40nF at 50 Hz, which is reduced to 30nF per phase and evenly distributed among the filter stages.

The design of the CM inductor is more involved and a maximum window factor of 0.28 is considered. The design takes into consideration the variation of the complex permeability of the cores as well as the total losses, where the maximum temperature rise is limited to 75°C.

The cores of the CM inductors are specified as a function of the required area product $A_e A_w$, which is a function of the switching frequency, rated DM current, CM voltage, number of windings, window factor, maximum current and flux density at the switching frequency or at the mains frequency (50/60 Hz). A series of CM chokes are designed in order to empirically determine linearized functions that are used for the filter calculations. Based on these designs the maximum current and flux densities are curve fitted and these curves are used in an automatic design procedure of the inductors.

The area product presents a quite predictable relation to the volume of an inductor [34]. A relation of the type $k.A_e A_w^{\frac{3}{4}}$ is commonly used, although for this work a power of 0.668 has been used for higher accuracy. Another approximated relationship is the maximum impedance at a given frequency and current as function of the area product [34]. With these relationships it is possible to estimate the volume of a CM choke as a function of rated current and required impedance at the frequency of interest.

4.4 Sparse Matrix Converter Power Density Limits   Using the presented filter design procedure the volume of the filter components are derived as function of the converter rating, switching frequency and total capacitance to ground C_g. The total volume of the EMC filter and forced-air cooled heat sink ($CSPI = 25\text{WK}^{-1}\text{dm}^{-3}$) for an SMC is displayed in Fig. 17. The contributions of the DM and CM filter volumes as well as the volume of the first DM capacitors $C_{DM,1}$ for a capacitance to ground C_g value of 20nF are given. It is observed that the DM filters dominate the filter's volume for lower switching frequencies. The increased volume of the CM filter at lower frequencies in Fig. 17(a) is a result of the increasing size of the output CM inductor. An increased total volume is seen at 150kHz due to the CE requirements and the necessity of filtering low order switching frequency harmonics.

From these results it is possible to derive the power density curves as a function of switching frequency. This is presented in Fig. 17(b) for three different capacitor technologies [34] [42] [43]. Since the power semiconduc-
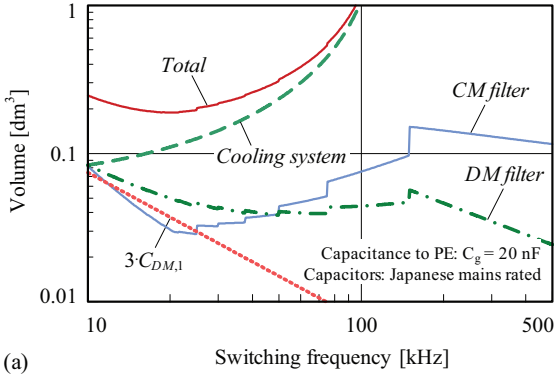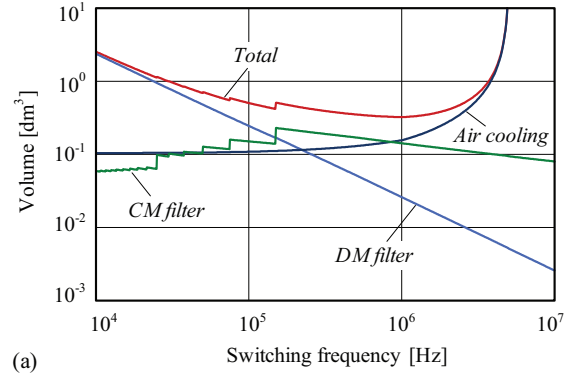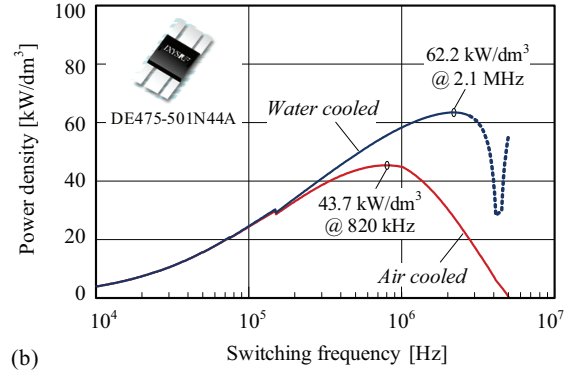
(a)
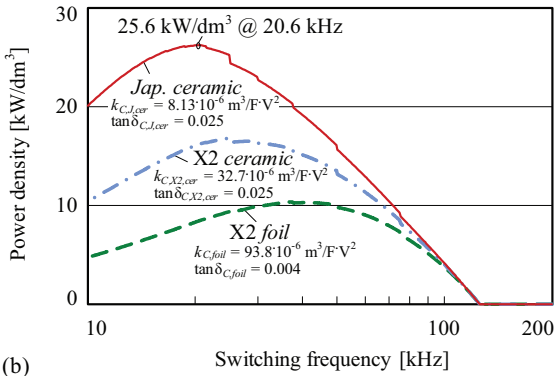
(b)

Fig. 17. (a) Total and partial EMC filter and heat sink volumes for a $230V_{RMS}$, M=0.7, 50 Hz, 5kW SMC. (b) Power density for three different capacitor technologies [34] [42] [43] as a function of the switching frequency considering only the EMC filter.

(a)

(b)

Fig. 18. (a) Total and partial volumes of EMC filters and cooling system for a Vienna Rectifier ($230V_{RMS}$ phase voltage, 800V output, 10kW output and X2 ceramic capacitors for $C_g = 2$ nF. (b) Power density for air and water cooling considering only the EMI filter and cooling system.

Fig. 19. Single-phase PFC circuit.

tor losses reduce the achievable power density at high switching frequencies, it is seen that a power density limit of 25.6kW/dm^3 is achieved with Japanese mains rated ceramic capacitors at an output stage switching frequency of 20.6kHz. For the foil capacitors the frequency is now 45kHz, but with much lower power densities.

4.5 Vienna Rectifier Power Density Limits The same procedure for the calculations is made for a 10kW VR and the results are shown in Fig. 18. The calculations for the volume of the cooling system of the power semiconductors (forced air and water) are included. For the forced air cooling system, a $CSPI = 25\text{WK}^{-1}\text{dm}^{-3}$ is used. While for the water cooled system the dimensions in Ref. (46) are utilized. The semiconductor losses are estimated for a IXYS DE475-501N44A RF MOSFET and two paralleled Cree SiC Schottky Diodes (10A/ 600V) [16] leading to a required thermal resistance from the heat sink to ambient in order to limit the junction temperatures to 125°C with an ambient temperature of 45°C. A total capacitance to ground of $C_g = 2$nF is considered. The DM capacitors are X2 rated ceramics [43]. In Fig. 18(a) it is seen that CM filter and cooling system volumes are the main contributors to the total volume and that a minimum volume is achieved for a switching frequency around 1 MHz for an air cooled system. The achievable power densities, for just the EMI filter and cooling sys-

tem, are presented in Fig. 18(b), where it is seen that a water cooled system is capable of further increasing the power density for frequencies higher than 1 MHz.

5. DC Link Capacitors

For power electronic systems based on a DC voltage link, the DC link capacitors contribute significantly to the converter volume and hence influence the power density of the total system. The DC link capacitors in a typical single-phase PFC (Fig. 19) are required to to "absorb" the high-frequency switching component i_H of the converter's output current i_Z, to equalize the power pulsations in case of single-phase systems, and to serve as an energy storage for providing hold-up. Hence, the selection of the capacitor must consider its rated current as well as the required storage capacitance. Typically the choice of capacitor is between electrolytic and foil types.

Fig. 20. Comparison of rated specific volumetric current densities s_C of 400V electrolytic capacitors. Family types: leaded (EE, M), snap-in (B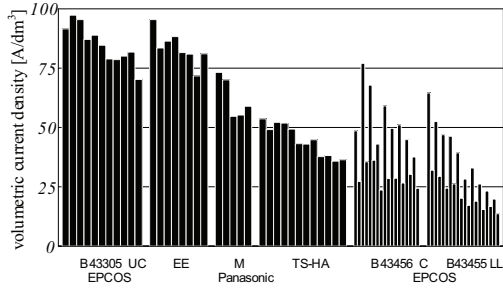43305, TS-HA), screw-terminal (B43456C, B43455LL); from left to right each type is increasing capacitance and size. B43456C and B43455LL are shown for natural and "base-plate" cooling.

5.1 Electrolytic Capacitor   Due to their fairly high current carrying capability and their high specific energy density, electrolytic capacitors are widely used. As a more detailed analysis shows, these capacitors primary have to be dimensioned according to the current carrying capability if special requirements concerning hold-up or over-voltage protection are neglected. Unfortunately, the rated RMS current of electrolytic capacitors cannot be easily estimated assuming that the specific volumetric current density s_C [A/dm^3] is approximately constant over a wide range of capacitor types. The rated capacitor current I_N for a specific loss resistance R_{ESR} essentially depends on the cooling condition of the component. Consequently, capacitors of a smaller volume (leaded or snap-in types) show a considerably higher specific current capability compared to large-can (screw-terminal) types (cf. Fig. 20).

5.2 Foil Capacitor   In three-phase systems, which require no low-frequency energy storage, the application of foil capacitors is possible. For example, a 15μF/1050V foil capacitor (EPCOS B32678) is specified to a rated current of I_N=29A. A volume of V_C=0.1dm^3 leads to a specific current density of almost s_C=290A/dm^3, which is about 3-times higher than very good electrolytic capacitors. The very high current capability of foil capacitors is a key advantage to maximize power density, however, due to the low capacitance value and the high Q-factor, foil capacitors easily tend to resonant.

5.3 DC Link Capacitor Current Stress   Using a similar procedure as detailed in Ref. (47), the DC link rms current components of a single phase PFC (Fig. 19) can be determined to be

$$I_Z = I\sqrt{\frac{16}{M3\pi}} \qquad I_C = I\sqrt{\frac{16}{M3\pi} - 1} \cdots \cdots (19)$$

where I is the ripple free DC output current and M is the modulation index. Considering the line-frequency power flow and assuming that the high- and low-frequency components of i_C are not correlated, the currents are given by

$$I_C^2 = I_L^2 + I_H^2;\ I_L = \frac{I}{\sqrt{2}};\ I_H = I\sqrt{\frac{16}{M3\pi} - \frac{3}{2}}.(20)$$

For a typical application where $M \approx 0.8$, this leads to $I_Z = 1.46I$, $I_C = 1.06I$, $I_L = 0.71I$ and $I_H = 0.79I$. For three-phase systems, such as a six-switch PFC, no line-frequency current I_L will appear, and the current stress of the DC link capacitor originates from the switching currents. Using the relations derived in Ref. (48) the DC link rms quantities are given by

$$I_Z = I\sqrt{\frac{20\sqrt{3}}{9M\pi}} \quad I_C = I_H = I\sqrt{\frac{20\sqrt{3}}{9M\pi} - 1} \cdots (21)$$

and are valid for unity power factor operation. For PFC-applications, a $M \approx 0.8$ is frequently used, which leads to $I_Z = 1.24I$ and $I_C = I_H = 0.73I$.

5.4 Single Phase DC Link Dimensioning   As indicated by Eq. (20), the DC link capacitor current i_C of a single phase converter does not only contains switching frequency components but is also characterized by a low-frequency component. The rated current I_N of electrolytic capacitors is characterized by a frequency dependency due to the fact that the capacitors loss resistance R_{ESR} decreases for increasing frequency. Consequently, the manufacturers usually specify the rated current I_N separately for the low and high frequencies or by $I_{N,L}$ and a multiplier k_C ($I_{N,H} = k_C I_{N,L}$) where $k_C \approx 1.4 \ldots 2$.

5.5 DC Link Capacitor Power Density Limit To provide an estimation of volume inherently required for realizing the DC link, the PFC's through-put power $P_{PFC} = U \cdot I$ (cf. Fig. 19) is related to the capacitor's volume V_C to define a power density $\rho_{PFC} = P_{PFC}/V_C$ for the DC link. Combining the relations derived before ($I_L = I/\sqrt{2}$, $I_{N,L} = 1.2I_L$) and using $I_{N,L} = s_C \cdot V_C$ we obtain $\rho_{PFC} = U \cdot s_C/0.85$. Choosing $s_C = 80$A/dm^3 (Fig. 20), which is valid for modern compact capacitors in the power range typically used for single-phase converters, and a DC link voltage of U=400V, we obtain a specific power density of 38kW/dm^3. Therefore, in single phase PFCs it is the DC link capacitor that becomes the power density limiting component.

A three-phase PWM converter only contains switching frequency components as calculated in Eq. (21) or $I_C = I_H = 0.73I(M \approx 0.8)$. Using again $P_{3PFC} = U \cdot I$ and considering that the DC link of three-phase converters is typically equipped with a series connection of two capacitors (e.g. 800V), a DC link capacitor power density limit of $\rho_{3PFC} = U \cdot s_C \cdot k_C/(2 \cdot 0.73)$ (assuming $k_C = 1.35$), results in $\rho_{3PFC} = U \cdot s_C/1.08$. A three-phase system typically has twice the output voltage of its single-phase counterpart, therefore $\rho_{3PFC} = 1.58\rho_{PFC}$ (60kW/dm^3) is valid, i.e. the three-phase system roughly requires 60% less capacitor volume. Therefore, for a 3-phase PFC the capacitor is not the power density limiting component.

6. Discussion

To enable an air-cooled system's overall power density

to reach the level required by 2020, according to Ref. (9), requires a major increase in efficiency or an increase in the heat sink or junction temperature. An increase of the heat sink temperature requires, for a given junction temperature, a decrease in the thermal resistance between junction and heat sink. This can be achieved by using higher thermal conductivity interface materials, or by optimum heat distribution and/or the use of larger semiconductor chip areas. However, this causes a reduced utilization of the power semiconductor and/or an increase of the realization costs [49]. Alternatively, higher junction temperatures can be used by selecting wide band-gap power semiconductors to replace the Si power semiconductors. An increase of the thermal conductivity of the heat sink by changing from aluminum to copper has a small influence since the remaining thermal resistance from the heat sink to air is relatively high.

To enable a further increase in the future power density, a gain can be made by thermally coupling the magnetic components and capacitors to the heat sink. The heat dissipation capability scales with the overall volume and not the surface area (see Fig. 5). To enable favorable thermal coupling, the use of conventional heatpipes [50] or anisotropic highly thermally conductive materials (solid heatpipes [36]) may find application. Through the use of a laminated structure in the magnetic core it is possible to dissipate the heat from inside the volume [51]. These concepts are therefore of interest since progress is expected to be made in material technology to provide increased thermal conductivity.

The increase in power density has been mainly due to the decrease in the volume of passive components through an increase in switching frequency. This has been brought about through the improvement of the switching characteristics of the power semiconductors. To achieve an increase in power density by a factor of two requires a tenfold increase in the switching frequency. As example, a three-phase, 10kW, unity power factor rectifier has a power density of $3.5 \mathrm{kW/dm^3}$ [52] for a switching frequency of 48 kHz and a power density of $8.5 \mathrm{kW/dm^3}$ for a 400 kHz switching frequency [38].

To further increase the power density with an increase in switching frequency, a proportional decrease in the switching times is necessary to maintain a constant efficiency. Switching times as small as 10ns are then needed for high power. A limiting factor becomes the acceptable level of switch over-voltage caused by the parasitic wiring inductances (current fall rates of $> 5 \mathrm{kA}/\mu \mathrm{s}$ could be typical) and/or the losses resulting from the internal and external capacitances [53]. Furthermore, voltage switching edges with greater than $100 \mathrm{kV}/\mu \mathrm{s}$ demand special dv/dt ruggedness in the gate drive circuits.

With an increase in switching frequency, arrangements to suppress the parasitic non-idealities of the leaded filter elements [54] [57] are required. In this context, the electromagnetic integration of inductive and capacitive components [54] represent a very interesting concept. However, for power levels within the range of several kW this is significantly limited by the lack of materials with high permeability and dielectric constants

that can be processed in planar layers [55].

Small power level systems can achieve high operating frequencies and extreme power densities using today's technology, e.g. a 100MHz VRM [56] with a power density of $3.78 \mathrm{kW/in^3}$ ($230 \mathrm{kW/dm^3}$ without housing). In further research, it is therefore important to examine to what extent the measure of power density is suitable for characterizing converter systems at very different power levels. Therefore, specific FOM values for different power level ranges should be determined and agreed upon.

Due to increasing demand for higher efficiencies, the use of the relative loss FOM is expected to increase. Therefore, it is important to analyze the effect that maximizing the power density has on efficiency. First considerations show that power density and maximum efficiency lie relatively close together. This is understandable, since the power density is thermally limited as the volume is minimized, and thus only a relatively small energy loss can be dissipated.

7. Summary

In this paper the power density barriers, based on today's technology, are shown to be caused by passive components and air cooling for all the fundamental types of power converters. To clearly document the technological limits, individual systems with an output power of 5 to 10kW have been considered in each case. A power density limit of $28 \mathrm{kW/dm^3}$ at 300kHz is calculated for an isolated DC-DC converter, $44 \mathrm{kW/dm^3}$ at 820kHz for a three-phase unity power factor PWM rectifier, and $26 \mathrm{kW/dm^3}$ at 21kHz for a sparse matrix converter. For single-phase AC-DC conversion a general limit of $35 \mathrm{kW/dm^3}$ results from the DC link capacitor. The practical power density of the converters is less than the indicated limit values since a finite volume must be occupied by the semiconductor modules, gate drivers, printed circuit boards and auxiliary power supplies.

For the power density increase to follow the past trend of doubling each decade, then the research focus must shift from the classical range of power semiconductors, topologies, modulation and control to the new areas of cooling concepts, high frequency magnet components, materials, interconnection techniques and packaging. Not only should the best possible materials be utilized but also multi-functional materials (e.g. thermal conduction of magnetic materials [50]), as well as undertaking three-dimensional integration of the converter systems. The design of highly compact systems must also be supported with multi-domain analysis tools, which not only provide simulation of the electrical circuit but also insight into the thermal, electromagnetic [58] and thermo-mechanical properties of the active and passive components. Only such a global optimization that includes the influences of the individual material properties [55] as well as temperature cycling will guarantee high reliability and result in a substantial improvement of the power converter's performance indices.

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Johann W. Kolar (Member) studied at the University of Technology Vienna, Austria, where he received his Ph.D. degree (summa cum laude). From 1984 to 2001 he was with the University of Technology in Vienna. He has proposed numerous novel converter topologies, e.g., VIENNA Rectifier and Sparse Matrix Converter. Dr. Kolar has published over 200 scientific papers in international journals and conferences and has filed more than 50 patents. He is a Professor and Head of the Power Electronics Systems Laboratory at ETH Zurich. The focus of his current research is on ultra-compact, intelligent AC-AC and DC-DC converters.

Uwe Drofenik (Non-member) received his M.Sc. (cum laude) and the Ph.D.(cum laude) degrees in electrical engineering from the Vienna University of Technology, Austria, in 1995 and 1999. He is currently performing scientific research and teaching at the ETH Zurich. During 1996 he was a researcher at the Masada-Ohsaki Laboratory at the University of Tokyo, Japan. In 2005 he received the "Isao Takahashi Award" from the IEE Japan.

Juergen Biela (Non-member) received his diploma degree with honours in electrical engineering from FAU Erlangen in October 2000. He then worked in the research department of A&D Siemens, Germany. From July 2002 he has been a Ph.D. student at ETH Zurich. Since December 2005 he is a PostDoc at the PES, ETH Zurich. His current research is focused on design, modelling and optimisation of PFC/DC-DC converters.

Marcelo Heldwein (Non-member) received his B.S. and M.S. degrees in electrical engineering from the Federal University of Santa Catarina, Brazil in 1997 and 1999. In March 1999 he worked as R&D engineer at the Federal University of Santa Catarina, Brazil. From 2001 to 2003 he worked as electrical design engineer at Emerson Energy Systems, Brazil. Since March 2003 he has been with the Power Electronic Systems Laboratory, ETH Zurich, as a PhD student.

Hans Ertl (Non-member) received the Dipl.-Ing. and Ph.D. degrees from the University of Technology Vienna, Austria, in 1984 and 1991, respectively. Since 1984, he has been with the Vienna University of Technology, where he is currently an Associate Professor with the Power Electronics Section of the Institute of Electrical Drives and Machines. His current research activities are focused on switch-mode power amplifiers and multicell topologies.

Thomas Friedli (Non-member) received his M.Sc. Degree with Distinction ETH Zurich in June 2005. During his M.Sc. studies he focused on power electronics, control engineering, signal processing and hardware development. His Master thesis research investigated a modular three-phase PFC (Delta-Rectifier). In September 2005, he joined the Power Electronic Systems Laboratory at ETH Zurich as a Ph.D. student.

Simon Round (Non-member) received the B.E. (Hons) and Ph.D. degrees from the University of Canterbury, Christchurch, New Zealand, in 1989 and 1993. From 1992 to 1995 he was a Research Associate in the USA and Norway. From 1995 to 2003 he was a Senior Lecturer in Electrical & Computer Engineering at the University of Canterbury. In September 2004, he joined the Power Electronic Systems Laboratory at ETH Zurich as a Senior Researcher.