Towards a 30 kW/liter, Three-Phase Unity Power Factor Rectifier

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Keywords: compact power supply, high power density, vienna rectifier, unity power factor

An increasing number of applications, especially in telecom and data server power supplies, require high power, highly efficient, compact, sinusoidal input current rectifiers. The input stage of these power supply systems can be realized with a direct three-phase rectifier topology, such as the Vienna Rectifier.

Two 400 kHz, 10 kW Vienna Rectifiers, a water cooled and a force air-cooled version (Fig. 1), achieving a power density of 10 kW/liter and 8.5 kW/liter respectively, are presented. Approximately one third of the volume is occupied by the EMI filter and to further improve the power density the switching frequency should be increased. A design for a 2.5 MHz rectifier is proposed and the challenges are highlighted. For this water cooled rectifier the power density increases to 18.5 kW/liter.

An analysis is then undertaken to determine the relationship between power density and switching frequency. The volumes of the EMI filter, boost inductors and the cooling system are determined. Based on the calculations it is possible to derive the maximum power density curves as a function of switching frequency (Fig. 2)
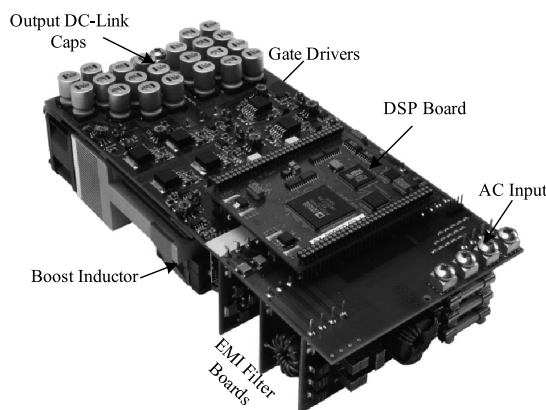
for a 10 kW rectifier using a minimized forced air cooling system and a water cooled power module. The theoretical maximum power density achievable, using a RF MOSFET and forced air-cooling, is 45 kW/liter at a switching frequency of 810 kHz. The power density substantially increases to 64 kW/liter if a water cooling system is employed.

The power density result does not take into account the volume occupied by the semiconductors in the power module, the DC output capacitors and auxiliary power supply. A more realistic or achievable maximum power density is 21 kW/liter for RF MOSFETs, forced air-cooled, with a switching frequency of 810 kHz, or 24 kW/liter for water cooling at a switching frequency of 2.1 MHz. If the desired goal of 30 kW/liter is to be achieved then improvements must be made by; reducing the semiconductor losses through better switching behavior from flat interconnection technology and lower capacitance structures, reducing the thermal resistance through double sided cooling, and developments in materials and packaging technology for passive components.

Fig. 1.   400 kHz forced-air cooled Vienna Rectifier. Dimensions of 250 mm x 120 mm x 40 mm. Weight of 2.1 kg
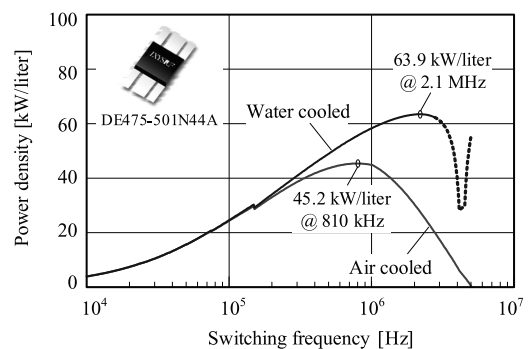

Fig. 2.   Estimated maximum power density for a 10 kW Vienna Rectifier for forced air and water cooling using IXYS RF MOSFET. Volume only occupied by EMI filter, boost inductors, and cooling system

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In this paper, a forced air-cooled, 400 kHz, 10 kW Vienna Rectifier with a power density of 8.5 kW/liter is presented. To further improve the power density, the switching frequency is increased to reduce the EMI filter volume. A design for an 18.5 kW/liter, 2.5 MHz rectifier is proposed. By using today's technology, it is calculated that the maximum power density for a forced air-cooled and water-cooled rectifier is 20.8 kW/liter and 24 kW/liter respectively. To achieve 30 kW/liter, improvements must be made in passive component material properties, reducing semiconductor losses and improving the cooling system.

Keywords: compact power supply, high power density, vienna rectifier, unity power factor

1. Introduction

An increasing number of applications, especially in telecom and data server power supplies, require high power, highly efficient, compact, sinusoidal input current rectifiers [1]. The input stage of these power supply systems can be realized with either a modular topology using a star-connection [2] or delta-connection [3] of single-phase boost rectifier modules, or a direct three-phase rectifier topology, such as the Vienna Rectifier (VR) in Fig. 1. The three-level VR topology allows lower voltage power semiconductors and a small input inductor volume [4]. Therefore, the VR is the ideal choice for a high power and high power density unity power factor rectifier.

New applications for high power density converters are in aircraft power supplies, where the weight and size of the converter, the sinusoidal input current quality, and the EMC performance are important factors [5]. Since future aircraft power systems will have a variable frequency ac voltage (360–800 Hz) the current controller bandwidth needs to be greater than 10 kHz. This requires a switching frequency over 100 kHz [6], which has the added benefit of decreasing the size and weight of the passive components.

The historical trend in power supply development is the continual increase in power density [7]. Based on this trend it is predicted in Ref. (7) that the power density will approach 30 kW/liter or 500 W/in^3 (1 liter = 1000 cm^3 = 61 in^3) after 2015. It is a significant challenge to achieve higher power densities as the converter must have an increasing efficiency, since power losses are more difficult to remove from a small volume, and/or an improved cooling system. This paper
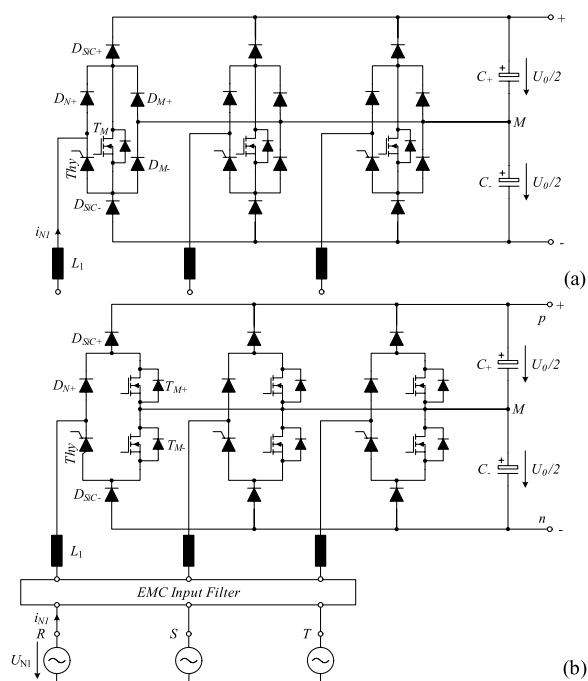
Fig. 1. Three-phase unity power factor rectifier topology implemented as (a) a three-switch or (b) six-switch version

investigates whether 30 kW/liter is possible for a 10 kW VR. Firstly, two 400 kHz VRs, a water and a forced-air cooled version with a power density of 10 kW/liter and 8.5 kW/liter, are presented. A design concept for a water cooled, 2.5 MHz VR is then proposed, which highlights the challenges of increasing the power density. The power density as a function of switching frequency for forced-air cooling is presented, which shows that a power density of 20.8 kW/liter is the limit with today's components.

2. Vienna Rectifier

The VR topology can be implemented with either three switches (Fig. 1(a)) or six switches (Fig. 1(b)) [4]. A six switch VR has lower conduction losses since the phase current flows through only one diode in each phase during the switch conduction. High speed, low reverse recovery diodes are connected to the positive and negative DC bus since they are subjected to the high frequency switching. The input diode and thyristor do not need to be fast switching components as they only switch the mains current. The thyristor also blocks the main current path during mains power up and allows a controlled pre-charge of the DC output capacitor voltage through a resistor and series diode that are connected in parallel to the thyristor.

The rectifier is typically designed to operate over a wide line-to-line input voltage range of 320–480 V_{RMS}, with a nominal input voltage of 400 V_{RMS}. The output voltage is regulated to be 800 V, which is divided into two 400 V outputs if required. For an output power of 10 kW, the input phase current is approximately 15 A_{RMS}.

3. 400 kHz Vienna Rectifier

The aim of the 400 kHz VR development is to demonstrate the feasibility of producing a three-phase unity power factor rectifier with a power density of 10 kW/liter. Two versions of the 400 kHz VR have been constructed. The first 400 kHz rectifier, capable of operating with a single phase mains voltage loss, achieved a 10 kW/liter power density using a water-cooling system. The aim of the second system is to achieve a similar power density with forced air-cooling. This rectifier is designed for three-phase operation only in order to reduce the volume of the DC output capacitors.

3.1 Water Cooled Rectifier   The three-switch VR (Fig. 1(a)) is selected for the first rectifier development since it has a reduced number of gate driver components. If discrete semiconductors are used in the power stage then a large area is occupied and long interconnections increase the wiring inductance, which increases the device's voltage stress and/or limits the switching speed. For this reason, it is advantageous to integrate all semiconductors of one bridge leg into one module, which contains a CoolMOS 600 V 47 A C2 MOSFET and each freewheeling diode D_{SiC} is realized as a parallel connection of 3 Silicon-Carbide (SiC) Schottky Diodes (6 A/600 V).

Three planar cores are used to construct a low profile boost inductor (Fig. 2) to produce an inductance of 32 μH, which is required to achieve a peak-to-peak current ripple of less than 20% of the peak phase current. The EMI filter of any power electronic converter typically occupies a significant volume and can not be ignored. To achieve the required power density of 10 kW/litre a 'zero-ripple' filter topology [8], which minimizes number of passive components, is used.

The complete VR is constructed on a single PCB as shown in Fig. 2. The input EMI filter can be seen on the bottom right side of the top photograph and above the input filter is the DSP digital control board. In the bottom-middle are the three multi-chip power modules, including the water cooler, and below the water cooler are the boost inductors. Directly above the module on the top of the PCB are the gate drivers
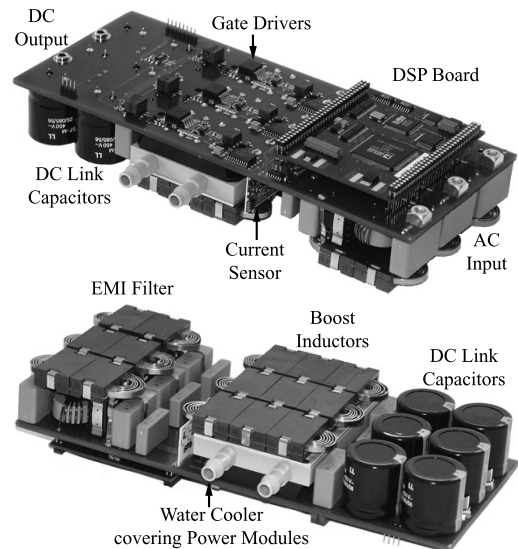

Fig. 2. 400 kHz, 10 kW/liter water-cooled Vienna Rectifier. Dimensions 250 mm x 100 mm x 45 mm.
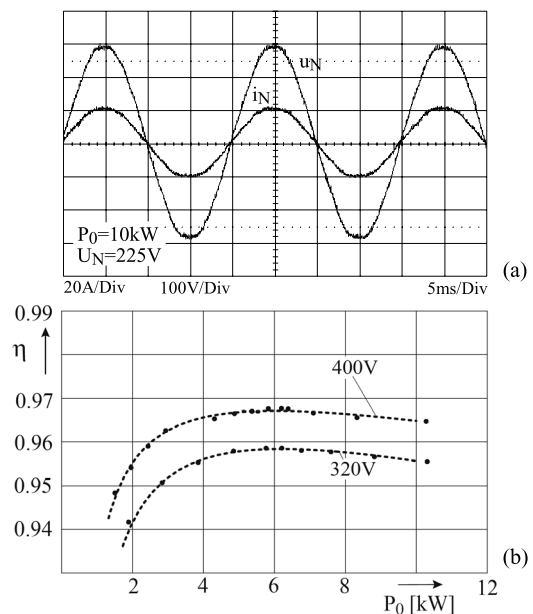

Fig. 3. Experimental waveforms and efficiency measurement of the 10 kW/litre VR

and on the bottom-left are the output capacitors, which are sized for single-phase loss operation.

It can be seen that the volume occupied by the EMI filter and DC link capacitors represents two-thirds of the total volume. The power device cooling is implemented with a custom water cooling system [9], although the power density figure does not take into account the volume occupied by the pump and radiator system.

Figure 3 shows that the rectifier produces sinusoidal input currents with a 2% THD at 10 kW output power and achieves an efficiency of over 96%.

3.2 Forced-air Cooled Rectifier   For the second rectifier the six-switch topology (Fig. 1(b)) is selected since it has lower conduction losses. A forced air-cooled heat sink traditionally occupies a large percentage of the rectifier's total volume. To minimize the heat sink it is important to
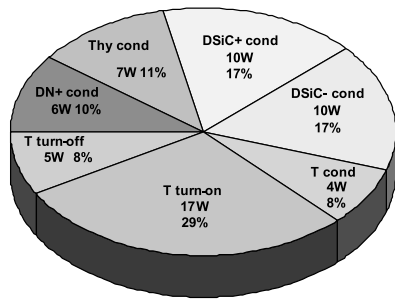
Fig. 4. Semiconductor losses at 400 kHz for one phase including the switch conduction (T_{cond}), turn-on and off ($T_{turn-on}$ and $T_{turn-off}$) losses. Total rectifier semiconductor losses are 171 W.

Fig. 5. Ceramic capacitor board mounted on top of the power module

minimize the semiconductor power losses since at high operating frequencies the switching losses dominate.

3.2.1 Semiconductor Losses Switching loss measurements of a variety of combinations of switch and diode types are undertaken, using techniques described in Ref. (10), to determine the combination that has the lowest switching losses. The combination of a CoolMOS 600 V, 47 A C3 MOSFET and two Cree SiC 10 A diodes produces the lowest switching losses and minimum voltage overshoot when driven with zero gate resistance by a 14 A IXDN414 gate driver and ceramic capacitors are directly placed between the SiC diode cathode and source of the MOSFET.

Using the data obtained from switching measurements and datasheet information of the other semiconductor devices, a prediction of the phase leg losses for 400 kHz operation is given in Fig. 4. The total switch losses account for 45% of the total phase leg losses of 57 W. The boost diode conduction losses are also significant, accounting for 34% of the losses. The predicted efficiency at 400 kHz is 95.6%.

3.2.2 Power Module and Gate Driver To minimize the volume occupied by the semiconductors, a single custom module has been produced, which contains the semiconductors (CoolMOS C3, SiC diodes, thyristors and line rectifier diode) for all three phases. The module layout has been specifically designed to have low inductance, where the input current is connected to the center connectors of the module and the output DC bus connections are on the outer sides.

Special gate driver requirements are necessary for a high switching frequency PWM rectifier in order to achieve a short signal propagation delay-time, good edge symmetry, and good common-mode transient immunity. To achieve this, a magnetic coupler (ADuM1100) and high-speed, high current gate driver (IXDN414) combination are used [11].

3.2.3 Boost Inductor A switching frequency of 400 kHz results in a boost inductor value of $32\,\mu H$ in order to maintain a maximum peak-to-peak ripple current of 20% at the specified output power of 10 kW. The boost inductor is designed as a pair of series connected $16\,\mu H$ inductors. Each inductor pair is constructed from two planar EPCOS ELIP N87 cores, since these cores offer a low profile and a good high frequency performance. The series connection is used in order to efficiently fill the converter volume and reduce the parasitic capacitance. Each boost inductor has a 6 turns winding of copper tape with dimensions of 3 mm x 0.8 mm. The volume occupied by 3 inductors is 0.095 liters.
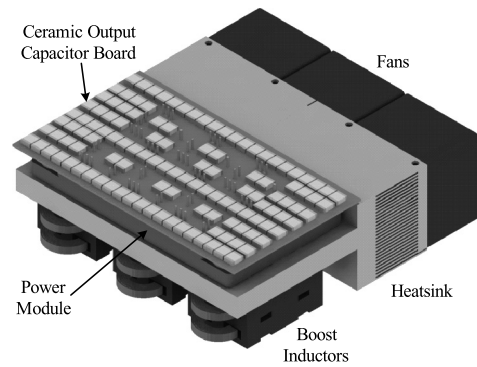
3.2.4 Capacitors The DC link capacitors are used to reduce the output voltage ripple and to provide energy storage. The overall DC output capacitance is $33\,\mu F$ (800 V) and the majority of capacitance is provided by low profile SMD $4.7\,\mu F$ 450 V electrolytic capacitors. To minimize the inductance between the boost diodes and the output capacitors, two banks of 50 ceramic capacitors (AVX 220 nF 630 V SMD) giving $11\,\mu F$, are mounted on a separate PCB that is directly placed on top of the power module (Fig. 5). This board has a similar low inductance as integrating the capacitors into the power module but is less problematic since the capacitors would be subjected to high thermal and mechanical stress inside the module.

3.2.5 EMI Filter In order to be compliant with the CISPR 22 class B conducted emission limits, a volume optimized EMI filter is designed. The filter comprises of differential (DM) and common mode (CM) stages. An optimal design of the EMI filter, based on the method in Ref. (12), requires knowledge of the estimated emission levels. To achieve the smallest possible DM filter volume a numerical procedure minimizing the total volume is implemented. The DM filter is designed as a three stage LC filter with the smallest total inductance and capacitance values being achieved if the same values are used for each filter stage, except for the boost inductors and the first DM capacitors.

The CM filter design procedure determines the required attenuation from circuit simulation results. Since the CM source impedance (impedance from the rectifier's CM voltage source to earth) is not well defined, it is set to a maximum of 10 nF, and includes all capacitances from the power module to earth (via the heat sink) and the load to earth. The same approach as for the DM filter is used, which leads to a three stage CM filter. Damping resistors are included into the design in order to prevent oscillations at the resonance frequencies.

The filters are designed for a high degree of compactness by using low profile components while keeping a good high frequency performance. The complete filter structure including DM and CM stage and the equivalent values for the components is given in Ref. (11). The volume occupied by the EMI filter is 0.384 liters.

3.2.6 Digital Controller The control of the high frequency rectifier system is based on average current mode control and is implemented in a dedicated control board based on an Analog Devices ADSP2199x DSP. The
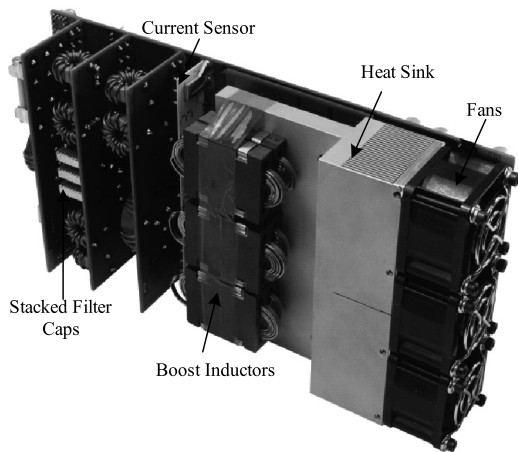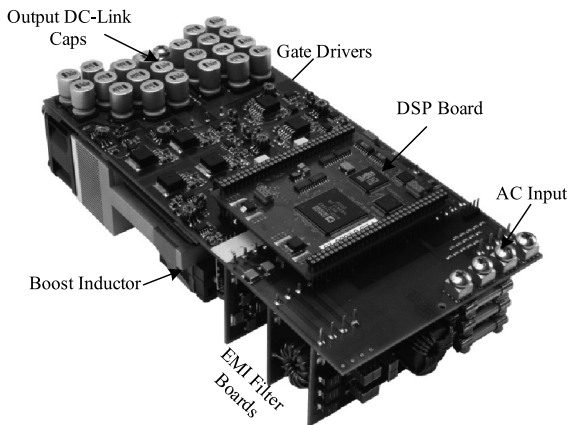
Fig. 6. Top and bottom views of the 400 kHz air cooled Vienna Rectifier. Dimensions of 250 mm x 120 mm x 40 mm. Weight of 2.1 kg

Fig. 7. Phase voltage and current of the 400 kHz VR, operating at 2.4 kW, 115 V_{RMS}, 800 Hz. Time base: 0.2 ms/div, i_{N1}: 5 A/div, u_{N1}: 50 V/div

controller structure consists of a cascaded controller with the current controller in the inner loop and a voltage controller in the outer loop. The DSP has an 80 MHz internal clock, which limits the 400 kHz PWM resolution to 6.8 bits. The rectifier control algorithms are implemented using assembler language to ensure the minimum interrupt processing time.

3.2.7 Hardware Construction and Operation The top and bottom hardware construction views are shown in Fig. 6. A 4-layer main power PCB carries the current from the input terminals, through the EMI filter boards and current sensors to the boost inductors and then to the ceramic capacitor board. From the capacitor board, the current flows through the power module and directly into the output capacitors and DC terminals. The gate drivers for the six MOSFETs and three thyristors are mounted underneath the digital controller board on the main power PCB. The EMI filter is implemented on three daughter boards following design rules to reduce the interaction between filter elements and to have a straight line current flow. The design of the rectifier has not been fully optimized for power density as can be seen by the numerous air spaces in Fig. 6. In a revision of the rectifier it is planned to further reduce the volume by removing the extra air spaces.

The width of the system is given by dimensions of the three 40 mm x 40 mm heat sink cooling fans. A custom optimized heat sink is used and the power module is mounted in the middle of the flat plate. The design uses high speed, high
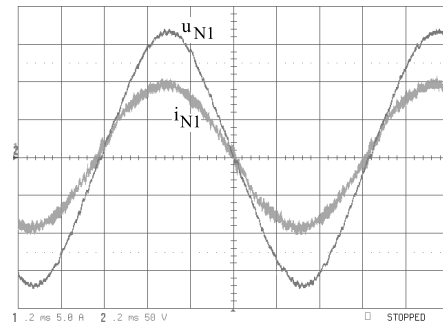
pressure San Ace fans to force the air over the fins and then out both sides of the heat sink. The heat sink is constructed from a block of aluminum, with a thermal conductivity of 220 W/(mK), and the fins are formed using spark erosion due to their small 0.75 mm thickness and spacing of 0.75 mm.

The rectifier dimensions are 250 mm x 120 mm x 40 mm, thus giving a total volume of 1.2 liters. For an output power of 10 kW this gives a power density of approximately 8.5 kW/liter for the forced air-cooled VR. At 10 kW and an ambient temperature of 45°C, the maximum MOSFET junction temperature of 125°C, which allows for a limited overload rating.

Figure 7 shows the three phase input currents and one input phase voltage when the rectifier is operated with a 230 V phase voltage, a 680 V output voltage and an output power of 4 kW. The line current has a value of 5.8 A_{RMS} shows and a THD of 4.75% (up to the 20th harmonic). As can be seen in the current waveforms there is additional distortion at the zero crossings of the phase current, which then causes distortion in the other phase currents. The controller is being refined to remove the phase voltage and current measurement sensitivity that causes these current distortions.

4. Towards 30 kW/liter

If the forced air-cooled rectifier (Fig. 6) is converted into a water-cooled rectifier by removing the fans and heat sink, and placing the water cooler under the power module, then the power density would increase by 36% to 11.3 kW/liter. What further steps can be undertaken to increase the power density further? Since a significant volume is occupied by the EMI filter and boost inductors, the power density could be increased by increasing the switching frequency. We now investigate what the power density would be and what issues need to be solved if the switching frequency is increased to, say, 2.5 MHz.

At 2.5 MHz all the system non-idealities become important and have to be considered in the design. The fishbone diagram (Fig. 8) summarizes all the contributing factors to non-ideal behavior of the VR. The significant non-idealities are the switching device delays, gate driver delays and variations, PWM resolution, A/D conversion and digital computation time and accuracy.

4.1 Semiconductor Selection Using the same semiconductors as for the 400 kHz air-cooled rectifier, a prediction of the phase leg losses for 2.5 MHz operation (Fig. 9)
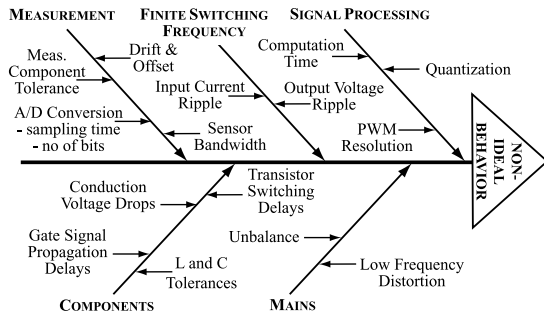
Fig. 8. Origins of non-ideal behavior of the VR resulting in AC-line current distortion
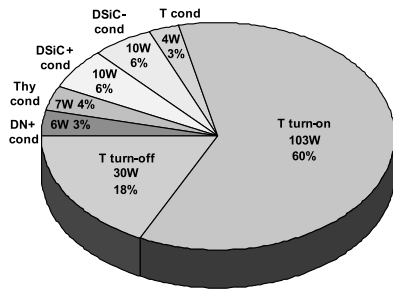

Fig. 9. One phase semiconductor losses at 2.5 MHz. Total semiconductor losses are 507 W

Fig. 10. Inductive turn-off switching characteristic for a CoolMOS C3 47 A 600 V device for drain currents of (a) 0.5 A and (b) 5 A

results in the total MOSFET losses now increasing to 78% of the total phase leg losses of 169 W. At this frequency, the total power module's losses, at rated power, are 507 W. This level of power loss is extremely difficult to dissipate with a compact air-cooled system, and therefore water-cooling must be utilized. The predicted efficiency decreases to 92.5% for 2.5 MHz operation compared with 95.6% at 400 kHz. This decrease in efficiency can only be justified when extreme power density is required.

A significant problem in using CoolMOS devices in very high switching frequency applications is their high capacitance, especially at low drain to source voltage. One main issue is the increasing turn-off delay time for smaller drain currents. This becomes a problem for the rectifier around the current zero-crossing since the switch takes longer to turn-off. To illustrate this, Fig. 10 shows the experimental measurements of the CoolMOS turning off an inductive current of 0.5 A and 5 A. For 0.5 A, the turn-off delay time is 600 ns and the voltage rise time is 480 ns, giving a total turn-off time of over 1 μs. While for 5 A the total turn-off time is reduced to 175 ns. For a 2.5 MHz switching frequency, the turn-off delay time at 5 A is 44% of the switching period. Therefore, alternative switches with reduced output capacitance must be used at very high switching frequencies. The current zero crossing will always be a problem since a low current increases the turn-off time substantially, even for a low output capacitance device. Therefore, even though the controller signals to turn off the switch, the switch may not actually turn off the current. An alternative discontinuous modulation method [13], in which the phase is clamped for 30° around the zero crossing, is especially interesting for the ultra-high switching frequency VR.

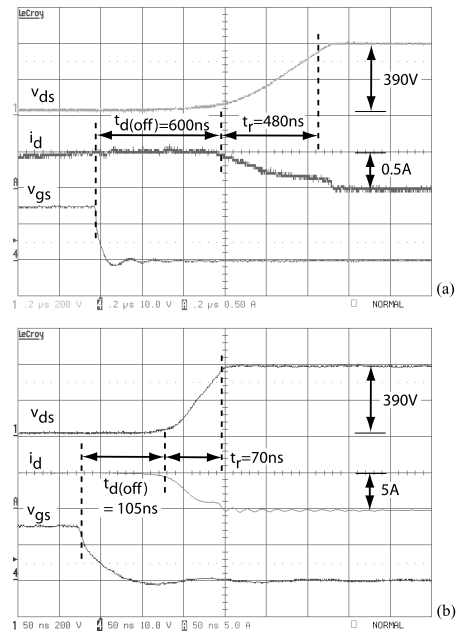An alternative to the CoolMOS are other vertical structure MOSFETs such as the APT MOS5 or MOS7, which have a lower capacitance and faster switching times but higher on resistance. The SiC JFET is another device that offers fast switching performance [14] and a low delay time, and has the added benefit for aerospace applications of being less sensitive to radiation. Presently, only a 1200 V, 6 A SiC JFET in a TO-220 package is available as a restricted sample. The JFET is a normally ON device, however this does not cause a problem during mains power up as the thyristors block the current path until the JFETs are actively turned off by a custom gate driver [14]. Measurements have been made to determine the switching loss and times at a 3 A drain current [14]. For the VR, we ideally want to use a 600 V part since it will have lower on resistance [15]. To compare the 6 A JFET with the higher current rating MOSFETs, it is assumed that 4 parallel connected JFETs have a similar current rating to the MOSFETs at a 90°C case temperature. The JFET switching energies are measured for the 1200 V device at 3 A and 600 V_{dc}, and then scaled for 400 V_{dc}, using Ref. (16), and multiplied by the number of parallel connected devices. It is assumed that the 600 V parts will have a lower overall capacitance, and therefore a 30% reduction in switching losses. The on resistance at 25°C is 0.3 Ω, and this increases to 0.5 Ω at a 125°C junction temperature. For a 600 V SiC JFET, the on resistance decreases to 0.2 Ω at 25°C [15].

Another possible device that has a low capacitance is the IXYS DE475-501N44A RF MOSFET. This device is mounted into a low inductance package, with stated switching times of 10 ns. The capacitance is almost three times smaller than the comparable CoolMOS device. A comparison of the possible switches is given in Table 1. The data is taken directly from datasheets, measured or estimated. Figure 11 shows the semiconductor loss distribution for 2.5 MHz operation of the 600 V SiC JFET and the RF MOSFET. The total semiconductor power losses using the CoolMOS, SiC JFET and RF MOSFET are 550 W, 545 W and 357 W

Table 1. Comparison of MOSFETs and SiC JFET

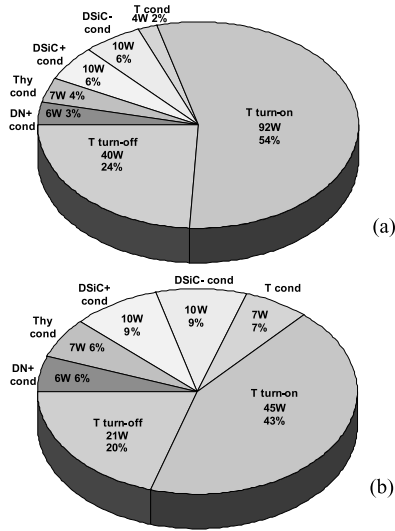|	CoolMOS C3 600 V, 47 A	MOS7 600 V, 49 A	SiC JFET 600 V, 4 x 6 A	RF MOS 500 V 48 A
R_{ds} @ 12 A, 25°C	60 mΩ (datasheet)	130 mΩ (datasheet)	0.2 / 4 = 50 mΩ	110 mΩ (datasheet)
R_{ds} @ 12 A, 125°C	155 mΩ (est.)	330 mΩ (est.)	0.35/4 = 88 mΩ	283 mΩ (est.)
E_{on} @ 400 V, 12 A	40 μJ	-	10.8 μJ*4 = 43 μJ (est.)	18 μJ (est.)
E_{off} @ 400 V, 12 A	11 μJ	-	4.5 μJ*4 = 18 μJ (est.)	9 μJ (est.)
Turn off delay, 10 A	86 ns R_g=0 Ω	65 ns R_g=0 Ω	≈30 ns (est.)	≈12 ns (est.)

Fig. 11. Single phase power loss distribution at 2.5 MHz for (a) SiC 600 V JFET (502 W total losses) (b) IXYS RF MOSFET (315 W total losses)
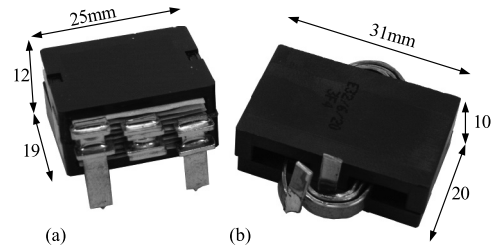

(a)

(b)

Fig. 12. Two different winding arrangements for the 6 μH boost inductor (a) stacked flat turns (b) tape wound turns
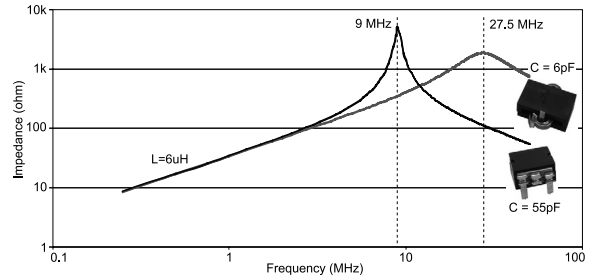

Fig. 13. Impedance of the stacked and tape winding boost inductors. Stack winding capacitance is higher with 55 pF compared to 6 pF
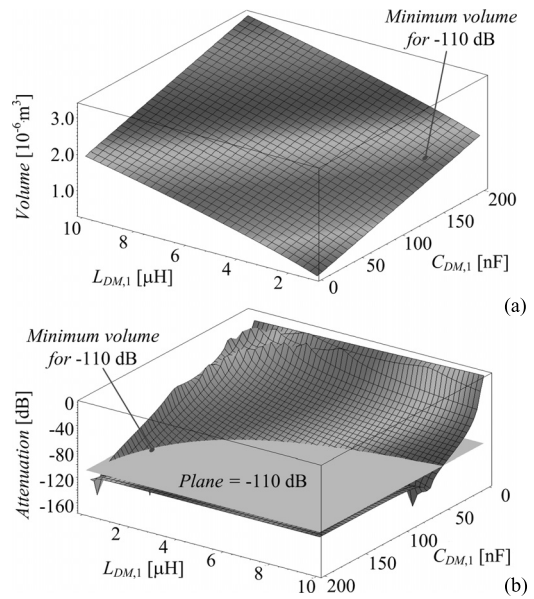

(a)

(b)

Fig. 14. Volume and attenuation surfaces for the DM filter design (a) volume dependence on L and C values, (b) attenuation at f_s = 2.5 MHz for L and C values and −110 dB Class B plane (gray). Colors correspond to colors in (a). Smallest volume is achieved with 1.5 μH/150 nF

respectively. Since the switching loss is the most dominant loss component and considering the requirement for minimum delay time to ensure high pulse exactness, the RF MOSFET seems to be the most obvious device for use in the 2.5 MHz VR.

4.2 Boost Inductor To meet the same maximum peak-to-peak current ripple of 20% at 10 kW, the boost inductance can be reduced to 6 μH at 2.5 MHz. The design of the inductor is very important to ensure a minimum parasitic capacitance, since this capacitance causes additional switching losses. Figure 12 shows two different construction possibilities for the ferrite inductors. Type (a) is constructed from parallel single turn stacked plates while type (b) uses a tape winding. From Fig. 13 it can be seen that the resonant frequency of stacked inductor is three times lower at 9 MHz compared to the tape wound inductor. Therefore the parasitic capacitance of the stacked inductor is 9 times larger, with a value of 55 pF, compared to the tape wound inductor. For 2.5 MHz operation the tape wound inductor is selected and the volume occupied by the three boost inductors is approximately 0.025 liters. This is a volume reduction of 74% compared to the 400 kHz inductors.

4.3 EMI Filter The EMI is designed using the same procedure described in Section 3.2.5. For the DM filter the required attenuation at 2.5 MHz is 110 dB and this value is used to design the filter. The volume minimization procedure results in equal values of inductors and capacitors respectively in each of the filtering stages. Once the boost inductor is designed, then there are only the DM inductance and capacitance to optimize. This procedure produces two 3D surfaces, one for the volume and one for filter attenuation, as illustrated in Fig. 14. It can be seen that to have the minimum volume at the required attenuation requires 1.5 μH inductors and 150 nF capacitors per phase. The filter structure, containing the three filter stages, is shown in Fig. 15.

The CM inductor positioned closest to the power converter

486
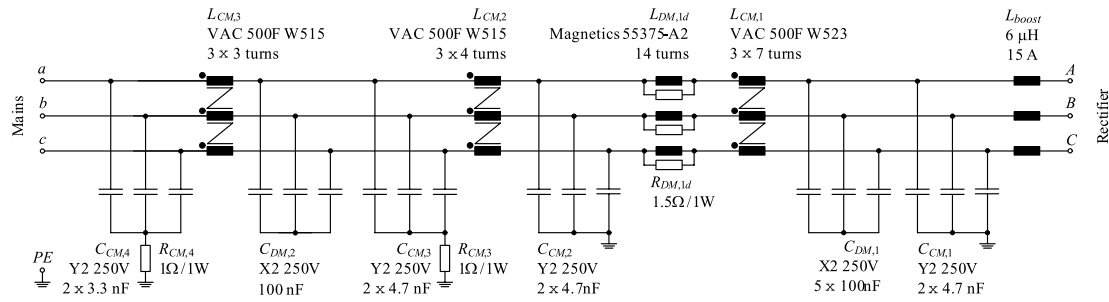
IEEJ Trans. IA, Vol.128, No.4, 2008

Fig. 15. Proposed 2.5 MHz EMC filter. CM filter uses coupled inductors, and their leakage inductances form the DM filter with the X2 capacitors

Table 2. Values for DM Filter Components

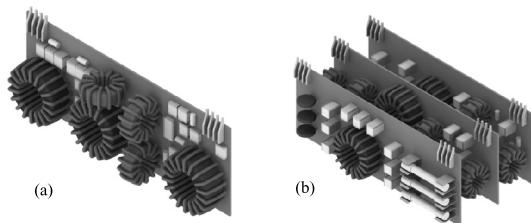| Design Sw. freq.	Stage 1		Stage 2		Stage 3	
	L (μH)	C (nF)	L (μH)	C (nF)	L (μH)	C (nF)
Optimized (400 kHz)	L_{boost} ≈ 30	850	10	850	10	850
Designed (400 kHz)	L_{boost} ≈ 30	500 500	8+(8μH// 3.3 Ω)+$L_{CM,\sigma}$	1000 1000	10 10	1000 1000
Optimized (2.5 MHz)	L_{boost} ≈ 6	150	1.5	150	1.5	150
Designed (2.5 MHz)	L_{boost} ≈ 6	500	(8 μH//3.3 Ω) $L_{CM,\sigma}$	C_{CM}	$L_{CM,\sigma}$	100
where C_{CM} are 9.4 nF Y capacitors and $L_{CM,\sigma}$ is the stray inductance of the CM inductor ($\approx 1.6 \mu$H).						

Fig. 16. 3D CAD drawing of EMI filters for (a) 2.5 MHz, 0.18 liters and (b) 400 kHz, 0.38 liters

is subject to a high CM voltage at the switching frequency and is designed so that cores losses do not cause over-heating. This CM inductor has a larger volume than the following stage CM inductors.

Based on the design procedure, the optimized and final design values for the 2.5 MHz filter components are presented in Table 2, which also shows the components used in the 400 kHz EMI filter (see Fig.7 in Ref. (11)). The reasons for changing the values of some of the components in the final design version is due to the availability of commercial SMD capacitors and the necessity of including passive damping in the last stage of the filter. Both designs use the stray inductance of the CM inductors for filtering DM emissions. The design for 2.5 MHz does not require separate DM inductors, but the damping network is kept in order to facilitate good performance of the rectifier's current controller.

The first D_M capacitor, $C_{DM,1}$, is kept to be 500 nF for the 2.5 MHz design because it uses the same PCB footprint as a 100 nF capacitor and allows a reduction in value of the following stages' capacitors.

The proposed EMI filter fits on to a single daughter board compared to three PCBs for the 400 kHz system as shown in Figure 16. The estimated volume of the single EMI board is 0.18 liters, a volume reduction of 54% by increasing the

switching frequency by 6.25 times.

4.4 PWM Generation The trend is towards fully digital control of power electronics using DSPs. The control and PWM generation of the 400 kHz VR is fully implemented in a DSP. At 2.5 MHz, the digital implementation in standard DSPs provides some challenges since the waveform PWM generation accuracy is dependent on processor clock frequency. Most DSPs for power electronic applications have clocks of approximately 100 MHz and therefore the resolution of the PWM generation is limited as the switching frequency is increased.

For double sided PWM, the resolution accuracy is 0.8% at 400 kHz and decreases to 5% at 2.5 MHz. This is not an acceptable resolution to generate accurate rectifier voltages. If the clock frequency is increased to 1 GHz then the step size of the PWM pulse width is reduced to 1 ns and this would provide sufficient accuracy at 2.5 MHz. New DSPs from TI are available on the market with a higher resolution (150 ps steps) for single sided PWM. A new custom control board with a 2808 TI DSP is being used, which will implement discontinuous modulation. Other variations, such as propagation time differences in gate drivers, also have a major influence on the PWM accuracy.

To overcome the resolution limits, it is possible to average a slightly varying 2.5 MHz PWM on-time duration over a fixed number of switching intervals, although a small amount of lower frequency distortion appears that is dependent on the number of cycles used for the averaging [17]. This results in a higher PWM resolution but requires a large inductor value, such as in the 400 kHz rectifier, to average the current waveform. Therefore, the rectifier's power density will reduce but since the volume of the EMI filter will reduce as the PWM frequency increases, there maybe be an overall power density gain. This is an interesting trade-off that requires further investigation. The calculation of the changing duty cycle would be difficult to implement in a standard DSP at 2.5 MHz without additional hardware or the use of a FPGA.

4.5 Proposed 2.5 MHz Rectifier Construction A proposed 3D CAD construction view of the 2.5 MHz rectifier is presented in Fig. 17. The 3-phase power module, as in the 400 kHz rectifier, sits on top of an optimized water cooler [9], and a ceramic capacitor board is directly placed on top of the module. Mounted below the water cooler are the 3 boost inductors and the output DC capacitor board, which is constructed using ceramic capacitors. The single EMI filter board is mounted at the front, just below the AC input. The estimated volume of the rectifier is 0.54 liters, giving
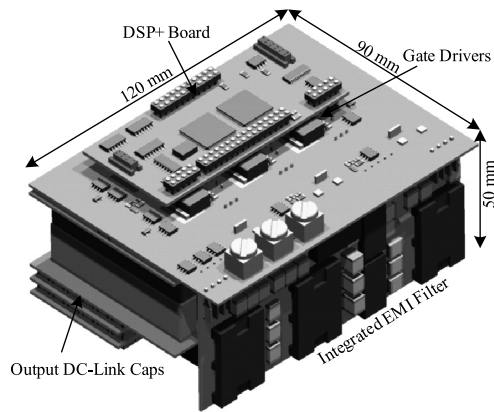
Fig. 17. Proposed 2.5 MHz VR hardware construction that gives a total volume of 0.54 liters and a power density of 18.5 kW/liter

Fig. 18. Estimated volume of the DM and CM EMI filters and air-cooling system for a 10 kW VR with (a) Cool-MOS and (b) RF MOSFETs. EMI filter designed to fulfill CISPR 22 class B limits.

a power density of 18.5 kW/liter. Compared to the water-cooled 400 kHz rectifier the power density has been increased by 85% by increasing the switching frequency to 2.5 MHz. In achieving this power density increase, the efficiency has decreased from 95.5% to 92.4%, assuming CoolMOS C3 switches are used in both systems.

4.6 Power Density Limit For an air-cooled rectifier there is a trade-off between the heat sink size due to increasing losses with switching frequency and reducing EMI filter size. In order to determine the optimal switching frequency an estimation of the volume of the main power converter components is important. A procedure to estimate the volume of the EMI filter and the cooling components has been developed [18].

It is assumed that the inductors use high performance materials, such as nanocrystalline for CM, Molypermalloy for DM, and ferrite for the boost inductors. To produce low volume inductors with a realistic temperature rise, optimum levels of magnetic flux and current density for various inductor designs are derived as functions of switching frequency and area product. Then empirical equations are derived, based on datasheet information, which relate the boxed volume of an inductor to its required area product.

The EMI capacitors are assumed to be X2 and Y2 rated ceramics, since these have the lowest volume. Based on data sheet information for different capacitors, empirical relations of volume as a function of rated voltage and capacitance are derived. With this information, volume minimized filters can be designed assuming natural air cooling.

For the forced air cooling rectifier it is assumed that the heat sink is optimized as in Ref. (19). The estimate for the volume of the cooling system is a function of the cooling system performance index, *CSPI* (25 W/K.liter in this case) and the thermal resistance from heat sink to the ambient $R_{th,ha}$ (calculated from the estimated losses and the power module layout), as given by

$$Vol_{HS} = \frac{1}{R_{th,ha} \cdot CSPI} [\text{liter}] \cdots\cdots\cdots\cdots\cdots (1)$$

The volumes of the DM (including the boost inductors), CM filter and forced air-cooled heat sink as a function of switching frequency are given in Fig. 18. It is observed that the DM filter occupies most of the converter space for
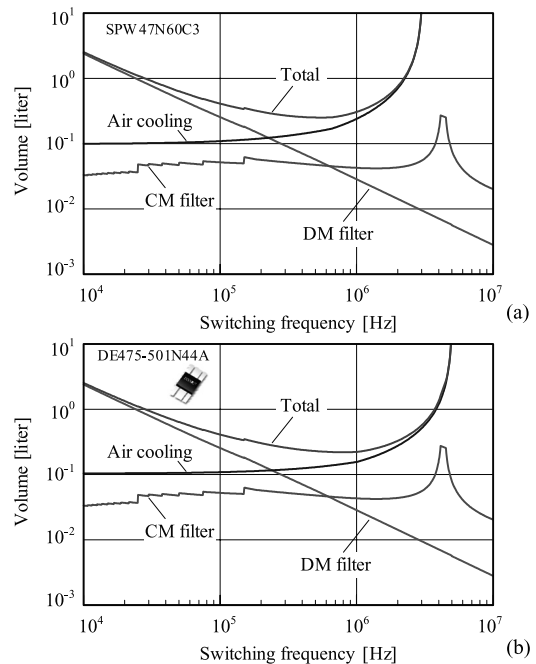
switching frequencies up to 150 kHz. Above this frequency the CM filter tends to be larger due to the high CM voltage generated by the converter. At approximately 600 kHz the cooling system starts to dominate and the minimum volume solution is produced at this frequency.

Based on the calculations it is possible to derive curves of the maximum power density as a function of switching frequency (Fig. 19) for a 10 kW rectifier using a minimized forced air cooling system and a water cooled power module as in Ref. (9). It is assumed that the volume is only occupied by the EMI filters, boost inductors, and the cooling system. It is seen that the theoretical maximum power density achievable, using CoolMOS semiconductors and forced air-cooling, is 39.9 kW/liter at a switching frequency of 540 kHz. This increases to 45.2 kW/liter and 810 kHz if a lower switching loss RF MOSFET is used. The power density substantially increases to 63.9 kW/liter if a water cooling system is employed. The water cooling curve is dashed beyond approximately 3 MHz because of the difficulty to achieve a thermal resistance of less than 0.1 K/W for the given power module. For the air-cooled system, above 3 MHz for the CoolMOS and 5 MHz for the RF MOSFET a negative thermal resistance is required. This means that the semiconductor losses and the thermal resistances internal to the power module are physically limiting the heat removal.

The power density results presented in Fig. 19 do not take into account the volume occupied by the semiconductors in the power module, the DC output capacitors and auxiliary power supply. If it is assumed that the digital controller and the gate drive circuitry are integrated into the existing SP6 power module, the power module volume would be 0.115 liters. The volume occupied by the DC output ceramic capacitors and auxiliary power supply is estimated to
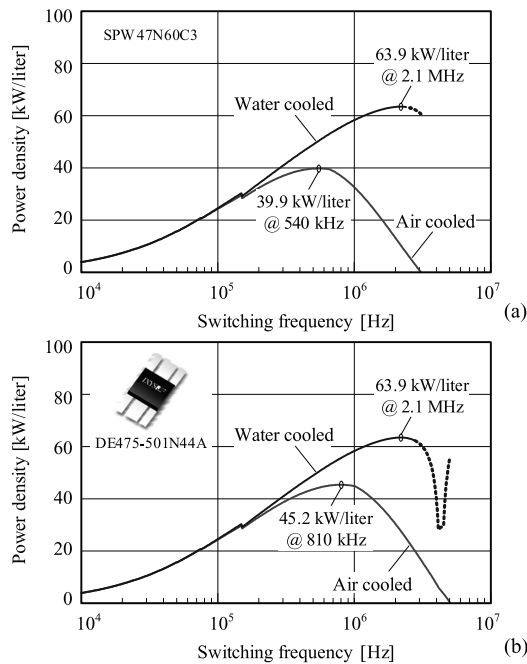
Fig. 19. Estimated maximum power density for a 10 kW VR for forced air and water cooling using (a) CoolMOS C3 MOSFET (b) IXYS RF MOSFET. Volume only occupied by EMI filter, boost inductors, and cooling system

be 0.125 and 0.02 liters respectively. Therefore, a more realistic or achievable maximum power density is

- 19.6 kW/liter for CoolMOS C3 MOSFETs switching at 540 kHz with forced air-cooling,
- 20.8 kW/liter for RF MOSFETs switching at 810 kHz with forced air-cooling,
- 24 kW/liter for either CoolMOS or RF MOSFETs switching at 2.1 MHz with water cooling.

The main limiting factors for increasing the power density are the materials available for the inductors and capacitors, the losses generated by the power semiconductors, and the available packaging technology.

5. Conclusions

Two 400 kHz, 10 kW VRs, a water cooled and a force air-cooled version, achieving a power density of 10 kW/liter and 8.5 kW/liter respectively, are presented. Approximately one third of the volume is occupied by the EMI filter and to further improve the power density the switching frequency should be increased. A design for a 2.5 MHz rectifier is proposed and the challenges due to the switching device delays and PWM generation are highlighted. For this water cooled rectifier, the power density increases to 18.5 kW/liter.

Using the technology available today, the maximum power density possible for a VR is 21 kW/liter when using a forced air cooling and 24 kW/liter for water cooling. If the desired goal of 30 kW/liter is to be achieved then improvements must be made by; reducing the semiconductor losses through better switching behavior from flat interconnection technology and lower capacitance structures, reducing the thermal resistance through double sided cooling, and developments in materials and packaging technology for passive components.

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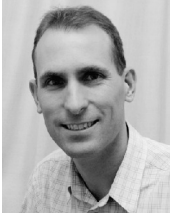
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