Interleaved Triangular Current Mode (TCM) Resonant Transition, Single Phase PFC Rectifier with High Efficiency and High Power Density

C. Marxgut, J. Biela and J.W. Kolar
Power Electronic Systems Laboratory, ETH Zurich
Physikstrasse 3, 8092 Zurich, Switzerland
Email: marxgut@lem.ee.ethz.ch, www.pes.ee.ethz.ch

***Abstract*—This paper presents a new topology for a highly compact and highly efficient single-phase Power Factor Corrected (PFC) rectifier system. The new topology consists of several interleaved boost stages which operate in a mode called Triangular Current Mode (TCM) in order to simultaneously achieve a high power density as well as a high efficiency. Applying TCM, ZVS is achieved over the full mains period by proper control of the power MOSFETs. The high TCM inductor current ripple is not transferred to the mains as the superposition of all boost cell input currents results in a smooth mains current waveform. Furthermore, one bridge leg operates synchronously to the mains frequency and connects the mains directly to an output rail. This results in very low common mode noise and only a small common mode filter has to be considered. The excellent behavior of this topology also applies to inverter operation.**

***Index Terms*—Single phase PFC rectifier, Triangular Current Mode (TCM), High efficiency, Power Sheet**

I. Introduction

Conventional boost PFC rectifiers employing an input rectifier bridge followed by a boost converter suffer from relatively high conduction losses in the rectifier bridge when operating in Continuous Conduction Mode (CCM). Therefore bridgeless topologies [1] are applied where the number of active devices in the conduction path is reduced, as can be seen in Fig. 1 (a).

In [2] the topology in Fig. 1 (a) is optimized in respect of efficiency and power density where it is shown that a trade-off between conduction losses and switching losses has to be found. The conduction losses depend on the drain-source resistance while the switching losses are determined by the output capacitance of the MOSFETs. A large chip area leads to a small on-resistance but a large output capacitance and vice versa. Hence, an optimization has to be done to determine the optimal number of switches to be connected in parallel.

The reverse-recovery effects of the diodes D_{11n} and D_{11p} (cf. Fig. 1 (a)) have great impact on the efficiency due to switching losses which are generated by the reverse-recovery currents. It is thus beneficial to use SiC diodes which have negligible reverse-recovery effects and hence switching losses can be reduced. However, these diodes have a large forward voltage drop which increases the conduction losses. Furthermore, the bridgeless topology exhibit considerable common mode (CM) noise as the output rails are floating for the complete mains

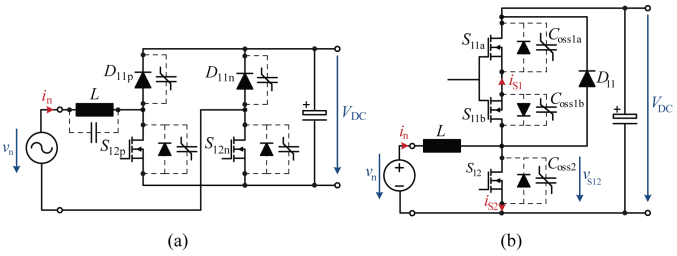

Fig. 1. (a) Basic bridgeless topology with parasitic capacitors. D_{11p} and S_{12p} shape i_n for $v_n > 0$ whereas D_{11n} and S_{12n} shape i_n for $v_n < 0$. (b) Bridge leg for the positive half line cycle for synchronous rectification. S_{11b} forces i_{S1} through diode D_{11} after turn-off of S_{11a}.

period. Consequently, arrangements with either capacitors or diodes as CM return path have to be applied to reduce the CM noise which lead to additional losses [2]–[4].

To eliminate the effect of the high forward voltage drop of SiC diodes, synchronous rectification could be applied where the diodes are connected in parallel with active switches to minimize the conduction losses. However, as the forward voltage drop of a SiC diode is larger than the forward voltage drop of the body diode of a paralleled MOSFET, the current will not commutate to the SiC diode after the MOSFET is turned off. As a result an antiseries switch (cf. S_{11b} in Fig. 1 (b)) has to be considered to commutate the current to the SiC diode when switch S_{11a} is in the off-state.
However, as indicated in Fig. 1 (b), MOSFETs exhibit non-linear parasitic drain-source capacitances which have a large capacitance value for low voltage levels. Therefore, at each switching action of S_{12} capacitor C_{oss1a} has to be charged and due to the large capacitance a large charging current flows through the bridge leg. Thus the charging of C_{oss1a} and the discharging of C_{oss2} result in considerable losses.

In order to avoid the large charging current in the MOSFET's output capacitance, ZVS is required where the capacitor C_{oss1a} is charged to the output voltage V_{DC} and C_{oss2} is discharged before turn-on of switch S_{12}. In discontinuous conduction mode (DCM), ZVS can be achieved because the inductor current declines to zero and a subsequent oscillation between inductor and parasitic MOSFET capacitors starts in which the voltage over S_{12} drops to zero and the voltage over S_{11} increases

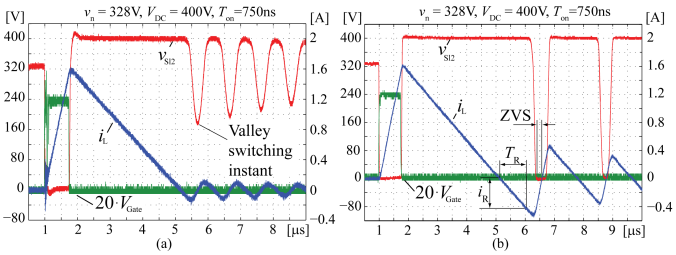

Fig. 2. Measurement results of a boost cell without (a) and with (b) an extended reverse conduction time T_R (cf. Fig. 4 (c) and (d)). To minimize the switching loss, valley switching can be applied in (a) whereas the extension of T_R allows ZVS over the complete mains period.

to the output voltage. The SiC diode is no longer necessary as in DCM the inductor current decreases to zero and hence the degrading reverse-recovery behavior of the body diode is irrelevant.

However, ZVS can only be applied in a specified input voltage range. If the input voltage exceeds half of the output voltage V_{DC} valley switching (VS) [5] can be applied where the turn-on instant of the boost switch is at the moment when the boost switch's voltage is minimal which can be seen in Fig. 2 (a).

In order to overcome the problem of loosing ZVS over the mains period, a new topology is proposed [6], [7]. The basic schematic can be seen in Fig. 3 (a). The bridge leg formed by S_{11} and S_{12} operates at high switching frequency and with ZVS. The bridge leg formed by S_{N1} and S_{N2} operates synchronously to the mains frequency. The inductor current is actively decreased below zero by increasing the on–time of S_{11} for positive and S_{12} for negative input voltages, respectively (cf. Fig. 2 (b)). As soon as a defined current flows through the inductor, an oscillation takes place and due to the increased energy in the inductor, the voltage over the switch which is about to turn on declines to zero and ZVS can be achieved. Considering Fig. 2, it can be seen that soft switching can be achieved in (b) due to the increased inductor current whereas in (a) switching losses cannot be avoided. This operation principle will be explained in detail in **section II**. Due to the triangular shaped current waveforms, this converter is called Triangular Current Mode (TCM) resonant–transition PFC rectifier.

As the inductor current ripple in TCM reduces the power factor and the THD, a multi-cell configuration can be considered whereas the superposition of the inductor currents results in a reduced input current ripple. In Fig. 3 (b) the schematics of a 3–cell configuration is shown. The interleaving of the inductor currents has to be assured by a proper control scheme which is discussed in **section III**.

The bridge leg which operates synchronously to the mains frequency connects either the output ground or the output bus to the mains which reduces common mode EMI noise significantly. In **section IV** an EMI filter design of the proposed topology is performed.

The topology in Fig. 3 (b) divides the transfered power and hence the losses into several bridge legs and inductors. This rectifier system is therefore beneficial for PCB integrated

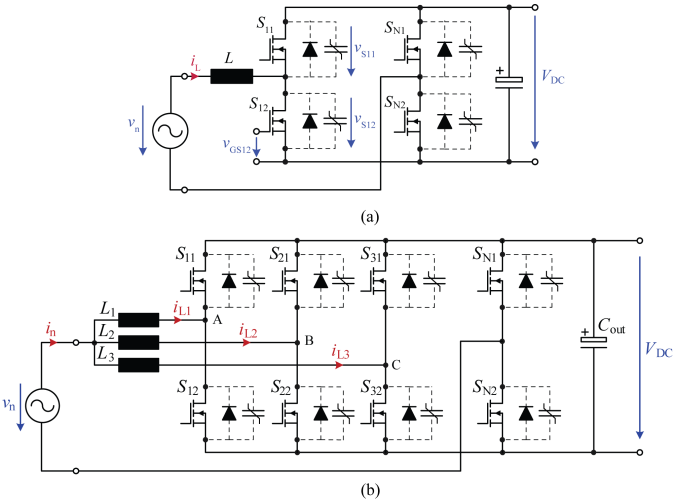

Fig. 3. (a) Single cell and (b) 3–cell configuration of a TCM PFC rectifier system with ZVS.

systems where a low heat dissipation of each element is crucial. In **section V** an ultra flat converter system called Power Sheet is introduced and measurement results for this 200 W system are shown.

II. Basic Operation

Considering the schematic given in Fig. 3 (a), switch S_{N2} is in on-state for positive input voltages v_n. This results in the simplified circuit given in Fig. 4 (a) where a single boost cell is shown. Suppose further that the input voltage v_n is larger than $V_{DC}/2$. Typical input current waveforms for critical conduction mode are depicted in Fig. 4 (c) [5]. The switching period is split into two main intervals and two short resonant transition intervals.

Interval 1

During *Interval 1* switch S_{12} is closed and voltage v_n is applied across inductor L. Hence current i_L in the inductor increases linearly. As soon as current i_S is reached or the on-time of switch S_{12} defined by the system control has passed switch S_{12} is turned off which is the end of *Interval 1* and the beginning of *Interval 2*.

Interval 2

Immediately after the turn-off instant the nonlinear MOSFET capacitance C_{oss2} is still without charge and forms together with L, C_L and C_{oss1} a resonance circuit. Since the output capacitance C_{oss2} of a MOSFET is very high (up to several nano-farads) for low voltage levels (cf. Fig. 4 (b)), voltage v_{S12} is rising slowly at the beginning. When voltage v_{S12} increases capacitance C_{oss2} decreases and hence the voltage slope becomes steep. Before voltage v_{S12} reaches the output voltage V_{DC} the voltage slope of v_{S12} deceases again since v_{S11} is very low when v_{S12} is large and therefore the capacitance of C_{oss1} is large (cf. Fig. 4 (b)) and hence the slope of v_{S11} and v_{S12} is small. The inductor current i_L keeps increasing at the beginning of *Interval 2* until v_{S12} exceeds the input voltage v_n.

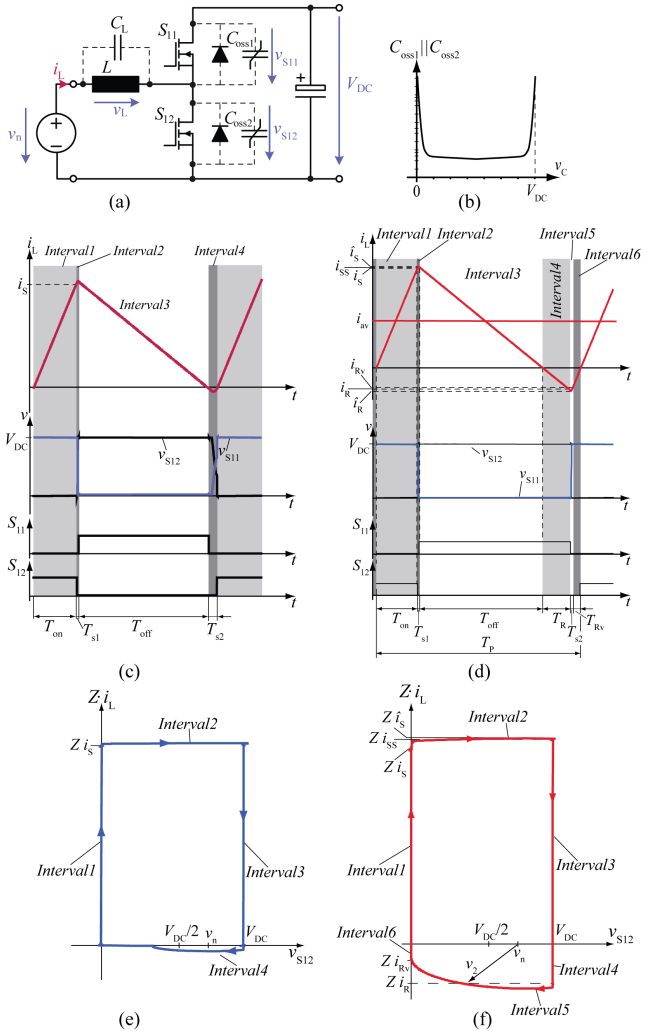

Fig. 4. (a) Single boost cell configuration for the positive half line cycle. (b) Parallel connection of the nonlinear MOSFET capacitors. (c) Current and voltage waveforms for valley switching. (d) Current and voltage waveforms for the proposed ZVS strategy. (e) *V-Zi* plot for valley switching. (f) *V-Zi* plot employing ZVS.

As soon as the inductor voltage v_L is negative the current i_L decreases.
This interval can only be described by solving a nonlinear differential equation of the charge $q(t)$ in the capacitors.

$$L \cdot \frac{d^2q(t)}{dt^2} + v_C(q(t), t) = v_n \tag{1}$$

Interval 3

When capacitor C_{oss2} is charged to the output voltage V_{DC} and C_{oss1} is discharged *Interval 3* starts and the inductor current i_L commutates to the body diode of S_{11}. After a short delay S_{11} can be turned-on at zero voltage in order to reduce conduction losses compared to pure diode operation. During this interval voltage v_L across the inductor is negative and hence the current decreases.

Interval 4

Once inductor current i_L reaches zero, S_{11} is turned off and *Interval 4* is started. Inductance L and the parasitic capacitors of the MOSFETs form a resonant circuit which starts to oscillate. The behavior of this oscillation is depended on the input voltage v_n. If input voltage v_n is less than half of output voltage V_{DC}, ZVS can be achieved since voltage v_{S11} rises to V_{DC} and v_{S12} declines to zero.
However, if input voltage v_n exceeds half of the output voltage V_{DC} the oscillation of voltage v_{S12} does not reach 0V. Hence ZVS cannot be achieved but the turn-on instant has to coincide with the instant when v_{S12} is minimal in order to minimize the switching losses (cf. Fig. 4 (c) and Fig. 2 (a)). This is pointed out in the *V-Zi* plot in Fig. 4 (e). The *V-Zi* plot shows a state graph of voltage v_{S12} and inductor current i_L which are the state variables in the system. If the system trajectory reaches the ordinate after a switching cycle, ZVS can be achieved. Thus the *V-Zi* plot clearly shows whether or not ZVS can be achieved (cf. Fig. 4 (f)) and Fig. 4 (e)).

To overcome the drawback of loosing ZVS during the mains period the following idea can be applied. Considering the current waveform in Fig. 4 (d) it is obvious that *Intervals 1 – 3* are similar to the waveforms in Fig. 4 (c). However, at zero crossing of inductor current i_L switch S_{11} is kept turned on and hence the current keeps decreasing linearly what happens in *Interval 4*.

Interval 5

As soon as a defined current i_R is reached or a given reverse conduction time T_R has passed S_{11} is turned off and an oscillation starts (*Interval 5*). During this oscillation, voltage v_{S12} reaches 0V contrary to the former case in Fig. 4 (c) due to the increased inductor current i_L. The negative current i_R enlarges radius v_2 of the oscillation trajectory in the *V-Zi* diagram (cf. Fig. 4 (f)) so that voltage v_{S12} is able to drop down to 0V. Consequently, ZVS can be achieved over the complete mains period by controlling the on-time of S_{11} and hence controlling the forced reverse current i_R in the inductor L.

Interval 6

During *Interval 6* the current i_L is commutated to the body diode of S_{12} and hence increases linearly. During this interval S_{12} can be turned on at zero voltage.

Average current i_{av}

The average current i_{av} is dependent on the input voltage v_n and can be controlled by the on-time T_{on} and the reverse conduction time T_R during each switching cycle. From Fig. 4 (d) it can be concluded that there is an infinite set of combinations $\{T_{on}, T_R\}$ which leads to a desired average current i_{av} since an increase in T_{on} can be compensated by a respective increase of T_R so that the integral of the current i_L over the switching period keeps constant. The infinite set of applicable parameters $\{T_{on}, T_R\}$ can be used to adjust the switching period which is particulary important for interleaving

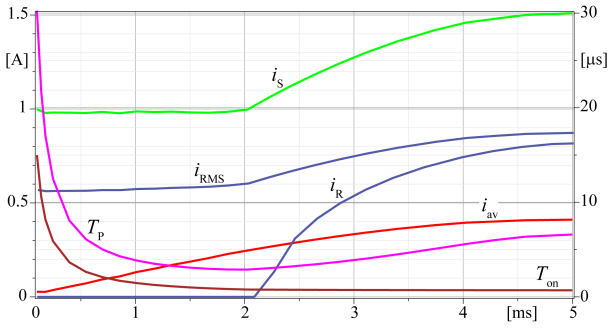

Fig. 5. Numerical results for the average current i_{av}, RMS current i_{RMS}, peak current i_S, reverse current i_R, on-time T_{on} and switching period T_P for a quarter of the mains period ($P_{out} = 200$ W).

of several boost cells. However, large values of i_S and i_R result in an increased RMS value of i_L and hence increased losses. It is thus benefical to keep the switching period as short as possible.

The average current i_{av} can be calculated numerically by integrating each interval (cf. Fig. 4 (d)) over a switching period for an input voltage v_n.

$$i_{av} = \sum_{Interval\,j=1}^{6} \frac{1}{T_j} \cdot \int_j i_L(t) \cdot dt$$

$$T_1 = T_{on}, \quad T_2 = T_{S1}, \quad T_3 = T_{off}$$
$$T_4 = T_R, \quad T_5 = T_{S2}, \quad T_6 = T_{Rv}$$

By solving this equation for a given set of input voltages a table is obtained in which the timing parameters are listed as a function of the input voltage v_n to obtain the required average current i_{av}.
In Fig. 5 numerical results of the average current i_{av} and the RMS current i_{RMS} are shown for a quarter of the mains period. It can be seen that a reverse current i_R is necessary from an input voltage of 200 V. The figure shows further the on-time T_{on}, the switching period T_P and the peak current i_S.

III. Multi-Cell Operation

A drawback of the proposed TCM PFC rectifier is the large ripple of the inductor current i_L which results in a reduced power factor, a large THD value and hence a large DM EMI filter. To obtain a smooth input current a multi-cell configuration can be considered (cf. Fig. 3 (b)) where the superposition of several inductor currents results in a smooth input current i_n. However, the interleaving of the respective inductor currents has to be controlled.

In Fig. 6 the simulation results of a 200 W 3–cell configuration PFC rectifier systems are shown. As can be seen the discontinuous inductor currents are well interleaved which results in smooth input current i_n. Applying a 1^{st} order low pass filter with a cut-off frequency of 20 kHz an input current i_n^* can be obtained which has a THD value of 1.5 %.
A proper control is crucial for the exact interleaving of the inductor currents. The timing of the switches depends strongly

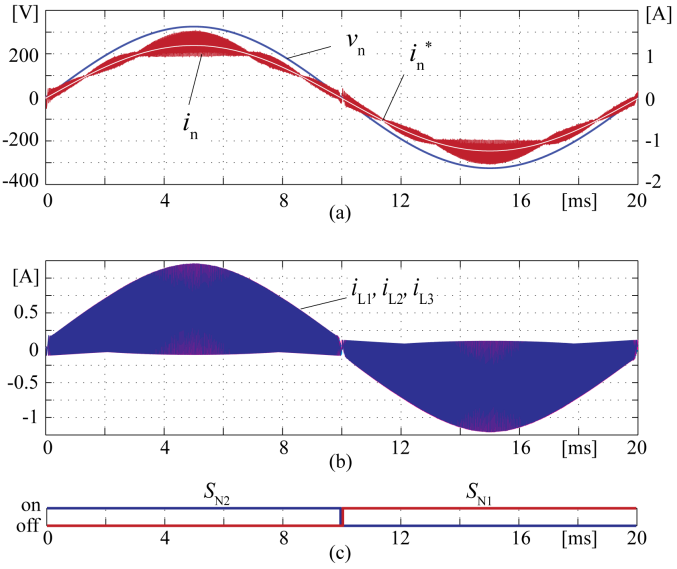

Fig. 6. Simulation results for a 3–cell configuration 200 W system (cf. Fig. 3 (b)). (a) Mains voltage v_n, input current i_n and 1^{st} order low pass filtered input current i_n^* ($f_c = 20$ kHz). (b) Inductor currents. (c) Gate signals of the low frequency switching bridge leg.

on the boost inductances and parasitic output capacitances of the switches, so any parameter tolerances have be compensated by the control.

In Fig. 7 the control structure is shown. It consists of a inductor current control for each boost cell which also controls the interleaving of the currents and a superimposed output voltage control.
The control of the switches is performed with a state machine which has the timing data (T_{on}, T_R and T_{S2}) and a zero crossing signal of each inductor current as parameters. The timing data has nonlinear behavior during a mains period and due to the complex analysis and the high switching frequency of the boost cells the DSP would be too slow to derive the parameters under operation. Therefore, the parameters are derived a priori (cf. Fig. 5) and stored in a lookup table for a discrete number of input and output voltages. The timing data is thus continuously read out of the table during operation and sent to the state machine which is implemented in a FPGA.
In addition the sign of the input voltage v_n is transferred from the DSP to the FPGA. Depending on this sign either the lower switches (S_{12}, S_{22}, S_{32} in Fig. 3 (b)) or the upper switches (S_{11}, S_{21}, S_{31} in Fig. 3 (b)) operate as boost switches or freewheeling switches, respectively. Additionally, the sign of the input voltage controls the bridge leg consisting of S_{N1} and S_{N2} in Fig. 3 (b) which is pointed out in Fig. 6 (c).

The state machine goes through each interval of a switching period (cf. Fig. 4 (d)). So after the on-time T_{on} has passed the state machine waits a constant delay time T_{S1} before the freewheeling switch is turned on. After zero crossing of the inductor current i_L, the reverse conduction time T_R (*Interval 4* in Fig. 4 (d)) passes which ensures ZVS over the mains period. Subsequently, an oscillation interval occurs in

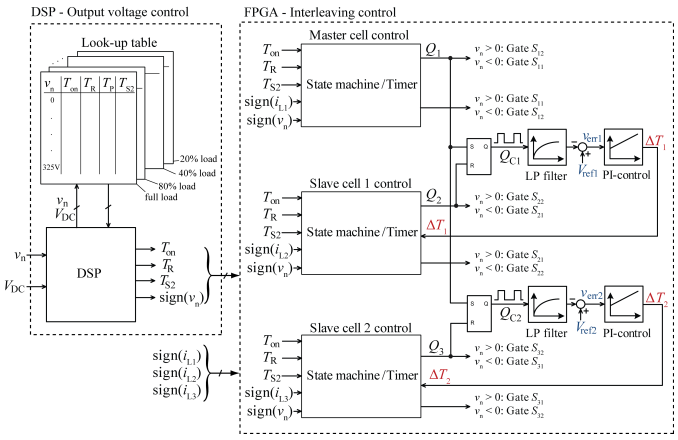

Fig. 7. Schematic of the control structure of the converter system which is subdivided in an interleaving current control and a superimposed output voltage control.

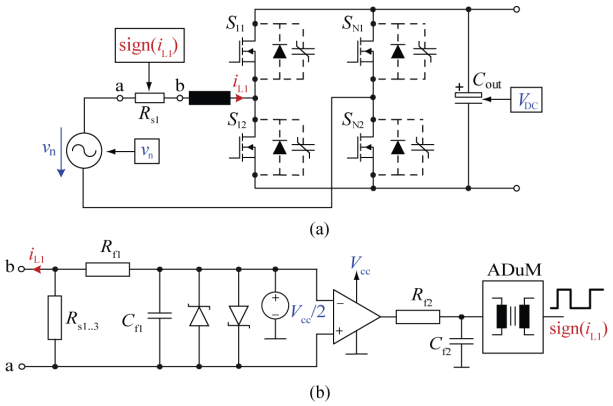

Fig. 8. (a) Measurement of input voltage v_n, output voltage V_{DC} and zero-crossing of the inductor current sign(i_L) is required for a proper system control. In (b) the measurement of the zero-crossing of the inductor current is shown which is realized by a shunt resistor.

which the current commutates back to the body diode of the boost switch. The new switching period is initiated by the zero crossing of inductor current i_L.

The zero crossing of the inductor currents is measured with a shunt resistor in the inductor path which can be done for low power converter systems. In Fig. 8 (b) the zero crossing measurement schematic is shown which consists of comparator stage and a subsequent galvanic isolation for the signal. An alternative method including a saturable current transformer which is beneficial for high power converters can be found in [8]. However, for low power, low profile and high frequency systems the shunt resistor is beneficial as the power dissipation in the shunt is low due to the low inductor currents whereas the high switching frequency would lead to considerable core losses in a current transformer.

In Fig. 8 (a) the shunt resistor is shown in the schematics and it is pointed out that the input voltage v_n, the output voltage V_{DC} as well as the zero crossing signal of the inductor current sign(i_L) is required for the proposed control scheme.

The interleaving control method is based on [9]–[11]. The three boost cells are subdivided into a master cell and two slave cells. It should be noted that this interleaving control can easily be extended to more interleaved stages as well.

The principle of the control is explained in Fig. 9. The zero crossing signals of the inductor currents are used to control a flip-flop's output signal Q_{C1} whereas the master cell sets and the slave cell resets the flip-flop. For positive input voltages v_n the rising edges of the zero current signal trigger the flip-flop while the falling edges have to be considered for negative input voltages.

If the respective inductor currents (i_{L1} and i_{L2} in Fig. 9) are almost synchronous, the set and the reset instant are very close so that Q_{C1} is either on or off for almost the complete switching period. On the other hand, if the inductor currents are well interleaved and have a phase lag of 180° then the flip-flop's output Q_{C1} is on for the first half of the period and off for remaining time. So if the signal Q_{C1} is averaged over some switching periods and compared to a reference value V_{ref1} an error signal v_{err1} can be obtained which changes the period time of the slave cell in order to obtain perfect interleaving. The reference value $V_{ref\,x}$ can be derived by

$$V_{ref\,x} = x \cdot \frac{V_{sig}}{\#cells} \tag{2}$$

whereas V_{sig} is the flip-flop's output voltage and x is the considered slave cell number. For a 3–cell configuration, the reference value of the first slave would thus be 1.6 V and the reference value for the second slave would be 3.3 V for a signal voltage of 5 V.

The actuating signal ΔT is then added to the current on-time T_{on} and the reverese conduction time T_R. This allows a manipulation of the slave's switching period without changing its average current i_{av}. Fig. 10 (a) shows a linear behavior of the switching period T_P for different parameter sets $\{T_{on}, T_R\}$. The slave's switching period can thus be increased by enlarging T_{on} and T_R accordingly to Fig. 10 (a).

This, however, is only possible if the slave's period time T_{P2} has to be increased because the reverse conduction time T_R cannot be decreased under its lower limit. Otherwise, ZVS operation would be lost. So in this case only T_{on} is changed which causes a transient average current reduction (cf. Fig. 10 (a)).

In Fig. 10 (b) the control response after a disturbance or a start up is shown. After a few switching cycles proper interleaving is obtained, so a fast control response after disturbances is ensured by this control scheme.

The output voltage V_{DC} is controlled by adapting the timing data which is sent to the FPGA. Fig. 11 shows the on-time T_{on} as a function of the output power P_{out}. As can be seen this relation is almost linear. Hence the timing data can easily be adapted by scaling. However, in order to keep calculation errors small, data tables for several output power values are stored as is indicated in Fig. 7. Based on these tables a linear regression can be performed by the DSP which allows an accurate control of the average value of input current i_{av} and hence the output voltage V_{DC}.

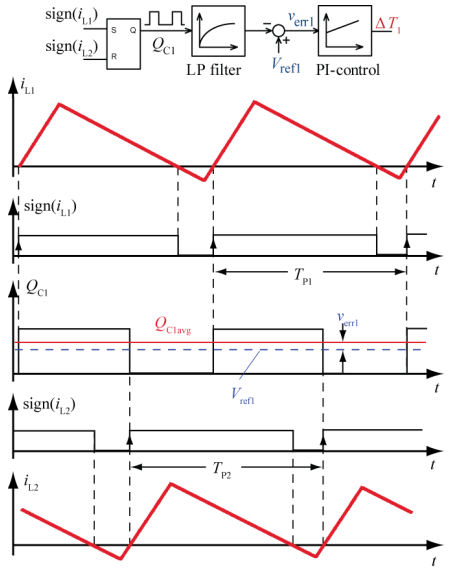

Fig. 9. Evaluation of the control signal for the interleaving control (cf. Fig. 7) which is based on the sign of the inductor currents $i_{L1} - i_{L3}$.

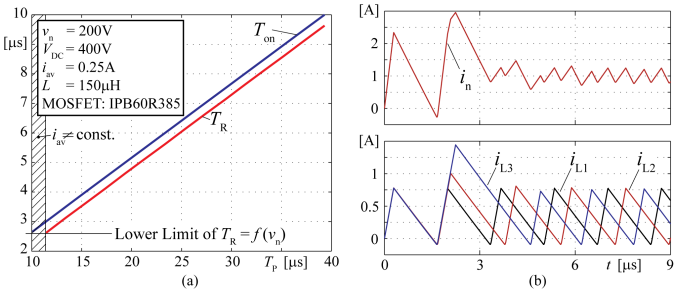

Fig. 10. (a) On-time T_{on} and reverse conduction time T_R as a function of the switching period T_P. So in order to adjust the switching period T_P, a corresponding parameter set $\{T_{on}, T_R\}$ can be found for a constant average current i_{av}. The lower limit of T_R is a function of the input voltage v_n. Below this limit i_{av} cannot be kept constant. (b) Simulation results of the interleaving control. After a few switching periods the interleaving of the inductor currents i_{L1-L3} is achieved properly after a disturbance.

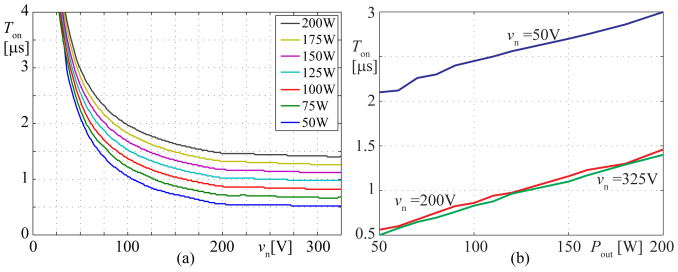

Fig. 11. (a) On-time T_{on} as a function of the input voltage v_n and the output power P_{out} as parameter. (b) On-time T_{on} as a function of the output power P_{out} for several input voltages v_n. As can be seen the relation between T_{on} and P_{out} is almost linear.

IV. EMI Filter Design

As already mentioned in the introduction, this topology has beneficial properties concerning EMI noise. Due to the interleaving of several boost cells the high ripple content of the inductor currents i_{L1} through i_{L3} is reduced. Consequently, the differential mode noise is reduced resulting in a smaller filter size. However, in order to obtain good efficiency at light load conditions it is beneficial to operate with a reduced number of parallel cells [12]. The partitioning of the output power is shown in Table I. As the DM filter has to be designed for the worst case scenario of operation, the EMI spectra of all operation modes are investigated.

TABLE I
CELL SHEDDING PARTITIONING.

P_{out}	Number of active cells
0 – 70 W	1
71 W – 130 W	2
131 W – 200 W	3

In Fig. 12 (a) simulation results of the DM EMI spectrum are given. The spectrum is shown up to 3 MHz which is reasonable for simulation-based EMI design. It can be seen that single cell operation mode of the converter exhibits the most DM noise as expected because although the current ripple amplitude is low for light load which results in a decrease of EMI noise of several dB, the complete current ripple is transferred to the mains. As a consequence the DM filter has to be designed for this operation mode [13].

A two stage filter has been considered whereas the first stage consists of C_{DM1}, L_{DM} as well as a damping resistor R_d and a bypass inductor L_b. The second stage consists of C_{DM2} and the LISN resistor as indicated in Fig. 12 (c). The parameter values can be found in Table II. The attenuated DM EMI spectrum is shown in Fig. 12 (a) for the single cell configuration and it can be seen that Class B is achieved with a safety margin of 10 dB.

In Fig. 12 (b) the common mode noise is shown for 3–cell operation at 200 W. It is obvious that CM noise is maximal for the 3–cell configuration as all three bridge legs are then varying between V_{DC} and 0V. A capacitance of 50 pF has been considered between points A and earth, B and earth, as well as C and earth (cf. Fig. 3 (b)) which is based on the assumption that MOSFETs and earth plane build a plate capacitor setup. Again a two stage filter is designed whereas C_{CM1} and L_{CM} form the first stage and C_{CM2} together with the LISN resistor are the second stage. The parameters of the CM filter can be seen in Table II. The attenuated CM EMI spectrum is shown in Fig. 12 (b).

The EMI filter structure consisting of differential mode and common mode filter is shown in Fig. 12 (c). The DM inductor can partially be realized by the leakage of the CM choke which reduces the filter size. In order to get a symmetrical setup the DM inductor and the damping network are divided to both lines.

V. Laboratory Setup

In order to validate the analysis and the simulation results, a 200 W prototype has been designed with an extreme aspect ratio

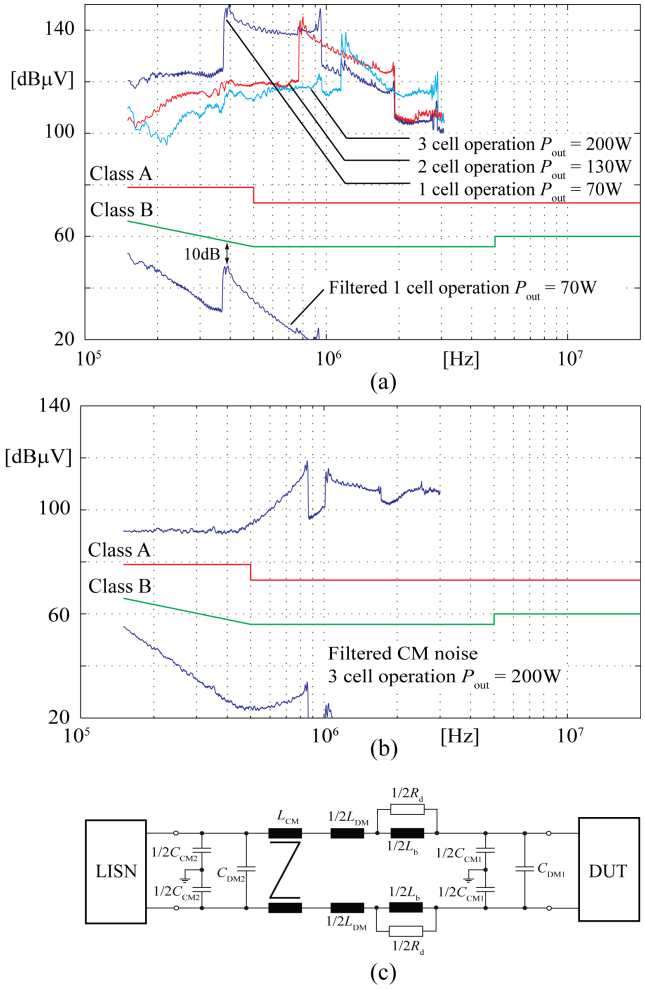

Fig. 12. (a) Differential mode EMI spectrum for 1–cell, 2–cell and 3–cell operation at different load conditions. Measurements would show a noise floor at about 30 – 40 dBµV which is not considered in the simulation. (b) common mode EMI spectrum for full load condition. (c) Schematic of the EMI filter structure [13].

TABLE II
EMI FILTER PARAMETERS.

DM Filter			CM Filter		
C_{DM1}	=	1 µF			
L_{DM}	=	90 µH	C_{CM1}	=	100 nF
R_d	=	4.7 Ω	L_{CM}	=	160 µH
L_b	=	90 µH	C_{CM2}	=	140 nF
C_{DM2}	=	1.4 µF			

so that the thickness of the converter system does not exceed 1 mm. In order to obtain an ultra flat system several components have to be integrated in the PCB. In the proposed topology the losses are distributed to several boost cells. This is of special interest due to the stringent thermal limitations in the PCB. This low profile converter system is called Power Sheet [14] and finds various application in mobile electronics, smart surfaces, lighting and solar energy systems. Fig. 13 shows a 3D design of the 200 W converter system which is designed to achieve a low profile. As can be seen most of the components are still surface mounted which simplifies tests and measurements. In a

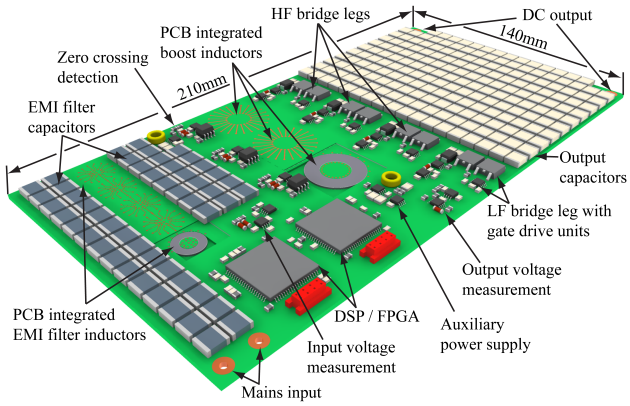

Fig. 13. CAD drawing of a 200 W 3–cell interleaved TCM PFC rectifier. The output capacitor is realized by a SMD caps bank in order to obtain a small profile. The boost inductors and the EMI filter inductors are realized with integrated cores [14]. The bridge legs are separated into low frequency (LF) and high frequency (HF) bridge legs.

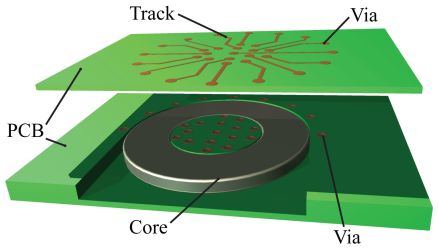

Fig. 14. Principle of PCB integrated inductors. The cores are integrated in the PCB whereas the winding is realized as tracks and vias [14].

further step each component is integrated into the PCB which results in a low profile converter system.

The boost and the EMI filter inductors are already integrated in the PCB [14]. Fig. 14 shows the integration principle of the boost inductance where the core is embedded in the PCB and the windings are realized as tracks and vias. The circuit parameters of the converter system are given in Table III.

In Fig. 15 measurement results for the circuit given in Fig. 4 (a) are shown. Here, for two different input voltages ($v_n = 60$ V and $v_n = 325$ V) several switching cycles are measured. In both cases ZVS is achieved which confirms the simulation results and the analysis.

TABLE III
CIRCUIT PARAMETERS.

Inductors	
L	150 µH
MOSFETs IPB60R385CP [15]	
$R_{DS(on)}$	385 mΩ @ 25 °C
V_{DS}	650 V
$Q_{g,typ}$	17 nC
Output Capacitor [16]	
C_{out}	220 nF
V_{max}	630 V
230 in parallel	

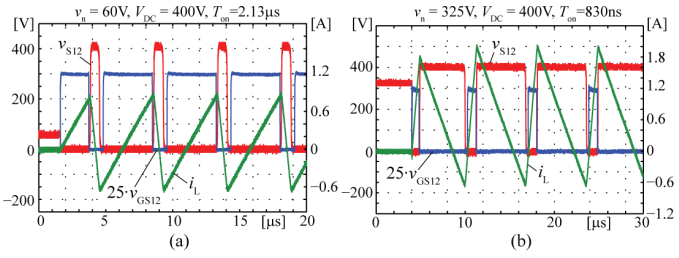

Fig. 15. Measurement results for the circuit given in Fig. 3 (a). In (a) operation for $v_n = 60$ V is shown whereas in (b) $v_n = 325$ V. As can be seen ZVS can be achieved for each case.

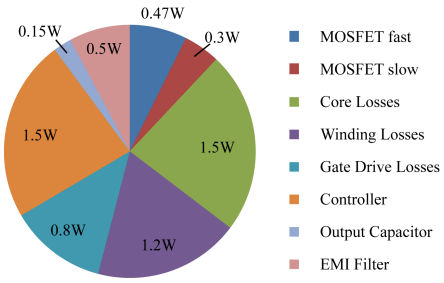

Fig. 16. Loss distribution of the PFC converter system at nominal load of 200 W and components corresponding to Table III. The total losses are 6.42 W which results in an efficiency of 96.9 %.

A breakdown of losses for a 3–cell configuration at 200 W output power is shown in Fig. 16. Here the switches are subdivided in fast MOSFETs and slow MOSFETs which corresponds to their switching frequency. Since zero voltage switching is achieved over the complete mains period no switching losses have to be considered. The high operation frequency, however, which varies between 400 kHz and 600 kHz causes considerable losses in the gate drive circuits. Consequently, the MOSFETs should have a low gate charge in order to minimize these losses. The total power loss is 6.42 W and hence an efficiency of 96.9 % can be achieved.

The proposed topology can be applied to high power systems of several kWs [8].

VI. Conclusion

In this paper a topology of a highly compact and highly efficient single-phase PFC rectifier system is presented. The converter consists of several paralleled boost-cells operating in Triangular Current Mode (TCM) with resonant transition and one bridge-leg which switches at the zero crossing of the mains voltage. ZVS is achieved over the full mains period by proper control of the power MOSFETs. The superposition of the discontinuous inductor currents results in a reduced input current ripple. A control scheme is discussed in detail which include current control, interleaving control and a superimposed output voltage control.

The low frequency bridge leg connects one of the output rails to the mains. This results in reduced common mode noise compared to conventional bridgeless PFC rectifier systems. Conducted EMI emission is discussed for both differential mode and common mode noise. A filter is designed in order to attenuate the noise in worst case operation which is single cell operation for DM noise and 3–cell operation for CM noise. So the topology combines several desireable properties:

- Minimal conduction loss due to synchronous rectification
- ZVS over the complete mains period
- Reduced conduction loss as the MOSFET's output capacitances do not affect the losses and larger chip areas can be used
- Smooth input current due to the multi-cell configuration
- Low common mode noise
- Bidirectional operation possible

An ultraflat 200 W PFC rectifier has been built up and measurement results are shown which confirm analysis and simulations. An efficiency of 96.9 % can be achieved with this topology.

References

[1] B. Lu, R. Brown, and M. Soldano, "Bridgeless PFC implementation using one cycle control technique," in *20th Annual IEEE Applied Power Electronics Conference and Exposition, (APEC)*, vol. 2, pp. 812–817 Vol. 2, 2005.

[2] J. W. Kolar, J. Biela, and J. Miniboeck, "Exploring the pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2 % efficiency vs. 7 kW/dm^3 power density," in *14th International Power Electronics and Motion Control Conference. (IPEMC), IEEE*, 2009.

[3] P. Kong, S. Wang, and F. C. Lee, "Common mode EMI noise suppression in bridgeless boost PFC converter," in *22nd Annual IEEE Applied Power Electronics Conference, (APEC)*, pp. 929–935, 2007.

[4] H. Ye, Z. Yang, J. Dai, C. Yan, X. Xin, and J. Ying, "Common mode noise modeling and analysis of dual boost PFC circuit," in *26th International Telecommunications Energy Conference, (INTELEC)*, pp. 575–582, 2004.

[5] L. Huber, B. Irving, and M. Jovanovic, "Effect of valley switching and Switching-Frequency limitation on Line-Current distortions of DCM/CCM boundary boost PFC converters," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, pp. 339–347, 2009.

[6] J. W. Kolar, J. Miniboeck, J. Biela, and C. Marxgut, *Bidirektionaler, verlustarm schaltender Konverter (Modulation and topology for a bidirectional, soft switching PFC converter)*. Patent Application, 2009.

[7] J. W. Kolar, J. Biela, and D. Hassler, *Bidirektionaler, verlustarm schaltender Konverter (Control concept and topology for a bidirectional, soft switching PFC converter)*. Patent Application, 2010.

[8] J. Biela, D. Hassler, J. Miniboeck, and J. W. Kolar, "Optimal Design of a 5 kW/dm^3 / 98.5 % TCM Resonant Transition Single Phase PFC Rectifier," in *IEEE/IEEJ International Power Electronics Conference, (IPEC/ECCE Asia), Sapporo, Japan*, 2010.

[9] L. Huber, B. Irving, and M. Jovanovic, "Closed-Loop control methods for interleaved DCM/CCM boundary boost PFC converters," in *24th Annual IEEE Applied Power Electronics Conference and Exposition, (APEC)*, pp. 991–997, 2009.

[10] M. Elmore, "Input current ripple cancellation in synchronized, parallel connected critically continuous boost converters," in *11th Applied Power Electronics Conference and Exposition, (APEC)*, vol. 1, pp. 152–158 vol.1, 1996.

[11] X. Xu and A. Huang, "A novel closed loop interleaving strategy of multiphase critical mode boost PFC converters," in *23rd IEEE Applied Power Electronics Conference and Exposition, (APEC)*, pp. 1033–1038, 2008.

[12] C. Wang, M. Xu, F. C. Lee, and Z. Luo, "Light Load Efficiency Improvement for Multi-Channel PFC," in *39th IEEE Power Electronics Specialists Conference, (PESC)*, 2008.

[13] R. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*. Springer, 2nd ed., 2001.

[14] C. Marxgut, J. Biela, and J. W. Kolar, "Design of a Multi-Cell, DCM PFC Rectifier for a 1 mm thick, 200 W Off-line Power Supply - The Power Sheet," in *6th International Conference on Integrated Power Electronic Systems. (CIPS), IEEE*, 2010.

[15] Homepage Infineon. http://www.infineon.com.

[16] Homepage Murata. http://www.murata.com.