Analysis of the Trade-Off Between Input Current Quality and Efficiency of High Switching Frequency PWM Rectifiers

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***Abstract*— Due to their basic physical properties, power MOSFETs exhibit an output capacitance $C_{\rm oss}$ that is dependent on the drain-source voltage. This (nonlinear) parasitic capacitance has to be charged at turn-off of the MOSFET by the drain-source current in rectifier applications which yields input current distortions. As a detailed analysis shows, the nonlinear behavior of this capacitance is even more pronounced for modern super junction MOSFET devices. Whereas $C_{\rm oss}$ increases with increasing chip area the on-state resistance of the MOSFET decreases accordingly. Hence, a trade-off between efficiency and input current distortions exists. A detailed analysis of this effect considering different semiconductor technologies is given in this work and a Pareto curve in the η-THD space is drawn which clearly highlights this relationship. It is further shown, that the distortions mentioned can be reduced considerably by application of a proper feed-forward control signal counteracting the nonlinear switching delay due to $C_{\rm oss}$. The theoretical considerations are verified by experimental results taken from 10 kW laboratory prototypes with the switching frequencies of 250 kHz, and 1 MHz.**

***Index Terms*— Input current quality, Efficiency, Super junction, High frequency power converters.**

I. Introduction

Driven from new applications fields, e.g. power electronics in aircraft [1] modern rectifier systems have to satisfy increased requirements concerning efficiency, weight and compactness. Furthermore, they will have to comply with upcoming standards containing rigorous input current harmonic limits. Active PWM-rectifiers with low total harmonic distortion (THD) of the input current and a high power factor are required. Active three-phase rectifiers typically show a large high-frequency noise level and passive low-pass filters have to be used to reduce conducted emissions (CE). These passive elements together with the boost inductance occupy a relative large portion of system volume (approx. 30 %) and their size can only be reduced by increasing the switching frequency [2].

As presented in [3], the three-phase/level rectifier topology shown in **Fig. 1** emerged as an ideal topology for a high power density unity power factor rectifier. Due to its reduced semiconductor voltage stress, high efficiency MOSFETs with a blocking voltage of 600 V can be applied even for a grid voltage of $V_{\rm N} = 230\,{\rm V}$ and an output voltage of $V_{\rm o} = 800\,{\rm V_{DC}}$. In order to achieve a high system efficiency conduction losses as well as switching losses have to be reduced. The on-state resistance of high-voltage (HV) MOSFETs ($V_{\rm BR,SS} = 600\,{\rm V}$) is dominated by the drift region resistance and it is well known that this resistance

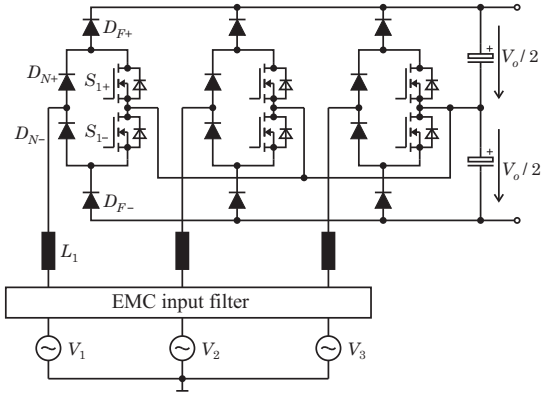


Fig. 1: Active three-phase/level PWM-rectifier used to study the trade-off between input current quality and efficiency.

is intrinsically dependent on the break-down voltage $V_{\rm BR,SS}$ of the device

$$R_{\rm DS,on} \propto {V_{\rm BR,SS}}^{2.4...2.7} \tag{1}$$

(cf., [4]). Super junction (SJ) devices, e.g. CoolMOS [5], break with this rule and achieve much lower area specific on-state resistances [6]. Switching losses are often dominant for high-frequency (hard) switched converters. In order to limit switching losses, the switching speed must be increased if the converters' switching frequency is rised. The switching speed is determined mainly by parasitic elements of the power devices (MOSFETs and diodes) and by the wiring. Hence, the parasitic capacitances of the MOSFET mainly influence the system behavior and efficiency [7]. In respect of losses a more meaningful Figure Of Merit (FOM)

$$FOM = \frac{1}{R_{\rm DSon} E_{400\rm V}} \tag{2}$$

can be defined, where R_{DSon} is the MOSFETs on-state resistance and $E_{400\rm V}$ is the stored energy in the MOSFETs output capacitance ($C_{\rm oss}$) at $V_{\rm DS} = 400\,{\rm V}$. Modern SJ devices exhibit smaller output capacitances (at $V_{\rm DS} = 400\,{\rm V}$) than standard HV-MOSFETS and are therefore ideally suited for hard-switched high-frequency rectifier systems. The MOSFETs output capacitance is proportional to the chip area $A_{\rm Chip}$ and shows a strong nonlinear dependency on the applied drain-source voltage. For typical SJ devices this capacitance rises from a few 100 pF to over 10 nF for low-blocking voltage levels. As reported in [8] this effect causes long delay times at turn-off of the device which results in significant current distortions at lower current levels. This effect is even more distinctive if higher switching frequencies

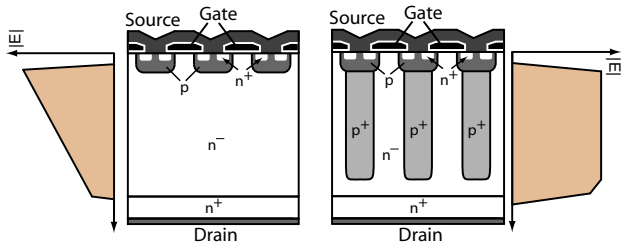


Fig. 2: Cross-section and electrical field distribution of (a) a conventional HV-MOSFET and (b) a super junction device (e.g. CoolMOS)). Whereas the HV-MOSFET shows a triangular shaped electrical field distribution a SJ device shows a mostly squared distribution.

are used or if a device with a large chip area is applied. This is in basic contradiction to the requirement of low conduction losses (low $R_{\mathrm{DS,on}}$). A trade-off between efficiency and input current quality has to be accepted at selection of the switches.

In section II and III the origin and impact of this input current distortions are analyzed in detail, and in section V the power losses of the rectifier system are calculated. Based on these results a η-THD Pareto Front is derived in section VI which clearly illustrates the trade-off between efficiency and input current quality. More information about the Pareto Front concept can be found in [9].

II. Switching Model of a Power MOSFET

In **Fig. 2** the structure of a "conventional" high-voltage MOSFET is shown together with the structure of a SJ device. For HV-MOSFETs a low-doped n^- drift-zone (resulting in a wide depletion zone at blocking of the device) is used to achieve the required breakdown voltage. The degree of doping and the length of this n^- layer is therefore dependent on the breakdown voltage and as the full drain-source current has to flow through this layer also the on-state resistance of the device depends on the breakdown voltage which finally results in the relation given in (1). As also depicted in **Fig. 2(a)** the structure of a HV-MOSFET results in a triangular electrical field distribution.

In order to further improve the on-state resistance of high voltage MOSFETs SJ devices have been introduced [5]. SJ devices are based on the idea of charge-balancing between alternating n- and p-regions during the blocking state. As apparent in **Fig. 2(b)** p-pillars are inserted which range deep into the n^- layer. The additional charge of the higher doped n-layer (used to reduce the on-state resistance) is balanced by the p-doped regions[1] and this yields a lateral electrical field component. If a blocking voltage is applied to the device the space charge region initially grows laterally along the p-n junction and at a relative low blocking voltage, e.g. 50 V, the full area is depleted. In order to further increase the blocking voltage the depleted region acts like a pin-structure and only the vertical electrical field component is increased for higher blocking voltages resulting in an almost rectangular electrical field distribution. The SJ-structure has been analyzed in detail in [10] and the calculation shows, that the on-state resistance is only linearly dependent on the breakdown voltage

$$R_{\mathrm{DS,on,SJ}} \propto V_{\mathrm{BR,SS}} \ . \tag{3}$$

The operating principle of SJ devices is based on a perfect charge compensation in the n- and p-pillars and as it is shown in [11] a charge imbalance would yield a reduced breakdown voltage $V_{\mathrm{BR,SS}}$. The fabrication of mostly charge compensated n- and p-pillars is hence the key to enable this technology. Detailed information on the device physics, realization issues and behavior of SJ devices can be found in [12]-[14].

[1]Since the additional charges in the n^--layer are compensated by the p-columns these devices are also called "charge-compensated devices".

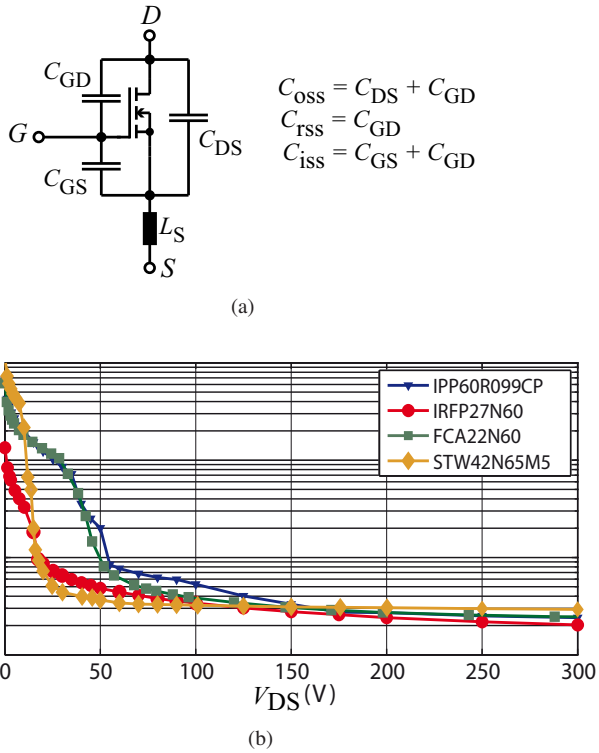


Fig. 3: (a) Equivalent circuit of a power MOSFET valid for frequencies up to several MHz. (b) Measured area specific output capacitance C^*_{oss} as a function of the applied blocking voltage V_{DS} of several SJ devices from different manufacturers compared to a HV-MOSFET (IRFP27N60).

In **Fig. 3(a)**, a simplified equivalent circuit of a power MOSFET is shown which is valid for frequencies up to several MHz. The capacitances C_{GS}, C_{GD} and C_{DS} are actually distributed over the whole surface area of the device and are lumped to these single capacitors. In addition, the parasitic inductance of the source lead L_{S} is depicted. High di/dt-rates of the drain-source current induce a voltage that reduces the effective gate voltage in terms of a negative feedback. This parasitic inductance has a major impact on switching losses and its impact can only be reduced by increasing the gate-voltage. Whereas C_{GS} shows only minor variations with applied V_{DS} the capacitances C_{GD} and C_{DS} are strongly dependent on V_{DS}.

If a blocking voltage is applied to a HV-MOSFET a space charge region grows into the epi-layer n^- and this junction-depletion capacitance is modeled by the capacitance C_{DS}. It is directly proportional to the chip area A_{Chip} and shows for HV-MOSFETs the relation

$$C_{\mathrm{DS}} \approx A_{\mathrm{Chip}} \cdot C^*_{\mathrm{DS}} \frac{1}{\sqrt{V_{\mathrm{DS}}}} \tag{4}$$

TABLE I: Parameters of the MOSFETs used for benchmarking.

	$V_{\mathrm{BR,SS}}$ (V)	A_{Chip} (mm^2)	C^*_{oss} ($\mathrm{nF/mm}^2$) (300 V)	$R^*_{\mathrm{DS,on}}$ (Ω mm^2) (25 °C)	$(R_{\mathrm{DSon}}E_{400\mathrm{V}})^{-1}$ $(\Omega\mu\mathrm{J})^{-1}$ (FOM)	Q^*_{G} ($\mathrm{nC/mm}^2$) (15 V)	$E_{400\mathrm{V}}$ (μJ) (400 V)
IPP60R099CP	650	30	2.4	2.7	0.97	2.8	11.5
IRFP27N60	600	59	2	10.6	0.44	3.0	12.5
STW42N50M5	650	33	2.9	2.6	1.58	4.3	8
FCA22N60	600	19.5	2.45	3.2	0.81	3.89	7.5
SiC JFET	1200	8	12.5	0.36	2.26	7.5[1)]	4.9

[1)] V_{gate} =2.5 V.

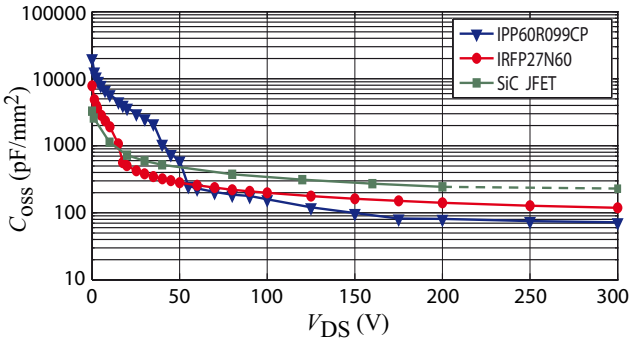


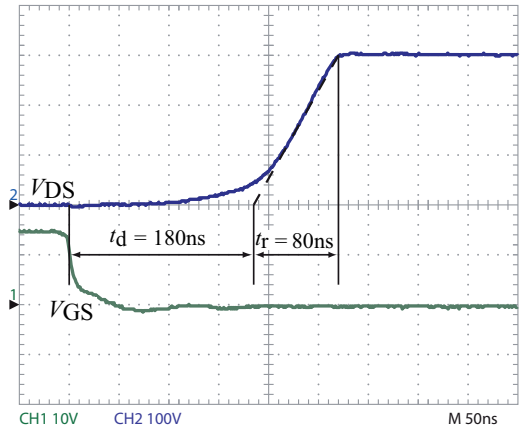
Fig. 4: Measured output capacitance C_{oss} of a HV-MOSFET (IRFP27N60), a SJ device (IPP60R099CP) and a SiC-JFET (1200 V/30 A, normally OFF) as a function of the applied blocking voltage V_{DS}.

(cf., [15]). The voltage dependence of the gate-drain capacitance C_{GD} is very similar to C_{DS} even if it is not a junction-depletion capacitance but this is not discussed further here for the sake of brevity.

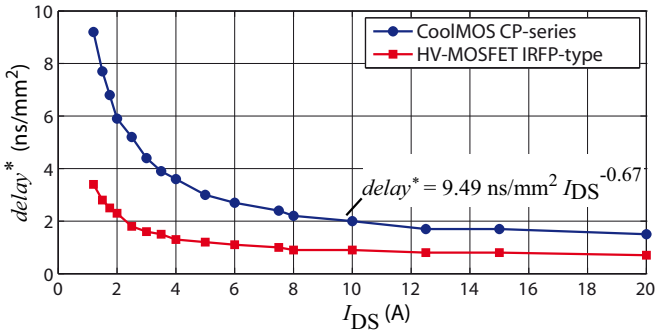
Fig. 3(b) shows the measured output capacitance per chip area $C^*_{\mathrm{oss}} = C^*_{\mathrm{DS}} + C^*_{\mathrm{GD}}$ of a "conventional" HV-MOSFET (IRFP27N60) compared to the output capacitance of SJ devices of different manufacturers. The behavior given in (4) is obvious for the HV-MOSFET.

In SJ MOSFETs, the space charge region starts to grow along the p-n junctions of the inserted p-stripes if a blocking voltage is applied to the device which yields to a drastically increased internal surface of the pn-junction [16]. Consequently, C_{oss} is very large at low V_{DS} and (4) is not valid for these devices. At a relative low blocking voltage ($\approx$ 50 V) the depletion layers of the pn-junctions merge and at this point C_{oss} decreases abruptly. According to **Fig. 3(b)** all SJ-devices show this effect and the devices from different manufacturers only differ in the drain-source voltage where this abrupt decrease occurs.

In **Fig. 4** the measured output capacitances C_{oss} of a SJ device (IPP60R099CP) and a HV-MOSFET (IRFP27N60) are plotted together with the output capacitance of a 1200 V/30 A normally-off SiC-JFET device (SJEP120R063). Specific parameter of the devices are listed in TABLE I. The small chip area required for the SJ device yields to a small C_{oss} at V_{DS}=300 V. Because of the larger chip area, the HV-MOSFET shows a higher C_{oss} at V_{DS}=300 V but its capacitance only rises according to (4) and is much smaller than the C_{oss} of the SJ device for $V_{\mathrm{DS}} < 50$ V. In comparison to the devices based on the Si-technology, the SiC JFET requires the smallest chip-area but shows the largest C_{oss} at 300 V. However, only a rather small rise can be observed at smaller drain-source voltages.



(a)



(b)

Fig. 5: (a) Measured inductive turn-off switching characteristic of the SJ device IPP60R099CP at a drain current of 1.3 A and (b) measured chip area dependent turn-off delay of the CoolMOS CP-series and the HV-MOSFET IRFP-type as a function of I_{DS}.

A. *Turn-off delay of MOSFET*

In PFC-applications C_{oss} has to be charged by the input current at turn-off of the MOSFET and the voltage-rise of V_{DS} is therefore dependent on the input current. **Fig. 5(a)** shows the measured turn-off behavior of the MOSFET IPP60R099CP for an input current of 1.3 A. The total turn-off delay can be separated in a pure delay time t_{d}, where the dramatically increased C_{oss} for $V_{\mathrm{DS}} < 50$ V is charged, and in a rise time t_{r}. This current dependent turn-off delay distorts the intended pulse pattern in terms of extended on-times and its influence rises with increased switching frequency. The drain source current dependent turn-off delays of several SJ devices of the CoolMOS CP-series (Infineon Inc., e.g. IPP60R099CP) and HV-MOSFETs (Vishay Siliconix Inc.,

TABLE II: Parameters used to approximate the turn-off delays by (5).

Semiconductor family	$delay^*$	α
CoolMOS CP-series	9.49 ns/mm^2	-0.67
IPP60R099CP	284 ns $(I_{\mathrm{DS}})^{-0.67}$	
HV-MOSFET IRFP-type	3.64 ns/mm^2	-0.54
IRFP27N60	214 ns $(I_{\mathrm{DS}})^{-0.54}$	

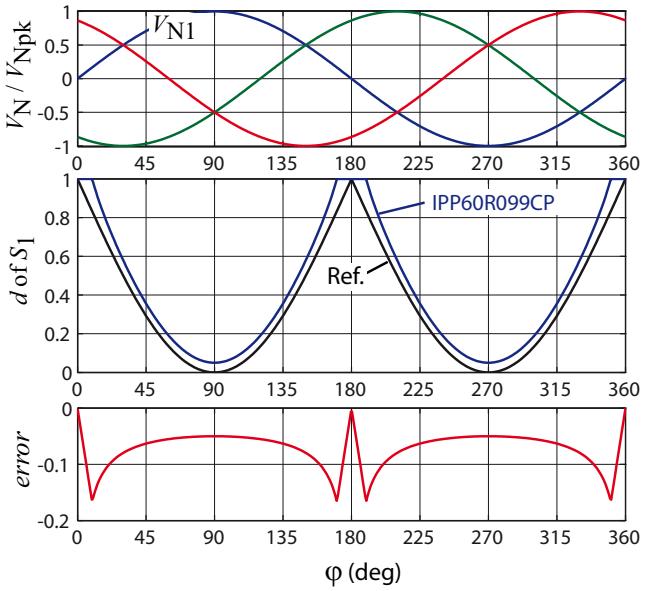


Fig. 6: Required duty cycle of phase L_1 (switch S_1) and effective duty cycle because of the turn-off delay of the MOSFET for a switching frequency of 1 MHz and P_{o} =5 kW.

e.g. IRFP27N60) have been measured. Using the specific chip areas of the devices (cf., TABLE I) the chip area specific turn-off delays of the two semiconductor families can be calculated. The results are plotted in **Fig. 5(b)**. In general, the SJ-devices show a higher chip-area specific turn-off delay than the HV-MOSFET devices. In addition, the SJ-devices show a comparatively pronounced increase of turn-off delay at smaller I_{DS}. According to [15] C_{oss} shows only minor dependence on temperature and hence the turn-off delay can be modeled without consideration of the temperature which has been confirmed by measurements. The measured turn-off delays can be approximated by

$$delay \approx A_{\mathrm{Chip}}\ delay^* \left(\frac{I_{\mathrm{DS}}}{\mathrm{A}}\right)^{\alpha} \tag{5}$$

which will be used in the next section to determine the resulting input current distortions. The parameters for the two semiconductor families are listed in TABLE II.

III. Evaluation of Input Current Distortions

In the following the effects of this duty cycle distortion will be analyzed. The required duty cycle $d_i \in [0 \ldots 1]$ of phase number i of the intended rectifier system is given by

$$d_i = 1 - \frac{\hat{V}_{\mathrm{N}}}{V_{\mathrm{o}}/2}\left|\sin\left(\varphi_{\mathrm{N}} - \frac{2\pi}{3}(i-1)\right)\right| \tag{6}$$

where for the sake of simplicity a possible third-harmonic injection used to increase the input voltage range at a given

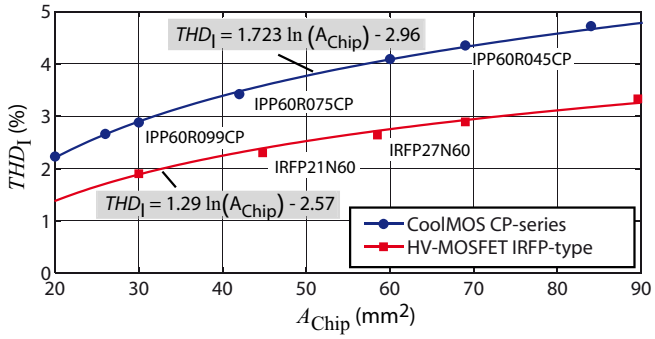


Fig. 7: Simulated THD of the input currents as a function of chip area for a 10 kW rectifier system with a switching frequency of 1 MHz ($f_{\mathrm{N}} = 50$ Hz, $V_{\mathrm{N}} = 230$ V,Vo $= 800$ V).

output voltage level is not included. This duty cycle is calculated by the controller and the generated pulse patterns of (6) are, dependent on the input current enlarged by the turn-off delay of the MOSFET (cf., **Fig. 5(b)**). Note, that the duty cycle is limited to 1 (MOSFET is permanently on). In **Fig. 6** the required duty cycle (Ref.) for an output power of P_{o}=5 kW of switch S_1 is plotted in conjunction with the grid voltages. As a unity power factor shall be achieved by the rectifier system, the input currents are assumed to be in phase with the input voltages and are therefore not shown. The required duty cycle is compared to the resulting duty cycle considering the turn-off delay for the SJ device IPP60R099CP and additionally the error is depicted. The biggest deviations can be observed in the vicinity of the phase-voltage zero-crossings where the duty cycle is near 100%. It is also apparent, that small duty cycles (turn-on times smaller than the turn-off delay) can not be realized. Of course, a duty cycle of zero (MOSFET is permanently OFF) can be achieved but this point of discontinuity is not shown in **Fig. 6**.

Subsequently, the measured delays given in **Fig. 5** are used in a computer simulation to determine the resulting input current distortions. This is not easily possible in an analytical manner as the current controller is partially able to compensate this error. The current controller is designed according to [17] and for evaluation of the input current distortions the THD-value of the input current is calculated. The results of this calculation for a switching frequency of 1 MHz ($V_{\mathrm{N}} = 230$ V,$V_{\mathrm{o}} = 800$ V,$P_{\mathrm{o}} = 10$ kW) are plotted in **Fig. 7**. A curve fitting is used to approximate the delays for further calculations and the corresponding functions for the two semiconductor families are also given. Consistent with **Fig. 5** the HV-MOSFET shows a better chip area dependent input current quality. This calculation can easily be repeated for systems with other switching frequencies (e.g. 250 kHz).

IV. Feed-forward Compensation of the Delay

The input current distortions caused by the turn-off delay of the MOSFET can be reduced considerably, if a feed-forward compensation is implemented. Thereto, the input current dependent turn-off delay d_{pre} given in (5) can be added to the current controller output $d_{1,\mathrm{contr}}$ in terms of a precontrol signal

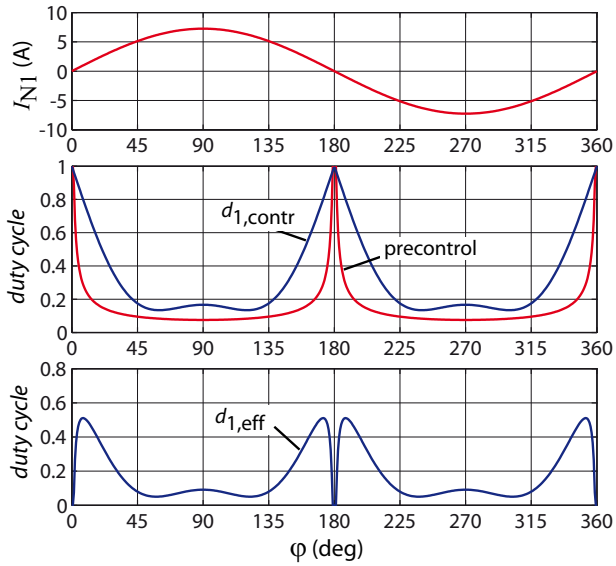


Fig. 8: Required duty cycle $d_{1,\mathrm{contr}}$ generated from the current controller and pre-control signal used to compensate the turn-off delays of the MOSFET leading to the resulting effective duty cycle $d_{1,\mathrm{eff}}$.

$$d_{1,\mathrm{eff}} = d_{1,\mathrm{contr}} - d_{1,\mathrm{pre}} \ . \tag{7}$$

As the calculation of $d_{1,\mathrm{pre}}$ (cf., (5)) is a time-consuming task in a digital controller realization, e.g. DSP, FPGA, etc., the delay given in **Fig. 6** can be approximated by piecewise linear functions.

Fig. 8 shows the required duty cycle $d_{1,\mathrm{contr}}$ in order to generate sinusoidal input currents. This duty cycle is generated by the current controller and a third harmonic injection is included which is used to increase the input voltage range. In addition, the necessary pre-control signal used to compensate the turn-off delay and the resulting effective duty cycle $d_{1,\mathrm{eff}}$ is plotted. The greatest influence of the pre-control signal can be observed in the vicinity of the input currents zero-crossings, where the duty cycle $d_{1,\mathrm{contr}}$ is almost 1. The duty cycle there has to be reduced considerably because the input current, which charges the output capacitance C_{oss} is small and enlarges the pulse width. According to **Fig. 8** the duty cycle distortion can be compensated over long periods but, dependent on the used switch, a minimum pulse-length of 100 ns-200 ns is required in order to fully turn-on the MOSFET which limits the effectiveness of the proposed feed-forward compensation signal. The pre-control signal also only compensates the signal distortions caused by the turn-off delays of the MOSFETs. As a result especially zero crossing distortions caused by the cusp-effect and by (small) phase differences between input voltage and input current, e.g. as they may occur in electronics for modern aircrafts because of the high, variable mains frequency of 360 Hz-800 Hz, will remain.

V. Power MOSFET Losses

As a next step the power losses of the rectifier system have to be calculated. In general, the power losses of a MOSFET P_{semi} can be divided into switching losses P_{sw} and conduction losses P_{con}

$$P_{\mathrm{semi}} = P_{\mathrm{sw}} + P_{\mathrm{con}} \ . \tag{8}$$

Although the conduction losses can be calculated using the on-state resistance R_{DSon} of the MOSFET, the determination of the switching losses is a more complex task. If the MOSFET turns on/off the inductive current has to commutate between the free-wheeling diode and the MOSFET. In consequence the diode and possible stray elements (stray inductances/capacitances of the wiring) have to be included in this calculation. Several research groups developed models for switching loss calculation [18]-[19] but, however, the most accurate approach is to measure the switching losses of the MOSFET diode combination. Due to the intended switching frequency of 1 MHz the SiC diode IDT10S60 has been selected. It is well known that SiC-diodes show no reverse recovery current and that a capacitive displacement current flows if a blocking voltage is applied.

Switching losses are usually separated into turn-on losses and turn-off losses. Turn-on losses can be determined by a voltage/current measurement according to [20]. At turn-off of the device the nonlinear capacitance C_{oss} is charged by I_{DS} and therefore causes no losses. However, according to [21], the energy stored in C_{oss} considerably contributes to the switching losses because C_{oss} has to be discharged at turn-on through the channel of the MOSFET. These losses are not covered by the switching loss measurement but can be calculated using the stored energy $E_{400\mathrm{V}}$ given in TABLE I.

A boost-type test circuit has been used to determine the turn-on losses. In order to give a fair comparison of different semiconductors the switching transients (v_{DS} and i_{DS}) of the SJ device IPP60R099CP are used as reference. The gate-resistors are modified until the switching transients approximately match with the reference and then the devices will show approximately equal turn-on losses (independent of the chip area). This is, however, only possible for devices showing approximately the same chip areas. The comparably fast switching transient reference for a device with a considerably larger chip area may not be achieved due to the internal gate-resistor of the MOSFET and the negative feedback behavior of the parasitic source inductance. In this work only MOSFET devices that are able to achieve the switching transient reference are considered. The measured turn-on switching loss energies as a function of I_{DS} and the junction temperature ($\Delta T = T_{\mathrm{j}} - 25\,^{\circ}\mathrm{C}$) are given in **Fig. 9**. For further loss calculations the measured turn-on switching energy curves can be fitted by

$$E_{\mathrm{on}}(\Delta T, I_{\mathrm{DS}}) = \left(k_0 + k_1 I_{\mathrm{DS}} + k_2 I_{\mathrm{DS}}^2\right)\left(1 + (\gamma I_{\mathrm{DS}})\Delta T\right) \ . \tag{9}$$

As a comparison of different CoolMOS devices with diverse chip areas shows, the energy stored in C_{oss} is also directly proportional to A_{Chip} and under consideration of (9) the total switching losses can be calculated by

$$P_{\mathrm{sw}} = \frac{1}{T_{\mathrm{N}}} \int_0^{T_{\mathrm{N}}} f_{\mathrm{s}} \ E_{\mathrm{on}}\left(\Delta T, I_{\mathrm{DS}}(t)\right) dt + f_{\mathrm{s}} E^*_{400\mathrm{V}} A_{\mathrm{Chip}} \tag{10}$$

where T_{N} is the period of the mains current. Additionally, the required gate drive power P_{g} can be expressed as a function

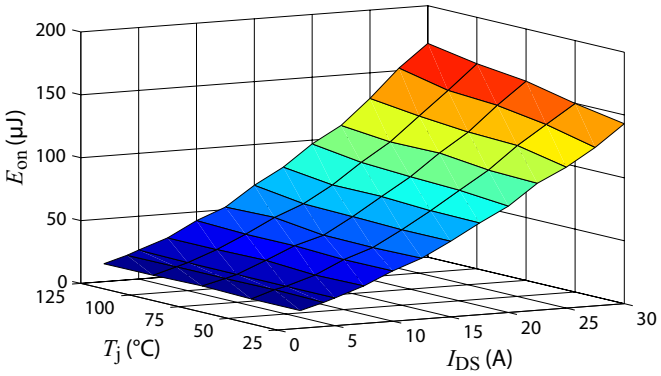


Fig. 9: Measured turn-on energies of the CoolMOS-CP semiconductor family as a function of drain-source current I_{DS} and temperature T_{j} at $V_{\mathrm{DS}} = 400\,\mathrm{V}$.

of the chip area

$$P_{\mathrm{g}} = Q_{\mathrm{g}}^{*} A_{\mathrm{Chip}} V_{\mathrm{g}} f_{\mathrm{s}} \ . \tag{11}$$

In order to calculate the conduction losses of the MOSFET its on-state resistance has to be determined. The R_{DSon} is a function of the junction temperature T_{j} and the drain-source current and a curve fit on data sheet values results in

$$R_{\mathrm{DSon}}(\Delta T, I_{\mathrm{DS}}) = \frac{R_{\mathrm{DSon,25}}^{*}}{A_{\mathrm{Chip}}} \left(1 + \alpha_1 \Delta T + \alpha_2 \Delta T^2\right) \left(1 + \beta_1 I_{\mathrm{DS}} + \beta_2 I_{\mathrm{DS}}^2\right) \tag{12}$$

where $R_{\mathrm{DSon,25}}^{*}$ is the chip area dependent on-state resistance at $T_{\mathrm{j}} = 25\,^{\circ}\mathrm{C}$ and $I_{\mathrm{DS}} = 0$. Hence, the conduction losses

$$P_{\mathrm{con}} = \frac{1}{T_{\mathrm{p}}} \int_0^{T_{\mathrm{p}}} R_{\mathrm{DS,on}}(\Delta T, I_{\mathrm{DS}}) I_{\mathrm{DS}}^2(t)\ dt \tag{13}$$

have to be calculated by integration over one mains period because (12) is nonlinear. The total MOSFET losses can be calculated by use of (8).

Both (9) and (12) require the junction temperature

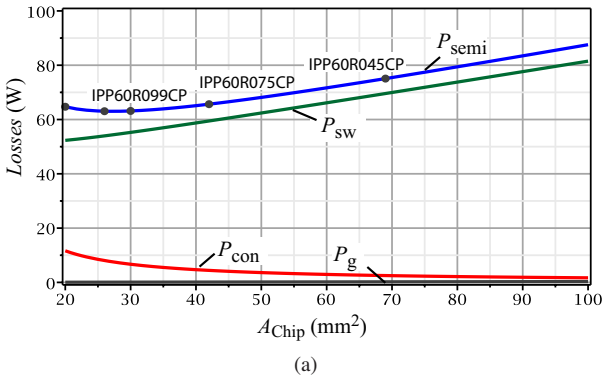
$$T_{\mathrm{j}} = T_{\mathrm{s}} + R_{th,js}^{*} A_{\mathrm{Chip}} P_{\mathrm{semi}} \tag{14}$$

which is a function of the chip area dependent thermal interface (expressed by $R_{th,js}^{*}$) to the heat sink (heat sink temperature T_{s}) and of the total semiconductor losses. Hence, (10) and (13) have to be solved iteratively by application of (8) and (14). In [22] a chip area dependent thermal resistance $R_{\mathrm{th,js}}^{*}$ is proposed where the whole chip is realized on a single power module using an Al_2O_3 DCB ceramic substrate. However, for the application at hand discrete semiconductors using the TO220 or TO247 housings shall be applied. Several devices have therefore been examined and if a thermal isolation sheet is also considered a chip area dependent thermal resistance of

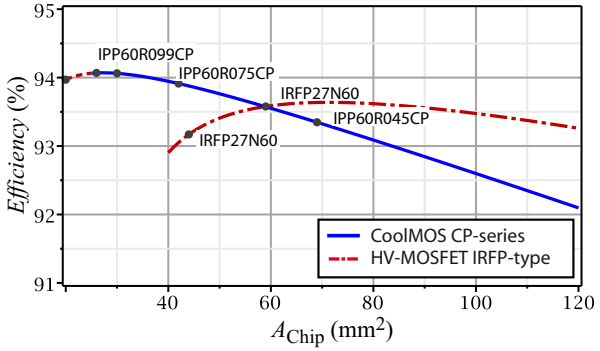
$$R_{\mathrm{th,js}}^{*} = 8.5\,\mathrm{K/W} \left(\frac{A_{\mathrm{Chip}}}{\mathrm{mm}^2}\right)^{-0.64} \tag{15}$$

can be approximated for semiconductors in the TO220 and TO247 case.

By use of (8)-(15) the chip area dependent power losses of SJ devices (CoolMOS-CP series) applied in the intended three-phase rectifier system (cf., **Fig. 1**) with a switching frequency of $f_{\mathrm{s}} = 1\,\mathrm{MHz}$ and an output power of $P_{\mathrm{o}} = 10\,\mathrm{kW}$



(a)



(b)

Fig. 10: (a) Dependency of the power MOSFET losses P_{semi} consisting of conduction losses P_{con} and switching losses P_{sw} on the chip area A_{Chip} at a switching frequency of $f_{\mathrm{s}} = 1\,\mathrm{MHz}$ and $P_{\mathrm{o}} = 10\,\mathrm{kW}$. (b) Calculated total system efficiency as a function of the chip area.

are calculated and the results are depicted in **Fig. 10(a)**. It is obvious that for a switching frequency of 1 MHz the total semiconductor losses are dominated by switching losses. The total semiconductor losses show a minimum at $A_{\mathrm{Chip}} \approx 27\,\mathrm{mm}^2$ which would be the optimal chip area for the intended rectifier system. A a result of **Fig. 10(a)** the SJ device IPP60R099CP is used in the realized prototype.

As a next step total system losses must be calculated. Only the results of this calculation are included in this work for the sake of brevity. Details about loss calculation of the intended rectifier system can be found in [23]. The resulting system efficiency for a system employing SJ devices of the CoolMOS-CP series is given in **Fig. 10(b)** together with the efficiency of a system using HV-MOSFETs. Due to the very high switching frequency and, in consequence, the high switching losses only an efficiency of $94\,\%$ can be achieved if SJ devices are applied. The junction temperature of the SJ devices for a chip area below $25\,\mathrm{mm}^2$ (marked with a red dotted line) would rise above the limit of $150\,^{\circ}\mathrm{C}$ and a practical realization would therefore be inhibited because of the limited performance of the thermal interface. Due to the significant higher chip area dependent R_{DSon}^{*} of HV-MOSFET devices a larger chip area is required for realization and a maximum efficiency of $93.6\,\%$ is achievable. The chip area dependent energy $E_{400\mathrm{V}}^{*}$ stored in C_{oss} of the HV-MOSFET is smaller than $E_{400\mathrm{V}}^{*}$ of the SJ devices (cf., TABLE I) and hence a system employing HV-MOSFETs would show a higher efficiency compared to a system using SJ devices for $A_{\mathrm{Chip}} > 60\,\mathrm{mm}^2$. However, as a realization using SJ-devices would show a higher efficiency at a smaller chip size a realization using SJ devices is preferred for a

switching frequency of 1 MHz.

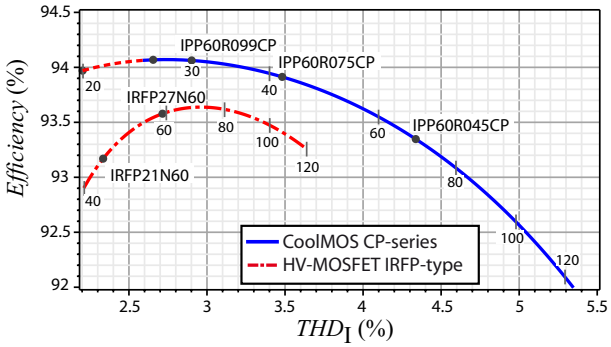
VI. η-THD Pareto Front

In section III the influence of the turn-off delay of the MOSFET on the input current quality has been evaluated (cf., **Fig. 7**). The result of this analysis is a curve showing the THD of the input currents as a function of the chip area. On the other hand the result of section V is an efficiency curve as a function of the chip area (cf., **Fig. 10**). The two results can be combined and the calculated system efficiency (η) can be plotted as a function of input current distortion ($\mathrm{THD_I}$) where A_{Chip} acts as a parameter. This results in a η-THD Pareto Front where the trade-off between efficiency and input current quality is clearly illustrated. The input current quality as well as the system efficiency are strongly dependent on the switching frequency. Thereby, for every selected switching frequency required to achieve an intended power density, an own η-THD Pareto Front can be drawn. **Fig. 11(a)** shows the resulting η-THD Pareto Front for a switching frequency of 1 MHz and an output power of 10 kW for the SJ devices (CoolMOS-CP) and HV-MOSFETs if the proposed pre-control signal is not used. The corresponding chip areas are marked in the two curves. A maximal efficiency of 94 % can be achieved for CoolMOS-CP devices and a $\mathrm{THD_I}$ of 3 % can be read at this point. A better THD is inhibited by the thermal interface of the devices. On the contrary a classical HV-MOSFET shows a substantial better THD at same chip size but is not able to show its strength because of higher losses.

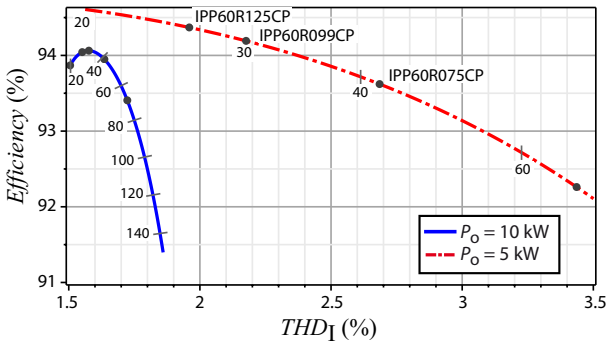
If the proposed pre-control signal is implemented the input current distortion can be mostly compensated which results in the Pareto Front given in **Fig. 11(a)**. A deviation of 10 % is assumed for the pre-control signal for simulation of the resulting THD . The THD stays below 2 % for a system operating at 10 kW. However, if the system is operated at partial load (e.g. 5 kW) a considerably increased THD can be read.

VII. Experimental Results

The calculation results are verified using a 10 kW rectifier system operating with a switching frequency of 1 MHz (cf., **Fig. 12**). The water cooled prototype shows the dimensions 195 mmx110 mmx33 mm which yields a remarkable power density of 14.1 kW/litre. A modern high-speed FPGA is used for implementation of the current controller [17]. The rectifier system employs the SJ device IPP60R099CP, which according to **Fig. 11** shows an optimal chip area. The measured input current taken from the prototype system operated with the proposed pre-control signal is given in **Fig. 13** where the measured efficiency is also depicted. Compared to the calculation results (**Fig. 10(b)**) the realized system shows a slightly reduced efficiency. The reason has been found in (additional) parasitic capacitances of the PCB-layout of the rectifier system which lead to higher switching losses. However, in order to be able to benchmark different semiconductor families the results of the switching loss measurements, where all measurements are taken on the same test setup, are used in section V. The rectifier prototype is operated using the feed-forward compensation signal as in practice an operation without this compensation signal would yield heavily distorted input currents at the zero crossings.



(a)



(b)

Fig. 11: Graphical representation of the trade-off between input current quality (expressed by the $\mathrm{THD_I}$ value) and efficiency for a 10 kW rectifier system with a switching frequency of 1 MHz. (a) System operated without pre-control signal and (b) with pre-control signal at 10 kW and 5 kW. Corresponding chip areas A_{Chip} are marked in the curves.

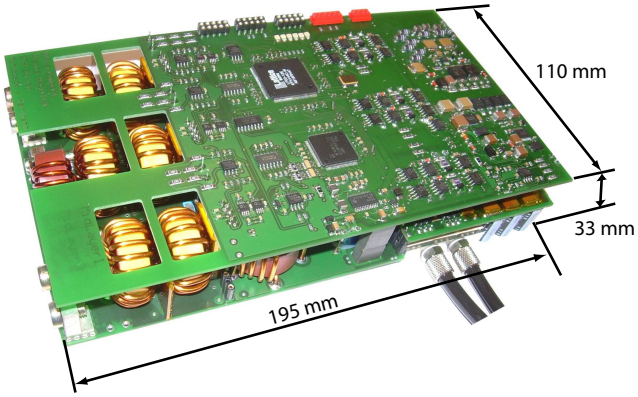


Fig. 12: 10 kW three-phase/level rectifier system with a switching frequency of 1 MHz (Dimensions: 195 mm x 110 mm x 33 mm, power density: 14.1 kW/litre).

In order to verify the effectiveness of the proposed pre-control signal a 10 kW rectifier prototype with a switching frequency of 250 kHz is used instead of the rectifier system with $f_{\mathrm{s}} = 1\,\mathrm{MHz}$. The measurement results of the rectifier system operating at $f_{\mathrm{N}} = 400\,\mathrm{Hz}$ and $P_{\mathrm{o}} = 4.7\,\mathrm{kW}$ with and without the pre-control signal are given in **Fig. 14**. Whereas the system without the pre-control shows significant input current distortions at the zero-crossings of the measured phase and at the zero-crossings of the two other phases (every 60 °) input current quality is improved considerably if the pre-control is enabled. A $\mathrm{THD_I}$ of only 3.4% is measured without the feed-forward signal and a $\mathrm{THD_I}$ of 1% is achieved if the proposed pre-control signal is used. The measurement clearly illustrates that the turn-off delay yields

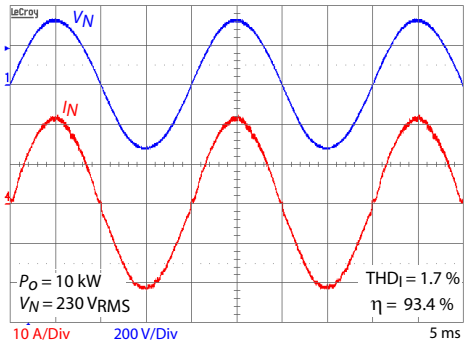


Fig. 13: Measured input current waveform taken from the 10 kW rectifier system operated with the proposed pre-control signal at $f_s = 1\,\text{MHz}$ ($f_N = 50\,\text{Hz}$, $V_o = 800\,\text{V}$); CH1 (blue): V_{N1}, 200 V/Div, Ch2 (red): I_{N1}, 5 A/Div, time base: 1 ms.

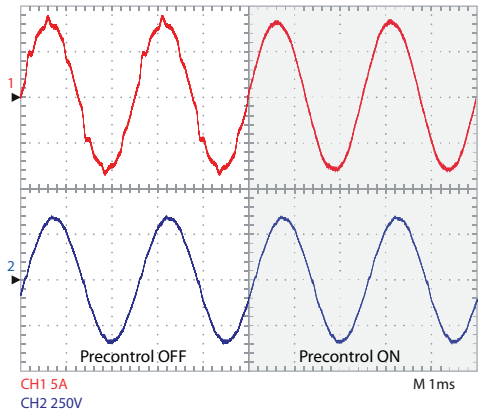


Fig. 14: Measurement of the input current with and without feed-forward compensation of the turn-off delay. Measurement is taken from a system with $f_s = 250\,\text{kHz}$ (V_N=230 V, $f_N = 400\,\text{Hz}$, $V_o = 800\,\text{V}$, $P_o = 4.7\,\text{kW}$); Ch1 (red): I_{N1}, 5 A/Div, CH2 (blue): V_{N1}, 250 V/Div, time base: 1 ms.

significant input current distortions even at a "moderate" switching frequency of 250 kHz.

VIII. Conclusion

Because of the parasitic output capacitance C_{oss} of the MOSFET the duty cycles generated from the controller are enlarged in relation to the input current. This yields substantial input current distortions. This effect is even more distinctive if SJ devices are used instead of classical HV-MOSFETs. However, SJ devices offer a considerably reduced on-state resistance which leads to reduced conduction losses. Due to the smaller chip area required to realize a specific R_{DSon}, SJ devices also show smaller switching losses. This relationship between efficiency and input current quality has been illustrated in a Pareto curve in the η-THD space. Indeed, SJ devices show higher input current distortions but a realization using HV-MOSFETs results in a considerably reduced efficiency compared to a realization using SJ devices. It has been shown that the input current distortions can be reduced significantly if a proper pre-control signal is applied. Hence, SJ devices are particularly suited for this type of rectifier if the proposed pre-control signal is applied.

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