Exploring the Pareto Front of Multi-Objective Single-Phase PFC Rectifier Design Optimization - 99.2% Efficiency vs. 7kW/dm^3 Power Density

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***Abstract*—Up to now, in the development of power electronics systems, the reduction of the initial costs or the increase of the power density have been of primary concern. However, with increasing energy costs also the power conversion efficiency is gaining higher and higher importance. Accordingly, while maintaining high power density, an efficiency as high as possible must be obtained.**

In this paper the maximum attainable efficiency and the dependency of the efficiency limit on technological parameters is determined for single-phase PFC boost rectifiers. In a first step basic PFC boost rectifier topologies are briefly compared with regard to high efficiency and a dual-boost PFC rectifier with integral common-mode filtering is selected as basis for the investigations. Next, simple approximations of the technological limits of the system performance are calculated in the efficiency-power density plane. With this, the Feasible Performance Space and the reduction in power density which has to be accepted for increasing the efficiency are clarified, and the trade-off limit curve (Pareto Front) of a multi-objective, i.e. efficiency *and* power density design optimization is determined. Furthermore, a comprehensive numerical efficiency optimization is carried out which identifies an efficiency limit of 99.2% for a 3.2kW system. The theoretical considerations are verified by experimental results from a laboratory prototype of the ultra-high efficiency system achieving 99.1% efficiency at a power density of 1.1kW/dm^3, as well as those from an ultra-compact dual-boost PFC rectifier (95.8%, 5.5kW/dm^3) and a very low switching frequency (3kHz) conventional PFC boost rectifier (96.7%, 2kW/dm^3). Finally, the sensitivity of the efficiency optimum with regard to various technological parameters is analyzed and an outlook on the further course of the research is given.

I. Introduction

At present 40% of the total worldwide energy use is based on electricity generation, whereby the mean conversion efficiency of fossil energy into electrical energy is only around 35% [1]. By 2030 an increase in electricity use by 50% is forecast, whereas the generation efficiency will only increase to 38%. A large fraction of this energy will subsequently be converted and conditioned by power electronics systems. Thus, in view of the low generation efficiency, the energy efficiency of the power electronics converters will gain eminent importance in the conservation of resources.

Up to now, in the development of power electronics systems, reduction of the initial costs or increase of power density have been of primary concern [2]–[5]. Efficiency increase was only indirectly required, since a lower system volume provides a smaller surface for power loss dissipation. However, with the primary goal of high efficiency and the continued requirement of high power density, now a multi-objective requirement exists for the further development of power electronics systems. While maintaining high power density ρ, as high an efficiency η as possible must be obtained and/or the performance of the system must be analyzed in a multi-dimensional performance space (cf. Fig. 1), i.e. in the efficiency-power density plane (η-ρ-plane).

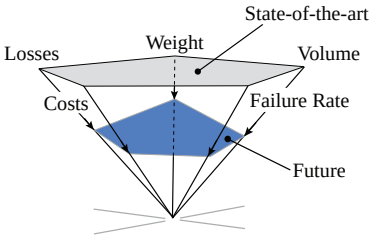

Fig. 1: Intended future improvement of main performance indices of power electronics converters. For assessing the converter performance relative quantities, i.e. output power density ρ (kW/dm^3), efficiency η, output power per unit weight γ (kW/kg), and the cost related output power σ (kW/€) are used.

The technological limits of power electronic systems with regard to the performance index power density were clarified in [3] without special concern with the efficiency. Hence in a next step, the following must be determined:

- the maximum attainable efficiency of power electronic systems
- the dependence of the efficiency limit on technological parameters and
- the reduction in power density to be accepted with increased efficiency [6], i.e. the trade-off limit curve of optimal designs (Pareto Front) in the η-ρ-plane.

The present work is concerned with the answers to these questions, taking the example of single-phase PFC boost rectifiers. In Section II the design process in general and the subsequent evaluation of the power electronics systems are first illustrated and shown in abstract form as mathematical mapping of a Design Space into a System Performance Space. Then the single-objective and multi-objective optimization of

this mapping are discussed.

In Section III topologies of PFC boost rectifier systems are briefly compared with regard to high efficiency, and a dual-boost PFC rectifier with integral common-mode (CM) filtering is selected as the basis for further investigations. In Section IV simple approximations of the technological limits of the system performance are calculated in the η-ρ-plane, i.e. the Feasible Performance Space is determined. Next a comprehensive optimization is carried out with regard to efficiency (Section V).

Then in Section VI experimental results from a laboratory sample of the ultra-high efficiency system are shown as well as those from an ultra-compact dual-boost PFC rectifier and a low-frequency conventional PFC boost rectifier. In Section VII the prediction of the Pareto Front of a simultaneous efficiency and power density optimization of the system is discussed. Finally, in Section VIII the sensitivity of the efficiency optimum with regard to various technological parameters is analyzed and in Section IX an outlook on the further course of the research is given.

II. Multi-Objective Optimization of Power Electronic Converter Performance

The essential steps in the design process and the subsequent evaluation of a power electronic system based upon performance indices are shown in Fig. 2 in simplified graphic form. Fundamentally, a circuit topology and an associated modulation and control process must be selected and the component values and control parameters, etc., determined in such a way that system specifications and regulations are fulfilled. The system must hence, e.g., deliver in a defined range of input voltage the required output power, the switching frequency ripple of the output voltage must be limited to an upper limit, the correction of the output voltage after a load step must take place in a defined maximum time and the regulations regarding EMI emission must be complied with. Furthermore, typical minimum requirements regarding system performance, e.g. regarding the costs or the efficiency must be fulfilled. Selection of the components must be done in such a way that material limits, such as the maximum junction temperature of the power semiconductors or a maximum flux density swing of magnetic material or the maximum current loading of a filter capacitor are complied with.

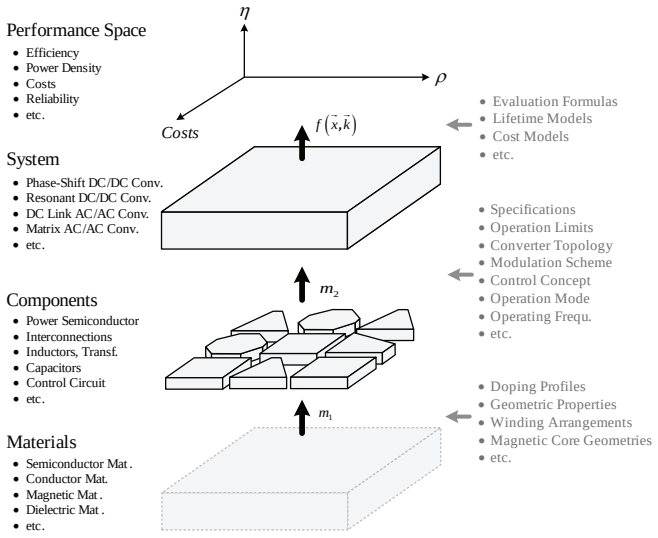

Fig. 2: Abstracted graphical representation of the design and assembling of a power electronics converter as transition m_1 from materials to components and subsequently from components to the required system (transition m_2). The assessment of the design quality is by performance indices and/or in a Performance Space (mapping $f(\vec{x},\vec{k})$, (4)).The transitions m_1 and m_2 are defined by parameter values and/or values of design variables x_n which are selected in the course of the design considering the required system specifications and minimum performance requirements, i.e. equality and inequality constraints. Furthermore, design constants k_l and limits of the employed materials are taking influence on m_1 and m_2. Overall, the design process and the design evaluation can be described as a mapping of a multi-dimensional Design Space with coordinate axis x_n and k_l into a multi-dimensional Performance Space which is defined by the performance indices p_i (Fig. 5).

The components are realized starting from a material base, i.e. semiconducting and conducting materials, magnetic materials, dielectrics and insulating materials, etc., whereby a multitude of design variables is to be specified. E.g., with regard to magnetic components, a core material must be selected and the core geometry, winding arrangement, winding cross-section and also the realization of the winding with stranded wire, round wire or a copper foil, etc. specified. Other components, e.g. power semiconductors or semiconductor modules can no longer be influenced in the design, but are available from semiconductor manufacturers in prefabricated form for various application areas (e.g. components with low on-state voltage but higher switching losses). The design is thus limited to the selection of a suitable component.

Overall this means a large number of design variables and design constants, which must be specified in the course of dimensioning in such a way that the system specifications are fulfilled and a target performance attained. Hence from a mathematical viewpoint, in a multi-dimensional Design Space,

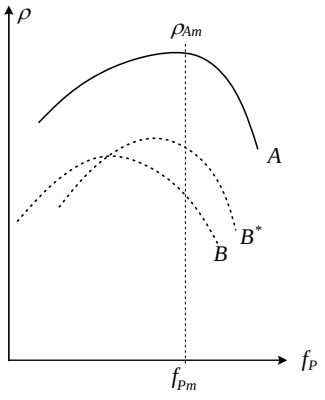

Fig. 3: Optimization of the power density ρ of a converter (single-objective optimization) by optimal selection of the switching frequency f_P and further design variables x_n (not shown). Based on a mathematical description of the mapping of the Design Space into the Performance Space, the performance of different converter topologies (A or B) or the influence of changing the operation mode (B or B^*) can be shown in direct dependency of f_P or x_n and an optimum parameter value f_{Pm} can be selected.

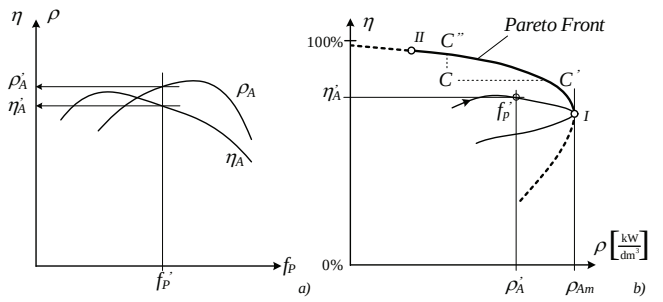

Fig. 4: Representation of the power density optimization (single-objective optimization, cf. a)) of a system concept A according to Fig. 3 in the power density / efficiency plane (η-ρ-plane, cf. b)). In case the efficiency is included into the optimization, a whole set of solutions results, according to the different weightings w_i of the objectives (cf. (7)). The best possible, i.e. Pareto-optimal solutions of this multi-objective optimization are defining the Pareto Front. For solutions along the Pareto Front the improvement of the efficiency in any case results in a reduction of the realizable power density ρ. A design C therefore is not Pareto-optimal, as solutions C' and C'' exist which show a high power density at the same efficiency (cf. C') or a higher efficiency at same power density (cf. C''). The end points *I* and *II* of the Pareto Front are defined by the results of single-objective optimizations concerning power density or efficiency.

in which each design variable

$$\vec{x} = (x_1, x_2, \dots x_n) \tag{1}$$

or design constant

$$\vec{k} = (k_1, k_2, \dots k_l) \tag{2}$$

is assigned a coordinate axis, a design vector must be specified such that the side conditions defined by system specifications or a minimum performance requirement

$$\vec{r} = (r_1, r_2, \dots r_m) \tag{3}$$

are fulfilled [7], [8]. Here also the circuit topology, modulation and control processes, etc. can be seen as design variables.

Typically there are considerably more design variables than side conditions, so that a large number of different designs is possible. Within the scope of an optimization, this multitude of solutions can be limited to one optimal design, which e.g. maximizes a system performance index defined as quality criterion

$$f\left(\vec{x}, \vec{k}\right) \rightarrow \text{Max}, \tag{4}$$

whereby one has to consider as side conditions functions

$$g_i\left(\vec{x}, \vec{k}, \vec{r}\right) = 0 \qquad i = 1, 2, \dots p \tag{5}$$

$$h_j\left(\vec{x}, \vec{k}, \vec{r}\right) \geq 0 \qquad j = 1, 2, \dots q \tag{6}$$

which describe the inner converter function and the system requirements or specifications, and minimum values of other Performance Indices [7]. If for example the efficiency is chosen as the quality criterion, the calculation of $f\left(\vec{x}, \vec{k}\right)$ in the course of the optimization the sum of the losses $\sum P_{Vi}$ of a design must be determined and therefrom the efficiency calculated according to $\eta = 1 - \sum P_{Vi}/P_O$ (where P_O is the output power).

Referred to Fig.2 the transitions m_1 and m_2 are defined by specifying the design variables. By optimizing a performance index and subsequent calculation of all other performance indices a point in the multi-dimensional Performance Space is then assigned to the system thus formed. Hence overall the Design Space is mapped into the Performance Space, or a performance vector is assigned to a design vector.

In order to simplify the optimization (4), in the field of power electronics the switching frequency f_P, which influences a large number of internal characteristics of a design (e.g. the cross-section of the magnetic core of a transformer and its core and winding losses, as well as the switching losses of the power semiconductors) and is in non-linear dependence on these characteristics, is often selected as an explicit parameter. As shown in Fig. 3 with the example of a power density optimization, the optimization can then be represented clearly or the sensitivity of the optimum with regard to f_P be directly stated. Furthermore, the topology is typically not an element of the Design Space, but the optimization is analyzed on the basis of different circuit structures (A or B), or for a defined basic circuit structure and various operating modes (B and B^*, e.g. hard or soft switching, or operation in continuous or discontinuous conduction mode).

As mentioned in the introduction, however, in future several quality criteria will have to be fulfilled simultaneously for a design (multi-objective design), so that

$$\sum w_i f_i\left(\vec{x}, \vec{k}\right) \rightarrow \text{Max}; \qquad \sum w_i = 1 \tag{7}$$

results as a mathematical requirement. The weightings of the individual criteria determine the compromise between the individual optimization goals, e.g. between power density and efficiency. Overall, then, there results not a single best solution but a set of solutions (cf. Fig. 4), i.e. a Pareto Front in the Performance Space [9], [10] (connection I-II in Fig. 4). For points of the Pareto Front an increase in the efficiency is only possible with a decrease in the power density (increase of weighting w_η and decrease of w_ρ), i.e. the design is for the chosen parameters w_η and w_ρ the best possible and no design exists that would offer the same power density at higher efficiency. A design with performance C is in this sense not Pareto-optimal, since it is dominated both by a design C' or by a design C'' (cf. Fig. 4).

It is now interesting to analyze the result of a single-objective power density optimization in the η-ρ-Performance Space. Corresponding to a weighting $w_\eta = 1$, $w_\rho = 0$, with optimal switching frequency f_{Pm} (cf. Fig. 3) the point I of the Pareto Front is reached; for other values of the switching frequency a non-Pareto-optimal performance exists.

To summarize, then, to determine the best possible compromise between the efficiency and the power density, the design of power electronics systems must be represented as a mathematical mapping $f\left(\vec{x}, \vec{k}\right)$ of the Design Space into the Performance Space with corresponding side conditions g_i and h_j (cf. Fig. 5) and the Pareto Front for various circuit topologies A, B or modulation processes or operating modes B, B^* etc. determined. In this way the best possible concept can be chosen for a required target performance (η, ρ), or via

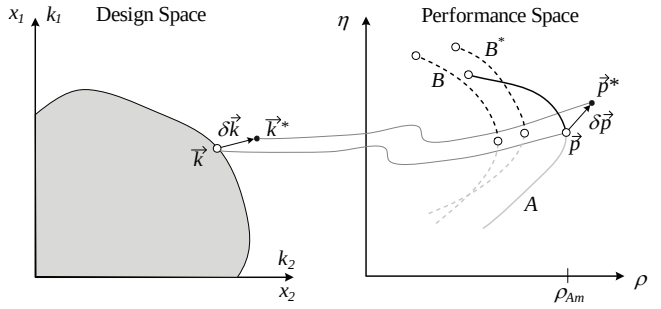

Fig. 5: Abstraction of the multi-objective design of a power electronics converter as mapping of a multi-dimensional Design Space (or Parameter Space, shown for two dimensions) into a multi-dimensional Performance Space (shown for two dimensions). Performing a multi-objective optimization identifies the Pareto Front which allows an immediate and comprehensive comparison of converter concepts and/or the selection of the concept best fitting given performance requirements. Furthermore, based on the mathematical description of the mapping of the Design Space into the Performance Space the sensitivity $d\vec{p}/d\vec{k}$ of the system performance concerning an improvement $d\vec{k}$ of the technology basis and/or an increase of the limit values of design constants could be directly analyzed. This facilitates a systematic roadmapping of technologies.

comparison of the performance of industrial systems with the theoretically best possible concept, a technology evaluation carried out. Furthermore, the influence of further technological developments $\delta\vec{k}$ in the material or technology base may be simply estimated, since the mathematical analysis/optimization shows directly the resulting gain $\delta\vec{p}$ in system performance. Thus, the optimization can also be employed in the reverse direction to determine the most effective change in a technology, i.e. serve as the basis for a technology roadmapping process.

In the following, the η-ρ-Pareto Front for single-phase PFC boost rectifiers is analyzed. There, in order to reduce the computing effort, the Pareto Front is not calculated directly, but an efficiency maximization is performed and then the η-ρ-Pareto Front approximated analytically. The dependencies of the Pareto Front on technological parameters then become directly clear.

III. Selection of a High-Efficiency Single-Phase PFC Topology

The basis of efficiency optimization is the choice of a suitable circuit topology that enables minimal semiconductor losses to be attained with low semiconductor expense and hence low realization costs. The basic concepts of single-phase PFC boost rectifiers are shown in Fig. 6. As also described in [11], with regard to low conduction losses, preferably a bridgeless PFC boost rectifier (or dual-boost PFC rectifier, cf. Fig. 6b)) should be selected, since then with keeping S_2 continuously in the on-state for $u_N > 0$ (and/or S_1 for $u_N < 0$) in the turn-on interval, only two MOSFET on-resistances and in the turn-off and/or boost interval only one diode and one power MOSFET lie in the current path. SiC Schottky diodes are preferably used here as freewheeling diodes with regard to low switching losses. The use of relatively complex soft-switching topologies [12], [13] can thus be avoided and is hence not further discussed here. If for a conventional boost PFC rectifier (Fig. 6a)) equally low conduction losses were

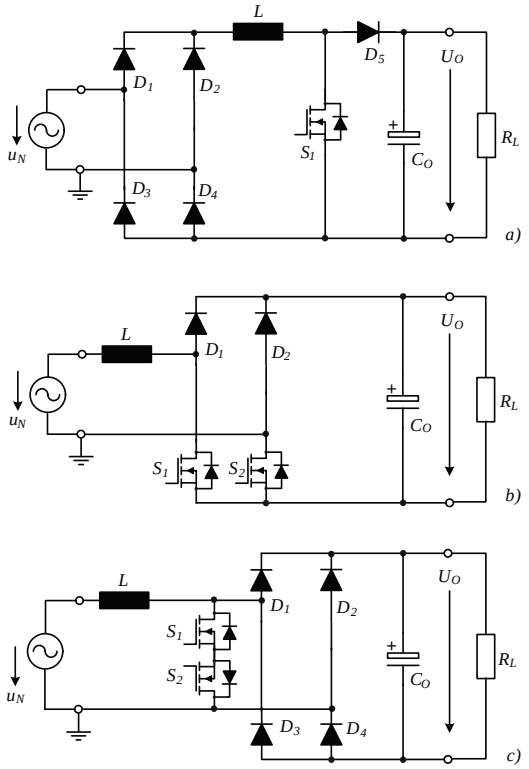

Fig. 6: Basic topologies of single-phase power factor corrected (PFC) boost-type rectifier systems; a) conventional PFC boost rectifier, b) bridgeless or dual-boost PFC rectifier, c) dual-boost AC-switch PFC rectifier.

to be attained in the turn-on and boost state, four power MOSFETs, i.e. a synchronous rectification would have to be used instead of the diodes $D_1 - D_4$ of the input rectifier bridge, i.e. in total a MOSFET chip area of 9 A_{Chip} (A_{Chip} is the chip area of a single boost transistor of Fig. 6b)), as well as one SiC freewheeling diode. As a further alternative for the dual-boost AC-switch PFC rectifier (Fig. 6c), [14]), the diodes of one bridge leg, e.g. D_2 and D_4 could be replaced by power MOSFETs and D_1 and D_3 realized as SiC diodes [11]. In summary, with regard to the chip area or semiconductor requirements (Fig. 7), the bridgeless PFC boost rectifier is clearly preferable when high efficiency is demanded.

However, a switching frequency common-mode (CM) voltage occurs at the output for the system depicted in Fig. 6b), in contrast to the circuits shown in Figs. 6a) and c), where one rail of the output voltage bus is always connected to a mains voltage terminal via a diode or in the case of the synchronous rectification described above, via a power MOSFET. If the boost inductance is divided to the two AC input lines with the aim of lowering the conducted interference emission [15], the common-mode voltage u_{CMn} of the negative output voltage bus n shows the time behavior depicted in Fig. 8. From simple consideration,

$$u_{CMn} = \frac{1}{2} u_N \qquad \text{for } S = \text{on} \tag{8}$$

$$u_{CMn} = \frac{1}{2}(u_N - U_O) \qquad \text{for } S = \text{off} \tag{9}$$

applies independent of the polarity of the mains voltage.

Considering the duty cycle of the switching power transistor S

$$d = 1 - \frac{u_N}{U_O}, \tag{10}$$

there then follows the local mean value $\overline{u}_{CMn}$ of u_{CMn} referred to a pulse period

$$u_N \geq 0 \qquad \overline{u}_{CMn} = 0 \tag{11}$$

$$u_N < 0 \qquad \overline{u}_{CMn} = u_N. \tag{12}$$

According to [16], a switching frequency variation of the output CM voltage can be suppressed by two return and/or clamping diodes (Fig. 9a)); there then exists a coupling of mains and output comparable to the circuit in Fig. 6a) or Fig. 6c). As described in [17], the boost inductance should be preferably implemented as shown in Fig. 9a) to minimize the design volume. L_{DM1} and L_{DM2} are realized here with magnetic cores of the same type and the same number of turns. Because of the inverse coupling of the windings and the series connection of L_{DM1} and L_{DM2}, the voltages coupled to the non-current carrying side then cancel each other out, i.e. no short circuit of the sum voltage occurs over S_1 and D_3 or S_2 and D_4. Then, contrary to a magnetically separated realization of the inductors, always the series connection of L_{DM1} and L_{DM2} is effective, which enables approximately a halving of the core volume [17]. However, in order to obtain the same low conductive losses as for the circuit in Fig. 6b), the diodes D_3 and D_4 would have to be replaced again by synchronous rectifiers, so that overall a chip area requirement of $4A_{Chip}$ would result (Fig. 7).

It is therefore obvious to consider alternative possibilities of suppressing the output CM voltage of the circuit depicted in Fig. 6b). Here it is of advantage to employ a CM filter concept known from three-phase PWM rectifier systems [18], [19], for which the output in principle also exhibits a switching-frequency CM voltage. The resulting circuit of the dual-boost PFC rectifier with integral CM filter is shown in Fig. 9b). Instead of the clamping diodes, CM filter capacitors C_{CM1} and C_{CM2} are employed here for high-frequency connection of the output to the mains. The switching-frequency part of the CM voltage u_{CMn} is then absorbed by a CM inductance L_{CM}. The dimensioning of L_{CM} can simply be considered via a CM equivalent circuit diagram of the system [11] and the associated time behavior of switching-frequency common-mode voltage $^1/_2 u_{S\sim}$ with $u_{S\sim} = u_S - \overline{u}_S$) (Fig. 10); here u_S is the voltage occurring across the switching power transistor, e.g. across S_1 for $u_N > 0$.

For the interference sources effective between n and earth

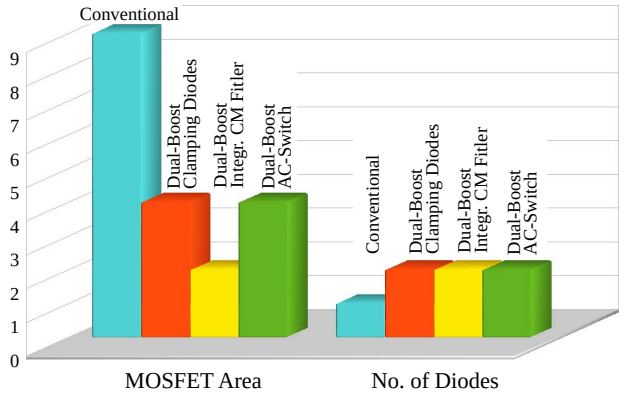

Fig. 7: Total MOSFET chip area required for equal conduction losses of the converter topologies shown in Fig. 6a) and c) and Fig. 9a) and b). Furthermore shown: Quantity of required fast recovery (SiC) freewheeling diodes. For the topology Figs. 6a) the diodes D_1-D_4, and for Figs. 6c) diodes D_2 and D_4 are replaced by power MOSFETs. The same is true for D_3 and D_4 in Fig. 9a).

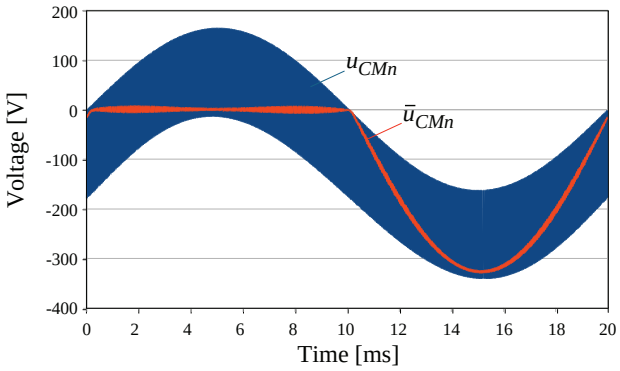

Fig. 8: Common-mode (CM) voltage u_{CMn} of the dual-boost PFC (measured from the negative output voltage rail n towards earth) for a symmetric partitioning of the boost inductor to the AC lines; $\overline{u}_{CMn}$ denotes the local average value of u_{CMn} related to a pulse period $T_P = 1/f_P$.

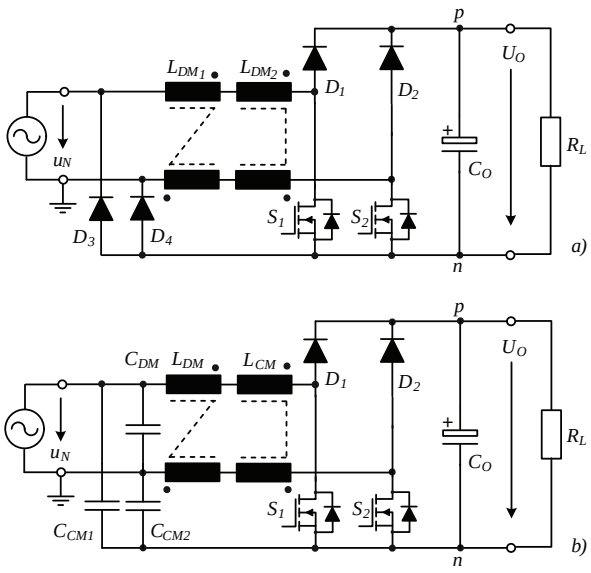

Fig. 9: Circuit measures for avoiding a high-frequency CM voltage of the output of a dual-boost PFC rectifier; a) clamping diodes; b) capacitive coupling of the output voltage to the mains and/or earth. The inverse magnetic coupling of the partial windings of L_{DM1} and L_{DM2} in a) allows to simultaneously utilize both inductors for each input current direction; the total voltage appearing across the partial windings not participating in the current conduction is equal to zero, accordingly diode D_3 or D_4 is not forced into conduction. As always only one partial winding of L_{DM1} and L_{DM2} is conducting current, L_{DM1} in contrast to L_{CM} of b) does not act as a CM inductor.

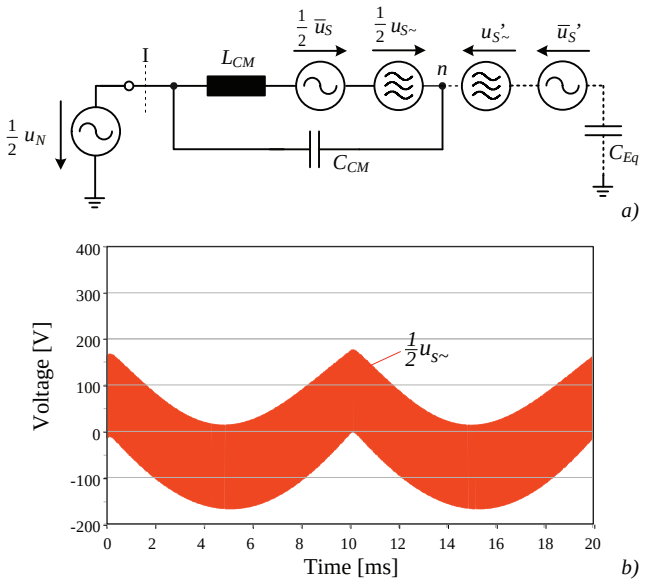

Fig. 10: CM-equivalent circuit of the converter shown in Fig. 9b) ($C_{CM} = C_{CM1} + C_{CM2}$) and time behavior of the switching frequency CM voltage $1/2\, u_{S\sim}$ of the negative output voltage rail n. $1/2\, u_{S\sim}$ is low-pass filtered by L_{CM} and C_{CM} providing typ. about 60dB attenuation. Assuming an ideal magnetic coupling of the partial windings the boost inductor L_{DM} is not active for CM filtering Due to the earth connection of one mains terminal the AC side CM voltage is defined by half the mains voltage. After capacitive coupling of n to the mains and/or earth via C_{CM} only the drain voltage u_S (related to n) of the switching power MOSFET is remaining as high frequency noise source which can be translated into an equivalent noise source u_S'=$\overline{u}_S'$ + $u_{S\sim}'$ and an equivalent coupling capacitance C_{Eq} considering the parasitic earth capacitances C_p + C_n of the positive and negative output voltage rails p and n.

follows

$$\overline{u}_S' = \frac{C_S}{C_{Eq}}\overline{u}_S \qquad u_{S\sim}' = \frac{C_S}{C_{Eq}}u_{S\sim} \tag{13}$$

with

$$C_{Eq} = 2C_S + C_p + C_n$$

(C_S is the parasitic capacitance between the drain of a power MOSFET and earth, C_p and C_n are the earth capacitances of the positive and negative output voltage rail, p and n).

The common-mode inductance L_{CM} and the equivalent capacitance $C_{CM} = C_{CM1} + C_{CM2}$ ($C_{CM1} = C_{CM2}$) act as low-pass filters for the CM voltage $1/2 u_S = 1/2(\overline{u}_S + u_{S\sim})$, whereby the low-frequency part $1/2\overline{u}_S$, with corresponding dimensioning, is absorbed to a large extent by C_{CM} and hence causes only a relatively low flux density swing of L_{CM}. The magnetic dimensioning of L_{CM} thus has only to be performed for a switching-frequency voltage of maximum $\pm U_O/4$ with 50% duty cycle (Fig. 10). As a concrete dimensioning and experimental verification shows (Chapter V), there results a typical design volume of L_{CM} comparable with the boost inductance L_{DM}.

However, through C_{CM}, as also through the diodes D_3 or D_4 (Fig. 9a)), the CM interference emission through the parasitic drain capacitance C_S of the switching power transistor switching, represented in Fig. 10a) by the equivalent interference voltage $u_S' = \overline{u}_S' + u_{S\sim}'$ and C_{Eq}, is fed directly to the mains. Accordingly, in order to comply with the radio disturbance regulations of CISPR 22 Class B, a further CM filter stage must be placed on the mains side next to L_{CM} and C_{CM} or D_3 and D_4 (Position I in Fig. 10a)).

Note: For a dual-boost converter structure with magnetically isolated inductances in both AC input lines, a balancing of the CM interference emission could be employed as shown in Fig. 14 of [20] because of the phase opposition of the CM voltages of the drains of the power MOSFETs S_1 and S_2 (cf. Fig. 13 in [19]) instead of D_3 and D_4 or C_{CM}. However, a switching-frequency CM voltage of the output then still occurs; furthermore, the balancing is influenced by the earth capacitance of the load connected to the output. For this reason, this concept is not be pursued further here.

In summary, the circuit in Fig. 9b) exhibits clear advantages over that in Fig. 9a) with regard to the total semiconductor area required for specified conduction and switching losses. If L_{CM} and L_{DM} are implemented with the same magnetic cores as L_{DM1} and L_{DM2} in Fig. 9a), i.e. only one magnetic core used for L_{DM}, the effective boost inductance is halved or the differential mode ripple increases by a factor of 2. As a result, a 6dB higher DM interference level is to be expected which, however, can be relatively simply lowered by increasing the capacitance of the DM filter capacitor C_{DM}. By use of the second magnetic core for the realization of L_{CM}, the CM interference level is reduced to a value comparable to Fig. 9a). With regard to electromagnetic compatibility both concepts are thus to be regarded as equal. Accordingly, for further considerations, Fig. 9b) is chosen as basis. For the system specifications we set:

TABLE I: Specifications of the considered single phase PFC rectifiers.

Output power P_O	3.2kW
Line voltage U_N	230±10%
Output voltage U_O	365V
Ambient Temperature	45°C

There, two parallel subsystems each with 1.6kW output power are employed in order to be able to switch off one system in the partial load region and thus assure a high efficiency over as wide a load range as possible.

In connection with efficiency maximization it is important to point out that the freewheeling diodes of the dual-boost topology cannot be complemented by synchronous rectifiers, i.e a super-junction MOSFET with antiserial low voltage MOSFET. This is because the power MOSFET working as a synchronous rectifier would represent a temporary short circuit when switching on the boost transistor again, because of the high output capacitance at low voltage, and thus lead to a massive increase in switching losses.

IV. Analytical Approximation of η-ρ-Performance Limits

In the following, before numerical optimization (Chapter V), the limit of the system performance attainable in the η-ρ-plane, i.e. the Feasible Performance Space [21] will be

determined in the form of simple analytical approximations. The considerations refer to a bridgeless PFC boost rectifier (Fig. 6b) or Fig. 9b)) in the continuous conduction mode, but are basically also applicable for other converter types. The goal is to represent the performance limit in dependency on technological parameters such as the Figure of Merit (FOM) of the power transistors [22]–[25], or the energy density of the boost inductances or of the performance index of the cooling system in order to obtain, apart from the basic curve of the limits, also a statement on the possible expansion of the feasible performance space by future further development or improvements of technologies.

As shown by the considerations in [3], maximization of the power density of power electronics systems demands a relatively high switching frequency to obtain a low design volume of the magnetic components and the EMI filter. However, this results in a corresponding rise in frequency-dependent losses (switching losses, skin and proximity effect losses, etc.), and hence a relatively low efficiency. If the switching frequency is increased above the power density maximum, the volume of the cooling device finally dominates. Correspondingly, the output power density ρ is reduced with decreasing efficiency until finally in the theoretical limiting case $\eta = 0$ the entire input power is converted into losses, i.e. $\rho = 0$ results. The η-ρ-limit of the system performance at low efficiency is thus decisively determined by the cooling system and can be simply stated analytically.

If on the other hand the performance limit for high efficiency is to be approximated, in any case lower switching frequencies than for the power density maximum must be taken into account. In order to retain a relative switching-frequency ripple of the input current, the inductance and/or design size of the boost inductor must be increased with the reciprocal of the frequency. Since at low switching frequencies the losses in the boost inductor are small, there remain then the conduction losses of the freewheeling diodes and the conduction and switching losses of the power transistors as a (small) loss fraction, which can be dissipated via natural convection without explicit cooling devices. The power density is thus decisively determined by the boost inductance, while the losses are dominated by the power semiconductors. This relation is simple to formulate, whereby at a given switching frequency a possibility of maximizing the efficiency appears through optimum choice of the power MOSFET chip area used. Finally, for the overall power density associated with this efficiency, the design volume of the output capacitor C_O must be considered. The capacitance required or the design volume of C_O is determined by the output power because of the pulsation of the power flow with twice the mains frequency occurring in principle for single-phase systems. The output capacitance can thus be formally assigned a power density ρ_C, which must be combined with the power density ρ_L of the boost inductor L_{DM} and L_{CM} (are considered to show equal design volume), in order to determine the overall system power density.

A. Power Semiconductors

With the losses of the power semiconductors an upper limit of the efficiency and therewith a limit in the η-ρ-plane is determined. In the following first the influence of the forward voltage drop of the output diodes and then the influence of the conduction and switching losses of the MOSFETs is investigated.

1) Output Diodes: As could be seen in Fig. 9b), the power transferred to the output flows via a freewheeling diode which causes a voltage drop $U_{F,D}$. In case an equivalent DC-DC boost converter with a duty cycle D and an ideal switch is considered, the relation of input and output voltage is

$$\begin{aligned} U_I &= (U_O + U_{F,D})(1-D) \\ &= U_O \left(1 + \frac{U_{F,D}}{U_O}\right)(1-D). \end{aligned} \tag{14}$$

This results in

$$\frac{U_O}{U_I} = \frac{1}{\left(1 + \frac{U_{F,D}}{U_O}\right)(1-D)}. \tag{15}$$

Furthermore, the output current is given by

$$I_O = I_I(1-D). \tag{16}$$

Using these equations and expressing the output power yields

$$\begin{aligned} P_O = U_O I_O &= U_I I_I \frac{1}{\left(1 + \frac{U_{F,D}}{U_O}\right)} \\ &= U_I I_I \left(1 - \frac{U_{F,D}}{U_O}\right) = P_I \eta \end{aligned} \tag{17}$$

Consequently, the efficiency as function of the diode forward voltage drop is

$$\eta = \left(1 - \frac{U_{F,D}}{U_O}\right), \tag{18}$$

which represents a horizontal line in the η-ρ-plane.

2) Power MOSFETs: Besides the output diodes also the conduction and switching losses of the MOSFETs limit the achievable efficiency. The conduction losses can simply be calculated with the on-resistance and the RMS current through the MOSFET. The switching losses are mainly determined by the output capacitance of the MOSFET, which is discharged via the MOSFET during turn-on. The additional switching losses caused during the commutation of the inductive current are negligible for the considered highly efficient system, since the time for the commutation decreases linearly with an increasing chip area. As for a high efficiency a large chip area is required, the commutation losses become relatively small in comparison to the losses due to the output capacitance, which increase with the chip area. Therefore, the MOSFET losses are approximately given by

$$P_{V,T} = R_{DSon} I_{RMS}^2 + f_P \frac{C_{eq} U_O^2}{2} \tag{19}$$

with

$$R_{DSon} \sim \frac{1}{A_{Chip}}$$
$$C_{eq} \sim A_{Chip} \tag{20}$$

where C_{eq} is a constant equivalent capacitance, which results in the same switching losses as the voltage dependent output capacitance C_{oss} of the switching MOSFETs. The voltage dependency of C_{oss} could be approximated by

$$C_{oss} = C_0 \sqrt{\frac{U_O}{u_{DS}}} \tag{21}$$

with

$$C_0 = C_{oss} \quad \text{at} \quad U_O, \tag{22}$$

what results in

$$W_{C_{oss}} = \frac{2}{3} C_0 U_O^2 \tag{23}$$

for the energy stored in the output capacitance at a blocking voltage U_O. Consequently, the equivalent capacitance is

$$C_{eq} = \frac{4}{3} C_0. \tag{24}$$

Additional capacitances as for example the parasitic capacitance of the output diodes or of the boost inductors, which also cause switching losses, could be considered in a similar way but are neglected in the following considerations.

In (19) it could be seen that the conduction losses decrease and the switching losses increase with increasing chip area. Therefore, there is an optimal value of the chip area, which minimizes the MOSFET losses. This could be seen in Fig. 11, where the MOSFET losses are plotted as function of the chip area with the switching frequency as parameter.

With the low switching frequency required for a high-efficiency system and the optimized chip area, the MOSFET losses become relatively small, so that the volume of the heat sink for the MOSFETs is negligible. Thus, the system volume is mainly defined by the volume of the output capacitor and the volume of the boost inductor, which increases with decreasing switching frequency. In order to get a relation between the losses and the volume, i.e. between η and ρ, in the following a relation between the switching frequency and the inductor volume is derived. With this relation the switching frequency in (19) is eliminated. Accordingly, a direct relation between the losses and the volume is obtained. The volume of the output capacitor is independent of the switching frequency and is just considered in the end, when the system power density is calculated.

Efficiency limit with $R_{th,j-a} = 0$: In a first step, the dependency of the MOSFET on-resistance on the temperature is neglected (i.e. for the thermal resistance $R_{th,j-a} = 0$ is assumed) in the calculation of the efficiency limit, but will be discussed later.

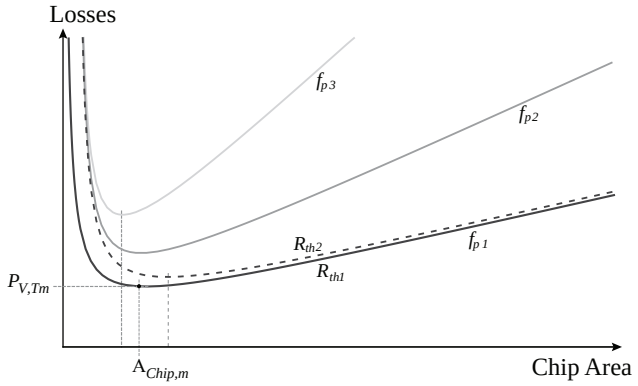

Fig. 11: Dependency of the sum of conduction and capacitive switching losses of a power MOSFET on the chip area A_{Chip}. The capacitive switching losses are due to the output capacitance C_{oss}. Parameter: Switching frequency f_P and thermal resistance R_{th}. A larger chip area reduces the conduction losses ($R_{DSon} \sim 1/A_{Chip}$) but results in increased capacitive losses ($C_{oss} \sim A_{Chip}$). Accordingly, depending on f_P minimum total losses are achieved for a chip area $A_{Chip,m}$. For higher thermal resistance $R_{th2} > R_{th1}$ and/or higher junction temperature and on-resistance the loss minimum is shifted to higher chip areas but despite that also higher total losses do occur.

For determining the power density of the inductor as function of the switching frequency, the relative ripple current is utilized. In case an equivalent DC-DC boost converter with a duty cycle D is considered, the ripple of the inductor current is given by

$$\Delta i_L = \frac{V_I}{L} D T_P \rightarrow \frac{\Delta i_L}{I_L} = \frac{V_I}{I_L L} D \frac{1}{f_P}$$
$$\rightarrow L = \frac{V_I D}{\alpha_{\Delta i_L} I_L} \frac{1}{f_P} \tag{25}$$

with the relative ripple current

$$\alpha_{\Delta i_L} = \frac{\Delta i_L}{I_L}.$$

Furthermore, the inductor volume is approximately proportional to the stored energy, i.e.

$$V_L = \alpha_{V_L} \frac{1}{2} L I_L^2, \tag{26}$$

where α_{V_L} is a technology factor of the inductor, which relates the volume to the stored energy.

With the inductance value calculated in (25) and the approximation $I_L \approx I_{L,RMS} \approx I_I$, the inductor volume is

$$V_L \approx \alpha_{V_L} \frac{1}{2} \frac{V_I D}{\alpha_{\Delta i_L} I_I} \frac{1}{f_P} I_I^2 = \frac{D \alpha_{V_L}}{2 \alpha_{\Delta i_L}} P_I \frac{1}{f_P}. \tag{27}$$

Assuming a high efficiency, i.e. $P_O \approx P_I$, the power density of the inductor is given by

$$\rho_L = \frac{P_O}{V_L} = \frac{2 \alpha_{\Delta i_L}}{D \alpha_{V_L}} f_P, \tag{28}$$

which could be solved for the frequency f_P.

Inserting this expression for the frequency into (19) and assuming that the MOSFET current is $I_{T,RMS} \approx \sqrt{D} I_I$, the MOSFET losses are given by

$$P_{V,T} = \frac{\sqrt{D} I_I^2}{G^*} \frac{1}{A_{Chip}} + \frac{1}{2} U_O^2 \frac{D \alpha_{V_L}}{2 \alpha_{\Delta i_L}} \rho_L C^* A_{Chip} \tag{29}$$

with

$$R_{DSon} = \frac{1}{G^*}\frac{1}{A_{Chip}}$$
$$C_{eq} = C^* A_{Chip}.$$

There, G^* is the conductivity per unit area and C^* is the equivalent capacitance per unit area.

Equation (29) could be summarized to

$$P_{V,T} = \beta_R \frac{1}{G^*} P_O^2 \frac{1}{A_{Chip}} + \beta_C \rho_L C^* A_{Chip} \qquad (30)$$

with

$$\beta_R = \frac{\sqrt{D}}{U_O^2 (1-D)^2}$$
$$\beta_C = \frac{1}{2} U_O^2 \frac{D \alpha_{V_L}}{2 \alpha_{\Delta i_L}},$$

where it could be seen that the conduction losses are decreasing and the switching losses are increasing with increasing chip area A_{Chip}. Therefore, there is an optimal chip area resulting in minimal overall losses and equal conduction and switching losses. The optimal area is

$$A_{Chip,opt} = \sqrt{\frac{\beta_R}{\beta_C \rho_L G^* C^*}} P_O. \qquad (31)$$

Inserting this expression into (30) and assuming again a high efficiency ($P_O \approx P_I$) results in

$$P_{V,T,m} = \gamma_V \sqrt{\rho_L \frac{C^*}{G^*}} P_O \approx \gamma_V \sqrt{\rho_L \frac{C^*}{G^*}} P_I \qquad (32)$$

with

$$\gamma_V = 2\sqrt{\beta_R \beta_C}. \qquad (33)$$

Since $P_{V,T}/P_I = 1 - \eta$, the maximal achievable efficiency at a given power density is

$$(1-\eta) = \gamma_V \frac{\sqrt{\rho_L}}{FOM_{\eta\rho 1}} \qquad (34)$$

with

$$FOM_{\eta\rho 1} = \sqrt{\frac{G^*}{C^*}},$$

when considering the MOSFET losses and the inductor volume. There, $\sqrt{G^*/C^*}$ is the Figure of Merit $FOM_{\eta\rho 1}$ (with the unit $\sqrt{\text{Hz}}$) reflecting the performance of the switch technology. The higher the conductance and the lower the parasitic capacitance of the switch is, the higher is the maximal achievable efficiency. Furthermore, the power density of the inductor is limiting the efficiency. With increasing switching frequency the inductor volume decreases, i.e. the power density increases. However, the efficiency is decreasing due the higher switching losses.

Efficiency limit with $R_{th,j-a} > 0$: So far, the increase of the on-resistance of the MOSFET in (19) due to the increasing junction temperature, which is rising with increasing losses, has been neglected. The on-resistance as function of temperature is given by

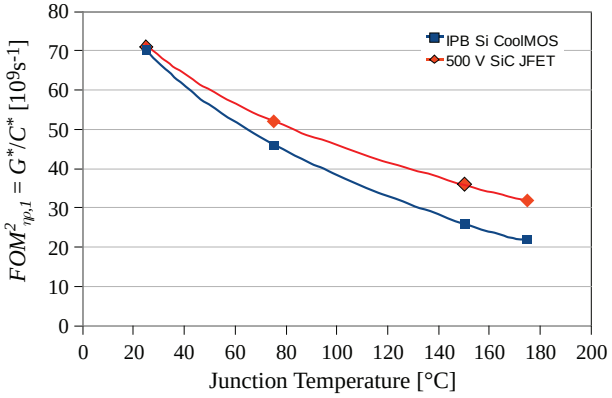

Fig. 12: Dependency of the power density Figure-of-Merit $FOM_{\eta\rho 1}$ $=\sqrt{G^*/C^*}$ of a 650V Si CoolMOS IBP60R099CP (Infineon, chip area 28mm^2) and of a 500V (620V avalanche voltage) SiC J-FET (SiCED, normally on, 5.75mm^2) on the junction temperature. In both cases the calculation of G^* and C^* is based on the total chip area, i.e. the area required for edge termination is not subtracted). Parameters for T_j=75°C and U_O=400V: CoolMOS: 4.2 Ohm*mm^2, 5.1 pF/mm^2; SiC J-FET: 1.7 Ohm*mm^2, 11.6 pF/mm^2.

$$R_{DSon} = R_{DSon,25}\left(1 + \alpha \Delta T_j\right)$$
$$= R_{DSon,25}\left(1 + \alpha P_{V,T} R_{th,j-a}\right). \qquad (35)$$

This relation is inserted in (19) and the resulting expression solved for the losses $P_{V,T}$ resulting in

$$P_{V,T} = \frac{R_{DSon,25} I_{RMS}^2 + {}^1\!/_2 f_P C_{eq} U_O^2}{1 - R_{DSon,25} \alpha R_{th,j-a} I_{RMS}^2}. \qquad (36)$$

Again, the on-resistance $R_{DSon,25}$ and the effective capacitance are dependent on the chip area A_{Chip}, so that an optimal chip area exists which results in minimal losses. Similar to (30),

$$P_{V,T} = \frac{\beta_R P_O^2 + \beta_C \rho_L C^* G^* A_{Chip^2}}{G^* A_{Chip} - \beta_R P_O^2 \alpha R_{th,j-a}} \qquad (37)$$

is resulting for the losses as function of A_{Chip}. Optimizing the chip area for minimal MOSFET losses results in

$$A_{Chip,opt} = \frac{P_O \gamma_\nu}{4\beta_C \rho_L G^* C^*}\left(\rho_L C^* \alpha R_{th,j-a} P_O \gamma_\nu + \sqrt{\rho_L C^*}\sqrt{\alpha^2 R_{th,j-a}^2 C^* P_O^2 \gamma_\nu^2 \rho_L + 4G^*}\right). \qquad (38)$$

Analogously to (34), this results in

$$(1-\eta) = \frac{\gamma_\nu \sqrt{\rho_L}}{FOM_{\eta\rho 1}}\left(P_O \gamma_\nu \sqrt{\rho_L}\frac{1}{2\,FOM_{\eta\rho 2}} R_{th,j-a} + \sqrt{1 + \rho_L P_O^2 \gamma_\nu^2 \frac{1}{4\,FOM_{\eta\rho 2}^2} R_{th,j-a}^2}\right) \qquad (39)$$

with

$$FOM_{\eta\rho 2} = \sqrt{\frac{G^*}{C^*}}\frac{1}{\alpha}$$

There, the original figure of merit $FOM_{\eta\rho1} = \sqrt{G^*/C^*}$ as well as the new figure of merit $FOM_{\eta\rho2}$ reflecting the cooling conditions of the semiconductor determine the maximal achievable efficiency. The lower the dependency of R_{DSon} on the temperature and/or the lower the thermal resistance between the junction and the ambient is, the smaller is the influence of the second figure of merit and the higher is the maximal efficiency. With increasing α or $R_{th,j-a}$ the square root dependency of the minimal losses on ρ_L changes to a more linear dependency.

In the calculations it has been assumed, that the thermal resistance is independent of the chip area, what is true in case the thermal resistance is mainly determined by the case-to-ambient resistance as this is the case for PCB mounted MOSFETs. In case of a forced air cooling the total thermal resistance is mainly determined by the junction-to-case resistance, which is also dependent on the chip area. A similar calculation as explained above could be performed in this case. However, this leads to relatively lengthy expressions, which are omitted here for the sake of brevity.

B. Input Inductor

Besides the semiconductors, the magnetic components are the main cause for losses in the PFC system. There, the losses of the magnetic components decrease with increasing volume, as will be shown in the following by a simplified considerations, where only a purely sinusoidal current I_{RMS} is assumed in the inductor and where HF effects are neglected. This basic tendency, however, is also valid in case the HF effects are included as verified with numeric calculations and could be used to describe the dependency of the losses in the PFC inductor on the inductor volume.

First, the core losses are expressed as function of the geometry and the Steinmetz parameters, which can be obtained from the data sheets of the core material.

$$\begin{aligned} P_{Co} &= C B^{\beta} f^{\alpha} V_{Co} \\ &= C \left(\frac{UT}{N A_{Co}}\right)^{\beta} f^{\alpha} A_{Co} l_{Co} \\ &= C \left(\frac{U}{N}\right)^{\beta} f^{\alpha-\beta} \frac{1}{\sqrt{k_{CW}}} k_{SC} A_{Co}^{\frac{3}{2}-\beta} \end{aligned} \tag{40}$$

with

$$k_{CW} = \frac{A_{Co}}{A_W}$$

k_{SC} = Shape Factor of Core.

Second, the winding losses neglecting the HF-effects are calculated as function of geometry.

$$\begin{aligned} P_{Wdg} &= R_W I_{RMS}^2 = \frac{N^2 l_W}{\sigma A_W k_{CU}} I_{RMS}^2 \\ &= \frac{N^2 k_{CW} k_{SW}}{\sigma \sqrt{A_{Co}} k_{CU}} I_{RMS}^2 \end{aligned} \tag{41}$$

with

k_{SW} = Shape Factor of Winding.

Since the winding losses increase with the number of turns N and the core losses decrease with N, there is an optimal number of turns N_{Opt} resulting in minimal losses. This N_{Opt} is calculated in the third step and then used to eliminate N in the winding and core loss equations.

By minimizing $P_{Co} + P_W$ as function of N with respect to the losses one obtains

$$\begin{aligned} N_{Opt} = U_I \, D \, 2^{-\frac{1}{2+\beta}} \\ \cdot \left(\frac{A_{Co}^{2\beta-4} k_{CW}^3 U_I^4 D^4 k_{SW}^2 I_{I,RMS}^4 f^{-2\alpha+2\beta}}{C^2 \, \beta^2 \, k_{SC}^2 \, \sigma^2} \right)^{\frac{-1}{4+2\beta}} \end{aligned} \tag{42}$$

for the optimal number of turns.

For relating the losses and the inductor volume, the core and the winding volume are expressed by

$$V_{Co} = A_{Co} k_{SC} \sqrt{A_W} = A_W^{\frac{3}{2}} k_{CW} k_{SC} \tag{43}$$

$$V_W = A_W k_{SW} \sqrt{A_{Co}} = A_W^{\frac{3}{2}} k_{SW} \sqrt{k_{CW}}. \tag{44}$$

Solving this for the core area and setting $V_L = V_{Co} + V_W$ results in

$$A_{Co} = k_{CW} \left(\frac{V_L}{k_{CW} k_{SC} + k_{SW} \sqrt{k_{CW}}} \right)^{\frac{2}{3}}. \tag{45}$$

Inserting the optimal number of turns and the expression for the core losses in the sum of (40) and (41) and summarizing the constants in $k_{\sum} = f(\beta)$ results in the total losses

$$P_L = k_{\sum} V_L^{\frac{4(2-\beta)}{3(2+\beta)} - \frac{1}{3}} f^{\frac{2\alpha-2\beta}{2+\beta}} I_{RMS}^{\frac{2\beta}{2+\beta}} U^{\frac{2\beta}{2+\beta}}. \tag{46}$$

Assuming for example $\beta = 2$ and $\alpha = 1$ results in

$$P_L \sim \frac{U I_{RMS}}{\sqrt{f} V_L^{\frac{1}{3}}} \tag{47}$$

which shows that the losses decrease with an increasing inductor volume.

This tendency is also verified in case a more comprehensive model for the losses is used, what could be seen in Fig. 13,

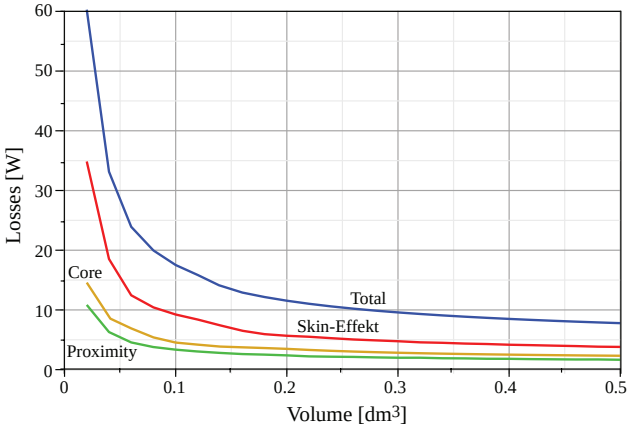

Fig. 13: Winding losses, i.e. resistive losses considering skin and proximity effect and core losses of an inductor in dependency of the inductor volume. The core geometry is optimized for minimum total losses; winding losses due to the fringing field of the air gap are not considered. An increase of the overall inductor volume results in a reduction of the total losses.

where the losses of an inductor utilizing an E-Core and litz-wire are shown in dependency of the inductor volume. In the loss calculations the skin- and the proximity-effect losses but not the losses due to the fringing field of an air gap are considered (1-D approach [26]). The current is assumed to be 20A and the inductor voltage to be sinusoidal with an amplitude of 300V and a frequency of 100kHz.

As the losses in the inductor monotonically decrease with increasing volume, the inductor volume must be limited during the minimization of the system losses (cf. Chapter V). This indirectly influences also the optimal operating frequency and the power density of the system.

C. Output Capacitor

For the output capacitor either electrolytic or film capacitors could be used. With electrolytic capacitors a higher power density is achieved due to the higher capacitance per volume. However, the losses in the electrolytic capacitors due to the ESR and the leakage current are significantly higher than with film capacitors. Thus, film capacitors are required for high efficiency designs as considered in this paper. The film capacitors also have a higher ripple current rating per capacitance.

In the following both technologies are shortly investigated with respect to achievable power density. There, a hold up time requirement is not considered, so that the capacitance value is determined by the ripple voltage in case of the film capacitor and by the ripple current in case of the electrolytic capacitor. In case a hold up time has to be provided, the capacitance value is determined by this requirement, which directly results in a volume for the capacitors.

1) Film Capacitors: With film capacitors, the volume scales linearly with the stored energy [3] since the thickness of the capacitor is mainly determined by the thickness of the dielectric layers. Therefore, the volume could be calculated by

$$V_{CF} = \gamma_{V_{CF}}^{-1} \frac{1}{2} C_F U_O^2, \tag{48}$$

where $\gamma_{V_{CF}}^{-1}$ (energy per volume) is the proportionality factor between the energy and the volume. In case the output voltage U_O is fixed the volume just scales with the required capacitance value C_F.

In the considered case, the output voltage is fixed and the capacitance value is determined by the ripple voltage. Approximating the capacitor current by a sinusoidal current with an amplitude equal to the average output current, the relative peak-to-peak output voltage ripple is given by

$$\alpha_{\Delta u_{CF}} = \frac{\widehat{u}_{CF}}{U_O} = \frac{P_O}{4\omega_N} \frac{1}{\frac{1}{2} C_F U_O^2} = \frac{P_O}{4\omega_N} \frac{1}{\gamma_{V_{CF}} V_{CF}}. \tag{49}$$

This could be directly converted to

$$\rho_{CF} = \frac{P_O}{V_{CF}} = 4\omega_N \alpha_{\Delta u_{CF}} \gamma_{V_{CF}} = \gamma_{CF} \gamma_{V_{CF}} \tag{50}$$

with

$$\gamma_{CF} = 4\omega_N \alpha_{\Delta u_{CF}}$$

for the power density of the output capacitors based on film technology.

2) Electrolytic Capacitors: In contrast to the film capacitors, which have a constant energy density, the energy density of electrolytic capacitors scales approximately linearly with the output voltage [3]. Assuming a constant output voltage, the energy density is fixed as with the film capacitor and the volume linearly depends on the capacitance value. As already mentioned, the capacitance value of the output capacitor is mainly determined by the ripple current in case of electrolytic capacitors and no hold up time requirements. Thus, the volume of the electrolytic output capacitor is proportional to the ripple current

$$V_{CE} = \gamma_{V_{CE}}^{-1} I_{C,RMS}. \tag{51}$$

The ripple current could be directly related to the output power

$$I_{C,RMS}^2 = \frac{1}{M} \left(\frac{4}{3\pi} - \frac{1}{4M} \right) \widehat{I}_N^2 \approx \frac{2M}{U_O^2} \left(\frac{4}{3\pi} - \frac{1}{4M} \right) P_O^2, \tag{52}$$

where M is the modulation index. With this relation the power density of electrolytic capacitors is given by

$$\rho_{CE} = \frac{P_O}{V_{CE}} = \frac{U_O}{\sqrt{\frac{8M}{3\pi} - \frac{1}{2}}} \gamma_{V_{CE}} = \gamma_{CE} \gamma_{V_{CE}}. \tag{53}$$

D. Cooling System

The cooling system is a major limitation for the achievable power density, especially in case the efficiency is low, so that a large amount of heat has to be dissipated. The losses in the semiconductor can be expressed as function of the efficiency

$$P_V = (1 - \eta) P_I = (1 - \eta) \frac{P_O}{\eta} \tag{54}$$

but can also be related to the temperature drop and the thermal resistance of the heat sink

$$P_V R_{th} = \Delta T \;\Rightarrow\; P_V = \frac{\Delta T_{s-a}}{R_{th}} = \Delta T_{s-a} G_{th} \tag{55}$$

With the cooling system performance index (CSPI) defined in [31], the R_{th} is directly related to the volume of the heat sink by

$$CSPI = \frac{1}{R_{th} V_H} = \frac{G_{th}}{V_H}. \tag{56}$$

With the CSPI the losses are given by

$$P_V = \frac{1 - \eta}{\eta} P_O = \Delta T_{s-a}\, CSPI\, V_H, \tag{57}$$

what finally results in the power density determined by the heat sink

$$\rho_H = \frac{P_O}{V_H} = \Delta T_{s-a}\, CSPI\, \frac{\eta}{1 - \eta}. \tag{58}$$

There, it could be seen that the power density is dominated by the heat sink in case of a low efficiency, which is basically not desirable, and that the power density reaches 0 for $\eta = 0$. With increasing efficiency the influence of the heat sink on the system power density decreases and the power density of the heat sink theoretically goes to infinity if the losses of the fan are neglected.

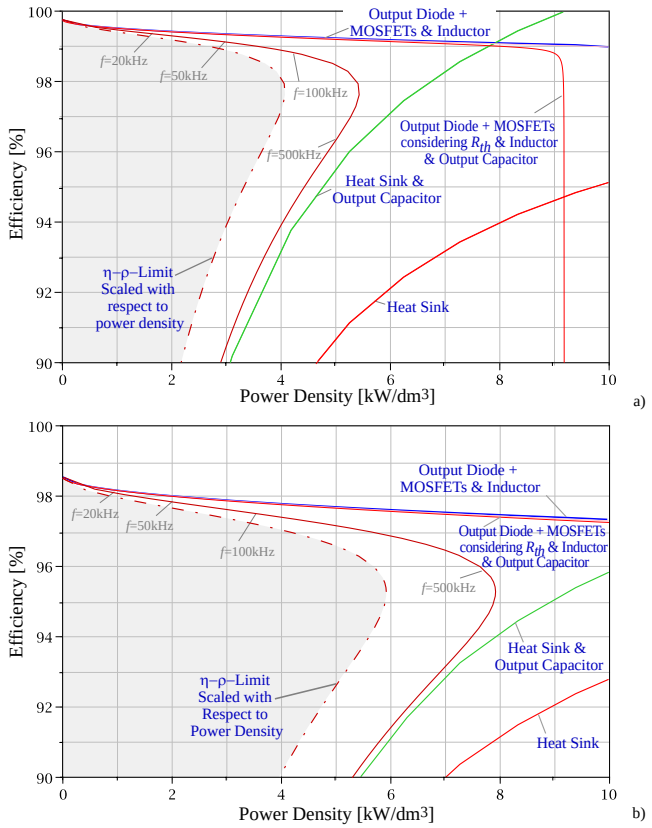

Fig. 14: Calculated performance limits of the dual-boost PFC rectifier (Fig. 9b)) in the η-ρ-plane for a high-efficiency design a) and a high power density design b). The assumed parameters (i.e. number of power MOSFETs and freewheeling diodes operating in parallel, output capacitance, etc.) are in accordance with the experimental systems described in Sections VI-A and VI-B). The cooling system performance index is based on the heat sink ICK S 40×40×20 by Fischer – in case of the ultra-compact system with and in case of the ultra-efficiency system without fan. The performance limits are defining a theoretical Feasible Performance Space which cannot be fully utilized concerning power density due the missing spatial integration of the components available for the system realization; the practical performance limit shown by a dash-dot line.

E. System Control and Auxiliary Supply

In addition to the main components also the control as well as the sensors and the gate drives cause losses, which are relatively independent of the operating point and system design. These constant losses result in a fixed efficiency reduction

$$\Delta\eta_{aux} = \frac{P_{aux}}{P_I} \approx \frac{P_{aux}}{P_O}, \tag{59}$$

which is a horizontal line in the η-ρ-plane. Also the leakage current in case of employing electrolytic capacitors for the output capacitor causes constant losses, which have to be added to the auxiliary power.

F. Overall System

In the previous paragraphs the different limitations in the η-ρ-plane caused by the semiconductors, the cooling system, the output capacitor and the auxiliary power have been discussed. In Fig. 14 the limiting lines for the parameters of a highly efficient (cf. section VI-A) and for the parameters of an ultra-compact system (cf. Section VI-B) are depicted.

For obtaining the limiting curve considering all influences at the same time, the equations for the power densities and efficiencies of the previous paragraphs have to be combined. There, losses which are not directly related to a volume (e.g. semiconductor losses without heat sink) or volumes which are not directly related to losses (e.g. output capacitor volume) can simply be combined to a single curve.

Adding for example the volume of the cooling system (cf. IV-D) and the volume of the output capacitors (cf. IV-C) results in

$$\begin{aligned}\sum V_\nu &= V_H + V_C \\ &= \frac{1}{\Delta T_{s-a}\, CSPI}(1-\eta)\frac{P_O}{\eta} + \frac{P_O}{\rho_C}.\end{aligned} \tag{60}$$

There, ρ_C stands either for ρ_{CE} or for ρ_{CF} depending on the applied technology for the output capacitors.

This results in the new power density

$$\rho_{HC} = \frac{P_O}{V_{HC}} = \frac{\rho_H \rho_C}{\rho_H + \rho_C} = \gamma_C \gamma_{V_C} \frac{1}{1 + \frac{\gamma_C \gamma_{V_C}}{\delta T_{s-a} CSPI} \frac{1-\eta}{\eta}}, \tag{61}$$

which gives the same results as just for the output capacitors in case of high CSPI values. For $\eta = 1$ the heat sink vanishes and the power density of the capacitor results and for $\eta = 0$ the heat sink dominates, so that the power density decreases to 0.

In general, the system power density could be calculated by

$$\rho_{ges} = \frac{1}{\sum\limits_i \frac{1}{\rho_i}}, \tag{62}$$

where ρ_i are the power densities of the different components. However, this expression does not directly relate the power density with the efficiency. For plotting the limit of the system it is better to calculate all volumes and losses as function of frequency, then add the volumes and the losses and finally make a parametric plot, with f_P as parameter. The result of this calculation is shown in Fig. 14 as the η-ρ-limit of the system for two sets of parameters – one for the ultra-efficient and one for the ultra-compact system.

Since in the calculation of the volumes only the net volumes of the individual components are considered and the volume required for mounting or the volume lost due to the not matching component shapes are not considered, the actually resulting system volume is smaller than the sum of the net component volumes. In order to account for this, the volumes have been increases by ⅓ based on experience with experimental systems [4].

V. Numerical Optimization

After fundamental clarification of the limits in the η-ρ-plane in Section IV, a numerical maximization of the efficiency of the PFC rectifier system will now be performed. In the optimization more detailed models of the inductors and semiconductor losses are utilized, so that an analytical solution for the optimal set of parameters is not possible. The degrees of freedom are the switching frequency f_P, the geometry of

the boost inductance, and the power semiconductor chip area A_{Chip}, i.e. the number of power MOSFETs and SiC diodes connected in parallel for realization of a power transistor S_1, S_2 and/or a freewheeling diode D_1, D_2.

The optimization is carried out for nominal power, i.e. for the continuous conduction mode. To assure a constant relative ripple of the input current, the inductance value of the boost inductor L_{DM} is varied inversely proportional to the switching frequency f_P. The volume of the boost inductor L_{DM} (Fig. 9b)) is limited to a fixed value (equal to the volume of L_{DM} in Section VI-A). Otherwise, the inductance volume would grow in the course of the optimization above all limits, because of the decreasing losses with increasing volume (cf. Section IV-B).

In the following first the optimization procedure and the utilized models are explained and thereafter results of the efficiency optimization are presented.

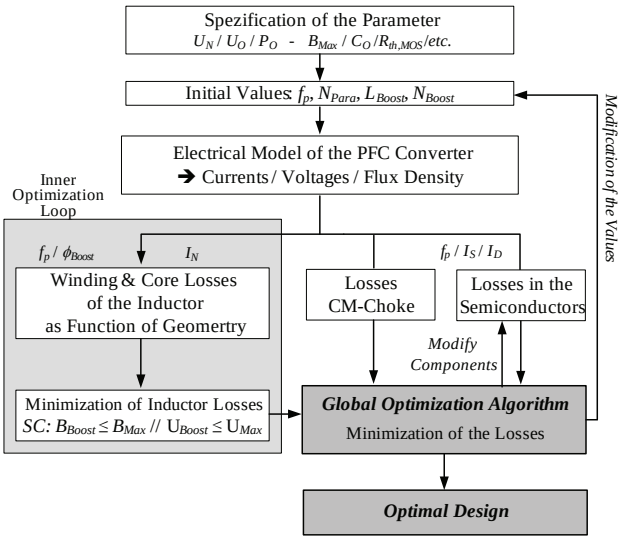

Fig. 15: Block diagram of the optimization procedure employed for maximizing the efficiency of the dual-boost PFC rectifier (Fig. 9b). Considering Fig. 13 an upper limit is defined for the boost inductor volume. All system specifications and design constants, i.e. parameters of the specific on-resistance $1/G^*$ and specific output capacitance C^* of the power MOSFETs, the forward characteristic of the freewheeling diodes, the thermal resistances of the power semiconductors etc. are selected in accordance with the experimental system in Section VI-A.

A. Converter Model

In Fig. 15 a flowchart of the developed procedure for optimizing the design variables (f_P, chip area of MOSFETs and diodes, number of turns and geometry of boost inductor) is shown.

The starting point of the procedure are the specifications of the converter system as for example the input/output voltages and the output power but also component limits as e.g. the maximal allowed flux density or the maximal junction temperature of the MOSFETs. Also the starting values of the design variables are set. With these values the currents/voltages of all the components are calculated and the losses in the semiconductor elements are determined. For the design of the boost inductor an inner optimization loop, which optimizes the number of turns and the geometry of the core and the winding for minimal losses, has been implemented. The global optimization algorithm adds the losses of the boost inductor, the CM-choke, and the semiconductors and varies then the free parameters, so that the overall system losses become minimal. In the system losses also the losses in the control, in the output capacitor and the EMI filter, which are assumed to be constant, are included.

In the following shortly the equations for the currents and voltages, the semiconductor losses as well as the magnetic components and the auxiliary power are summarized.

1) Semiconductors: The fundamental component of the input current is given by

$$i_{N(1)} = \widehat{I}_N \sin(\omega_N t) \tag{63}$$

with

$$\widehat{I}_N = \frac{P_N}{U_N}\sqrt{2}$$

where U_N is the RMS value of the mains voltage and P_N the input power. In addition to the fundamental component the ripple current

$$i_{N,r} = \frac{1}{2}\frac{U_O T_P}{L_{DM}}\frac{1}{M}\sin(\omega_N t)\sin\left(1-\frac{1}{M}\sin(\omega_N t)\right) \tag{64}$$

must be considered, where the modulation index M is defined as $M = U_O/\left(\sqrt{2}U_N\right)$. With the input current fundamental and the ripple current as well as the duty cycle

$$d = 1 - \frac{1}{M}\sin(\omega_N t) \tag{65}$$

the RMS current in the MOSFET and the average current in the rectifier diodes are calculated. Based on the currents the conduction losses of the semiconductors are determined. There,

$$R_{DSon} = R_{DSon,25} + \frac{R_{DSon,125} - R_{DSon,25}}{125°C - 25°C}\left(T_j - T_a\right) \tag{66}$$

is used for calculating the conduction losses in dependency of the junction temperature (T_a is the ambient temperature). By solving

$$T_j - T_a = \frac{R_{th,MOS}}{N_{P,MOS}}\left(P_{on} + P_{off} + R_{DSon} I_{RMS}^2\right) \tag{67}$$

for the junction temperature T_j, the losses can directly be calculated, without any iteration. There, $N_{P,MOS}$ is the number of parallel connected MOSFETs and P_{on}/P_{off} are the switching losses, which are calculated below. A similar equation is used for determining the junction temperature of the rectifier diodes, which influences the forward voltage drop.

The power transistors are controlled such, that each transistor is switching during half a mains period where the other transistor is turn-on for minimizing the conduction losses.

In a next step, the current values at the turn-on and the turn-off of the MOSFET are determined based on the above calculated input current. The switched currents are required for calculating the switching losses based on measured loss curves.

During the turn-on of the MOSFET the junction capacitance of the freewheeling diode as well as parasitic capacitances of the wiring and the respective boost inductor are charged or discharged. This results in a share of the turn-on losses, which are independent of the current. This is also true for the output capacitance of a power transistor, which has to be discharged during the turn-on. Additionally, current dependent losses are generated in the switching transisitor, so that the overall turn-on losses are given by

$$E_{on} = \frac{1}{2} Q_{SiC} U_O N_{P,Dio} + 4.32 \cdot 10^{-6} [\text{Ws/A}] I_{MOS}(t_k) + \frac{1}{2} C_{eq,MOS} U_O^2 N_{P,MOS}. \quad (68)$$

The numeric values have been obtained by measurements on the system shown in Fig. 20 and the components given in Table II.

Due to the large output capacitance of the parallel connected MOSFETs ZVS conditions are given during turn-off, so that the turn-off losses are very small and neglected in the considerations. This is also true for the switching losses of the SiC Schottky diodes employed as freewheeling diodes. Thus, the switching losses are mainly occuring during the turn-on of the MOSFETs.

2) Magnetic Components: Besides the semiconductors, the boost inductor is one of the major loss contributors. In the considered system the inductor is realized with foil windings and the basic design of the inductors geometrically determined by the four variables a, b, c and d as explained in [3]. With these variables for example the cross sectional area of the core or the window could be expressed and the losses in the core or the winding can be determined as function of these variables. This relation between the geometry and the losses enables then an optimization of the number of turns and the geometry for minimal losses.

For calculating the winding losses first the harmonics of the boost inductor current are calculated with a Fourier analysis. The time behavior of the inductor current is determined with (63) and (64) and the switching times. With the amplitude and the frequency of the harmonics the skin (69) and proximity (70) effect losses at each frequency are calculated with an 1-D approximation as for example presented in [26], [29], [30] and then – based on the orthogonality of the losses [32] – the losses at the single harmonics $\hat{I}_{L(i)}$ are added

$$P_S = \sum_i \frac{l_W}{2\sigma dh} \hat{I}_{L(i)}^2 \frac{\nu_i}{2} \frac{\sinh \nu_i + \sin \nu_i}{\cosh \nu_i - \cos \nu_i} \quad (69)$$

$$P_P = \sum_i \sum_m \frac{d l_W \nu_i}{\sigma h} \frac{\sinh \nu_i - \sin \nu_i}{\cosh \nu_i + \cos \nu_i} \hat{H}_{S(i)m}^2 \quad (70)$$

with

$$\hat{H}_{S(i)m} = \frac{2m-1}{4} \frac{\hat{I}_{L(i)}}{d}.$$

For calculating the proximity effect losses in the inductor, it is assumed that there is a gap in all three legs, i.e. the H-field ramps from $-H_{max}/2$ to $+H_{max}/2$. Furthermore, the losses in the winding due to the fringing field of the gap are neglected in order to simplify the calculations, what does not result in a too large error in the considered case as FEM simulations have proven. In all the calculations the losses are expressed as function of the variables a, b, c and d, so that it is possible to optimize the geometry of the core and the winding for minimal losses.

For the calculation of the core losses the flux density time behavior in the core must be determined. In the DM inductor the flux density follows a 50Hz major loop and minor magnetization loops with switching frequency. In such a case the core losses can be calculated based on the method proposed in [27], where the Steinmetz coefficients [28] are utilized for characterizing the core material and where the rate of change of the flux density (dB/dt) is the basis for the loss calculation. Here, these equations are applied and the losses are again described as function of the geometry for the loss optimization. With $U_{L,j}$ and t_j the voltage across the inductor is described as a piece wise linear function.

$$P_{Core} = \frac{k_i (\Delta B)^{\beta-\alpha}}{T} \sum_j \left(\frac{U_{L,j}}{N_L\, ab} \right)^{\alpha} \Delta t_j V_C \quad (71)$$

with

$$k_i = \frac{k}{2^{\beta+1} \pi^{\alpha-1} \left(0.2761 + \frac{1.7061}{\alpha+1.354} \right)} \quad (72)$$

In addition to the boost inductor, a CM-choke is used in the converter for reducing the EM noise emission as shown in Fig. 9b). In the considered system, this CM-choke has the same basic design as the boost inductor, so that the same basic equations for calculating the losses can be used as for the boost inductor. The time behavior of the current in the windings of the CM-choke is the same as for the boost inductors. However, the magnetic field required for calculating the proximity effect losses is different, since this field is only generated by the CM current. Due to the relatively small CM capacitors $C_{CM,1}$ and $C_{CM,2}$, the impedance of the capacitors at line frequency is relatively high, so that the low frequency component of the CM voltage appears across the CM-capacitors. Consequently, the flux density in the core of the CM inductor is mainly determined by the switching frequency component of the CM voltage $1/2 u_{S,\sim}$ (cf. Fig. 10). In the worst case $\pm U_O/4$ is applied to the CM inductor with 50% duty cycle. In order to simplify the calculation this situation is assumed to be present over the whole fundamental period. This does not lead to a significant error as the core losses of the CM inductor are relatively low anyway.

During the optimization the flux density is kept below the maximal admissible level and the inductor volume is limited to a defined value (cf. IV-B).

3) Output Capacitor & Auxiliary: For achieving a very high efficiency also minor loss contributions must be considered and minimized. There, for example the output capacitors could have a significant loss share, if electrolytic capacitors are used, since the leakage current of these capacitors is relatively high. Due to the ripple current several parallel connected

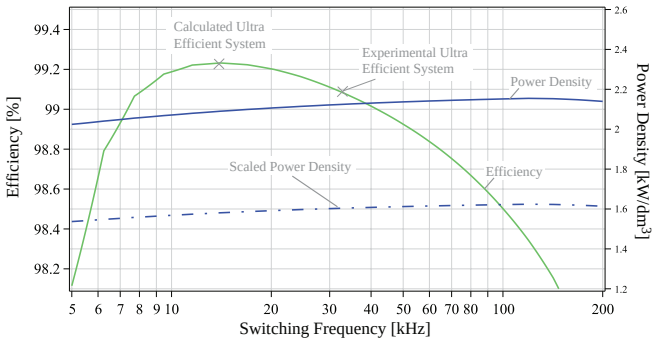

Fig. 16: Result of the efficiency optimization of the dual-boost PFC rectifier in dependency on the switching frequency f_P. Furthermore shown: Resulting power density ρ which is not considered in quality index of the optimization. The power density is calculated based on the sum of the volumes of the boost and CM inductors and the output capacitor C_O. For a practical realization the missing spatial matching of the components results in a reduction of the power density by typ. 30% [4],[5] (shown by dashed line).

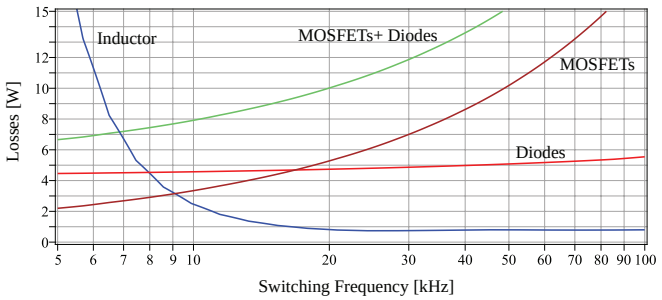

Fig. 17: Losses of the power semiconductors and of the boost inductor L_{DM} in dependency on the switching frequency f_P according to Fig. 16. The boost inductor volume is set to a constant value, the inductance is adapted inversely proportional to f_P. Therefore, for increasing f_P a lower inductance value has to be realized in the same volume resulting in lower boost inductor losses.

capacitors are required, so that the leakage current would be in the range of a few milliamperes. With an output voltage of up to 400V this results in significant losses of a few watts where the total loss budget of a 99% efficient converter with an output power of 1.6kW is only 16W. Therefore, foil capacitors are used in the considered system, which have a negligible leakage current and a very low equivalent series resistance. The losses in the dielectric material are also very low since the switching frequency voltage ripple is relatively small due to the relatively large capacitance value (cf. TableII). Therefore, the losses in the output capacitors simply can be approximated by

$$P_{C_O} = \frac{R_{ESR}}{N_{P,C_O}} I_{C,RMS}^2 \tag{73}$$

where N_{P,C_O} is the number of parallel connected capacitors.

Besides the output capacitors, also the DSP control, the current sensing and the gate drives have been designed for minimal losses. These losses are relatively independent of the specific converter design and are considered to be constant in the optimization.

B. Optimization Results

Based on the procedure described in the previous section, a dual boost PFC (cf. Fig. 9b) has been optimized for minimal losses. The peak value of the ripple of the input current, the volume of the CM inductance, as well as the data of the magnetic material, the output foil capacitors and the power semiconductors are selected here equal to those of the ultra-efficient experimental system in Section VI-A (cf. Fig. 20 and Table II).

A result of the calculations, where the global optimization algorithm has been replaced by a for-next loop for varying the operating frequency, is shown in Fig. 16. There, the optimized efficiency and the resulting power density based on the net volumes are shown as function of the switching frequency, so that besides the optimal operating point also the sensitivity of the operating point to frequency variations is shown. Additionally, a scaled power density accounting for unused space due to not matching geometric shapes of components in real systems is given. It is important to note, that the volume of the inductor is limited to maximal 0.3dm^3 for all considered operating points shown in Fig. 16. This limit comes from practical considerations and available core shapes and sizes.

The optimal efficiency of more than 99.2% is achieved for an operating frequency of approximately 15kHz. There, the theoretical power density is roughly 2kW/dm^3. With decreasing frequency the efficiency drops relatively rapidly due the limit of the inductor volume. The limit results in increasing losses of the inductor (cf. Fig. 17), since a growing inductance value must be realized in a limited volume. Without this limitation, the optimal efficiency would be theoretically at $f_P = 0$, what is not practical.

For increasing switching frequency the losses in the semiconductors increase. First the switching losses increase with increasing frequency and second, the optimal chip area resulting in minimal semiconductor losses decreases, so that also the conduction losses are increasing with switching frequency (cf. Fig. 17).

The distribution of the losses at the optimal operating point is shown in Fig. 18. Additionally, the loss distribution for the experimental system (cf. Section VI-A) is given for comparison. There, it could be seen that for the optimal system, the semiconductors cause the largest share of the system losses and that the forward voltage drop of the output diode has a significant influence on the efficiency. For the MOSFET losses it is important to note, that in the considered case the switching and the conduction losses are not equal at the optimal chip area (cf. Section IV-A2), since additional effects as for example the parasitic capacitance of the freewheeling diodes are considered in the optimization.

Furthermore, it could be seen that the passive components and the auxiliary supply/control have a relatively low influence on the achievable efficiency, what is true for the 15kHz as well as for the 33kHz system.

Finally, the results given in Fig. 16 are transferred to the η-ρ-plane shown in Fig. 19 (Curve: "Foil Capacitors"). Additionally, optimization results for the same set of parameters and electrolytic instead of foil output capacitors (Curve: "Electrolytic Capacitors") as well as for electrolytic capacitors and a smaller volume limit for the inductor (Curve: "Electrolytic

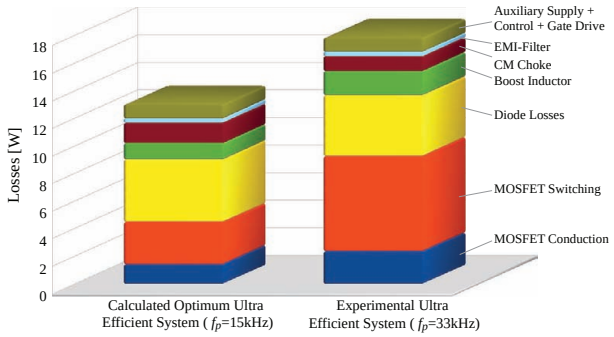

Fig. 18: Loss breakdown of the efficiency optimized design according to Fig. 16 (f_P=15kHz) and of the experimental ultra-efficient system according to Section VI-B (f_P=33kHz). For the experimental system due to the higher switching frequency besides higher switching losses also higher conduction losses do occur as the optimum MOSFET chip area decreases with increasing switching frequency (Section IV-A2).

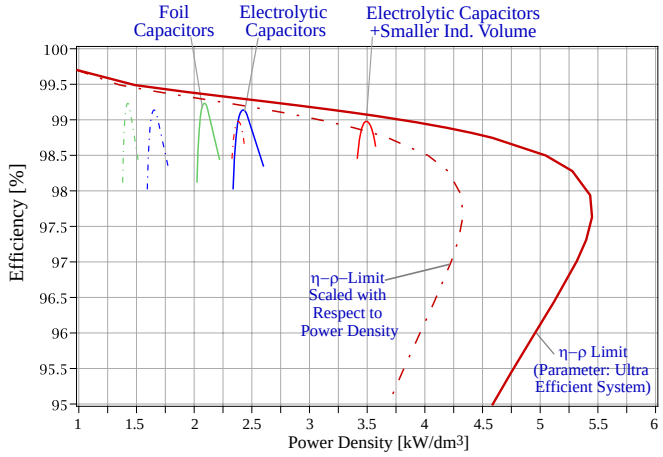

Fig. 19: Graphical representation of the optimization result according to Fig. 16 in the η-ρ-plane. Furthermore shown: Limit of the Feasible Performance Space according to Fig. 14a) and result of the optimization for realizing the output capacitor C_O by electrolytic capacitors instead of foil capacitors. Electrolytic capacitors show a higher capacitance per volume than foil capacitors but are on the other hand characterized by higher losses due to the equivalent series resistance (ESR) and leakage currents. Accordingly, the increase in power density is paid by a reduction in efficiency. Cutting the volume of the boost inductor to one third allows an additional increase in power density, but results again in a decrease of the efficiency, as the inductor losses increase with decreasing volume (cf. Fig. 13).

Capacitors + Smaller Ind. Volume") are depicted. Also the theoretical limiting curve for the η-ρ-plane is given (Fig. 14a)) and it could be seen that the theoretical considerations of Section IV nicely match the numerical optimization. All curves are also shown with 30% reduced power density, in order to consider the typical increase of required construction space due to not matching geometric shapes of components.

VI. Experimental Results

In order to verify the theoretical considerations on the limits in the Performance Space, i.e. on the position of the Pareto Front or its end points *I* and *II* (Fig.4), an ultra-efficient (Section 6.1) and an ultra-compact single-phase PFC boost rectifier system (Section 6.2) in dual-boost topology with integral CM inductance (cf. Fig.9b)) were realized. The system specification was set to the values given in Table I. Two parallel subsystems are arranged, each with 1.6kW output power. To lower the interference level, both systems include a triangular variation of the switching frequency with a period of 100ms, corresponding to the averaging time constant of the EMI measurement according to CISPR 22. This assures that the EMI measurement acquires the spectrum broadened by frequency modulation and reduced in interference amplitude.

To obtain a statement on the performance of a further, conceptually and technologically basically different single-phase PFC concept, also a laboratory model of a conventional PFC boost rectifier (Fig. 6a)) operating at very low switching frequency was constructed (Section VI-C). There, the volume of the boost inductor and the effort for the EMI filter were minimized by setting the switching frequency to 3kHz, i.e. to a value slightly above the spectral range covered by the harmonic regulations of IEC 61000-3 (50Hz...2kHz). Thus the 50^{th} is the first harmonic of the switching frequency to lie within the measurement range of CISP 22, which begins at 150kHz. Because of the natural drop of the harmonic amplitudes with increasing frequency, only an EMI filter with very low attenuation and/or low design volume is required. Furthermore, because of the low switching frequency, the control of the system can be implemented with a low-cost μC instead of a DSP.

A. Ultra-Efficient PFC Boost Rectifier

With a view to industrial applicability, the switching frequency of the ultra-efficient dual-boost PFC rectifier system is set to 33kHz, i.e. higher than the value of f_{Pm}=15kHz resulting from the optimization (Fig. 16). Accordingly, no operating noise of the converter occurs; moreover, the power density can be increased, but the efficiency can still be maintained above 99% because of the flat efficiency maximum (Fig. 16). The switching frequency is triangularly modulated between 30kHz and 36kHz, resulting in a broadening and amplitude reduction of the spectrum of the conducted EM interference emission without an overlap of the interference bands of the 5^{th} and 6^{th} harmonics of the switching frequency.

The output capacitance is realized with foil instead of electrolytic capacitors to avoid losses through ESR and leakage currents. Considering the low capacitance and/or energy density of foil capacitors, a relatively low capacitance 36x15uF is selected; the output voltage ripple with twice the mains frequency then has an amplitude of 25V.

Because of the low semiconductor losses, no explicit cooling device is required and the cooling can take place directly via the printed circuit board and natural convection. For a target efficiency >99%, a fan anyway could not be used because of its power consumption. In connection with a current measurement with low intrinsic power consumption (current transformer LEM FHS40) and the reduction of the calculating capacity of the DSP TI TMS 320 LF 2808 used for control from 100MIPS to 50MIPS, the overall auxiliary power consumption (incl. the efficiency of the auxiliary power supply of 85%) can thus be limited to 2W. The power components employed for realizing the system (Fig. 20) are listed for one 1.6kW subsystem in the left column of Table II.

Fig. 20: Laboratory prototype of the ultra-efficient 3.2kW dual-boost PFC rectifier according to Fig. 9b) composed of two interleaved 1.6kW units; overall dimensions: 275x130x85mm; output power density: 1.1 kW/l.

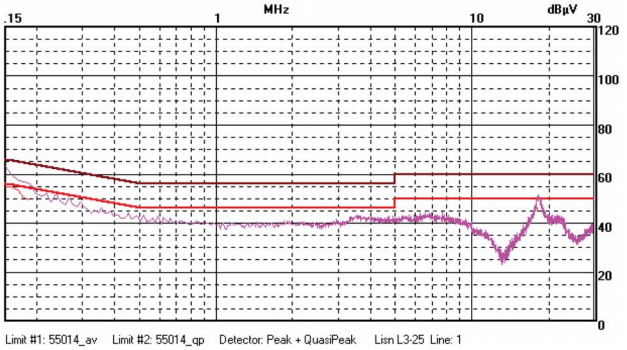

Fig. 21: Measured peak conducted EMI of the system depicted in Fig. 20. In addition to the integrated CM filtering L_{CM} and C_{CM} shown in Fig. 9b) a further CM filter stage and DM filter capacitor has been employed on the mains side (Position I in Fig. 10) in order to ensure compliance with CISPR 22-QP Class B.

By means of a calorimeter the efficiency of the system in the nominal operating point was determined to be 99.1%. The resolution of the efficiency measurement here is 0.01%. The calorimeter was calibrated with a comparative measurement. For this purpose, the system was placed with short-circuited output in the calorimeter and fed with a low AC voltage. Here only losses occur which can be very precisely measured electrically (precision of 0.2%, at 0.1% voltage and current measurement precision). The thermal conditions and air flows within the calorimeter are approximately the same as for the generation of output power. In contrast thereto, with a calculation of the efficiency based upon an electrical measurement of the input and output power, the error would amount to max. ±0.4%.

Overall, the 3.2kW system has dimensions of 275×130×85mm and thus a power density of 1.1 kW/dm^3. As shown in the optimization (Fig. 16), by lowering the switching frequency to 20kHz and adjusting the number of power MOSFETs and SiC diodes connected in parallel, an increase of the efficiency to 99.15% would be possible. By the use of SiC freewheeling diodes of a new type (IDD08SG60C) with lower reverse recovery and/or junction capacitance charge, a further improvement to 99.2% could easily be obtained.

B. Ultra-Compact PFC Boost Rectifier

In [3], a switching frequency of f_P=810kHz was calculated as giving the maximum power density for a 10kW three-phase PWM rectifier system (see Fig.30 in [3]). This frequency value can also serve as a guideline for the realization of a single-phase PWM rectifier system of maximum power density having the same output power as the power of one phase of the three-phase system. However, as the practical realization of the high switching frequency system shows, for very high switching frequency a high distortion of the rectifier input voltage would occur in the region of the current zero crossing [34]; this is due to the high output capacitance of the super-junction MOSFETs. Hence a switching frequency of 450kHz is selected. Due to the very flat maximum of the power density over f_P, this means only a slight increase in design volume. Moreover, the pulse-width modulation can then be accomplished directly by the DSP (TI TMS 320 LF 2808, 100MIPS), without a FPGA. For lowering the level of the conducted EM interference emission, again a modulation of the switching frequency (±50kHz) is provided. In the right column of Table II, the main components of the system (Fig. 22) are listed for a 1.6kW unit.

The single power MOSFET used has for f_P=450kHz an approximately optimal chip area with regard to the best possible compromise between conduction and switching losses. For the CM filter inductor L_{CM}, the same magnetic core is used as for boost inductor L_{DM}. The output capacitance is determined by the permissible current loading capacity of the electrolytic capacitors. Overall, the 3.2kW system exhibits at the nominal point an efficiency of 95.8%; the dimensions of the system are 175×80×42mm, hence a power density of 5.5kW/dm^3 is achieved. By optimization of the cooling system and magnetic integration of L_{DM} and L_{CM}, this value could be increased to ≈7kW/dm^3.

TABLE II: Components of the ultra-efficient and the ultra-compact dual-boost PFC rectifier. The heat sink of the ultra-compact system is ICKS 40×40×30 Fischer, incl. fan, R_{th} =1.5K/W.

	Ultra-Efficient	Ultra-Compact
MOSFETs (CoolMOS)	per Leg 5× IPP60R099 600V / 0.099Ω	per Leg 1× IPW60R045 600V / 0.045Ω
Diodes (SiC Schottky)	per Leg 5× IDB10S60C 600V / 10 A	per Leg 1× CSD10060 600V / 10A
CM-Choke L_{CM}	3mH / 2 × 9 turns 3 × EELP 64 Core	2 × 10 turns 1 × EILP 38 Core
Boost Inductor L_{DM}	1mH / 2 × 9 turns 3 × EELP 64 Core	2 × 10 turns 1 × EILP 38 Core
C_{CM1}=C_{CM2}	280nF (ceramic)	110nF (ceramic)
Output Cap. Capacitor	18×450V/15µF (AVX) FFB from AVX	12×FFB 450V/82µF KXG Nippon Chemi
Second Stage of the EMI Filter (inserted at *I* in Fig. 10a))		
C_{DMI}	2µF	-
L_{CMI}	1.2mH	637µH (Vitroperm W409)
C_{CMI}	22nF	22nF (ceramic)
C_{DMII}	2µF	4×220nF
L_{DMII}	-	2×10µH EF25 N87
C_{DMIII}	-	1.76µF

Fig. 22: Laboratory prototype of the ultra-compact 3.2kW dual-boost PFC rectifier according to Fig. 9b) composed of two interleaved 1.6kW units; overall dimensions: 175x80x42mm; output power density: 5.5kW/l.

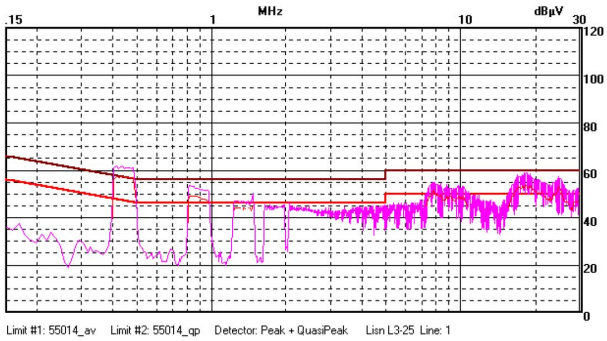

Fig. 23: Measured peak conducted EMI of the system depicted in Fig. 22. In addition to the integrated CM filtering L_{CM} and C_{CM} shown in Fig. 9b) a further CM and DM filter stage has been employed on the mains side (Position I in Fig. 10) in order to ensure compliance with CISPR 22-QP Class B.

C. Low-Frequency PFC Boost Rectifier

Because of the low constant switching frequency of f_P=3kHz, the boost inductor of the system shown in Fig. 24 is realized with conventional transformer laminations instead of ferrite. Moreover, for minimal realization effort, a conventional boost PFC rectifier system (Fig. 6a)) is selected instead of the dual-boost topology. The entire control is performed by means of a low-cost 14pin 8-bit μC (Microchip, PIC16F616, 5MIPS, SO14 package). Despite the low calculating capacity of the μC, an input current waveform fulfilling EN 61000-3-2 (Fig. 25) can be attained because of the low switching frequency. For the 3.2kW system, the following power components were employed (Fig. 6a)):

- S_1: IRGP4063 (IGBT)
- D_5: HFA25PB60
- D_1-D_4: GBJ2506
- Heat sink: Fischer SK88-75 1K/W (natural convection)
- L: EI96/59,7 (0.35mm lamination, material: C165-35)

For ripple and EMI filtering, a filter capacitance C=1μF is placed at the output of the bridge rectifier and a filter capacitance C=2.2μF is employed at the bridge rectifier input. In connection with a DM inductance L_{DM}=200μH in each AC line and a further DM filter capacitor C=2.2μF at the mains input, the radio interference regulations according to CISPR 22 Class B can be fulfilled.

Overall, the system exhibits at the nominal operating point an efficiency of 96.7% and incl. EMI filter dimensions of 200×80×100mm, i.e. a nominal output power density of 2kW/dm^3, and hence lies in performance significantly below that of the ultra-efficient or ultra-compact system. On the other hand, with regard to realization costs, significant advantages exist over these concepts. However, the application field of the system is limited by the acoustic noise of 68dB(A) measured at a distance of 1 meter.

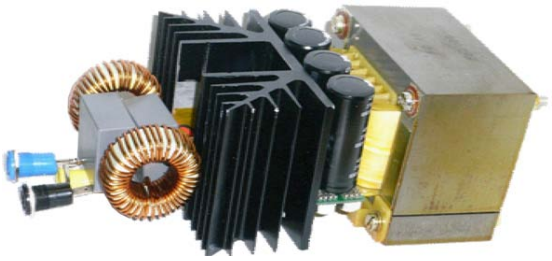

Fig. 24: Laboratory prototype of a low switching frequency conventional PFC boost rectifier (cf. Fig. 6a)). Overall dimensions: 200x80x100mm; output power density: 2kW/l. For EMI filtering only a single-stage DM filter is employed on the mains side in addition to filter capacitors at the input and output of the diode bridge.

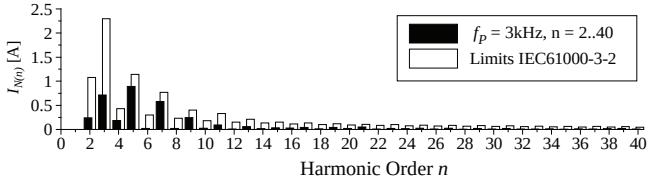

Fig. 25: Measured low frequency harmonics of the input current of the system depicted in Fig. 24. The system is in compliance with the harmonic limits defined in IEC61000-3-2.

Through doubling of the input inductance, the system also allows the realization of a single-pulse PFC rectifier with 100Hz switching frequency (p.1523 in [33]); the efficiency and power density of this system is also shown in Fig. 26.

VII. Prediction of the η-ρ-Pareto Front

In Fig. 26 the η-ρ-performance limits calculated in Section IV (Fig. 14a) and b)) and the results of the efficiency optimization in Section V are depicted, taking into account a reduction in power density by 30% that typically occurs in practical realization compared to the theoretical net values. Moreover, the characteristics of the experimental systems (Section VI) are shown. The performance limits were determined on the assumption of a design volume of the boost inductor running inversely to the switching frequency. Accordingly, an actual simultaneous optimization of efficiency and power density could still bring a slight improvement.

It is important to point out that different cooling technologies are used for the ultra-efficient system and the ultra-compact system. Thus, the only slight reduction in efficiency of the highly efficient system with increasing power density (≈0.5% decrease for increasing the power density by 1kW/dm^3) cannot be perpetuated up to high power densities, but reaches a thermal limit. A further increase in power density is then only possible by using an explicit heat sink (natural convection) whereby, however, the required increase in switching frequency leads to a decrease in the efficiency. Finally, at high switching frequencies forced convection cooling has to

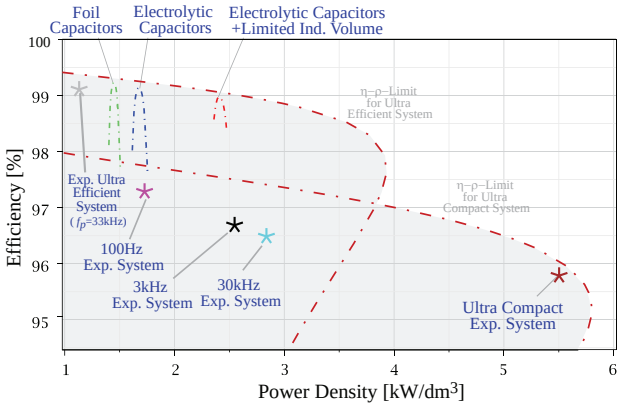

Fig. 26: Graphical representation of the performance of the experimental systems (Section V-B) in the η-ρ-plane in combination with the results of the efficiency optimization (Section V) and the η-ρ-performance limits calculated in of Section IV (a reduction in power density by 1/3 due to the missing spatial matching of the components is considered, cf. Fig. 14). The theoretical considerations are well predicting the actually achievable performance. For highly compact systems increasing the efficiency by 1% results in a decrease in power density by $\approx$1kW/dm^3. For ultra-efficient systems the same reduction of power density has to be accepted for improving the efficiency by 0.5%.

be used, whereby the power consumption of the fan causes a direct reduction in efficiency. However it is then possible to increase the power density up to a higher thermal limit, again with decreasing efficiency (typically 1% for each increase in power density of 1kW/dm^3).

VIII. Sensitivity Analysis

In Fig. 27 the loss breakdown of the ultra-efficient and the ultra-compact experimental systems is shown. By increasing the switching frequency from 33kHz to 450kHz, primarily the switching losses of the power MOSFETs and the power consumption of the gate-drive circuits are increased significantly. Furthermore, in order to keep the switching losses caused by the output capacitance of the power transistors low, the semiconductor area used for each of the switches S_1 and S_2 must be reduced, which results in an increase of the conduction losses. With a small design volume, the semiconductor losses can then be dissipated only by forced convection cooling; because of the power consumption of the fans, thereby the efficiency is further reduced. Finally, the pulse pattern calculation at switching frequency requires the full calculation

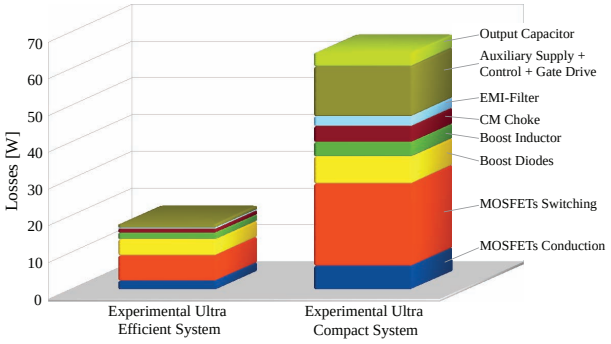

Fig. 27: Comparison of the breakdown of the power losses of the ultra-efficient and ultra-compact experimental dual-boost PFC rectifier.

capacity of the DSP used for control, which causes a higher power consumption and hence an increase in the auxiliary power. This shows that for high switching frequency or high power density, a gain in efficiency would primarily be possible by improvement of the $FOM_{\eta\rho 1} = \sqrt{G^*/C^*}$ of the power transistors and by means of a resonant gate drive. Alternatively, soft-switching concepts could be used whereby, however, a significantly higher complexity would have to be accepted.

Apart from its use for determination of the best possible design, the optimization described in Section V can also be employed for analyzing the sensitivity of the system performance with regard to selected design constants or technological parameters (Fig. 28). As the ultra-compact system, also the ultra-efficient system shows here a distinct dependence of the losses on the parameters G^* and C^* of the power transistors. Only a significant increase of the saturation limit of the magnetic core of the boost inductor could bring a comparable reduction in losses or a comparable gain in efficiency, since then a lower switching frequency for a given design volume of the inductor and thus lower losses of the power transistors would be possible. If the switching frequency is set to a constant value above the audible limit, i.e. f_P=20kHz (Fig. 28b)), this degree of freedom is eliminated and only G^* and C^* remain as main parameters for loss reduction. These considerations show clearly the possibility of studying

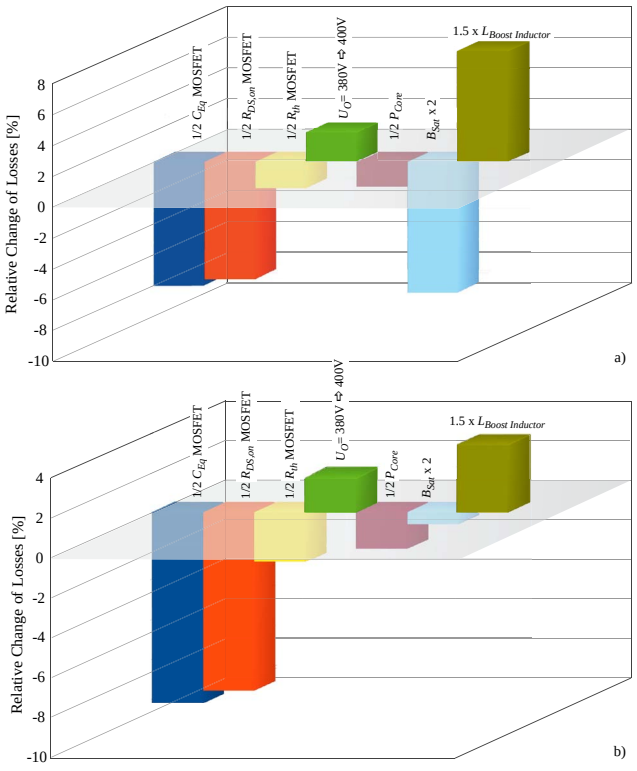

Fig. 28: Relative change of the total losses of the ultra-efficient dual-boost PFC rectifier for changing the characteristic values of the power MOSFETs (equivalent output capacitance and on-resistance) and the parameters of the magnetic material employed for realizing the boost inductor (core losses and saturation flux density). Furthermore, the influence of changing the output voltage level U_O and the value of the boost inductor ($\times$1.5) are considered. For a) the switching frequency is defined by the optimization procedure, for b) a constant switching frequency of f_P=20kHz is assumed.

the effects of an improvement in technological characteristics on the system performance, which can be employed as a basis for a targeted technology roadmapping.

IX. Conclusions

A reduction of the volume of an optimally designed inductor for a given current load is always coupled with an increase in power loss. Moreover, an increase of the switching frequency leads to an increase of high-frequency losses and of the switching losses of the power semiconductors, and hence finally to a decrease in efficiency. The realization of ultra-efficient systems is thus only possible at low switching frequencies and only with acceptance of a relatively low power density. As shown in this paper by the example of an approximation of the η-ρ-Pareto Front of single-phase dual-boost PFC rectifiers, based on today s technology a maximum efficiency of typically 99.2% can be attained at a power density of 1.1kW/dm^3. Increasing the switching frequency increases the power density; however, for an increase in the power density of 1kW/dm^3, a decrease in efficiency by 0.5% has to be accepted. For forced convection cooled highly compact systems, the η-ρ-Pareto Front exhibits a larger gradient because of the increase of the losses with the switching frequency. Here an increase of the power density by 1kW/dm^3 is connected with a decrease of the efficiency of typically 1%. With the use of all optimization options, a maximum power density of ca. 7kW/dm^3 at an efficiency of 97% could then be obtained.

The losses remaining in the efficiency maximum of ultra-efficient systems, with high design volumes and hence low inductive losses, are mainly caused by the on-state voltage drop of the freewheeling diodes and by the on-state losses and capacitive switching losses of the power MOSFETs. If the frequency is to be kept above the audible limit, an efficiency increase is possible only through improvement of the $FOM_{\eta\rho 1} = \sqrt{G^*/C^*}$ of the power transistors. It is of interest here that SiC power transistors, assuming the present state of development, show no advantages over Si super-junction transistors (Fig. 12). The further development of power semiconductors thus is of major importance for further increasing the efficiency.

If the power density is of secondary importance, the losses in the boost inductor can be kept low by adequate design size. The properties of the magnetic materials are thus primarily of importance when high efficiency *and* high power density are demanded. A high saturation flux density enables here low mean turn lengths and hence lower winding losses. For low hysteresis losses, a higher current ripple and a lower inductance value are possible for same core losses, resulting in a lower design volume.

The present work is only an initial step into the area of multi-objective optimization of single-phase PFC rectifier systems. For further research a multitude of topics remains. For example, one would have to consider

- a magnetic integration of the boost inductance L_{DM} and the common-mode inductance L_{CM} (Fig. 9b)), or
- a multi-stage realization of the integral CM filtering

for increasing the power density of the ultra-efficient system. Furthermore, the relatively coarse converter model, which is the basis of the optimization performed in this paper, could be expanded by a model of the EMI filter, which at high power density takes up typically 30% of the total volume of the converter. On this basis, a full multi-objective optimization with regard to efficiency and power density could be performed, i.e. the η-ρ-Pareto Front could be calculated directly. Further possibilities would be:

- to extend the optimization, which up to now has been referred to the nominal power, to the efficiency at 20%, 50% and 100% nominal power, in order to obtain a high efficiency over the entire output power range. Furthermore,
- a parallel connection of subsystems could be considered and their number optimized, whereby the operation of an individual system would have to be possible either in the continuous conduction mode or in the discontinuous conduction mode.
- Finally, the optimized distribution of a required total output power over the subsystems could be considered in such a way that minimal overall losses are assured for each output power level.

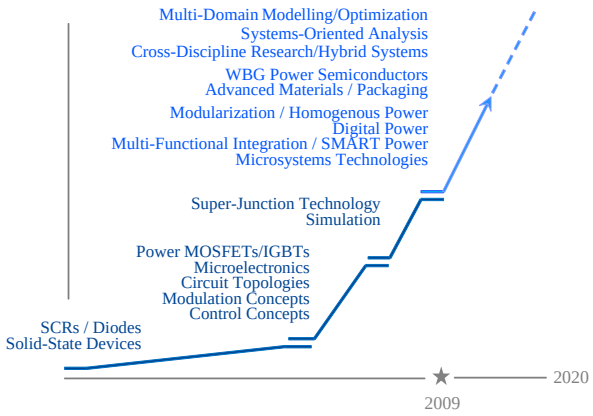

Fig. 29: Progress steps of solid state power electronics and related enabling technologies. Multi-domain modeling and optimization is a key element for ensuring a further highly dynamic development of the area.

In future, multi-objective optimization will assume great importance in power electronics research. Only by means of a mathematical model often non-linear effects of parameters like the switching frequency or the magnetic flux density swing can be understood and the best possible compromise found between competing optimization demands. Here, apart from efficiency and volume, the weight must be seen as an important performance index, especially for mobile applications. The increase in the weight of a power electronics converter causes in some cases only a slight increase in the overall weight, but can significantly raise the efficiency of the energy conversion and thus considerably increase the mission capability. Furthermore, the thermal cycling capability should be considered as a performance index, since the converter often represents a core component and is of central importance for the functioning of larger systems.

Finally, the Pareto Fronts and/or Pareto Surfaces should be determined in the Performance Space for different converter concepts, which on the one hand gives a representation of

the chosen circuit topology and of the modulation concept etc., and on the other hand of the component technologies employed. A performance comparison of competing concepts is thus directly possible. Furthermore, before the conception of a technology roadmap, different changes in a technology could be simply tested for their effect on the target performance, i.e. regarding their effectiveness. For this reason, multi-domain modeling and optimization has to be seen as an essential element of a continued highly dynamic development of power electronics (Fig. 29).

ACKNOWLEDGMENT

The Authors would like to acknowledge the contribution of Thomas Friedli, Ph.D. student at the Power Electronic Systems Laboratory of the ETH Zurich, who calculated the characteristic values G^* and C^* of Si CoolMOS and SiC J-FETs based on datasheet values, measurement results and physical models in order to determine the characteristic of the $FOM_{\eta\rho 1}$ of both devices in dependency of the junction temperature. Furthermore, the support of Dr. G. Deboy, Infineon Technologies AG, with providing power transistor samples for the experimental systems is highly appreciated.

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