

# Design Procedure for Compact Pulse Transformers with Rectangular Pulse Shape and Fast Rise Times

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**Abstract**—Pulse modulators based on solid state technology and for pulses in the  $\mu\text{s}$ -range often utilize a pulse transformer, since it could offer an inherent current balancing for parallel connected power semiconductors and the turns ratio of the pulse transformer allows to adapt the modulator design to the available switch technology.

The applications like radar systems, linear accelerators or klystron/magnetron modulators usually require a nearly rectangular pulse shape with a fast rise time and a as small as possible overshoot. In reality however, parasitic elements of the pulse transformer as leakage inductance and capacitances limit the achievable rise time and define the resulting overshoot. Therefore, in modulators based on pulse transformers, the design of the pulse transformer is crucial.

In this paper, a step by step design procedure of a pulse transformer for rectangular pulse shape with fast rise time is presented. Different transformer topologies are compared with respect of the parasitic elements, which are then calculated analytically depending on the mechanical dimensions of the transformer. Additionally, the influence of the limited switching speed of semiconductors and the nonlinear impedance characteristic of a klystron is analyzed.

## I. INTRODUCTION

In many application areas, the required output power level of test facilities in laboratories or in industry is rising and in more and more applications solid state modulators deploying for example IGBT modules, with a constantly increasing power handling capability, are utilized. In contrast to the spark gap switches, which can only be turned-on and have a limited life time and switching frequency, available fast semiconductor switches have a limited power handling capability, so that a parallel and/or series connection of the switches is required. The parallel connection of the semiconductors basically offers a more robust design due to the better capability of the switches to handle over-currents compared to over-voltage. In [1] it has been shown, that a modulator based on pulse transformer is the most suitable topology for pulses in the  $\mu\text{s}$ -range, since it could offer an inherent current balancing in parallel connected power semiconductors. Additionally, the turns ratio of the pulse transformer offers a degree of freedom that allows adapting the modulator design to the available switch technology.

In applications like radar systems, linear accelerators or klystron and magnetron modulators, where a nearly rectangular pulse shape is needed, however, the requirements with respect to rise times, overshoot or voltage droop are high. In Fig. 1 a) the waveform of a typical power modulator's output voltage and the designed power modulator for the specifications given in Fig. 1 b) is shown. Since in reality the transformer parasitics limit the achievable rise time and define the resulting overshoot, the proper design of the transformer is very important. On the one hand, non-ideal material properties like the limited permeability ( $\mu \neq \infty$ ) or the limited maximum flux density  $B_{max}$ , the maximum voltage-time-product respectively the minimum cut-off frequency  $f_u$  of the pulse transformer is defined. On the other hand, in real transformers no ideal magnetic coupling between windings can be achieved, which results in a certain leakage inductance  $L_\sigma$ . Additionally, the applied voltage to the transformer leads to a certain voltage distribution and the resulting charge transfer can be modeled by a distributed capacitances  $C_d$ , which in combination with the leakage inductance  $L_\sigma$  defines the upper cut-off frequency  $f_o$  of the real transformer. The output voltage with an almost rectangular pulse shape, however, exhibits a wide frequency spectrum. In order to transfer the voltage pulse with a minimum of pulse distortion, especially during the rise time, a maximum bandwidth has to be achieved, which means that the mentioned parasitics of the real transformer must be minimized.

In this paper, a general step by step design procedure of a pulse transformer is presented. In **section II** the influence of the

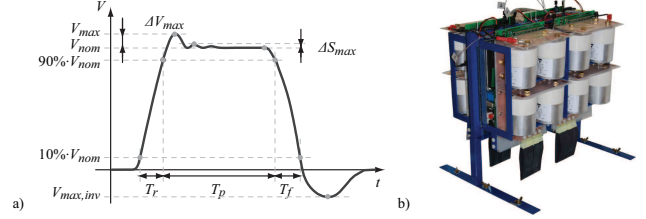


Fig. 1: a) Typical pulse waveform and b) picture of a 20 MW pulse generator. Specifications: Output voltage 170 kV, pulse duration 5  $\mu\text{s}$ , output power 20 MW, rise time < 500 ns and overshoot < 3 %.

parasitic elements  $L_\sigma$  and  $C_d$  is analyzed with a standardized pulse transformer model. During the rise time this model can be simplified, which allows to derive basic design equations concerning rise time and overshoot of the pulse transformer. Out of this, in **section III** different transformer topologies are compared in regard to the fastest achievable rise time. In order to define the mechanical dimensions, the leakage inductance  $L_\sigma$  and the distributed capacitance  $C_d$  are calculated analytically, as was presented in [2]. In **section IV** the influence of the limited switching speed of semiconductors and the nonlinear impedance characteristic of a klystron is evaluated. Experimental results of the built pulse transformer are shown in **section V**.

## II. PULSE TRANSFORMER'S EQUIVALENT CIRCUIT

In literature numerous electrical equivalent circuits considering LF and HF properties of pulse transformers have been proposed and IEEE standardized the equivalent circuit of pulse transformers [3] as shown in Fig. 2 a). In order to simplify the analysis of the transient behavior for operation with rectangular pulse voltages, the standardized equivalent circuit can be reduced to the equivalent circuit shown in Fig. 2 b) during the leading edge if  $n \gg 1$  [4]. Since the pulse rise time  $T_r$  is in the range of some 100ns, the influence of the core material, i.e.  $R_{Fe}$  and  $L_{mag}$ , can be neglected during the rise time.

Therefore, the rise time and the overshoot of the output voltage, are mainly defined by the leakage inductance  $L_\sigma$  and the distributed capacitance  $C_d$ . Assuming an ideal step voltage at the primary, the resulting output voltage  $v_{out}(t)$  can be calculated with the laplace-transform as described in [4].

$$v_{out}(t) = \frac{V_g R_{load}}{R_g + R_{load}} \left[ 1 - e^{-at} \left( \frac{a}{k} \sinh(kt) + \cosh(kt) \right) \right] \quad (1)$$

$$\text{with } k^2 = a^2 - b \quad \text{and}$$

$$2a = \frac{R_g}{L_\sigma} + \frac{1}{C_d R_{load}}, \quad b = \frac{1}{L_\sigma C_d} \left( 1 + \frac{R_g}{R_{load}} \right)$$

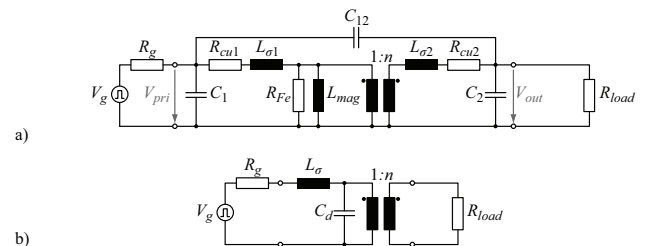


Fig. 2: a) IEEE standardized equivalent circuit of a pulse transformer and b) simplified equivalent circuit during the leading edge

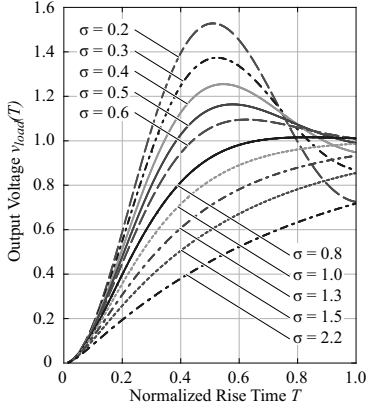


Fig. 3: Transient behavior of the normalized output voltage for different damping coefficients  $\sigma$

where the damping coefficient  $\sigma$  of (1) is given by

$$\sigma = \frac{a}{\sqrt{b}} = \frac{C_d R_g R_{load} + L_\sigma}{2\sqrt{R_{load} L_\sigma C_d (R_g + R_{load})}}. \quad (2)$$

For pulse generators based on capacitor discharge, the generator's impedance  $R_g$  can be neglected. Thus, the damping coefficient  $\sigma$  can be simplified to

$$\sigma = \frac{a}{\sqrt{b}} = \frac{1}{2R_{load}} \sqrt{\frac{L_\sigma}{C_d}} \quad (3)$$

In Fig. 3 the transient behavior of the normalized output voltage during  $T = \frac{\sqrt{b}}{2\pi} t$  is illustrated. A decreasing damping coefficient  $\sigma$  results in a faster rise time  $T_r$ . Starting from  $\sigma < 1$  a tradeoff between  $T_r$  and overshoot is found. Therefore, to achieve a minimum rise time  $T_r$ , the damping coefficient  $\sigma$  has to be selected as small as possible while the resulting overshoot has to be still below the maximum allowed value (cf. Fig. 1).

#### A. Overshoot

Considering (3),  $\sigma$  depends on  $L_\sigma$  and  $C_d$ , i. e. the pulse transformer's mechanical dimensions and on the load impedance  $R_{load}$ . In general,  $R_{load}$ , for example of a klystron, is defined by the application. Therefore, the pulse transformer's mechanical dimensions must be adjusted in order to fulfill the specifications of the pulse. Assuming a klystron load with  $R_{load} = 1500 \Omega$ , for a maximum overshoot of 3% a damping coefficient of  $\sigma = 0.75$  is needed (cf. (3)). Consequently, with a given  $R_{load}$  and  $\sigma$ , the ratio of leakage inductance  $L_\sigma$  and distributed capacitance  $C_d$  is fixed by

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma}{C_d}} \quad (4)$$

#### B. Rise Time

In addition to the overshoot, the rise time  $T_r$  of the output voltage can be derived from (1). As shown in (5),  $T_r$  is proportional to the product of  $L_\sigma$  and  $C_d$ .

$$T = \frac{\sqrt{b}}{2\pi} t, \quad T_r = 2\pi T_{10\%-90\%} \sqrt{L_\sigma C_d} \quad (5)$$

Factor  $T_{10\%-90\%}$  depends on the selected damping coefficient  $\sigma$  and equals the time in which the voltage  $v_{load}(t)$  rises from 10% to 90% (cf. Fig. 3). For  $\sigma = 0.75$  the factor is  $T_{10\%-90\%} = 0.365$ . Since the rise time  $T_r$  is proportional to  $L_\sigma \cdot C_d$ , the parasitics have to be minimized in order to achieve the fastest possible rise time. For example, to keep the rise time below  $T_r = 500$  ns,  $L_\sigma \cdot C_d$  has to be smaller than  $4.75 \cdot 10^{-14}$  if  $\sigma = 0.75$ .

With the assumed load impedance  $R_{load} = 1500 \Omega$ , the ratio of  $L_\sigma$  and  $C_d$  is given and the maximum values of  $L_\sigma$  and  $C_d$  are  $490 \mu\text{H}$  and  $97 \text{ pF}$  respectively for the given specifications (cf. Fig 1).

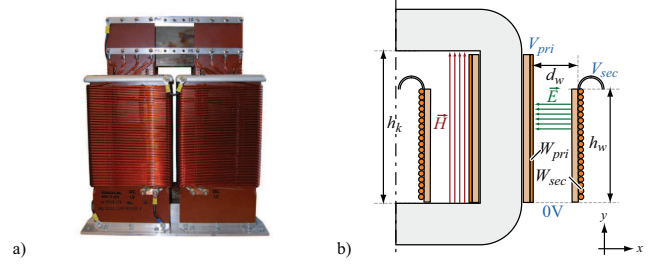


Fig. 4: a) Picture of a pulse transformer with parallel winding and b) 2D drawing of one leg with simplified run of the magnetic and electric field lines.

#### C. Design Criteria

In order to fulfill the requirements for the maximum overshoot and the maximum rise time, both a given ratio of  $L_\sigma$  to  $C_d$  has to be guaranteed and a maximum product of  $L_\sigma$  and  $C_d$  should not be exceeded.

In general, the pulse generator connected to the transformer's primary as well as the load connected to the secondary have a certain inductance  $L_{gen}$  respectively capacitance  $C_{load}$ , which also have to be considered. For example, in the application area, the capacitance of a klystron varies in the range of  $C_{load} = 40 - 120 \text{ pF}$  [5], which means that the capacitance of the transformer must be small to meet the pulse specifications. Therefore, (4) and (5) have to be extended to

$$2R_{load} \cdot \sigma = \sqrt{\frac{L_\sigma + L_{gen}}{C_d + C_{load}}} \quad (6)$$

$$T_r = 2\pi T_{10\%-90\%} \sqrt{(L_\sigma + L_{gen})(C_d + C_{load})} \quad (6)$$

#### III. TRANSFORMER TOPOLOGY

The ratio of  $L_\sigma$  and  $C_d$  can be varied by the mechanical dimensions of the transformer, i.e. the distances, the heights and the lengths of the windings. The product of  $L_\sigma$  and  $C_d$ , however, is defined by the transformer topology and can be assumed to be approximately constant [4]. Therefore, first the transformer topology resulting in the smallest  $L_\sigma C_d$ -product has to be selected. Afterwards, the mechanical dimensions must be calculated to achieve the needed  $L_\sigma C_d$ -ratio.

In the following, the  $L_\sigma C_d$ -product of three different transformer topologies is analyzed. The leakage inductance  $L_\sigma$  and the distributed capacitance  $C_d$  are calculated with the energy stored in the magnetic and electric field.

$$E_{mag} = \frac{1}{2} \mu \int_V \vec{H}^2 dV \equiv \frac{1}{2} L_\sigma \cdot I_{pri}^2 \quad (7)$$

$$E_{elec} = \frac{1}{2} \varepsilon \int_V \vec{E}^2 dV \equiv \frac{1}{2} C_d \cdot V_{pri}^2 \quad (8)$$

To simplify the comparison of the transformer topologies, first, only the energies between the windings are considered. Afterwards, for the transformer topology with the smallest  $L_\sigma C_d$ -product a more detailed calculation of the parasitics is investigated.

#### A. Parallel Winding

Due to the simple construction, the parallel winding topology is widely used. The primary and secondary are wound on two parallel bobbins, whose distance is defined by the required isolation. In Fig. 4 a picture and 2D drawing of the parallel winding are shown.

The leakage inductance is mainly defined by the volume and the magnetic field strength between the bobbins (cf. (7)). According to Ampère's law and assuming an ideal core material ( $\mu = \infty$ ), the magnetic field strength  $\vec{H}$  in the core window is given by the primary current times the number of turns  $N_{pri} \cdot I_{pri}$  and the height of the core  $h_k$ .

$$|\vec{H}| = \frac{N_{pri} I_{pri}}{h_k} \quad (9)$$

Using (7) and (9), the stored magnetic energy  $E_{mag}$  between the windings  $W_{pri}$  and  $W_{sec}$  can be calculated as

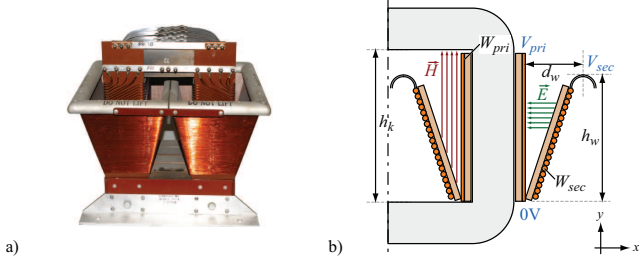


Fig. 5: a) Picture of a pulse transformer with cone winding and b) 2D drawing of one leg with simplified run of the magnetic and electric field lines.

$$E_{mag} = \frac{1}{2} \mu (N_{pri} I_{pri})^2 \frac{l_w \cdot d_w}{h_k} = \frac{1}{2} L_{\sigma} I_{pri}^2, \quad (10)$$

and the resulting leakage inductance  $L_{\sigma,parallel}$  for parallel winding is

$$L_{\sigma,parallel} = \mu \frac{N_{pri}^2 \cdot l_w \cdot d_w}{h_k}. \quad (11)$$

To calculate the distributed capacitance  $C_d$ , a linear voltage distribution  $V_{pri}(y)$  and  $V_{sec}(y)$  is assumed across the windings.

$$V_{pri}(y) = \frac{y}{h_w} V_{pri}; \quad V_{sec}(y) = \frac{y}{h_w} V_{sec} \quad (12)$$

Therewith, the voltage difference between the primary and secondary winding depending on the vertical position  $y$  is  $\Delta V(y) = V_{sec}(y) - V_{pri}(y)$ .

Due to the voltage difference between the windings  $W_{pri}$  and  $W_{sec}$ , the electric field lines run approximately horizontally (cf. Fig. 4 b)). Thus, the electric field  $\vec{E}(y)$  depending on the  $y$ -position is

$$|\vec{E}(y)| = \frac{\Delta V(y)}{d_w} = \frac{V_{pri} \cdot (n-1) \cdot y}{h_w \cdot d_w} \approx \frac{V_{sec} \cdot y}{h_w \cdot d_w}. \quad (13)$$

Considering (8), the stored energy between the windings  $W_{pri}$  and  $W_{sec}$  and therewith the distributed capacitance  $C_d$  are calculated.

$$\begin{aligned} E_{elek} &= \frac{1}{2} \varepsilon \int_0^{l_w} \int_0^{h_w} \int_0^{d_w} \left( \frac{V_{sec} \cdot y}{h_w \cdot d_w} \right)^2 dx dy dz \\ &= \frac{1}{6} \varepsilon V_{sec}^2 \cdot \left( \frac{l_w \cdot h_w}{d_w} \right) = \frac{1}{2} C_d \cdot V_{pri}^2 \end{aligned} \quad (14)$$

$$C_{d,parallel} = \frac{1}{3} \cdot \varepsilon \cdot \left( \frac{N_{sec}}{N_{pri}} \right)^2 \cdot \left( \frac{l_w \cdot h_w}{d_w} \right) \quad (15)$$

Finally, the  $L_{\sigma} C_d$ -product of the transformer topology with parallel windings is

$$L_{\sigma,parallel} C_{d,parallel} = \frac{1}{3} \cdot \varepsilon \mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}. \quad (16)$$

### B. Cone Winding

Since the distance between the windings of the transformer with parallel winding is constant but the voltage is increasing linearly in  $y$ -direction, the electric field between the windings also increases linearly. In order to achieve a constant electric field  $\vec{E}(y)$  the distance between the windings  $d_w$  has to be linearly decreased for smaller voltage differences, which results in an cone winding [4], [6] as shown in Fig. 5.

Compared to the parallel winding, with the cone winding the volume between the windings and therefore also the leakage inductance  $L_{\sigma}$  can be reduced by a factor of two. However, due to the smaller distance between the windings, the distributed capacitance  $C_d$  is increases.

To calculate the leakage inductance  $L_{\sigma}$  of the cone winding, like for the parallel winding, a constant magnetic field in  $y$ -direction

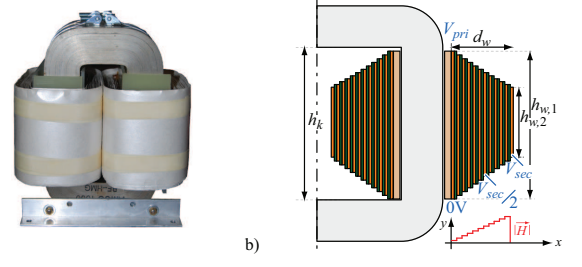


Fig. 6: a) Picture of a pulse transformer with cone winding and b) 2D drawing of one leg.

is assumed (cf. Fig. 5), which was confirmed by FEM-simulation as long as  $d_w \ll h_w$ .

Considering (7), the stored magnetic energy  $E_{mag}$  and the resulting leakage inductance  $L_{\sigma,cone}$  are

$$E_{mag} = \frac{1}{4} \mu (N_{pri} I_{pri})^2 \frac{l_w \cdot d_w}{h_k} = \frac{1}{2} L_{\sigma} I_{pri}^2 \quad (17)$$

$$L_{\sigma,cone} = \frac{1}{2} \cdot \mu \frac{N_{pri}^2 \cdot l_w \cdot d_w}{h_k}. \quad (18)$$

Due to the linearly increasing distance  $d_w(y)$  and the voltage distribution  $\Delta V(y)$  in  $y$ -direction, the electric field  $\vec{E}$  between the winding is constant and runs approximately parallel to the  $x$ -direction (cf. Fig. 5 b)).

Hence, the stored electric energy (8) for a cone winding and the distributed capacitance  $C_d$  are

$$E_{elek} = \frac{1}{4} \varepsilon V_{sec}^2 \cdot \left( \frac{l_w \cdot h_w}{d_w} \right) = \frac{1}{2} C_d \cdot V_{pri}^2 \quad (19)$$

$$C_{d,cone} = \frac{1}{2} \cdot \varepsilon \cdot \left( \frac{N_{sec}}{N_{pri}} \right)^2 \cdot \left( \frac{l_w \cdot h_w}{d_w} \right) \quad (20)$$

Finally, the resulting  $L_{\sigma} C_d$ -product of the cone winding is

$$L_{\sigma,cone} C_{d,cone} = \frac{1}{4} \cdot \varepsilon \mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}. \quad (21)$$

Compared to the parallel winding, with the cone winding the  $L_{\sigma} C_d$ -product of the transformer can be reduced by 25 %, which results in an rise time improvement of 13.4 %.

### C. Foil Winding

Finally, for the primary  $W_{pri}$  and secondary  $W_{sec}$  foil windings are considered. The secondary is directly wound on the primary winding as shown in Fig. 6. For the isolation of the turns a material with a low permittivity is used.

The thickness  $d_{iso}$  of the isolation can be kept small, since the voltage difference between two consecutive turns is just  $V_{w,w} = V_{sec}/N_{sec}$ . However, due to the increasing voltage difference between the turns and the core, the winding's height is linearly decreased from  $h_{w,1}$  to  $h_{w,2}$  (cf. Fig. 6 b)). The total thickness  $d_w$  of the winding is defined by the thickness of the isolation  $d_{iso}$  and the foil  $d_{cu}$  times the number of turns.

The leakage inductance  $L_{\sigma}$  of the foil winding is calculated again with the stored magnetic energy (cf. (7)). Based on Ampère's law, the magnetic field is gradually increasing with the number of turns  $n_L$ , since the enclosed amount of current is increasing gradually (cf. Fig. 6).

$$\vec{H}(n_L) = \frac{n_L I_{sec}}{h_k} \quad (22)$$

The total magnetic energy is the sum of all energies between two consecutive turns, which is

$$\begin{aligned} E_{mag} &= \frac{1}{2} \mu V(n_L) \sum_{n_L=1}^{N_{sec}} \vec{H}(n_L)^2 = \frac{1}{2} \mu \frac{I_{sec}^2}{h_k^2} V(n_L) \sum_{n_L=1}^{N_{sec}} n_L^2 \\ &\approx \frac{1}{4} \mu (N_{pri} I_{pri})^2 \frac{l_w \cdot d_w}{h_k} = \frac{1}{2} L_{\sigma} I_{pri}^2. \end{aligned} \quad (23)$$

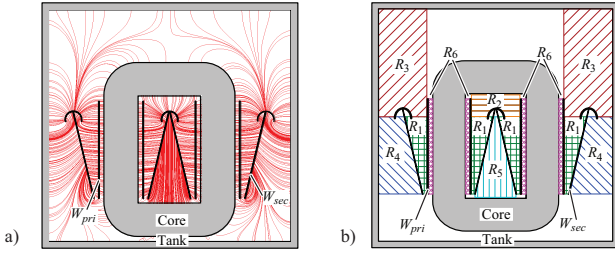


Fig. 7: a) Electric field  $\vec{E}$  of a transformer with cone winding placed in a tank and b) the six relevant regions to calculate the distributed capacitance  $C_d$ .

Thus, the resulting  $L_{\sigma, foil}$  is

$$L_{\sigma, foil} = \frac{1}{2} \cdot \mu \frac{N_{pri}^2 \cdot l_w \cdot d_w}{h_k}. \quad (24)$$

Capacitance  $C_d$  can be calculated as a series connection of parallel-plate capacitors between consecutive turns  $C_{w,w}$ . The distance of the plates equals  $d_{iso}$ , which can be expressed by the total winding thickness.

$$d_{iso} = \frac{d_w}{(k+1) \cdot N_{sec}} \quad \text{where} \quad k = d_{cu}/d_{iso} \quad (25)$$

Assuming a constant winding height  $h_w = (h_{w,1} + h_{w,2})/2$  the distributed capacitance  $C_d$  for the foil winding results in

$$C_{d, foil} = (k+1) \cdot \varepsilon \cdot \left( \frac{N_{sec}}{N_{pri}} \right)^2 \left( \frac{h_w \cdot l_w}{d_w} \right) \quad (26)$$

and the  $L_{\sigma}C_d$ -product is

$$L_{\sigma, foil}C_{d, foil} = \frac{k+1}{2} \cdot \varepsilon \mu \frac{N_{sec}^2 \cdot l_w^2 \cdot h_w}{h_k}. \quad (27)$$

#### IV. EXTENDED PARASITICS CALCULATION

Considering only the stored magnetic and electric energy between the windings  $W_{pri}$  and  $W_{sec}$ , the smallest  $L_{\sigma}C_d$ -product and therefore the fastest  $T_r$  can be achieved for the transformer with a cone winding. Since the considered volume contains the major share of the magnetic and electric energy, the calculated  $L_{\sigma}C_d$ -product is a reliable indicator for the selection of the transformer topology.

However, there is also a magnetic field  $\vec{H}$  and especially an electric fields  $\vec{E}$  between the winding and the core and, if the transformer is placed in a tank, also between the windings and the tank's wall. For example, in Fig. 7 a) the resulting electric field  $\vec{E}$  for a transformer placed in a tank is shown.

For reliably designing the transformer so that it meets the required pulse parameters, also these energies must be considered as could be seen in Fig. 8 a) where a measured and a calculated waveform considering only the energy between the windings is shown. It evidently illustrates the mismatch between measurement and the simple calculation of the parasitics. Since only the electric energy between the windings is considered, the distributed capacitance  $C_d$  is too small and results in a too small overshoot predicted by the transformer model.

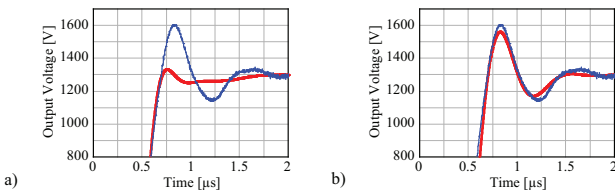


Fig. 8: Comparison of measured and calculated output voltage if a) only the energy between the winding and b) the energy in all regions is considered.

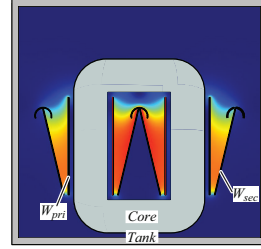


Fig. 9: Magnetic energy density for a pulse transformer with cone winding.

TABLE I: Relative stored electric energy of each region  $R_1 - R_6$  with and without tank.

Region	$R_1$	$R_2$	$R_3$	$R_4$	$R_5$	$R_6$
With tank	22.6%	6.4%	44.4%	25.2%	0.6%	0.8%
Without tank	33.9%	9.6%	44.3%	10.1%	0.9%	1.2%

#### A. Calculation of the Distributed Capacitance

To improve the prediction of the parasitics also the energy outside the windings is considered in the following. As shown in Fig. 7 b), the space around the transformer is divided into six relevant regions  $R_1$  to  $R_6$ . With geometric approximations, the stored energy in each region can then be calculated analytically. In [2] the detailed calculation of the distributed capacitance depending on the mechanical dimensions of the transformer is investigated. The output voltage predicted with the improved model is shown in Fig. 8 b).

For each design, the energies in all regions  $R_1 - R_6$  have to be calculated. With the total electric energy, the distributed capacitance  $C_d$  can be calculated. As an example, in Table I the relative stored electric energy in each region for a transformer with cone winding with and without tank is listed. There, it is assumed, that the distance between the upper end of the secondary winding and the tank is the same as the distance between primary and secondary, which is  $d_w$ .

Table I clearly shows that only about a quarter of the total electric energy is stored between the windings. Considering only  $R_1$ , in practice, the design of the transformer would result in a too large overshoot, since the real distributed capacitance would be much larger than the calculated one.

#### B. Calculation of the Leakage Inductance

Compared to the distributed capacitance  $C_d$ , the calculation of the leakage inductance  $L_{\sigma}$  is more challenging, since there no division into subregions is possible. To precisely calculate the stored magnetic energy, FEM simulations are used. In Fig. 9 the energy density for a pulse transformer with cone winding is illustrated.

The simulation shows, that the major part of the magnetic energy is concentrated in the region between the windings and the magnetic field  $|\vec{H}|$  is almost constant. Therefore, the simple calculation of the leakage inductance  $L_{\sigma}$  in section II (18) already matches the real leakage inductance relatively well. Compared to FEM simulation the relative error of the simple equation is in the range of 10 – 20% if  $d_w \ll h_w$ .

#### V. DESIGN PROCEDURE

As described in section II,  $T_r$  and the overshoot mainly depend on the ratio and the product of the total series inductance  $L_{gen} + L_{\sigma}$  and the total capacitance  $C_d + C_{load}$ . There, the basic equations were derived based on an ideal rectangular input voltage and a resistive load. However, in reality, the switching times of power semiconductors like IGBT modules are in best case in the range of some 100ns. Consequently, due to the reduced voltage slope of the input voltage also the rise time is increased, which results in a decreased overshoot. In addition, the impedance characteristic of the klystron is nonlinear and decreases with voltage, which also leads to an additional damping. Therefore, the influence of these effects has to be analyzed, since the design criteria like the needed damping coefficient  $\sigma$  and the resulting rise time  $T_r$  are changed.

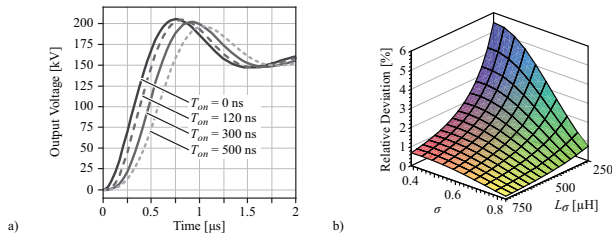


Fig. 10: a) Transient responses for different turn-on times  $T_{on}$  of the semiconductor and b) relative difference in overshoot for a turn-on time of  $T_{on} = 300$  ns.

#### A. Influence of Power Semiconductor Switching Speed

To calculate the influence of the limited switching speed of the power semiconductor on  $T_r$  and the overshoot, the real input voltage is approximated by a trapezoidal voltage. According to section II, the output voltage  $v(t)$  is again calculated with the laplace-transform and the equivalent circuit shown in Fig. 2 b).

In Fig. 10 a) the resulting transient responses of the output voltage for different turn-on times  $T_{on}$  respectively voltage slopes and for  $L_{\sigma} = 250 \mu\text{H}/C_d = 200 \text{ pF}$  are illustrated. Due to the increased  $T_{on}$ ,  $T_r$  is increased whereas the overshoot is decreased.

There, the relative reduction of the overshoot is not only depending on the switching speed  $T_{on}$  and the ratio of  $L_{\sigma}$  and  $C_d$  but also on the absolute values of  $L_{\sigma}$  and  $C_d$  (cf. Fig. 10 b)).

As shown in Fig. 10 a), for  $T_{on}$  in the range of  $\approx 100$  ns the influence of the limited switching speed can be neglected, which in the worst case results in a relative overshoot reduction of less than 0.4%. However, for switching times above  $T_{on} \approx 300$  ns the limited switching speed must be considered (cf. Fig. 10).

#### B. Influence of Nonlinear Klystron Impedance

In general, for the design and the initial operation of the power modulator, the klystron is substituted by an equivalent resistive load  $R_{load}$ . On the one hand, this substitution simplifies the design of the system and on the other hand, the klystron is an expensive and sensitive amplifier, which can be easily damaged during initial tests.

However, for the design of the power modulator, especially of the pulse transformer, the nonlinear impedance characteristic of the klystron has to be considered. As described in [7], [8], the klystron results in an higher damping compared to the equivalent resistance, whereas during the rising edge the damping coefficient changes from 0.6 to 0.9 due to the nonlinear impedance. Therefore, with a klystron load a smaller damping coefficient  $\sigma$  is needed compared to the equivalent resistive load.

According to [7], the klystron's impedance can be written as

$$I_k = k \cdot V_k^{\frac{3}{2}} \quad (28)$$

where  $k$  is the perveance of the klystron.

Considering (28), the klystron current  $I_k$  decreases more than linear with increasing klystron voltage, which results in an decreasing resistance for higher voltages and therefore in an decreasing overshoot compared to a linear load. The resulting transient responses for a klystron load and the resistive load are shown in Fig. 11 a) assuming  $L_{\sigma} = 250 \mu\text{H}$  and  $C_d = 200 \text{ pF}$ . The klystron leads to a significantly reduced overshoot compared to a resistive load.

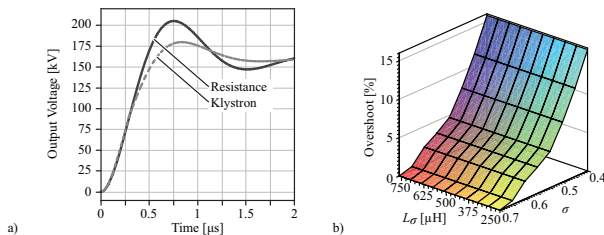


Fig. 11: a) Comparison of the transient responses for a klystron load and a resistive load b) relative difference in overshoot for a turn-on time of  $T_{on} = 300$  ns.

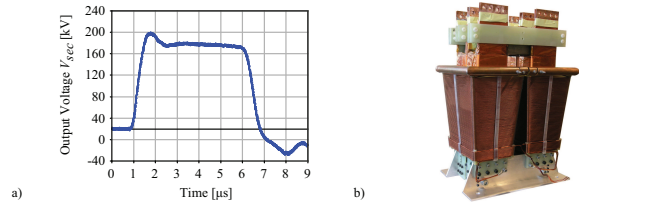


Fig. 12: a) Measured output voltage waveform and b) designed pulse transformer for the specifications given in Fig. 1.

Since the overshoot of 3% is specified for a klystron load, for the equivalent resistive load the pulse transformer has to be designed with an much higher overshoot, which is in this case 11%. Compared to the calculation in section II, the damping coefficient has to be decreased from  $\sigma = 0.75$  to  $\sigma = 0.58$ .

In contrast to the limited switching speed, the influence of the klystron load on the overshoot does not depend on the absolute values of  $L_{\sigma}$  and  $C_d$  but only depends on the damping coefficient  $\sigma$ , as shown in Fig. 11 b).

## VI. EXPERIMENTAL RESULTS

In Fig. 12 the measured output voltage and the built pulse transformer for 20MW power modulator with a klystron load is shown. The measured rise time  $T_r$  is below 500 ns and the overshoot with resistive load is 10.4%. Due to the larger damping, with the klystron the resulting overshoot will be below 3%.

## VII. CONCLUSION

In this paper, a step-by-step design procedure of a pulse transformer for rectangular pulse shapes and a fast rise time is presented. Based on the transformer model, it could be seen that the rise time of transformers is proportional to the product of the leakage inductance  $L_{\sigma}$  and the parasitic output capacitance  $C_d$  of the pulse transformer. This product is calculated for three different transformer topologies: parallel, cone and foil winding concepts and it is shown that with a cone winding the fastest rise time can be achieved.

The resulting overshoot is defined by the  $L_{\sigma}C_d$ -ratio. For the calculation of these parasitics an improved calculation procedure is proposed and validated by measurements.

In addition to the transformer parasitics, also the nonlinear impedance characteristic of a klystron and the limited switching speed of semiconductors have to be considered in the design of the transformer as it is shown in the paper.

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