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# Switching Transient Shaping by Application of a Magnetically Coupled PCB Damping Layer

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## ABSTRACT

An increasing number of power electronic applications require high power density. Therefore, the switching frequency and switching speed have to be raised considerably. However, the very fast switching transients induce a strong voltage and current ringing. In this work, a novel damping concept is introduced where the parasitic wiring inductances are advantageously magnetically coupled with a damping layer for attenuating these unwanted oscillations. The proposed damping layer can be implemented using standard materials and printed circuit board manufacturing processes. The system behavior is analyzed in detail and design guidelines for a damping layer with optimized RC termination network are given. The effectiveness of the introduced layer is determined by layout parasitics which are calculated by application of the Partial Element Equivalent Circuit (PEEC) simulation method. Finally, simulations and measurements on a laboratory prototype demonstrate the good performance of the proposed damping approach.

**Keywords:** High speed switching, Switching transients, Snubbers, Power factor correction

## 1. Introduction

Driven from new application fields (e.g. power electronics in aircrafts [1]) modern power electronic systems have to satisfy extended requirements concerning efficiency, weight and compactness [2]. Therefore the power density of power electronic systems (e.g. active rectifiers) has to be increased substantially. Whereas the size of the active components (switches and diodes) can be minimized by using a low profile power module including all semiconductor dies [3], the size of the passive components (EMI-filter, boost inductor etc.) has to be minimized by increasing the switching frequency.

An optimization of the size of the EMI-filter of a three phase active rectifier e.g. shows that a maximal power density of 24 kW/liter for a system with either Cool MOS or RF MOSFETs can be achieved if a switching frequency of 2.1 MHz is used [4].

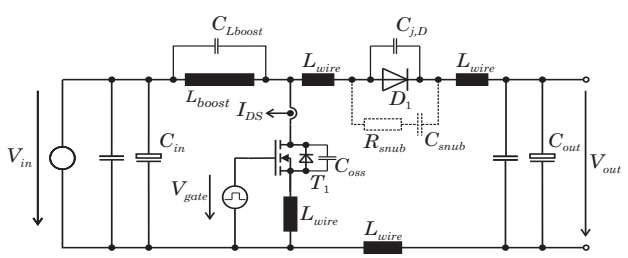


Fig. 1 Schematic of the boost circuit including parasitic elements

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For realizing a switching frequency in the MHz range, a very fast switching transition (voltage slopes of 30 kV/µs and current slopes up to 2 kA/µs) is required.

In Fig. 1 a (hard switched) boost-type test circuit is shown, which is used to analyze the switching behavior of CoolMOS and RF MOSFET devices in combination with SiC-diodes with regard to switching frequencies in the MHz range. Additionally, dominant parasitic elements of the power devices (parasitic capacitances $C_{oss}$ of the MOSFET, $C_{j,D}$ of the boost-diode and $C_{Lboost}$ of the boost inductors) are depicted as well as the wiring inductances $L_{wire}$ of the commutation path. These parasitic elements lead to current and voltage oscillations excited by the very fast switching transients (cf. Fig. 2). The oscillations increase the voltage stress of the semiconductor devices and generate EMI noise.

Basically, the ringing can be reduced by application of snubber circuits (a survey of snubber circuits can be found in [5] and [6]). An easy RC snubber as drawn in Fig. 1 for the boost diode is often used in power electronics to damp unwanted oscillations. Unfortunately, as will be discussed in greater detail in section 2, the losses of such a snubber circuit would be far too high for a switching frequency in the MHz range. At low current levels ferrite beads [7] or amorphous magnetic materials [8] can be used alternatively to limit the di/dt rate at turn-off of the boost diode, but these magnetic devices are not applicable at higher current levels because of their limited power dissipation capability. Furthermore, various diode recovery suppression circuits have been developed [9], but these circuits are also not very well suited for switching frequencies in the MHz range. Specific interconnection concepts with low-pass characteristics based on high-ε-materials have been reported in literature [10], [11]. These approaches, however, are applicable only in case of longer interconnection distances to achieve the desired damping behavior.

Active control of the switching transients, as known from IGBT gate drive circuit research [12], [14], would be an enhanced method for reducing the oscillations. This active control (to be implemented into the gate drive stage of the MOSFET), however, would require a control loop bandwidth in the frequency region of the oscillations to be damped (e.g., typ. 100 MHz for state-of-the-art power MOSFETs) and is therefore no option at present for a discrete realization.

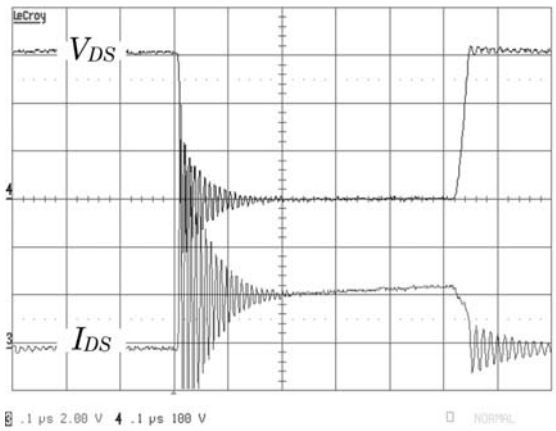


Fig. 2 Current and voltage wave shapes at turn-on of transistor $T_1$ at 20 A, $V_{DS}$ (100 V/div), $I_{DS}$ (20 A/div), time scale 100 ns/div.

In this paper, a novel magnetically coupled damping layer initially introduced in [15] will be proposed to realize the required damping. As shown in Fig. 3 the additional layer is inserted between the two wiring layers. If the copper path of the damping layer winding now is terminated by an appropriately designed RC network, the currents induced in the damping layer will significantly reduce the parasitic oscillations in the wiring layers. An optimized termination network results in a very good damping behavior and much lower losses compared to a classical snubber circuit. Furthermore, the damping network uses standard materials (FR4, copper) and no extra manufacturing processes are needed, which leads to lower realization costs.

In section 2 the proposed damping concept is analyzed in detail using a simple circuit model. Furthermore, the design and optimization of the termination network is given. Subsequently, a laboratory prototype of the mentioned boost converter employing the proposed damping concept is analyzed in detail in section 3. The parasitic wiring elements are calculated using the Partial Element Equivalent Circuit (PEEC) method and compared to measurements of the realized prototype leading finally to a precise model of the system. The resulting voltage and current wave shapes demonstrate the very good performance of the optimized damping.

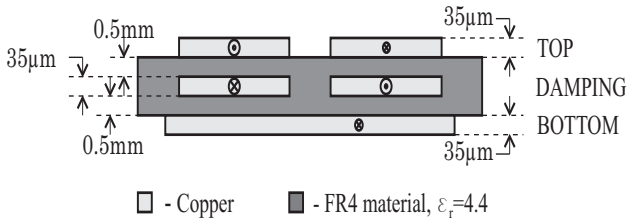


Fig. 3 Layer stack of the system with damping layer

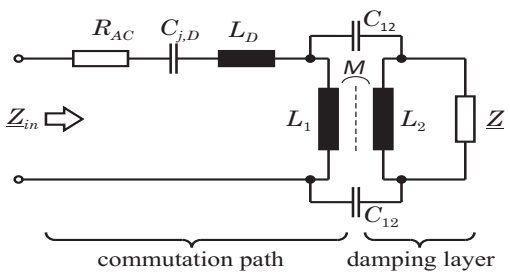


Fig. 4 Model of the circuit at turn-on of the MOSFET with damping layer

## 2. Analysis of the Proposed Damping Layer

The origin of the undesired switching transient oscillations shall be described briefly in the following. At turn-on of the MOSFET $T_1$ the converter's input current has to commutate from diode $D_1$ to MOSFET $T_1$. Since SiC-Schottky diodes are used, there is no reverse recovery current $I_{rr}$. However, a displacement current is charging the voltage dependent junction capacitance $C_{j,D}$ of $D_1$. This capacitance in connection with the wiring inductance $L_{wire}$ forms a series resonant circuit which is damped only by the on-state resistance $R_{DS,\text{on}}$ of $T_1$ and by the high frequency resistance of the wiring.

At turn-off of $T_1$ the input current has to commutate from MOSFET $T_1$ to diode $D_1$ and now the voltage dependent output capacitance $C_{oss}$ of the MOSFET forms a weakly damped series resonant circuit with the wiring inductance $L_{wire}$ of the PCB. In [16], the turn-off behavior of the MOSFET is analyzed and an analytical expression for the turn-off switching transient overvoltage is given. In the following only the behavior of the circuit at turn-on of the MOSFET shall be analyzed for the sake of brevity since the turn off behavior can be treated in a similar way.

In Fig. 4 a simple model for the turn-on behavior of the MOSFET including the damping layer is shown, where the following symbols are used:

- $R_{AC}$ HF-resistance of the wiring in the commutation path;
- $C_{j,D}$ Junction capacitance of the SiC-Schottky diode;
- $L_D$ Parasitic inductance of diode and MOSFET;
- $L_1$ Effective inductance of the commutation path;
- $L_2$ Inductance of the damping layer;
- $M$ Mutual inductance between commutation path and damping layer;
- $C_{12}$ Coupling capacitance between wiring layer and damping layer;
- $Z$ Termination network for damping layer.

Although the inductance of the commutation path can be minimized using a proper layout, a small residual value will remain. An excellent PCB layout offers stray inductances in the range of the parasitic inductances of the diode and the MOSFET. Hence the component parasitics have to be added to the model. Due to skin effect, the current of the high frequency oscillations flows only in a thin layer at the surface of the copper layer and so the HF-resistance $R_{AC}$ has to be considered. Additionally, the skin effect reduces the effective area of the copper "wires" and so the high frequency coupling capacitance $C_{12}$ is reduced to small values so that it can be neglected for sake of an easier modeling. Furthermore, the input inductors parasitic capacitance $C_{Lboost}$ can be neglected because the analyzed oscillations at turn-on of $T_1$ are not directly affected by $C_{Lboost}$.

The natural frequency $f_0$ and characteristic impedance $Z_0$ of the LC-tank at turn-on are given in (1). For SiC-diodes with some 100 pF junction capacitance and some 10 nH stray inductance $f_0$ lies in the 100 MHz range. To achieve a proper damping, the value of the damping resistor in series to the LC-tank has to be in the range of $Z_0$

$$f_0 = \frac{1}{2\pi\sqrt{L_{wire}C_{j,D}}}, \quad Z_0 = \sqrt{\frac{L_{wire}}{C_{j,D}}}. \tag{1}$$

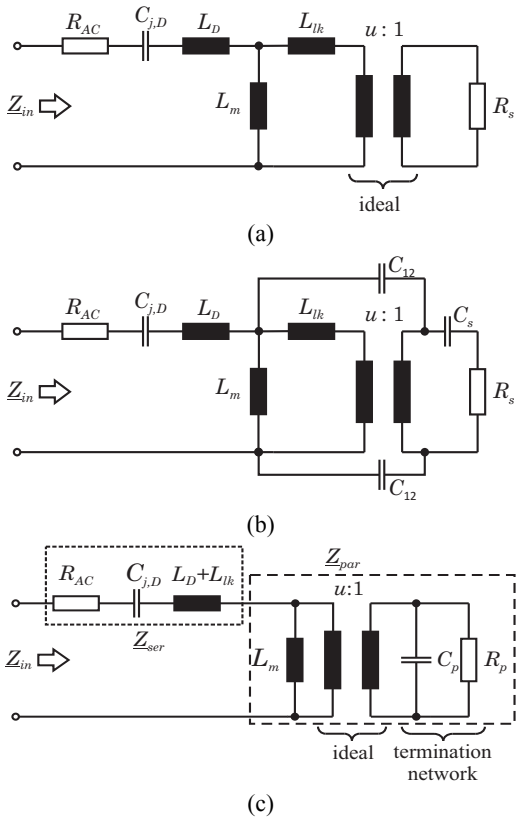


Fig. 5 Equivalent circuits of Fig. 4 for turn-on of the MOSFET for the proposed damping layer realizations (a) Damping by resistive material in the damping layer; (b) series R-C connection and (c) parallel R-C connection (leakage inductance considered on the primary side) as termination network of the magnetically coupled damping layer

With (1), the stray inductance of the commutation path can easily be determined by measuring the frequency of the voltage or current oscillation and by using the junction capacitance $C_{j,D}$ of the diode, specified in the datasheet.

By use of (1), a simple RC-snubber

$$C_{snub} = 3C_{j,D} = 300\,\text{pF}$$
$$R_{snub} \approx Z_0 = \sqrt{\frac{L_{wire}}{C_{j,D}}} = 11.8\Omega \tag{2}$$

can be designed for a SiC-diode with $C_{j,D}$=100 pF and an estimated wiring inductance of $L_{wire}$=14 nH.

According to[5] the power dissipation of the snubber-resistor can be estimated by:

$$P_{R,snub} \approx 2 f_s \frac{C_{snub} V_{out}^2}{2}. \tag{3}$$

If a switching frequency of $f_s$=1 MHz and an output voltage of $V_{out}$=400 V is assumed, the resulting power dissipation of $P_{R,snub}$=48 W emphasizes that RC-snubbers are not applicable advantageously for such high switching frequencies.

### 2.1 Approaches for the termination network

In this section several possibilities for realizing a magnetically coupled damping layer will be discussed.

#### A) Resistive material in damping layer

The idea of this realization is to use resistive material in the damping layer itself. The currents induced in the resistive damping layer generate losses and therefore damp the unwanted oscillations. A model of this approach is shown in Fig. 5 (a). The magnetically coupled damping layer is modeled by the magnetizing inductance $L_m$, the leakage inductance $L_{lk}$ (the full leakage inductance is considered on the secondary side) and an ideal transformer with a ratio of $u$:1. As is well known from coreless transformer designs [17], the magnetizing inductance $L_m$ is quite small as compared to the leakage inductance $L_{lk}$ because of the limited coupling of the layers. Therefore, the major part of the input current is flowing through the magnetizing inductance because

$$\left|X_m\right| = \omega L_m << \left|R_{damp} u^2 + j\omega L_{lk}\right|, \tag{4}$$

which results in a limited damping effect. The inductance $L_m$ (and hence the coupling of the two layers) could be increased using a ferrite core or a magnetic layer as done in [18]. However this also raises the inductance of the commutation path and, therefore, is no option in the case at hand. Beside the limited damping capability of this approach the demand of including resistive materials into the layer stack of the PCB is a drawback. Additional materials and production steps are required which results in significantly higher production costs of the PCB.

### B) Series R-C connection

The unwanted leakage inductance can be compensated if a well designed capacitor $C_s$ is placed in series to the resistor $R_s$ (cf. Fig. 5 (b)). This capacitance in connection with the leakage inductance $L_{lk}$ forms a series resonant circuit, which has to be tuned to a resonant frequency being equal to the oscillations to be damped. However, simulations of the proposed system showed that the coupling capacitance $C_{12}$ can not be neglected in this case and that even a very small coupling capacitance of a few pF overrides the positive effect of canceling the leakage inductance. The best results have been achieved by using a parallel connection of R and C as termination network which will be discussed in the following.

### C) Parallel R-C connection

As can be seen in Fig. 5 (c) the series resonant circuit, formed by $C_{j,D}$ and the sum of the inductances $L_{lk}$ and $L_D$, is connected in series with a well damped parallel resonant circuit, formed by the termination network and the inductance $L_m$. The two elements $C_p$ and $R_p$ have to be transferred to the primary side considering $u$:

$$C'_p = \frac{C_p}{u^2}, \qquad R'_p = R_p \cdot u^2. \tag{5}$$

If the natural frequency $f_{par}$ of the parallel resonant circuit is chosen according to

$$f_{par} = \frac{1}{2\pi\sqrt{L_m \cdot C'_p}} = f_{ser} = \frac{1}{2\pi\sqrt{(L_D + L_{lk}) \cdot C_{j,D}}} \tag{6}$$

leading to

$$C_p = \frac{L_D + L_{lk}}{L_m} C_{j,D} \cdot u^2 \quad , \tag{7}$$

and the damping resistor is chosen to

$$R_p \cdot u^2 = R'_p \approx Z_1 = \sqrt{\frac{L_D + L_{lk}}{C_{j,D}}} \quad , \tag{8}$$

the damping of the resulting system can be increased significantly. A Bode plot of the input impedance is given in Fig. 6. The damping of the system is increased when the magnitude of the input impedance is increased at the resonant frequency.

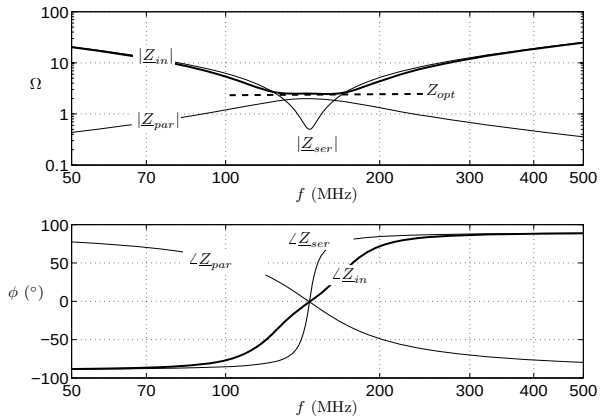


Fig. 6 Calculated Bode diagram of impedances $Z_{ser}$, $Z_{par}$ and $Z_{in}$ for the system: $L_1$=10 nH, $L_2$ = 10 nH, $M$ = 5 nH, $L_D$ = 6 nH and $C_{j,D}$ = 136 pF

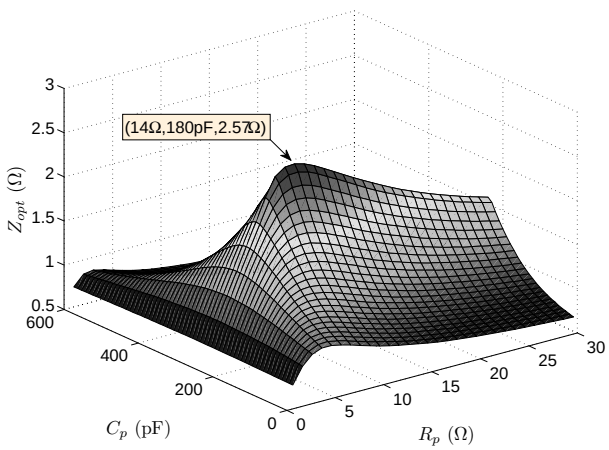


Fig. 7 Calculated magnitude of impedance $Z_{opt}$ as a function of the termination network parameters $R_p$ and $C_p$

$$\underline{Z}_{in} = \underline{Z}_{ser} + \underline{Z}_{par} \quad \text{with} \tag{9}$$

$$\underline{Z}_{ser} = \frac{1 + sR_{AC}C_{j,D} + s^2 C_{j,D}\left(L_D + L_{lk}\right)}{sC_{j,D}} \quad \text{and} \tag{10}$$

$$\underline{Z}_{par} = \frac{sL_m}{1 + s\frac{L_m}{R'_p} + s^2 L_m C'_p} \tag{11}$$

Since (8) is only an approximation, the optimal values for a maximal damping can be found by application of the following optimization function:

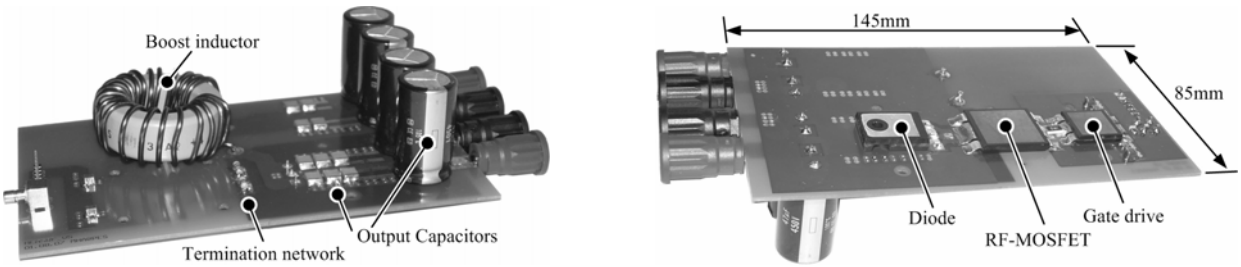


Fig. 8 Realized prototype of the boost circuit with PCB board wiring including a damping layer with optimized termination network. (a) TOP view and (b) BOTTOM view of the prototype which can directly be mounted on a heatsink.

$$Z_{opt} = \left| \underline{Z}_{in}\left(f, C_p, R_p\right) \right| \Big|_{\arg(\underline{Z}_{in}(f))=0^\circ} \rightarrow \max . \qquad (12)$$

The result of the optimization for an assumed system with the parameters $L_1 = 10$ nH, $L_2 = 10$ nH, $M = 5$ nH, $L_D = 6$ nH and $C_{j,D} = 136$ pF is depicted in Fig. 7 and the results are summarized in Table 1.

Tabel 1 Calculated values for the termination network according to (7) and (8), and results of the optimization according to (12).

| | $R_p$ | $C_p$ |
|---|---|---|
| Calculated values | 9 Ω | 186 pF |
| Result of optimization | 14 Ω | 180 pF |

## 3. Design of a Damping Layer

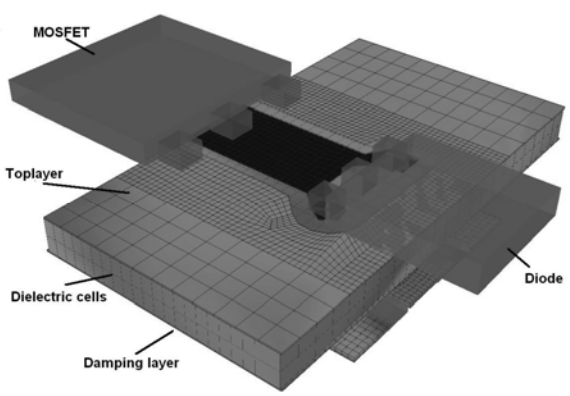


Fig. 9 PEEC model of the realized prototype with damping layer

### 3.1 Design of the realized prototype

The design of the damping layer is verified using a boost converter as design example (cf. Fig. 1). This circuit is also used to study the switching behavior of different MOSFET devices. To achieve very fast switching transients, a low impedance gate driver DEIC420 featuring a peak current capability of over 20 A is used. For the boost diode $D_1$ a 600 V SiC-Schottky diode CSD20060D is used; output capacitance $C_{out}$ and also input capacitance $C_{in}$ are partly realized by several 220 nF / 630 V ceramic type SMD capacitors, providing high current capability and low inductance.

In [19], it is shown that the switching losses are dominated by the intrinsic capacitance $C_{oss}(V_{DS})$ of the MOSFET when very fast switching is realized. Because of the low $R_{DS,on}$ of the CoolMOS SPW47N60C3 and its low output capacitance $C_{oss}$ at $V_{DS} = 300$ V, a superjunction power MOSFET seems to be an ideal choice for high speed switching. Unfortunately, as shown in [20], $C_{oss}$ rises from a few 100 pF to over 10 nF for very low blocking voltage levels. This results in long "delay times" at turn-off of the device, finally leading to significant current distortions for lower current values in single phase and three phase active rectifier applications. To overcome this drawback a RF switch-mode power MOSFET DE475-501N44 is used. This device shows a much less pronounced $C_{oss}(V_{DS})$-characteristic than superjunction MOSFETs. Additionally, the RF MOSFET utilizes a DE475 package which is optimized for high speed, high frequency, high power applications (Fig. 8). Because of the symmetrical package design, where the two source terminals lie on either side of the drain terminal, the

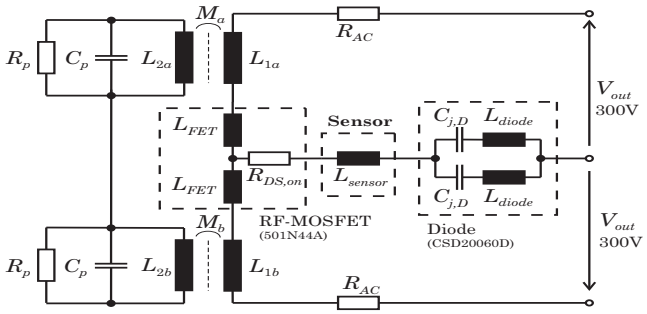


Fig. 10 Simplified model of the realized prototype with damping layer including parasitic elements of the RF-MOSFET, current sensor and the SiC-diode

parasitic inductance of the device can be reduced to less than 5 nH [21]. Due to the two source terminals two commutation paths have to be also considered. The layout of the boost circuit is optimized for very low wiring inductances in the commutation path. To form the proposed damping structure a copper loop (terminated by the proposed RC-network) is routed in a layer that is between the two wiring layers (cf. Fig. 3).The MOSFET current $I_{DS}$ is measured using a self-made AC-current probe. A short wire is required for inserting the current sensor into the circuit, resulting in an additional inductance of approximately 8 nH for the commutation path which has to be considered in the model of the damping circuit.

### 3.2 Design of the Damping Layer using PEEC-method

For designing an optimal termination network of the damping layer, the parasitic elements of the system have to be considered. These elements could be determined by impedance measurements on the realized hardware using an adequate impedance analyzer. However, due to the fact that such measurements in the pF / nH-range are rather difficult, an alternative method to determine the parameters in an early state of system design based on simulation without building a dedicated prototype shall be used.

For a simulation including layout parasitics, the PEEC method emerged as a computational effective and accurate technique [22], [23]. Here, the PCB layout is discretized into a large number of individual elements as shown in the 3D-model of the prototype layout (cf. Fig. 9). The PEEC method creates matrices of partial elements representing the magnetic and electric field couplings and the resulting equations subsequently are solved in a Spice-like circuit simulator. Recent development makes PEEC an integrated full wave method, which can handle non-orthogonal elements [24] as well as dielectrics [25].

Table 2 Measured and simulated parasitics of the realized prototype

| | Measurements (HP4294A) | Simulation (PEEC method) |
|---|---|---|
| $L_{diode}$ | 10.9 nH (per diode) | - |
| $C_{j,D}$ | 55 pF | - |
| $L_{FET}$ | 4 nH (per lead) | - |
| $L_{sensor}$ | 8 nH | - |
| $R_{AC}$ | 500 mΩ | - |
| $L_{1a}$ / $L_{1b}$ | 8.2 nH / 7.7 nH | 11.3 nH / 10.5 nH |
| $L_{2a}$ / $L_{2b}$ | 9.9 nH / 8.1 nH | 11.5 nH / 10.6 nH |
| $M_a$ / $M_b$ | 5 nH / 5.25 nH | 6.4 nH |

In Table 2 both simulation results of the PEEC method and measurement results, using the impedance analyzer HP4294A, are summarized. The difference between the measured and calculated layout inductances $L_{1i}$, $L_{2i}$ and $M_i$ has its origin in the measurement technique, which poses a challenge due to the compact geometry of an optimized layout. Since all parameters of the prototype are identified, a simplified model of the boost circuit can be drawn (cf. Fig. 10). Using the optimization of (12) results in $R_{p,opt}$= 22 Ω and $C_{p,opt}$= 184 pF for the termination network. The optimized components of the termination network are added to the PEEC model.

The capacitive coupling $C_{12}$ between the proposed damping layer and the circuit layout, which is neglected for the sake of easy modeling in section 2, lowers the damping performance. Due to the distributed nature of this

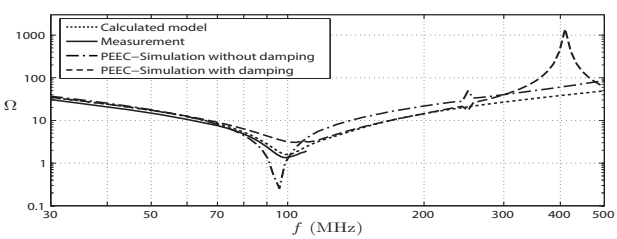


Fig. 11 Impedance measurement, calculated impedance using (9) – (11) and corresponding PEEC simulation of the commutation path, including the effect of the damping layer

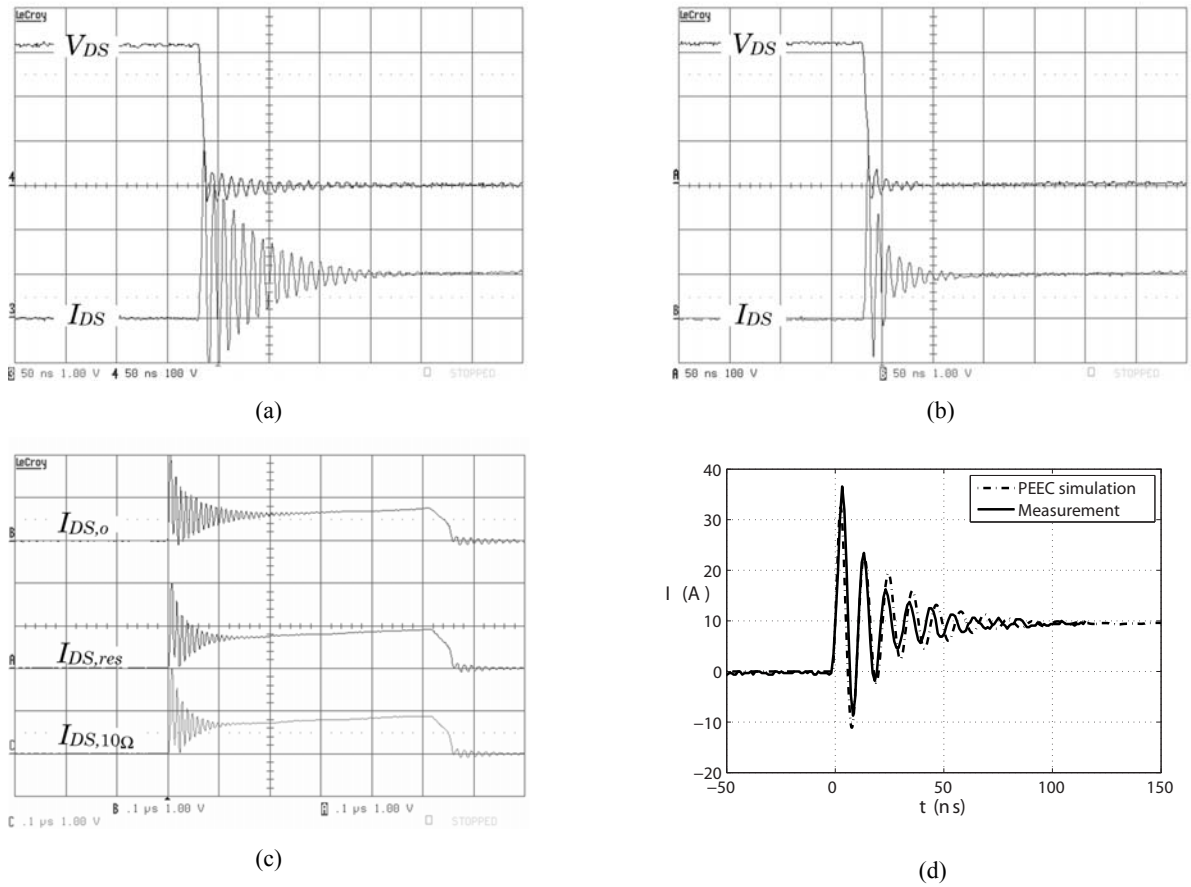


Fig. 12 Measurement results taken from the realized prototypes; (a) Measurement without damping layer and (b) with damping layer terminated with an optimized RC-network. $V_{DS}$ (300 V/div), $I_{DS}$ (10A/div), time scale 50 ns/div; (c) Purely resistive damping layer: $I_{DS,i}$ (10A/div), time scale 100ns/div; (d) Measured and calculated current shape obtained from a numeric Laplace transform of the impedance curve of Fig.11 .

parasitic capacitance it can not accurately be modeled by a single capacitor. Additionally, it's difficult to determine $C_{12}$ by measurement because of its small value in the pF-range. The PEEC method considers the distributed nature [26] and was thus used to verify the total effectiveness of the proposed layout, including the dielectric of the FR4 material with $\varepsilon_r = 4.4$, and a dissipation factor of $\tan \delta = 0.02$.

The simulated total impedance of the commutation path with optimized damping network, including the dielectric properties of the FR4 material ($\varepsilon_r = 4.4$), is depicted in Fig. 11. There is also an impedance measurement included, taken from the realized prototype, as well as the calculated impedance of the simplified model of Fig. 10. The measurements could only be performed up to 110 MHz due to the bandwidth limitation of the used impedance analyzer HP4294A. Comparing the simulation result without damping circuit to the results with optimized termination network ($R_{p,opt}$, $C_{p,opt}$) the damping effect on the resonance at 100 MHz is apparent. Additionally, a small shift in resonance frequency to a higher value is observed when the damping network is applied, which is due to the lowered inductance, since the magnetic fields of both layers attenuate each other. The resonance due to $C_{12}$ is above 400 MHz and has therefore not a significant influence on the ringing behavior at 100 MHz. Additionally, the PEEC simulation showed that the dielectric dissipation inside the FR4 material does not alter the damping behavior significantly. Therefore, it is reasonable to neglect dielectric loss effects in the model.

Hence, the entire effectiveness of the proposed damping layer and the validity of the simplified model of Fig. 10

are approved by PEEC simulation, even though the impedance analyzer measurement in Fig. 11 shows a slightly alleviated damping performance compared to the PEEC simulation. This deviation probably has its origin either in measurement errors of the small parasitic inductance values or the fact that the parasitic inductances of the switch and the diode were included as lumped inductances in the PEEC model, which do not couple magnetically with the layout inductances of the model. However, the similarity of simulation and measurement is acceptable, but also the simplified model with lumped elements shows good results.

## 4. Experimental Results

The realized prototype with optimized damping network has been tested for a boost converter output voltage of 300 V and for current levels up to 20 A. The results for a current of 10 A are given in Fig. 12 (for Fig. 12 (a) the damping layer of the PCB has been left open). It can be seen that the switching transient oscillations are reduced significantly using the damping layer. Although the first voltage/current peak is still present, the decay of the ringing is enhanced noticeably. In Fig. 12(c) a measurement of a purely resistive terminated damping layer is shown. For realization, a 0.2 mm transformer sheet is inserted between the two wiring layers with the thickness of 0.5 mm. The drain-source current $I_{DS,res}$ (with inserted transformer sheet) is compared to a measurement without any damping $I_{DS,o}$ and the measurement results confirm the limited damping capability of this approach. Additionally, the damping effect of a copper layer terminated by a 10 Ω resistor is shown ($I_{DS,10\Omega}$).

The time domain response of the commutation path exited by a step function is calculated based on the simulated impedance curve. In Fig. 12 (d) the numerical result of this transformation is compared to a current measurement taken from the realized prototype for a current of 10 A (the amplitude of the input step of the numerical system is scaled to obtain an equal final value). The oscillation frequency of the simulated system is slightly smaller compared to the measured value which can also be seen at the lower resonance point in Fig. 11.

The simulated maximum peak current and especially the damping effect, however, are in good agreement with the measurement results. Consequently, a PEEC simulation can be used to directly analyze the performance of the designed damping system in an early development state with good precision.

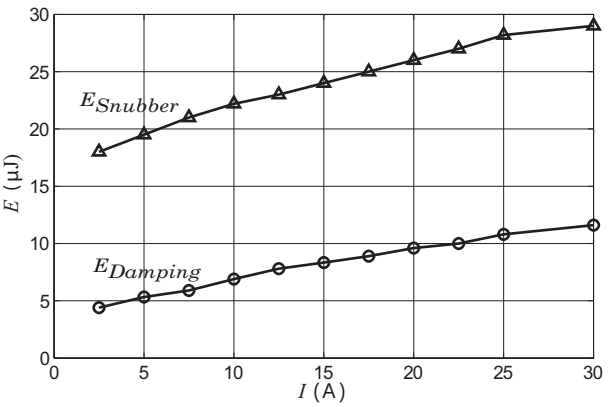


Fig. 13 Measured loss-energies of the proposed damping concept ($E_{Damping}$) compared with the loss-energies of a RC-snubber ($E_{Snubber}$) designed to achieve similar damping.

In Fig. 13 measured loss-energies of the damping resistors for the magnetically coupled damping layer are compared to losses generated by a RC snubber across the boost diode (cf. Fig. 1, $R_{snub}$=10 Ω, $C_{snub}$=150 pF). The measurements were done at $V_{out}$=300 V and the RC snubber is designed to achieve roughly the same damping behavior as the damping layer with optimized termination network. For the tuned damping layer with parallel RC-termination only the high frequency oscillations are coupled to the damping resistor in the termination network. On the contrary, the snubber capacitor $C_{snub}$ has to be charged / recharged in every switching cycle which results in significantly higher losses. This confirms that considerably damping can be achieved with the proposed damping layer by only moderate losses in the damping resistor even at switching frequencies in the MHz range.

## 5. Conclusions

In this paper a new passive damping layer is introduced for damping the undesired voltage/current ringing appearing at the switching instants of hard-switched power electronic converters. An additional copper layer,

terminated by an optimally designed RC-network, is inserted between the PCB wiring layers of the converter. A very simple model describing the overall system behavior, as well as design guidelines for the damping layer and the RC-termination network are given. The design and performance of the proposed damping layer is shown for a realized boost-converter circuit but the approach is also applicable to other converter topologies. For the arrangement and the optimization of the termination network, impedance measurements of the realized PCB would be necessary. It is shown that by application of the PEEC simulation method the system can be designed and analyzed in an early development state without an existing hardware prototype. Measurements, taken from the realized prototype show, that the switching transient oscillations can be reduced approximately as for application of RC snubbers. However, the proposed concept features significant lower dissipative losses.

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