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fraza Fraza d.o.o.

# Approaches to Overcome the Google / IEEE Little-Box Challenges

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**All Team Members of ETH Zurich/Fraunhofer/Fraza**

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# Outline

- The Google Little Box Challenge
- Selection of Converter Topology / Modulation Scheme
- *Components / Building Blocks*
- *3D-CAD Construction*
- *Experimental Results*
- Conclusions

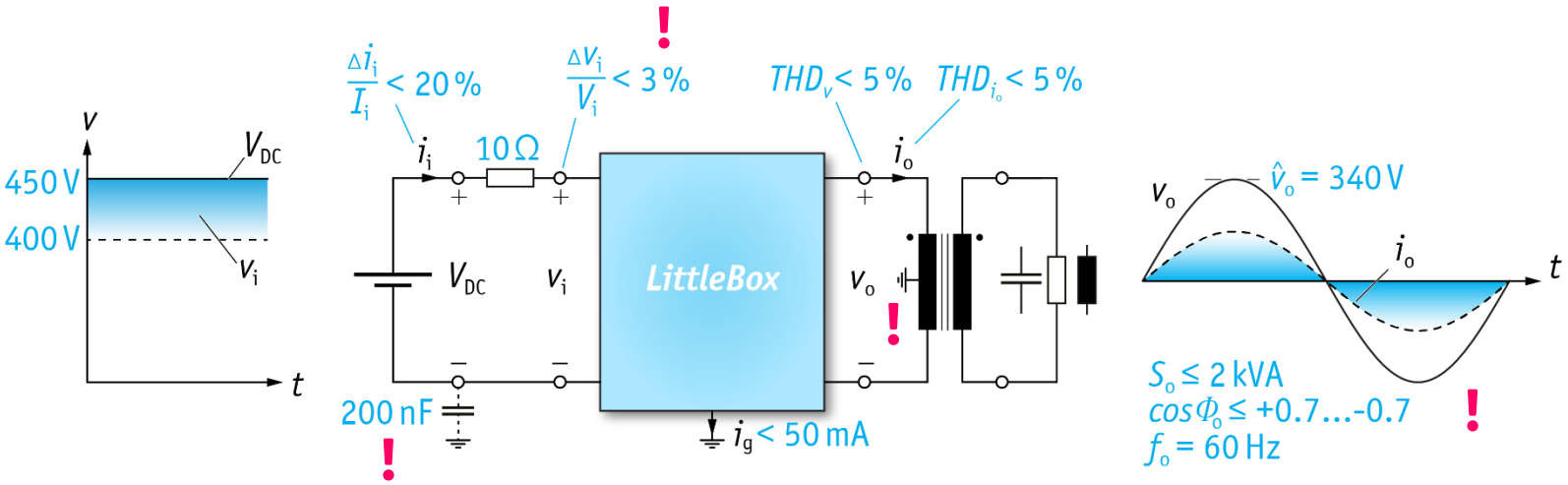
# The Google Little Box Challenge

*Requirements*
*Grand Prize*
*Team* →

# LiTTLE BOX CHALLENGE

Google | IEEE

- Design / Build the 2kW 1-ΦSolar Inverter with the Highest Power Density in the World
- Power Density > 3kW/dm³ (50W/in³)
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B




- Push the Forefront of New Technologies in R&D of High Power Density Inverters

# LiTTLE BOX CHALLENGE

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■ Push the Forefront of New Technologies in R&D of High Power Density Inverters

# The Grand Prize

- **Highest Power Density (> 50W/in$^3$)**
- **Highest Level of Innovation**

**$1,000,000**

- Timeline
  - Challenge Announced in Summer 2014
  - 650 Teams Worldwide
  - 100+ Teams Submitted a Technical Description until July 22, 2015
  - **18 Finalists / Presentation @ NREL on Oct. 21, 2015, Golden, Colorado, USA**
  - Testing @ NREL, Colorado, USA / Winner will be Announced in Early 2016

# Multi-National Team

- Switzerland
- Germany
- Slovenia

ETH zürich

Fraunhofer IZM

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■ Acknowledgment

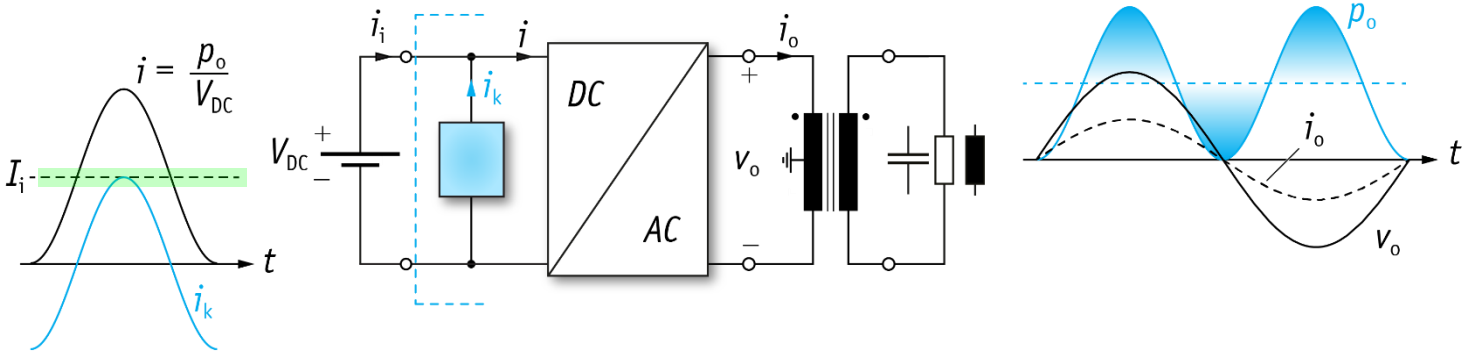
Infineon EPCOS TDK

- **Converter**
  - Topology
  - Modulation
  - Control →

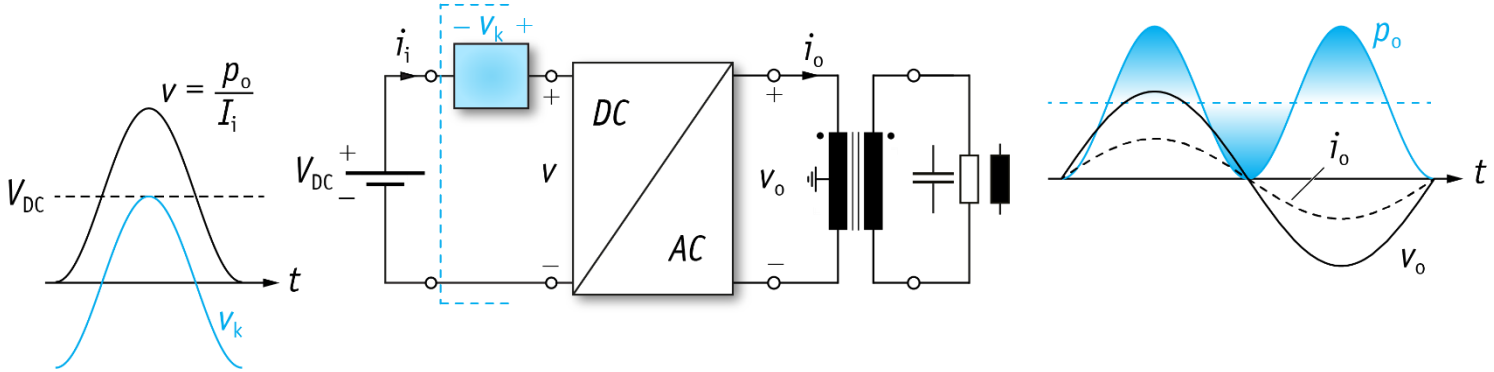
## *1-Φ Power Pulsation Buffer*

# Power Pulsation Buffer (1)

- **Parallel Buffer @ DC Input**



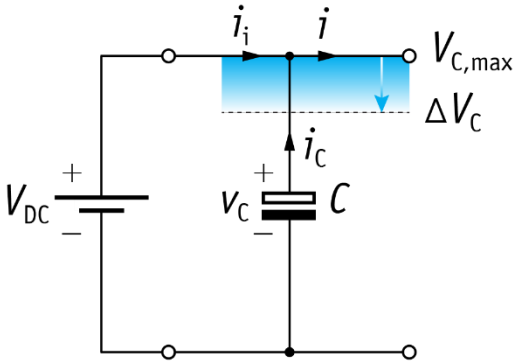

- **Series Buffer @ DC Input**

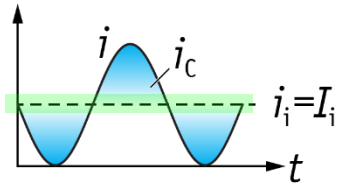


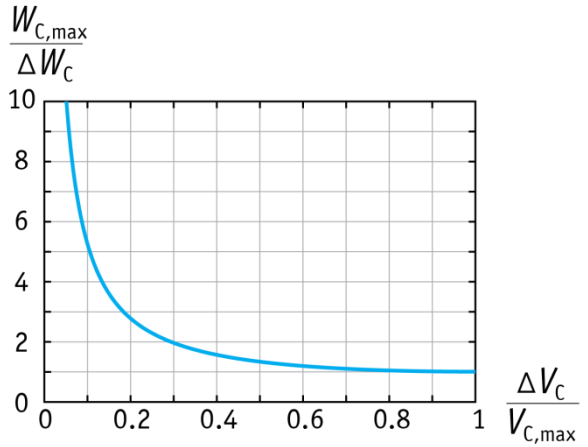

- **Parallel Approach for Limiting Voltage Stress on Converter Stage Semiconductors**

# Power Pulsation Buffer (2)

- Electrolytic Capacitor



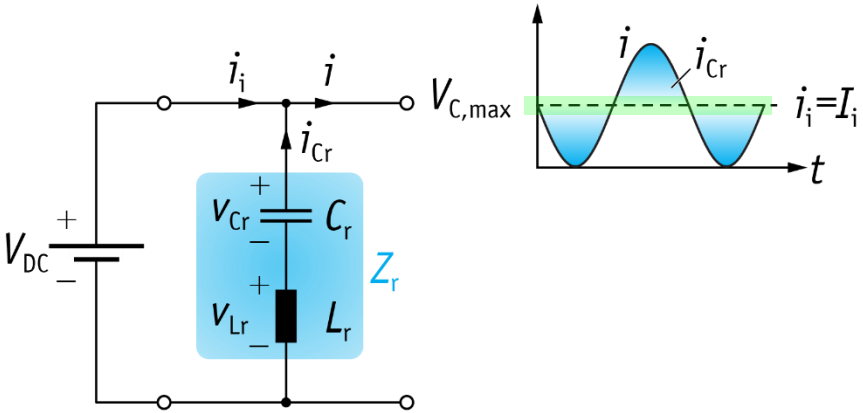



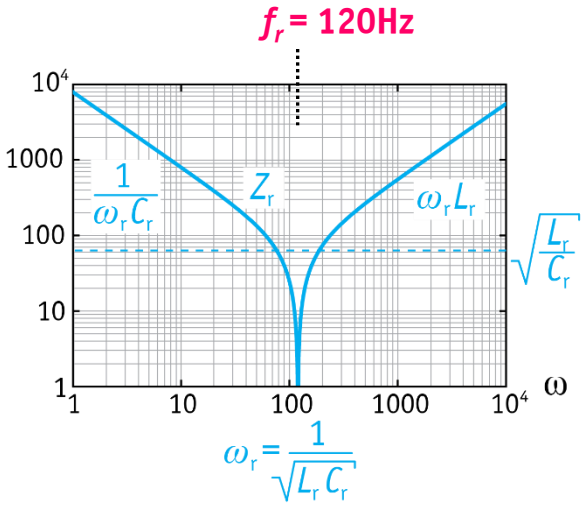

$S_0$ = 2.0 kVA
cos $\Phi_0$ = 0.7
$V_{C,max}$ = 450 V
$\Delta V_C / V_{C,max}$=3 %

- C > 2.2mF / 166 cm³ → Consumes 1/4 of Allowed Total Volume !

# Power Pulsation Buffer (3)

- Series Resonant Circuit / Used in Rectifier Input Stage of Locomotives



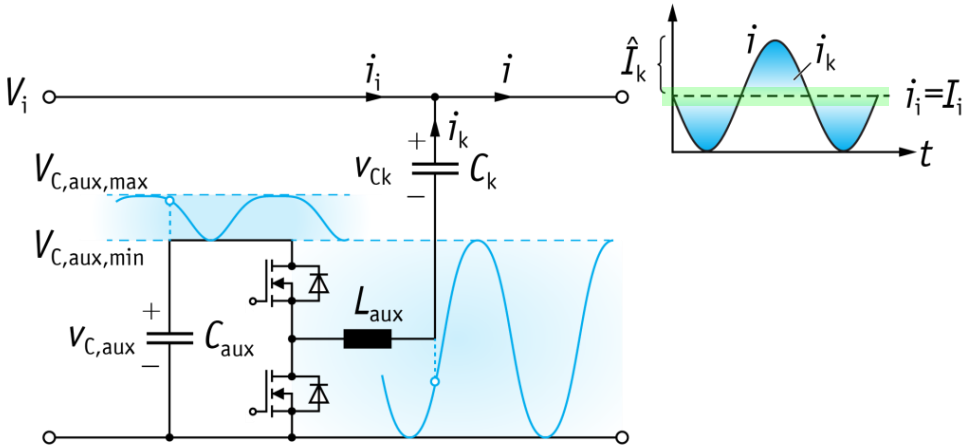



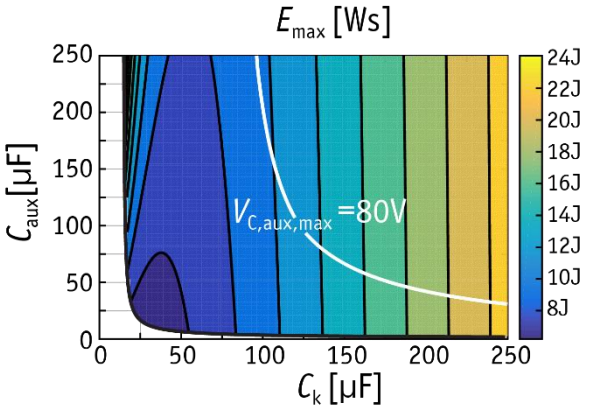

→ $C_r$ = 20 µF
→ $L_r$ = 127 mH @ $v_{Lr}$ = 400 V

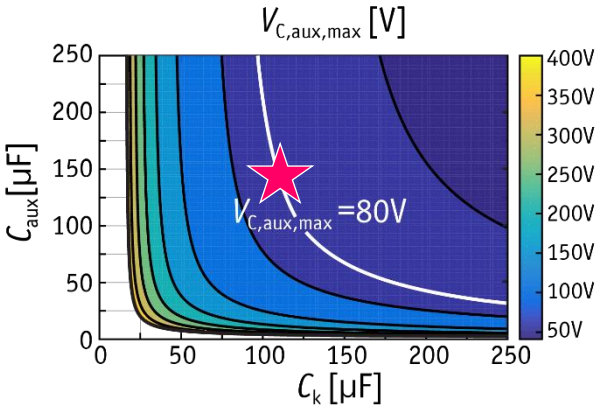
- Unacceptably Large Inductor Volume !

# Power Pulsation Buffer (4)

- Coupling Capacitor & Electronic Inductor



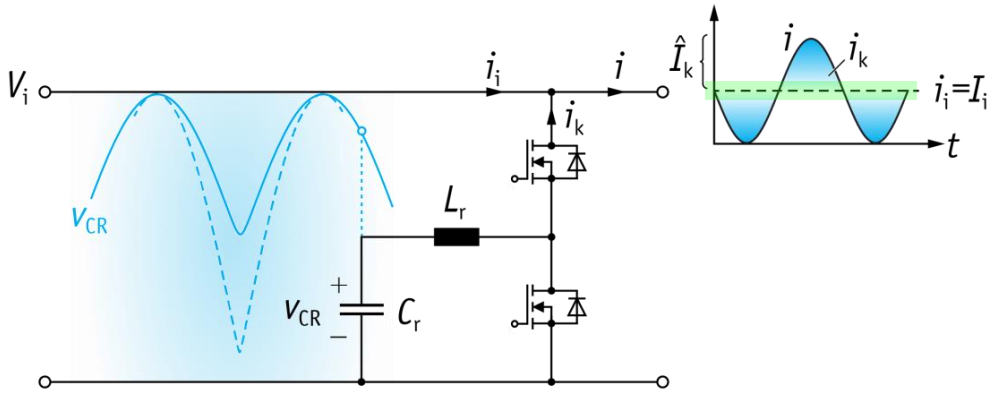




- Low $U_{C,aux}$ → Low Converter Losses
- High Values of $C_K$, $C_{aux}$ Required for Low $U_{C,aux}$
- Full-Bridge Aux. Converter Allows Lower $U_{C,aux}$

▲ Properties of Full-Bridge Aux. Conv.

# Power Pulsation Buffer (4-a)

- Large Voltage Fluctuation Capacitor & DC/DC Buck (Boost) Converter Stage
- Foil or Ceramic Capacitor



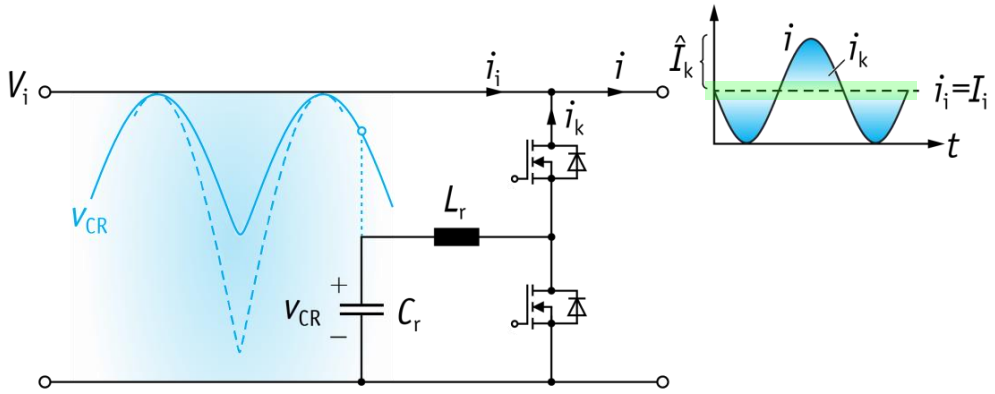

CeraLink TDK

108 x 1.2µF /400 V
$C_r \approx 140\mu F$
$V_{Cr} = 23.7cm^3$

- Very Good Compromise → $C_r$ - Volume / Power Electronics Complexity

# Power Pulsation Buffer (4-b)

- Large Voltage Fluctuation Capacitor & DC/DC Buck (Boost) Converter Stage
- Foil or Ceramic Capacitor




EPCOS
5 x 493µF/450 V
$C$= 2.46 mF

$V$= 48 cm$^3$

$V$= 166 cm$^3$

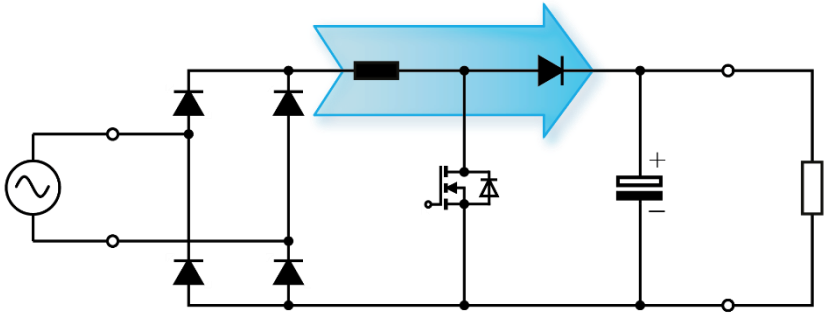
- Significantly Lower Volume Compared to Electrolytic Capacitors

## *Output Stage*
## *Topology / Modulation*

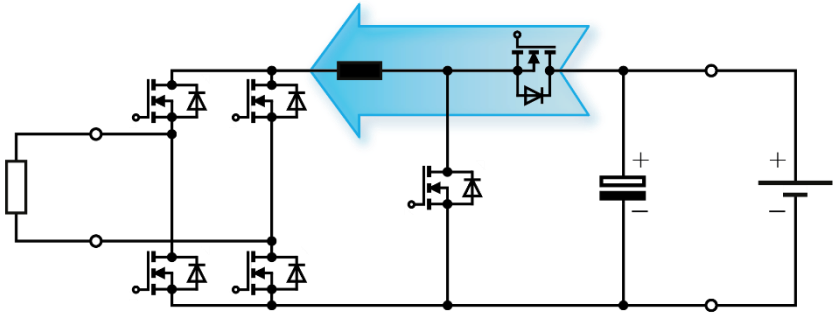
# Derivation of Output Stage Topology (1)

- **Inversion of Basic 1-Φ PFC Rectifier Topology**

– Boost-Type
1-Φ PFC Rectifier



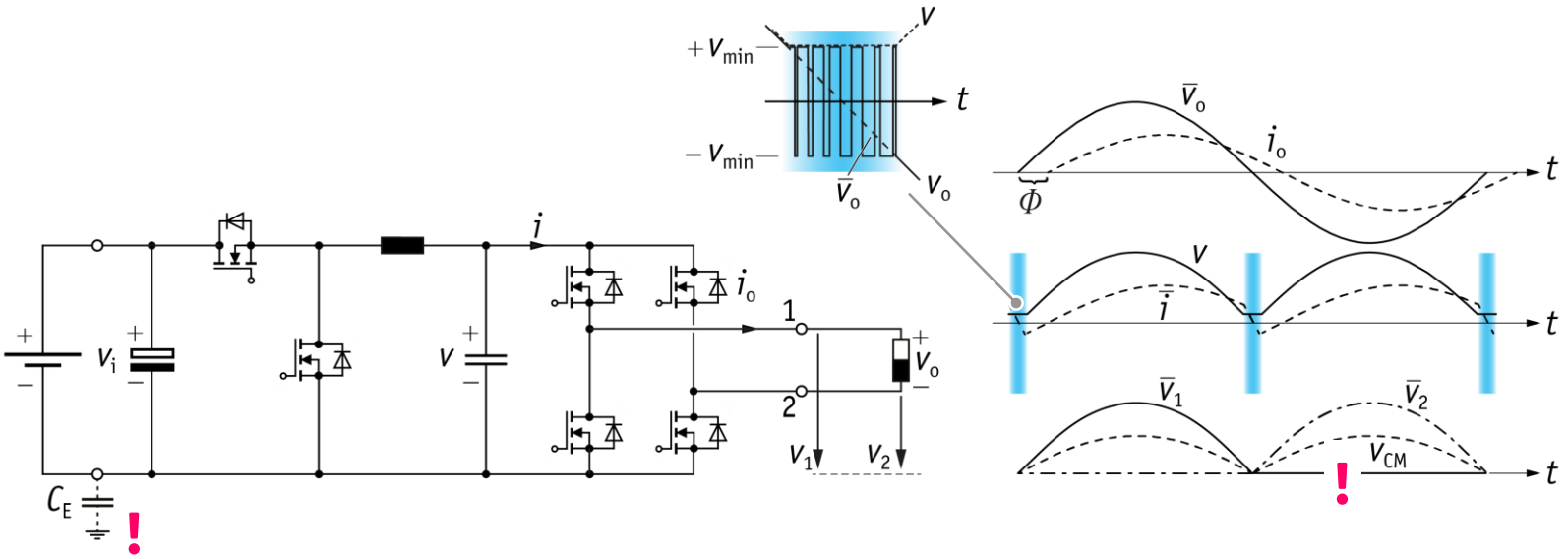
– DC/DC Buck Converter &
Mains Frequency "Unfolder"



- **Low-Frequency "Folder/ Unfolder" vs. PWM Operation of Output Stage**

# Derivation of Output Stage Topology (2)

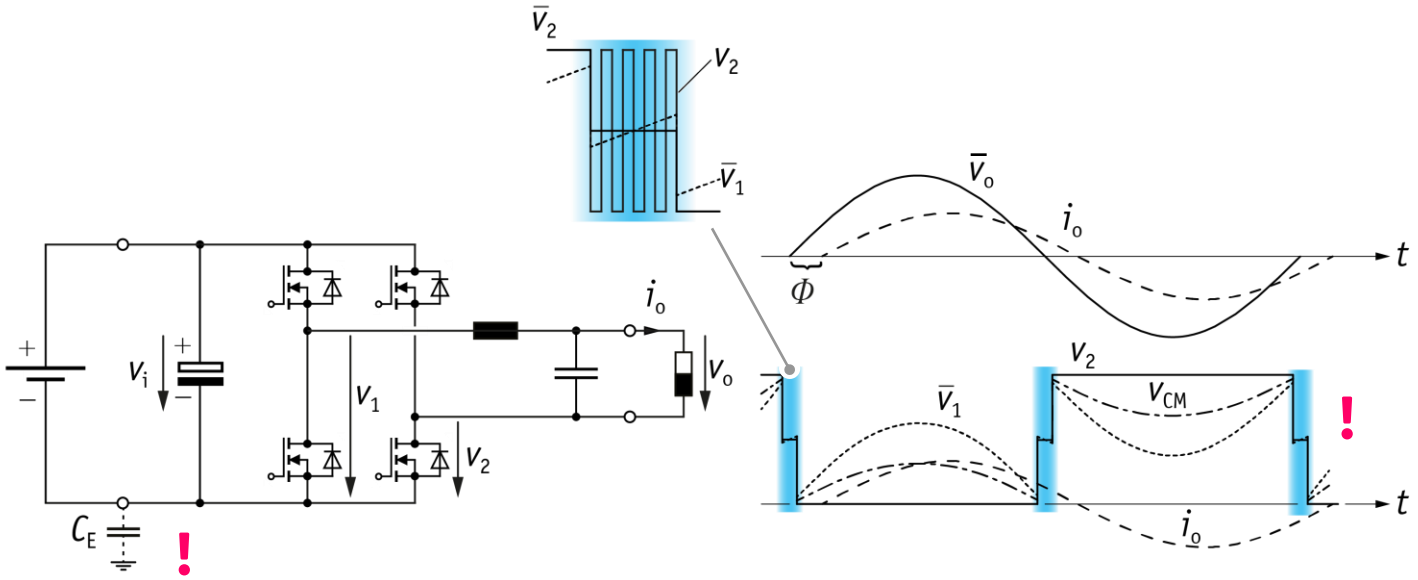
- DC/DC Buck Converter & Output Frequency "Unfolder"




- PWM Operation of Mains Frequency Inverter @ $U < U_{min}$
- CM Component of Generated Output Voltage

# Derivation of Output Stage Topology (3)

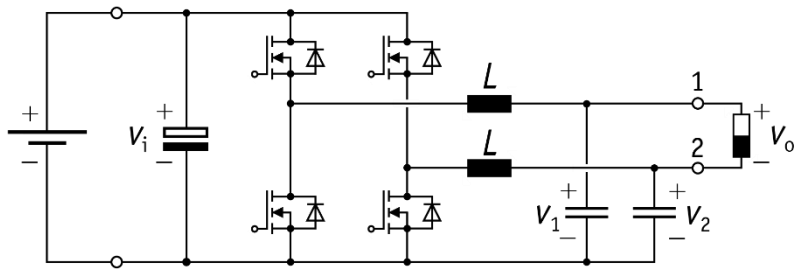
- Full Bridge Output Stage / Output Frequency Bridge Leg

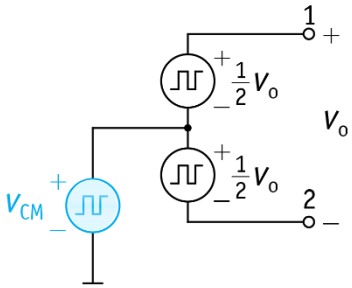


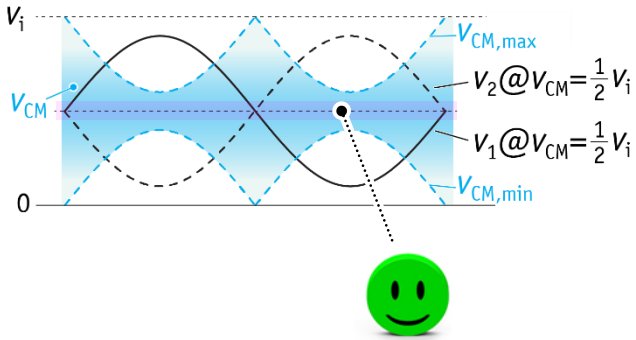

- PWM Operation of Mains Freq. Bridge Leg @ $|u| < u_{0,min}$
- CM Component $u_{CM}$ of Generated Output Voltage

# Derivation of Output Stage Topology (4)

- Full Bridge Output Stage / Full PWM Operation



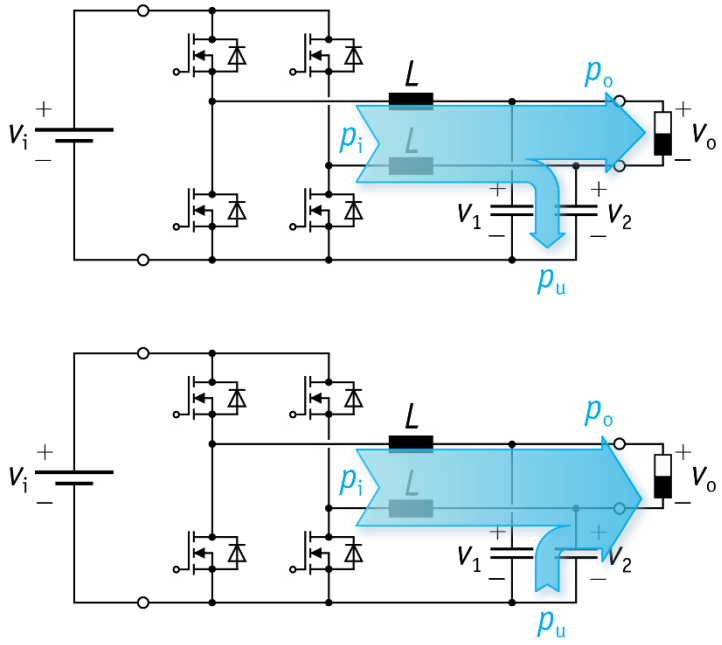



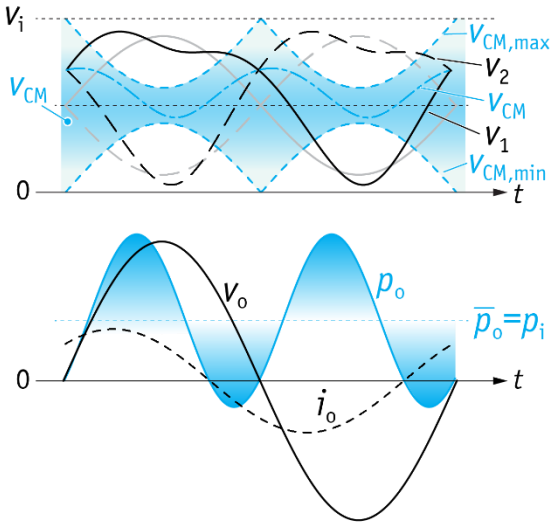



- DM Component of $u_1$ and $u_2$ Defines Output $u_0$
- CM Component of $u_1$ and $u_2$ Represents Degree of Freedom of the Modulation (!)

# Remark: AC Side Power Pulsation Buffer

- Full Bridge Output Stage / Full PWM Operation

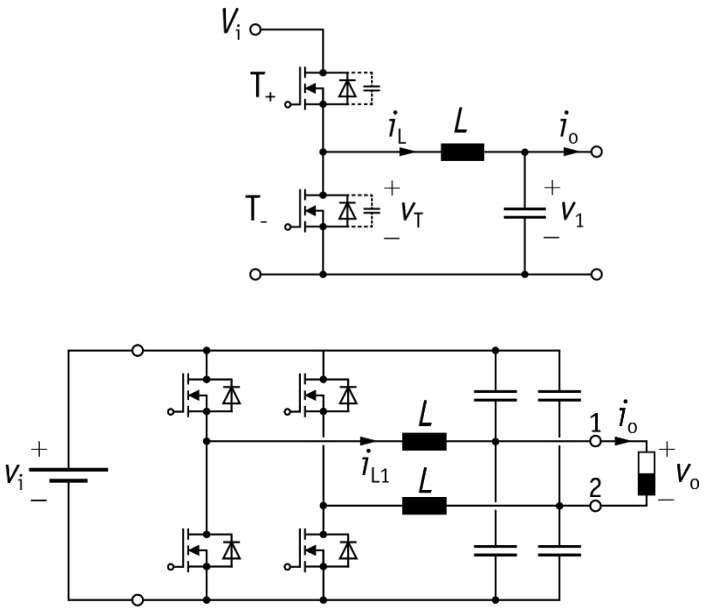


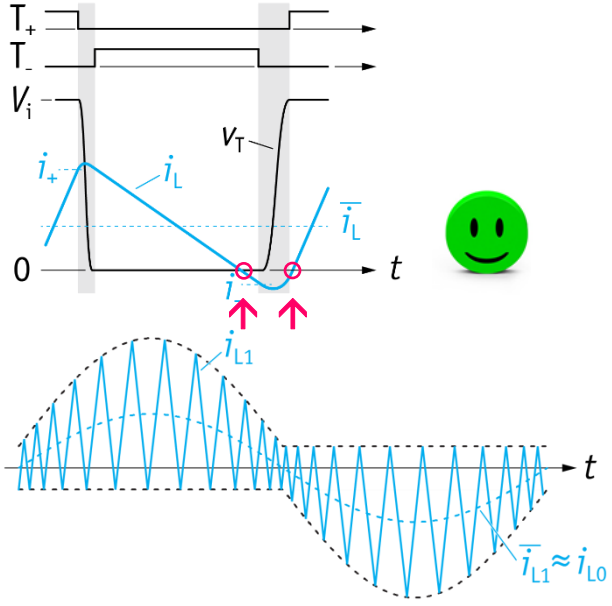




- CM Reactive Power of Output Filter Capacitors used for Comp. of Load Power Pulsation
- CM Reactive Power prop. 2 C
- DM Reactive Power prop. ½ C

# ZVS of Output Stage / TCM Operation

- Full Bridge Output Stage / Full PWM Operation

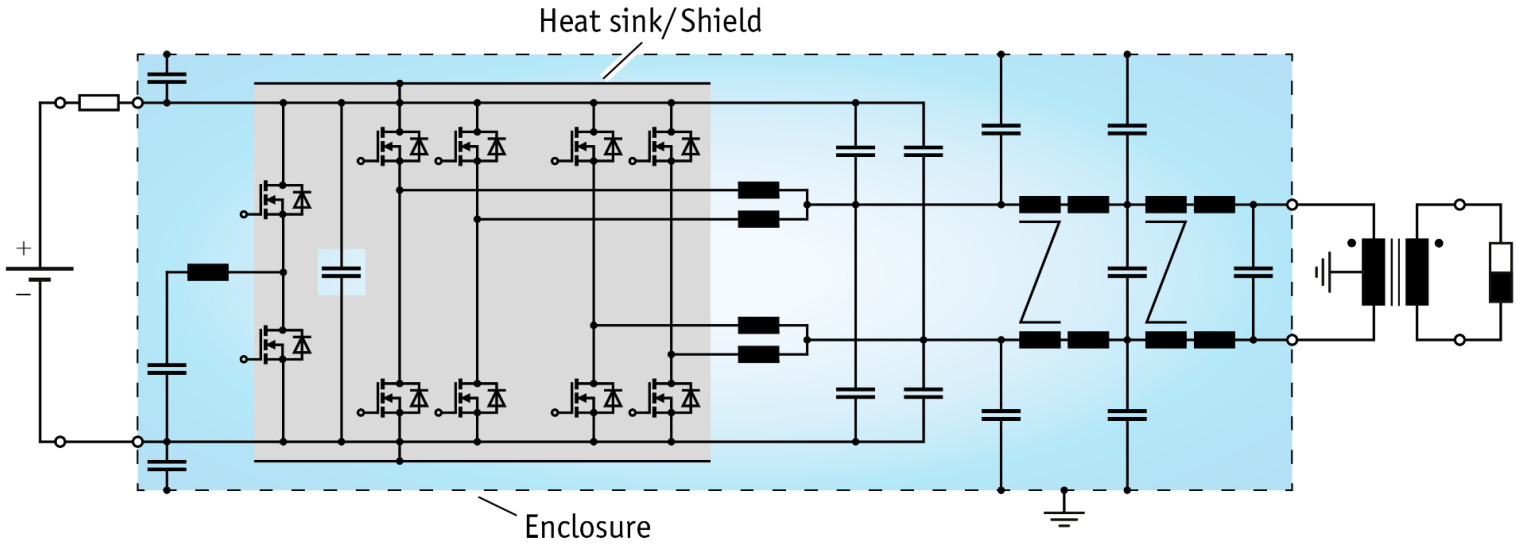



- Triangular Current Mode (TCM) Operation for Res. Voltage Transition @ Turn-On/Turn-Off
- Required Only Measurement of Current Zero Crossings, $i = 0$
- Variable Switching Frequency  Lowers EMI

# Selected Converter Topology

- Interleaving of 2 Bridge Legs per Phase - Volume / Filtering / Efficiency Optimum
- Active 1-Φ Output Power Pulsation Buffer

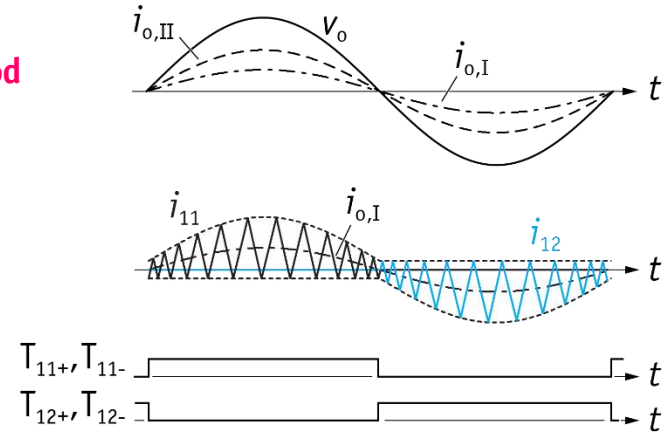


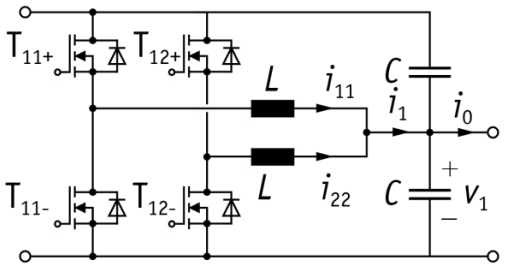

- ZVS of All Bridge Legs @ Turn-On/Turn-Off in Whole Operating Range – 4D TCM Interleaving
- Heatsinks Connected to DC bus / Shield to Prevent Capacitive Coupling to Grounded Enclosure

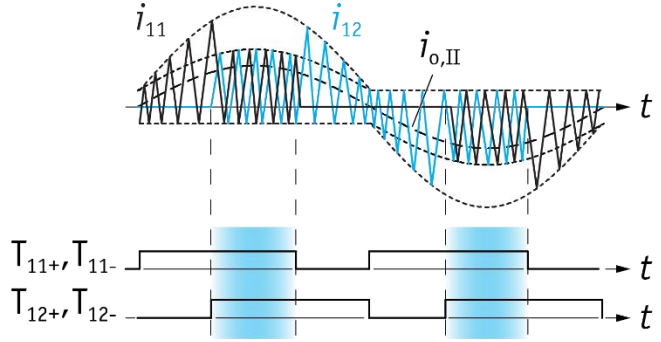
## *Interleaving*
## *Switching Frequ. Modulation*

# 4D-Interleaving

- Interleaving in Space & Time – Within Output Period
- Alternate Operation of Bridge Legs @ Low Power
- Overlapping Operation @ High Power



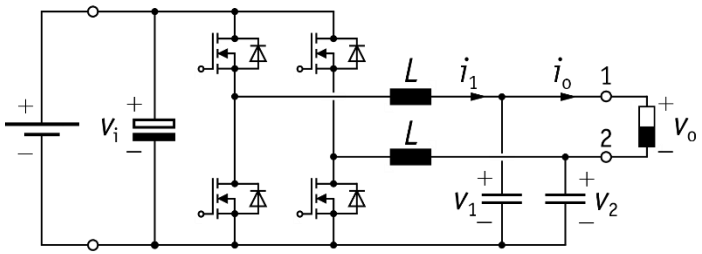



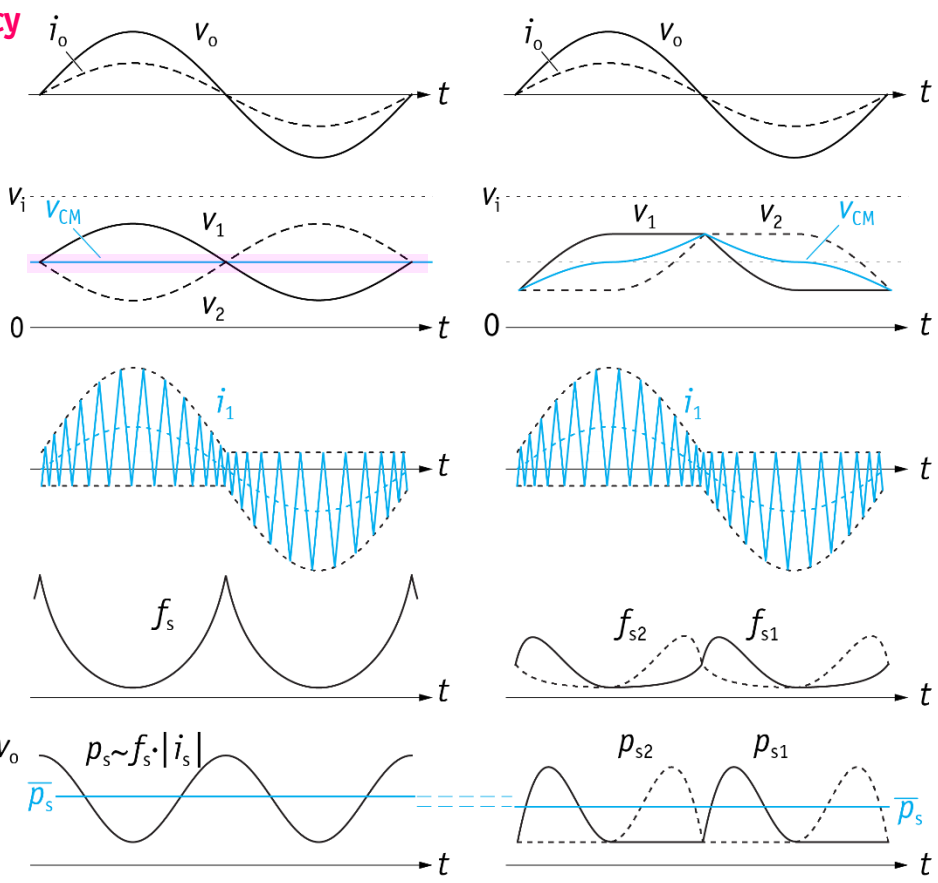




- Opt. Trade-Off of Conduction vs. Switching Losses / Opt. Balancing of Thermal Stress

# Remark: CM-Enhanced TCM Modulation

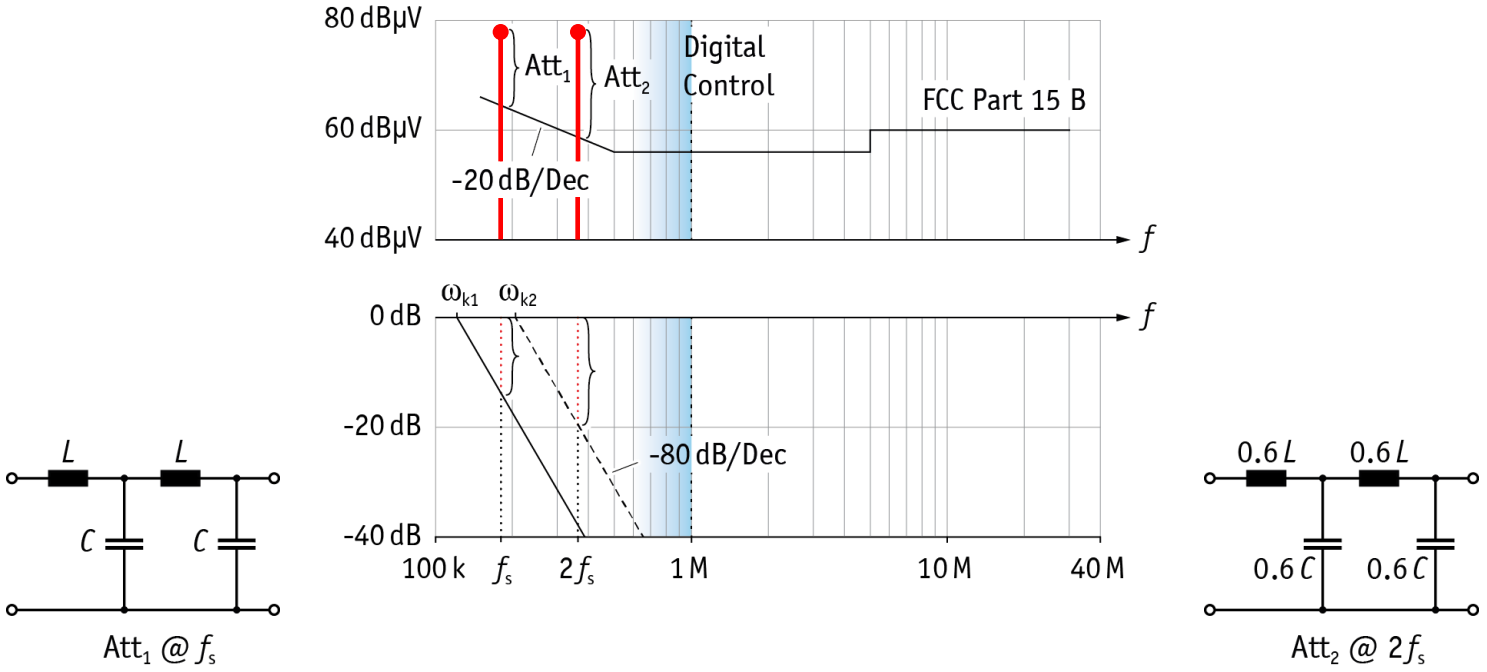
- CM Comp. of $u_1$, $u_2$ Changes Sw. Frequency
- Limits Sw. Frequency Variation
- Lower Sw. Losses



# Selection of Switching Frequency

- Significant Reduction in EMI Filter Volume for Increasing Sw. Frequency

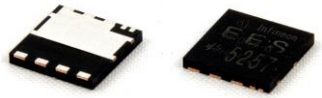



- Doubling Sw. Fequ. $f_S$ Cuts Filter Volume in Half
- Upper Limit due to Digital Signal Processing Delays / Inductor & Sw. Losses – Heatsink Volume

# Realization

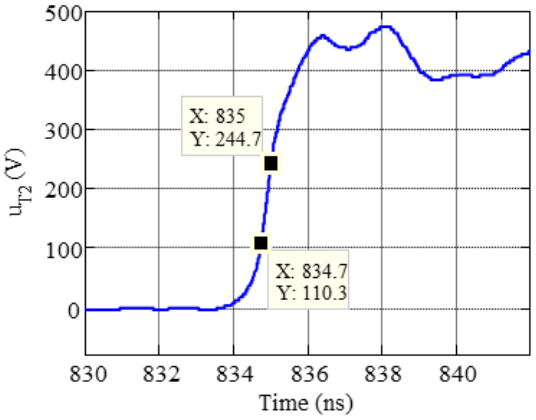
- Components
- Building Blocks →

# Power Semiconductors

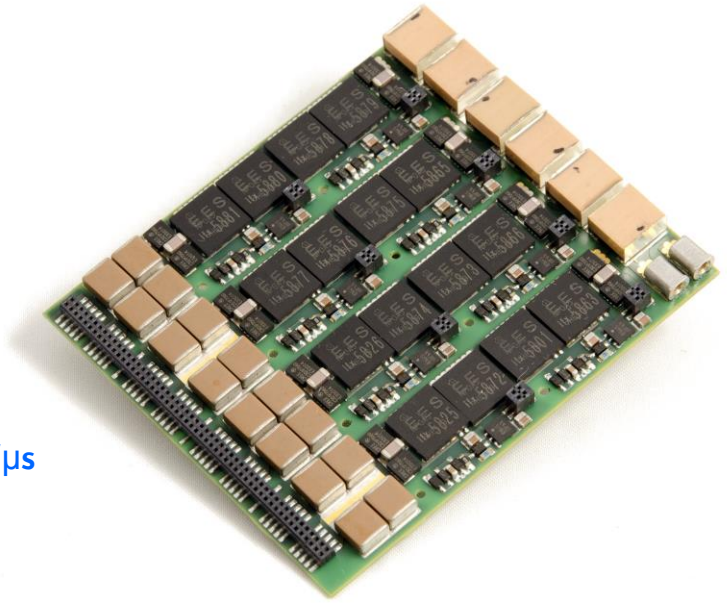


- 600V IFX Normally-Off GaN GIT - ThinPAK8x8
- 2 Parallel Transistors / Switch
- Antiparallel CREE SiC Schottky Diodes

- 1.2V typ. Gate Threshold Voltage
- 55 mΩ $R_{DS,on}$ @ 25°C, 120mΩ @ 150°C
- 5Ω Internal Gate Resistance



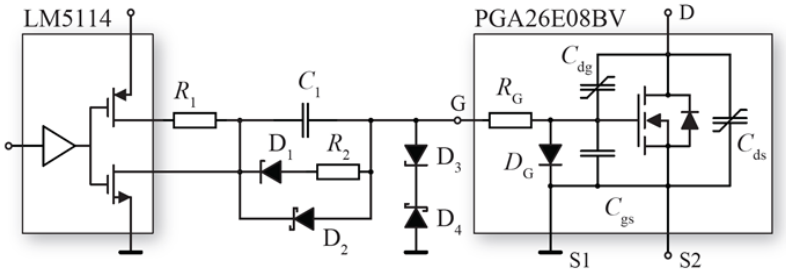

dv/dt = 500kV/µs

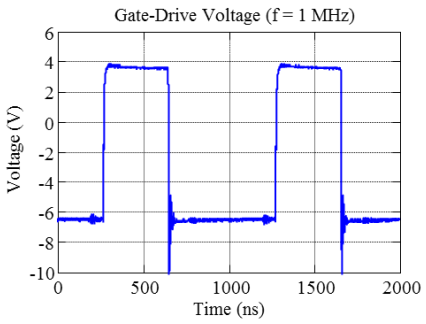


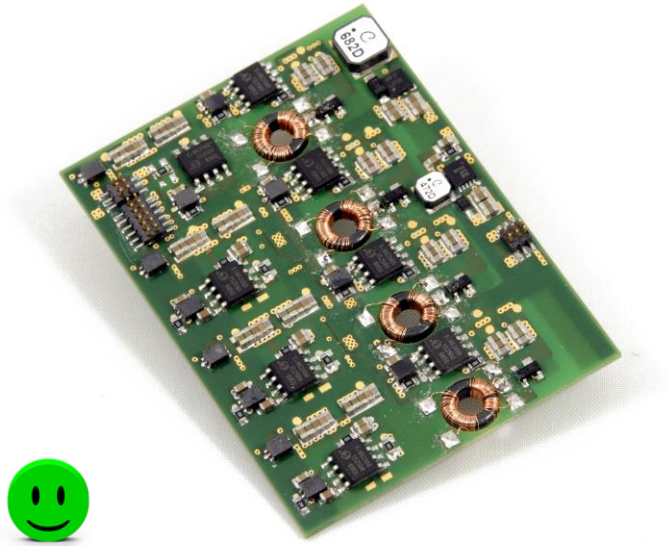
- CeraLink Capacitors for DC Voltage Buffering

# Advanced Gate Drive

- Fixed Negative Turn-off Gate Voltage Independent of Sw. Frequency and Duty Cycle
- Extreme dv/dt Immunity (500 kV/µs) Due to CM Choke at Signal Isolator Input



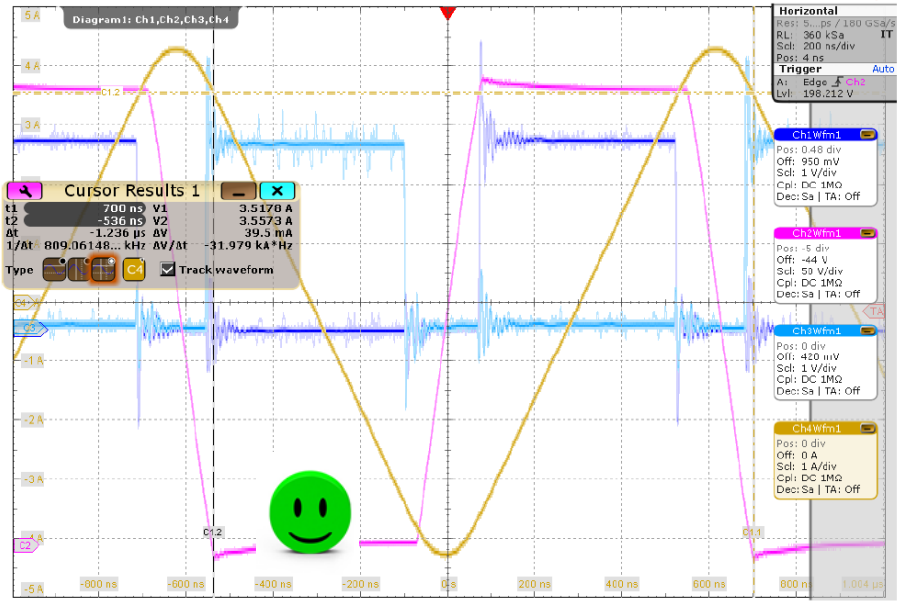



- Total Prop. Delay < 30ns incl. Signal Isolator, Gate Drive, and Switch Turn-On Delay

# Advanced Gate Drive

- Fixed Negative Turn-off Gate Voltage Independent of Sw. Frequency and Duty Cycle
- Extreme dv/dt Immunity (500 kV/µs) Due to CM Choke at Signal Isolator Input



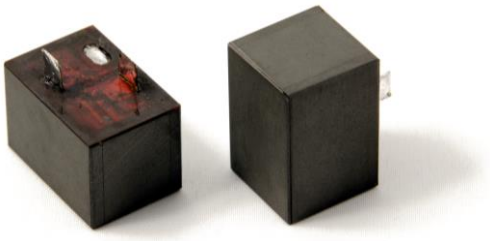

- Gate Voltage T+
- Gate Voltage T-
- TCM Inductor Current
- Transistor Voltage

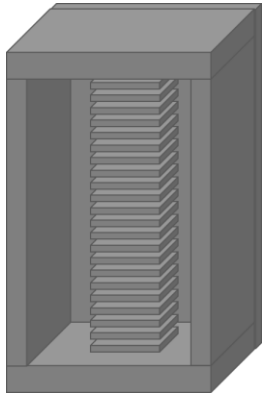
- Triangular Current Mode (TCM) Operation at No Load → ZVS and No Free Ringing of $u_{T+}$, $u_{T-}$ or $i_L$

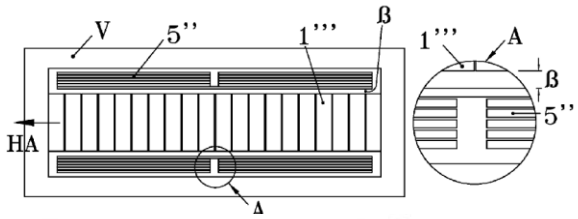
# High Frequency Inductors

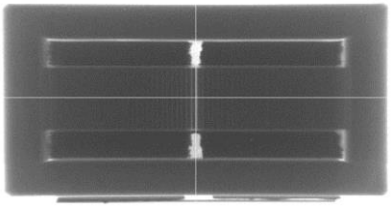
- Multi-Airgap Inductor with Patented Multi-Layer Foil Winding Arrangement Minim. Prox. Effect
- Very High Filling Factor / Low High Frequency Losses
- Magnetically Shielded Construction Minimizing EMI
- Intellectual Property of F. Zajc / Fraza

- L= 10.5µH
- 2 x 8 Turns
- 24 x 80µm Airgaps
- Core Material DMR 51 / Hengdian
- 0.61mm Thick Stacked Plates
- 20 µm Copper Foil / 4 in Parallel
- 7 µm Kapton Layer Isolation
- 20mΩ Winding Resistance / Q=800
- Terminals in No-Leakage Flux Area







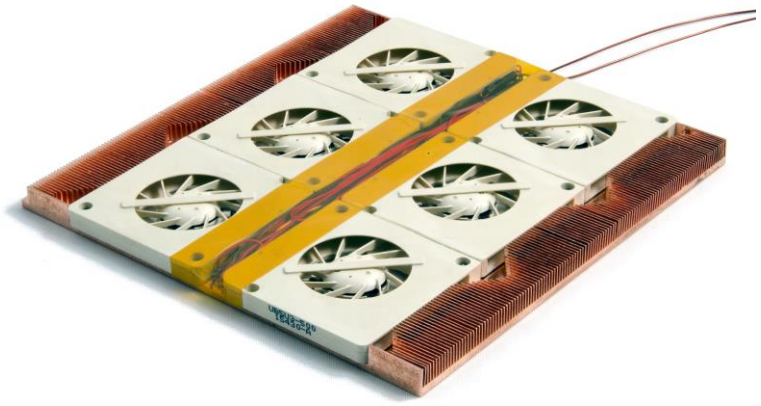



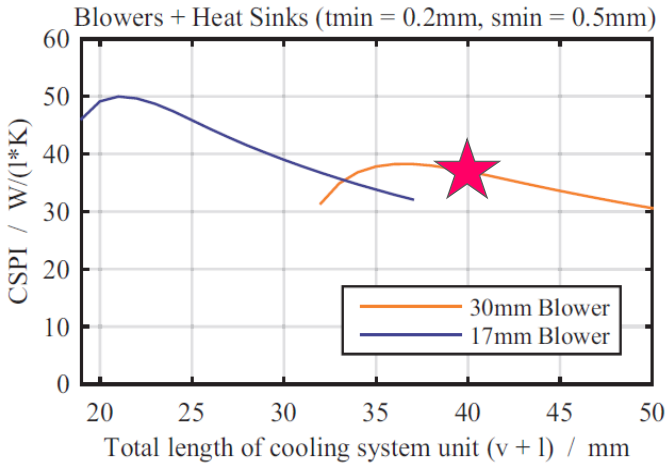
■ Dimensions - 14.5 x 14.5 x 22mm³

# Thermal Management

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters
- Outstanding Cooling Syst. Performance Index

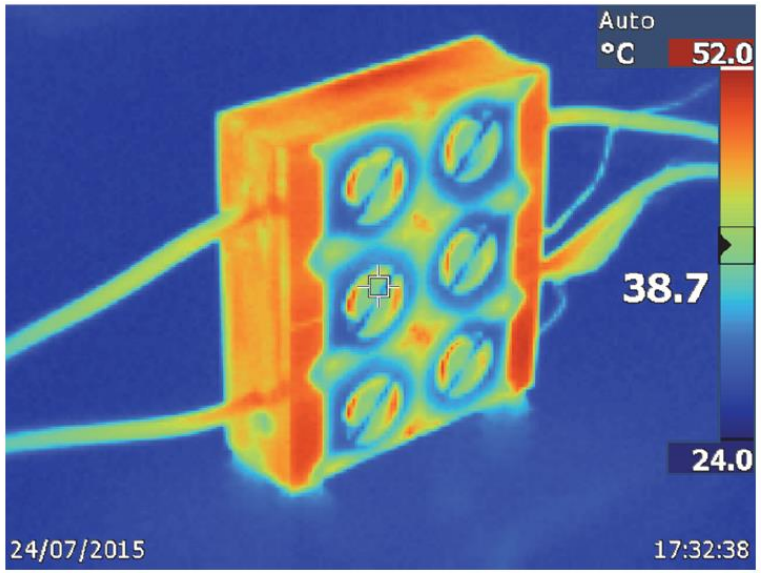
- 200um Fin Thickness
- 500um Fin Spacing
- 3mm Fin Height
- 10mm Fin Length
- CSPI = 37 W/(dm³.K)
- 1.5mm Baseplate





# Thermal Management

- 30mm Blowers with Axial Air Intake / Radial Outlet
- Full Optimization of the Heatsink Parameters
- Outstanding Cooling Syst. Performance Index

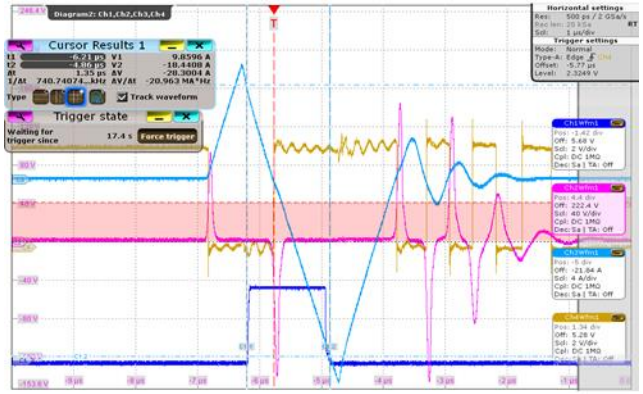


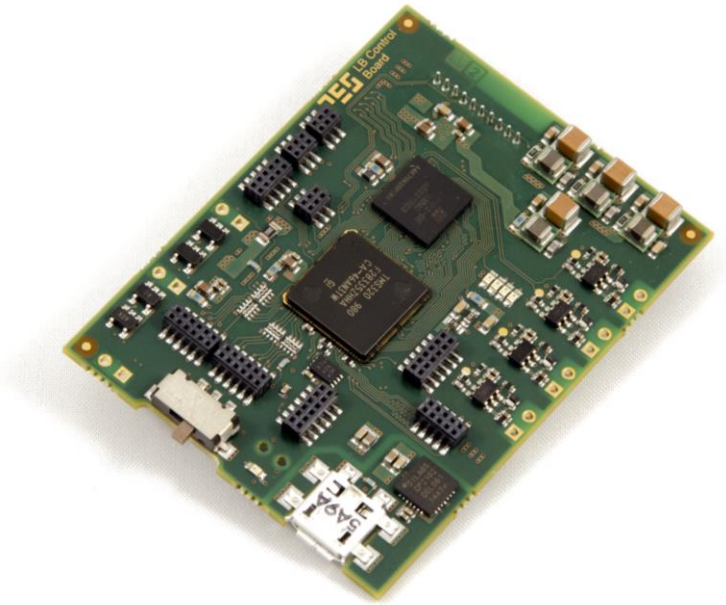

- Two-Side Cooling → Heatsink Temperature = 52°C @ 80W (8W Natural Convection)

# Control Board & i=0 Detection

- Fully Digital Control - Overall Control Sampling Frequency of 25kHz
- TI DSC TMS320F28335 / 150MHz / 179-pin BGA / 12mmx12mm
- Lattice FPGA LFXP2-5E / 200MHz / 86-pin BGA / 8mmx8mm

- TCM Current / Induced Voltage / Comparator Output



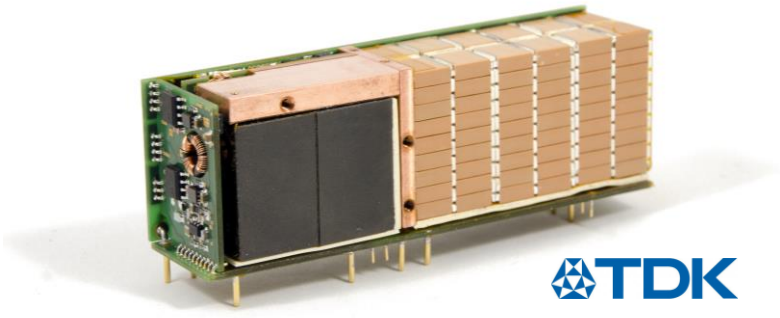



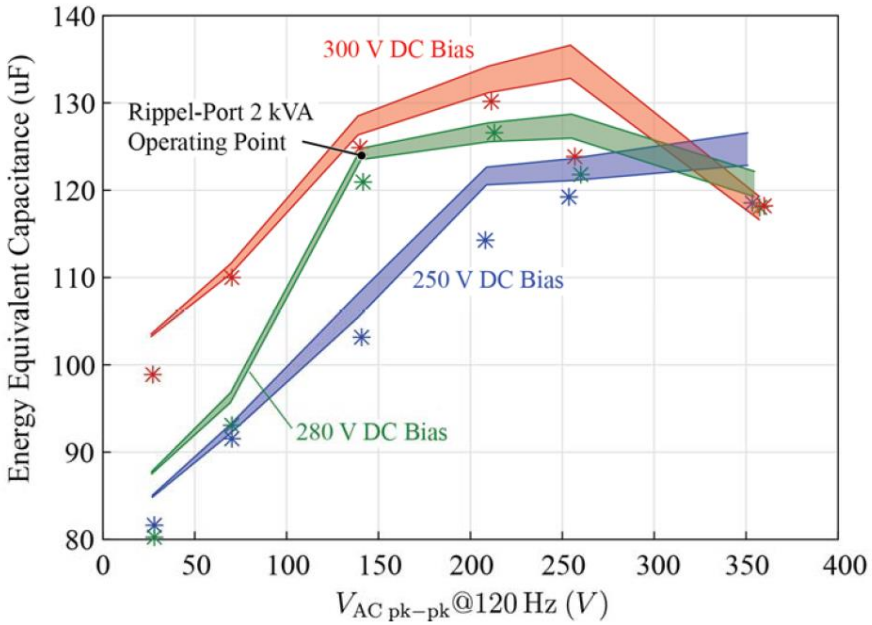
- i=0 Detection of TCM Currents Using R4/N30 Saturable Inductors
- Galv. Isolated / Operates up to 2.5MHz Switching Frequency / <10ns Delay

# Power Pulsation Buffer Capacitor

- High Energy Density 2nd Gen. 400VDC CeraLink Capacitors Utilized as Energy Storage
- Highly Non-Linear Behavior → Opt. DC Bias Voltage of 280VDC
- Losses of 6W @ 2kVA Output Power

- 108 x 1.2µF /400 V
- 23.7cm³ Capacitor Volume

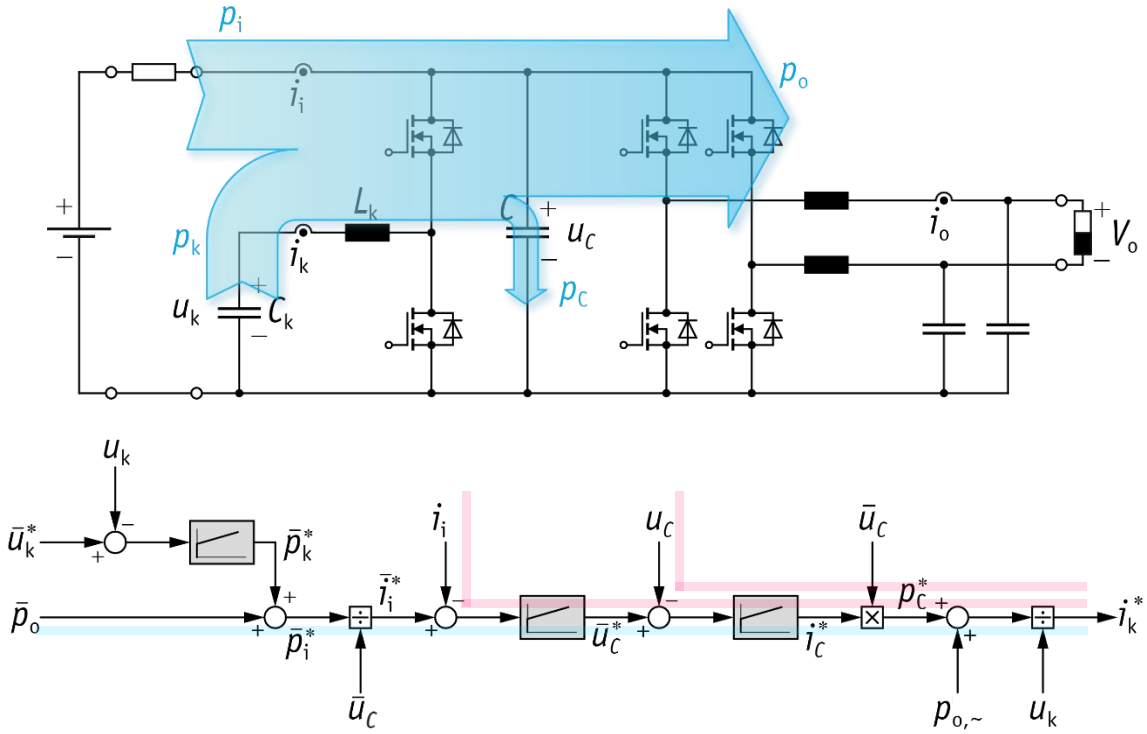



- Effective Large Signal Capacitance of C ≈140µF

# Control of Power Pulsation Buffer

- Cascaded Control Structure



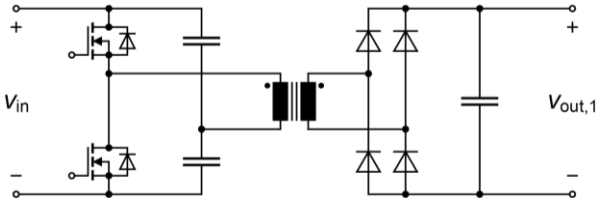

- Feedforward of Output Power Fluctuation
- Underlying Input Current / DC Link Voltage Control

# Auxiliary Supply & Measurements

- ZVS Constant 50% Duty Cycle Half Bridge with Synchr. Rectification
- Compact / Efficient / Low EMI

- 10W Max. Output Power
- 380V...450V Input Operating Range
- 16V...16V DC Output in Full Inp. Voltage / Output Power Range
- 90% Efficiency @ $P_{max}$



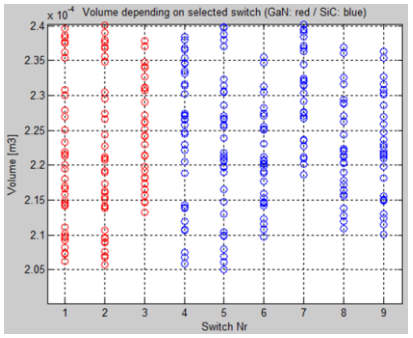


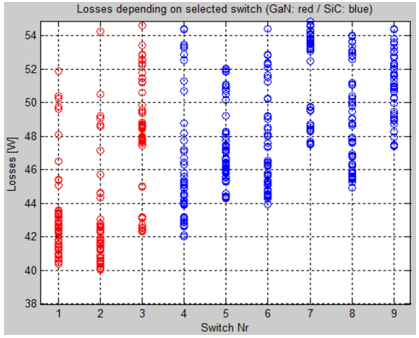


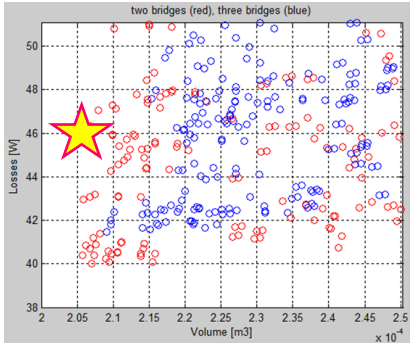
- 19mm x 24mm x 4.5mm (2cm$^3$ Volume )

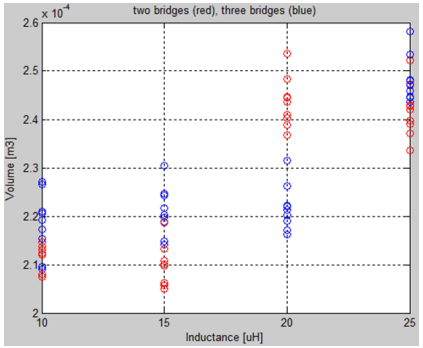
# Multi-Objective Optimization

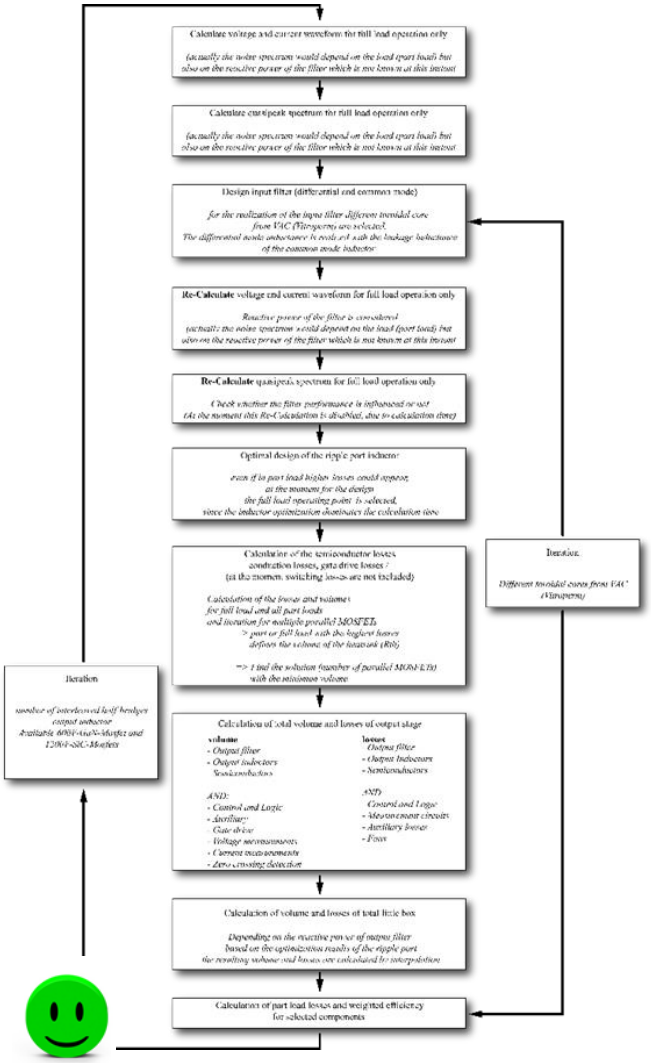
- Detailed System Models - Power Buffer/Output Stage/EMI
- Detailed Multi-Domain Component Models (incl. GaN & SiC)
- Consideration of Very Large # of Degrees of Freedom




■ Pareto Optimiz. → Minim. Vol. of 207cm³ w/o EMI Filter

*3D-CAD Construction* →

# 3D-CAD Construction (1)

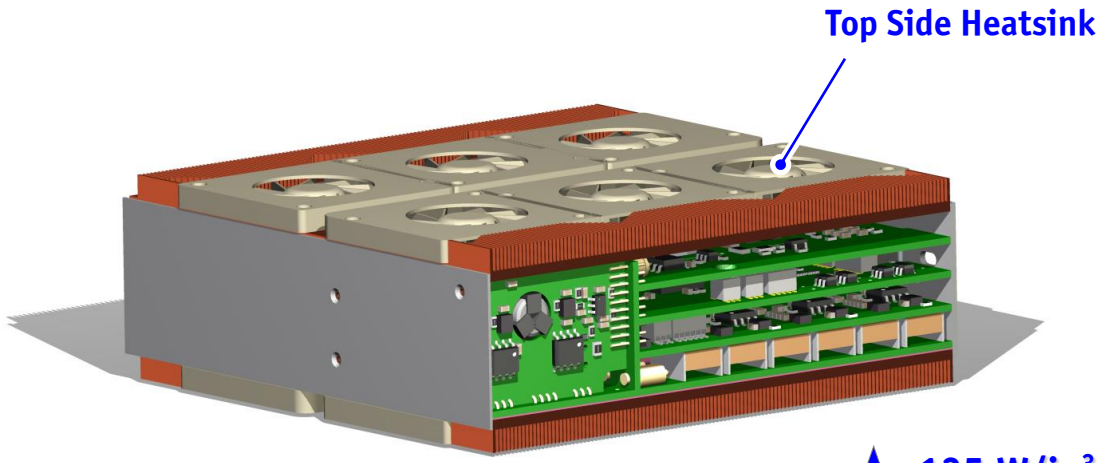
- **Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C**

★ **135 W/in³**

- 88.7mm x 88.4mm x 31mm **= 243cm³** (14.8in³ ) **→ 8.2 kW/dm³**

# 3D-CAD Construction (2)

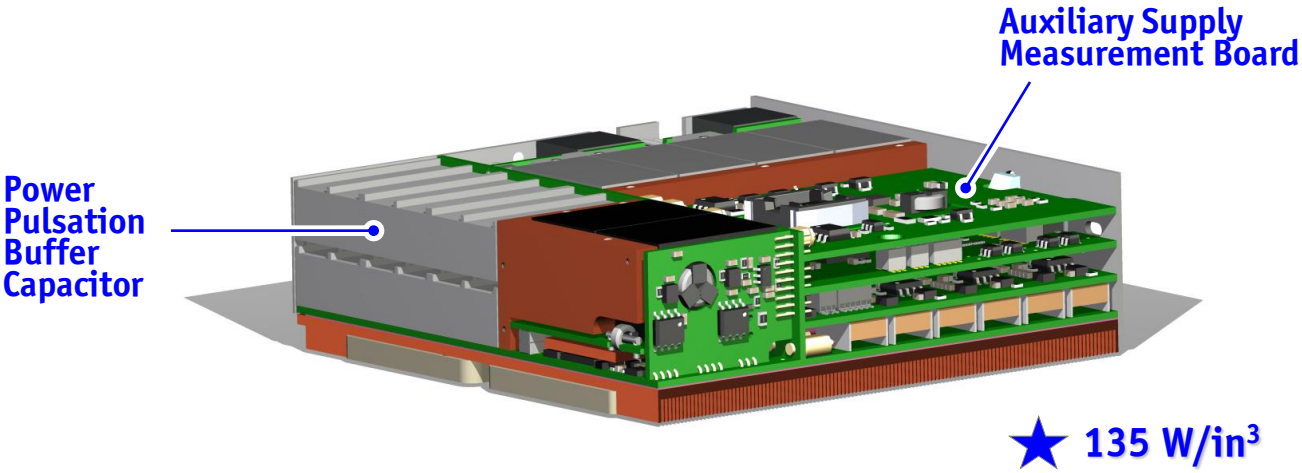
- **Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C**




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (3)

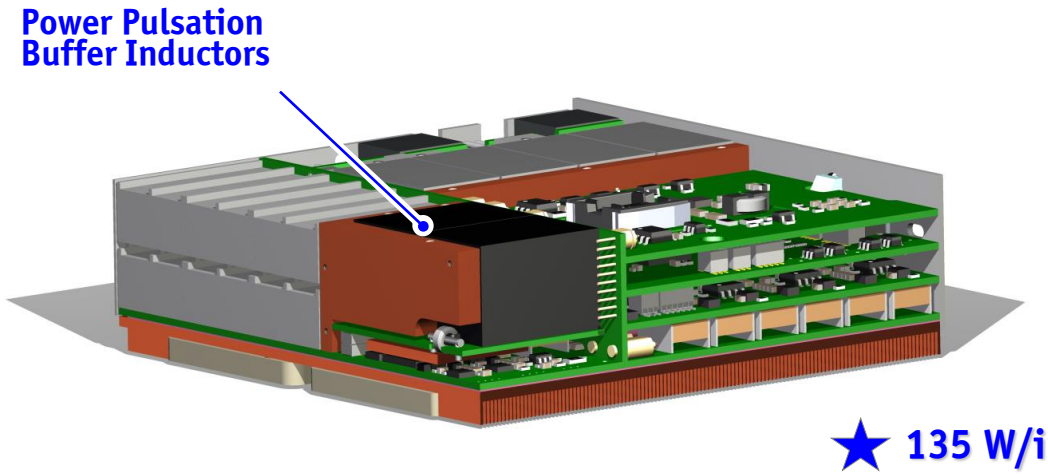
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (4)

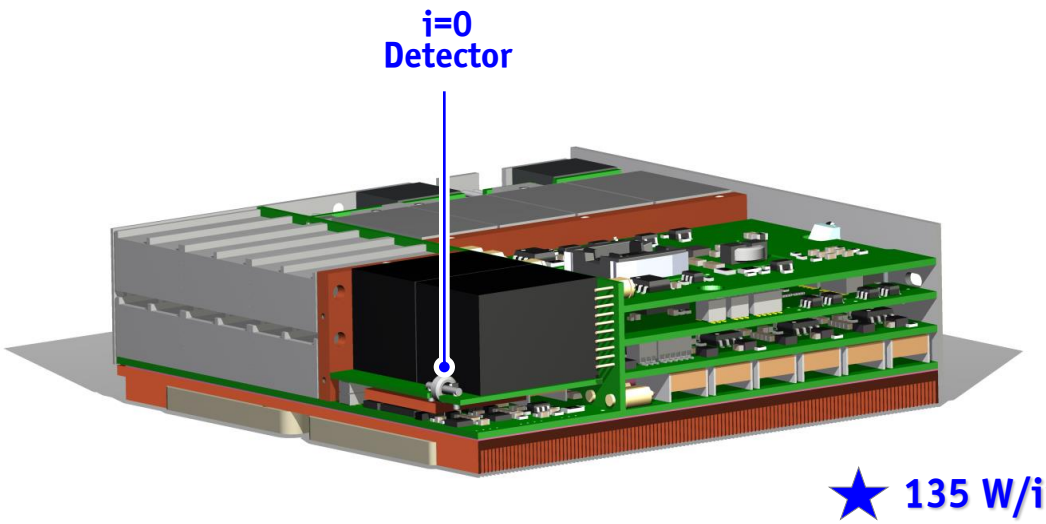
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (5)

- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C

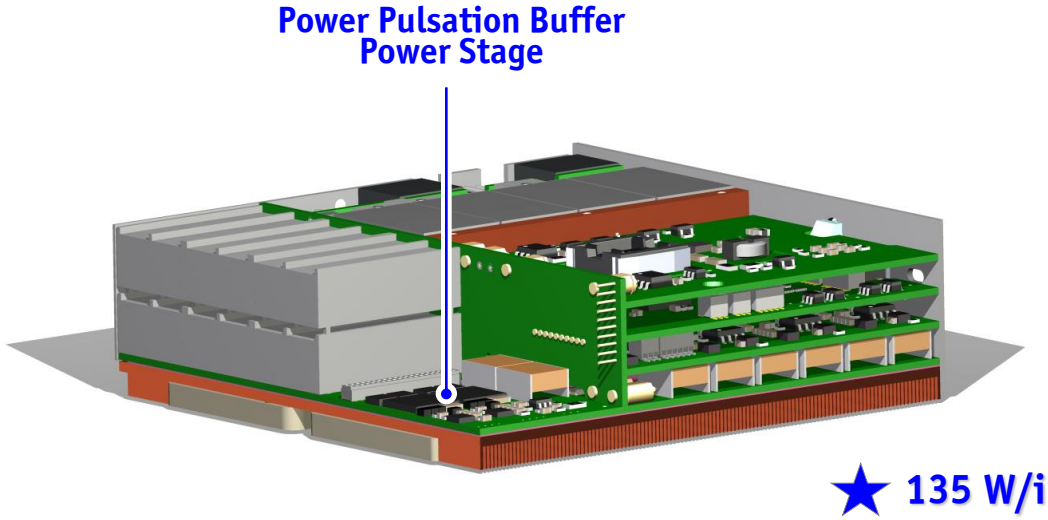



★ 135 W/in³

- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (6)

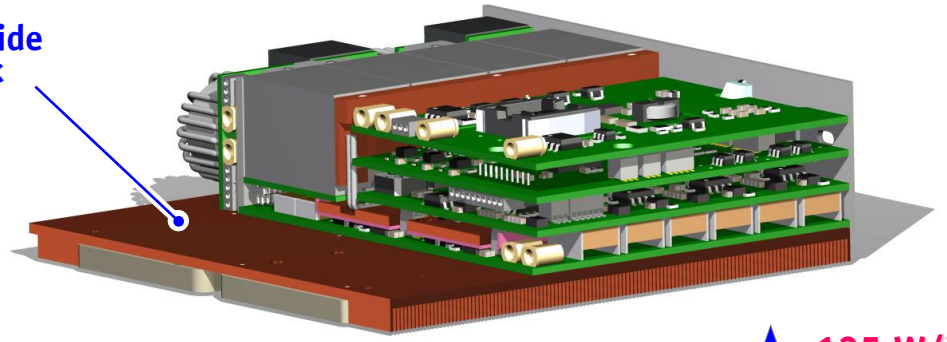
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (7)

- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C

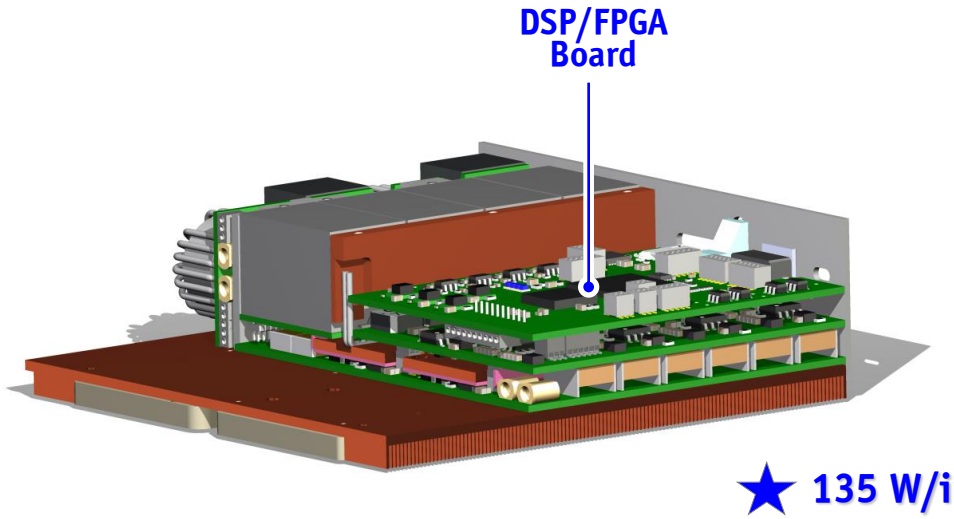



★ 135 W/in³

- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (8)

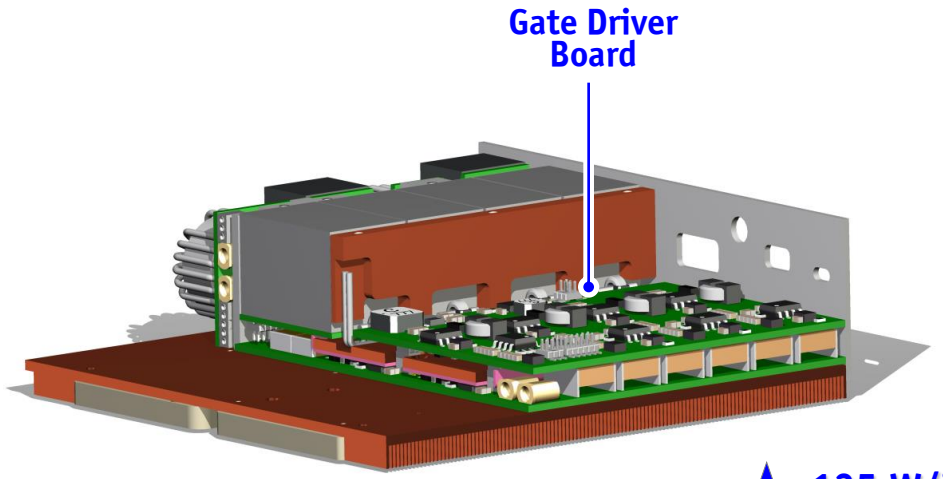
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (9)

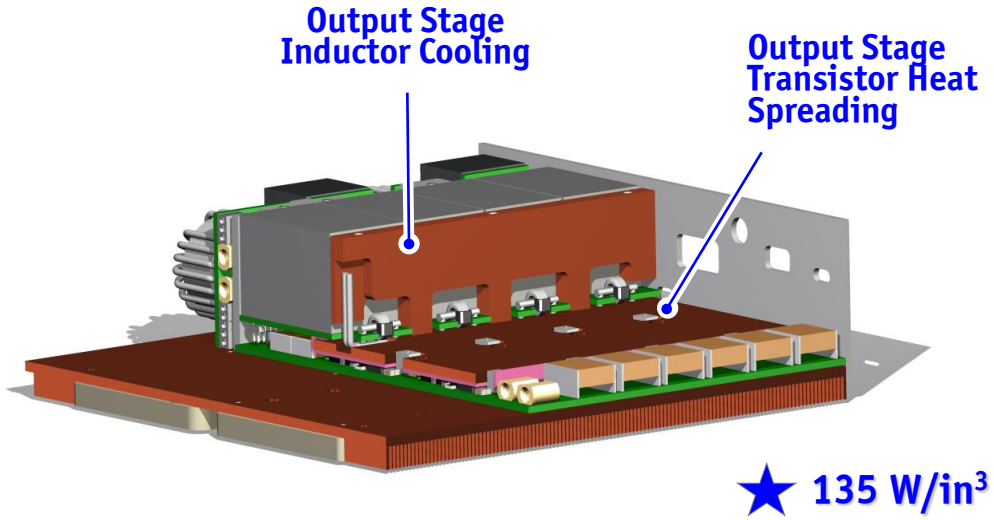
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (10)

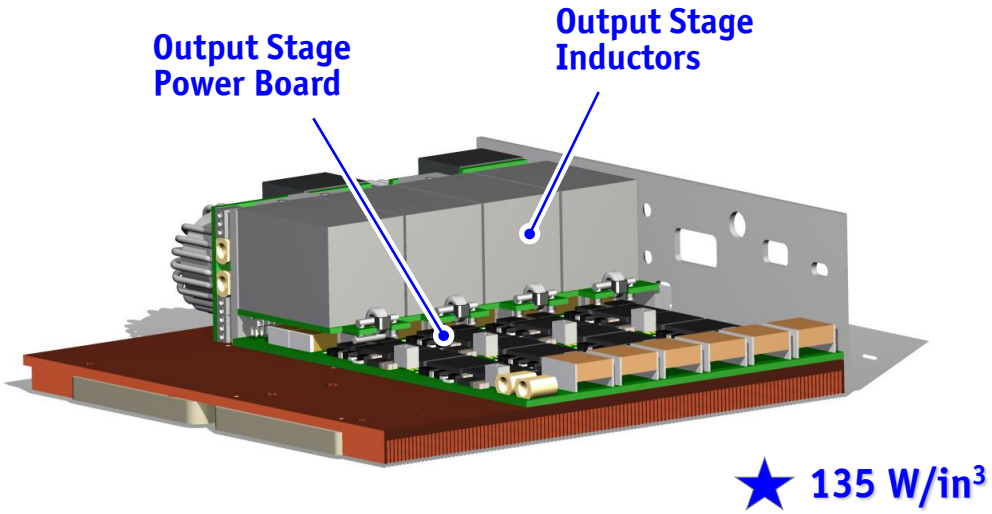
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (11)

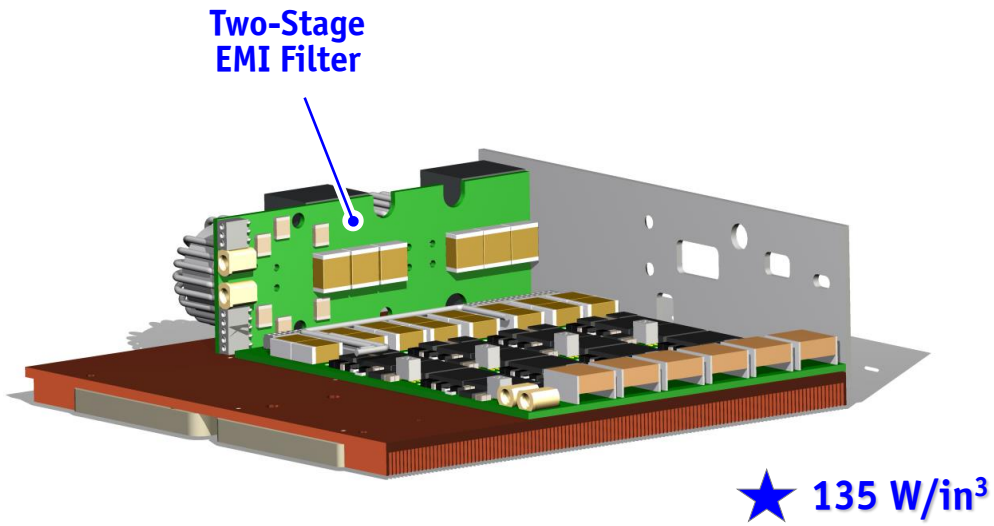
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (12)

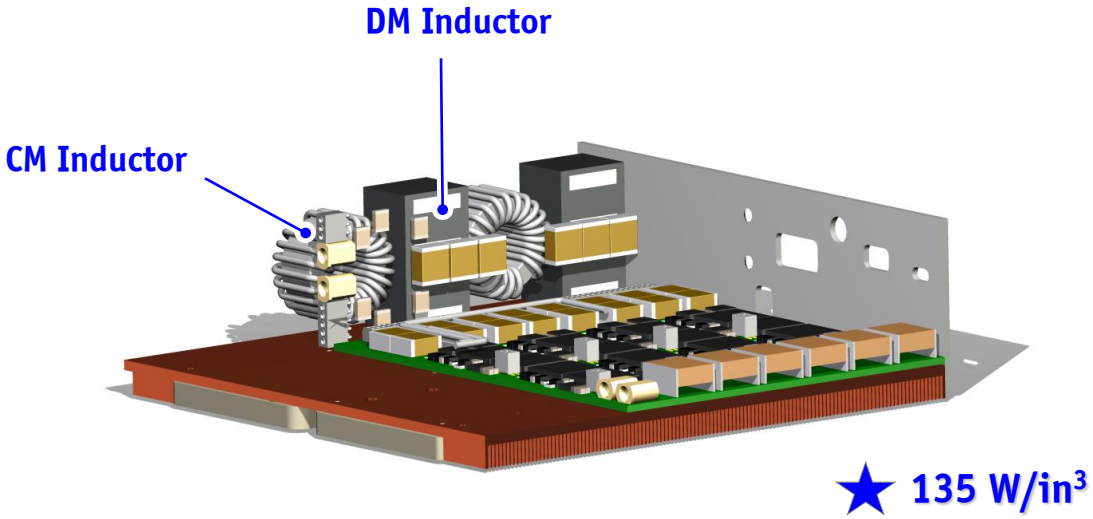
- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# 3D-CAD Construction (13)

- Built to the Power Density Limit @ η= 95% / $T_c$ < 60°C




- 88.7mm x 88.4mm x 31mm = 243cm³ (14.8in³ ) → 8.2 kW/dm³

# Experimental Results

*Hardware*
*Output Voltage/Input Current Quality*
*Thermal Behavior*
*Efficiency*
*EMI* 

# Little-Box Prototype I

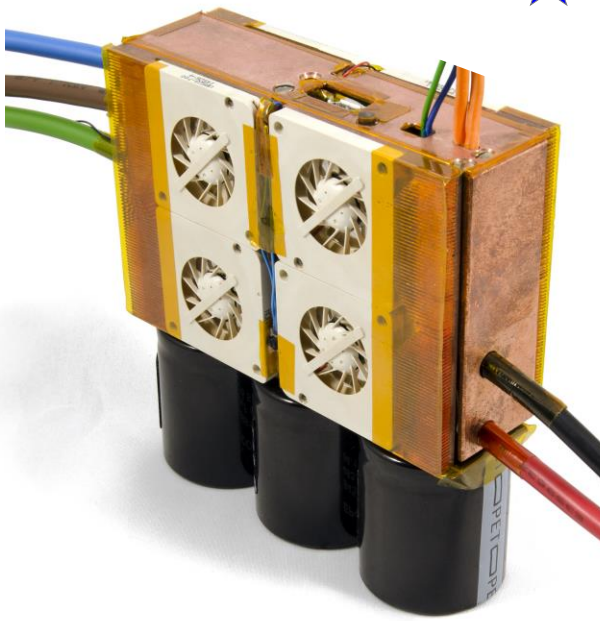
- System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer

★ 120 W/in³

273cm³
7.3 kW/dm³
97,5% Efficiency @ 2kW
$T_c$=58°C @ 2kW

$\Delta u_{DC}$= 2.85%
$\Delta i_{DC}$= 15.4%
$THD+N_U$ = 2.6%
$THD+N_I$ = 1.9%

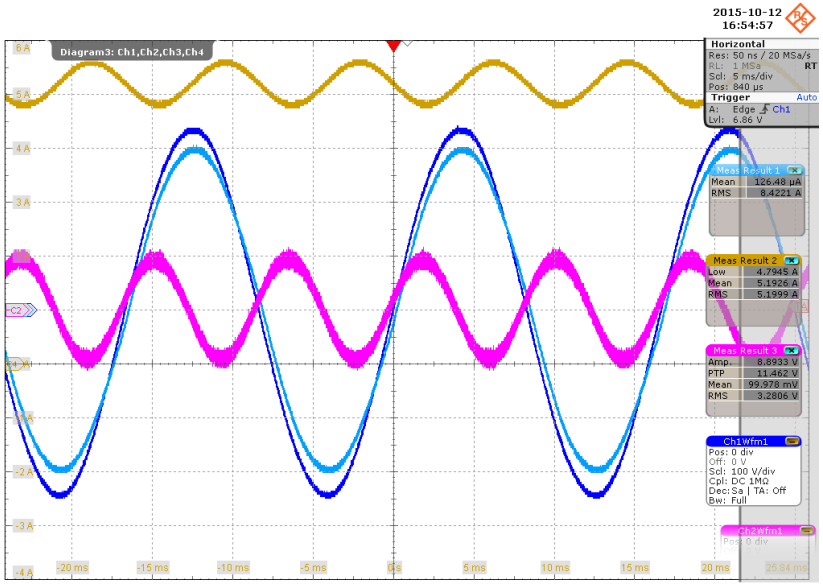
97mm x 90.8 mm x 31mm ( 16.6in³ )



- Compliant to All Specifications

# Measurement Results I-(1)

- System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer



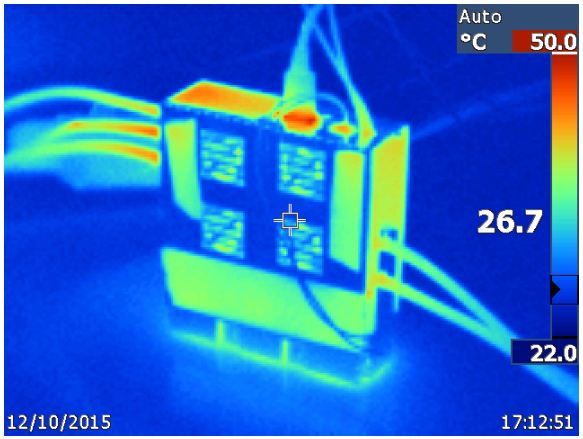

Ohmic Load / 2kW

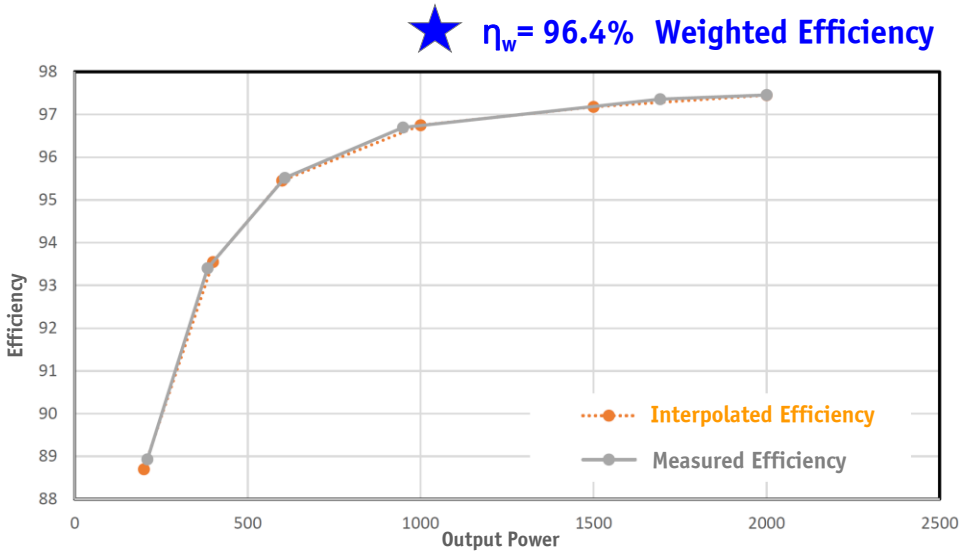
DC Input Current
DC Voltage Ripple
Output Voltage
Output Current

- Compliant to All Specifications

# Measurement Results I-(2)

- System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer



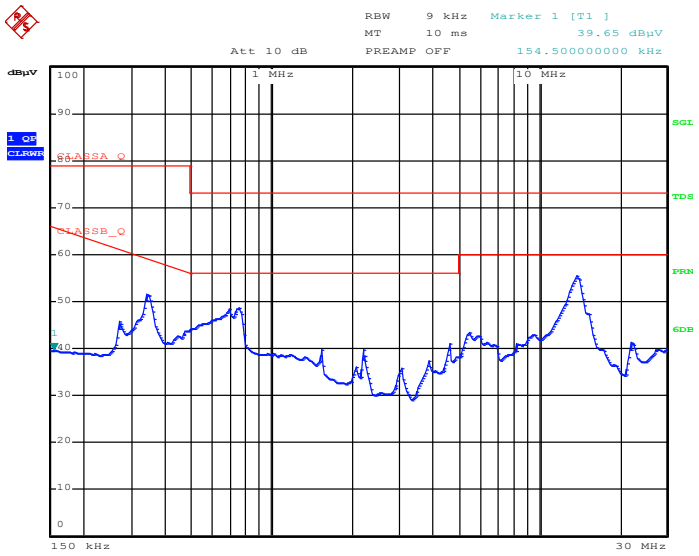




- Heating of System Lower than Specified Limit ($T_{C,max}$= 60°C @ $T_{amb}$= 30°C)

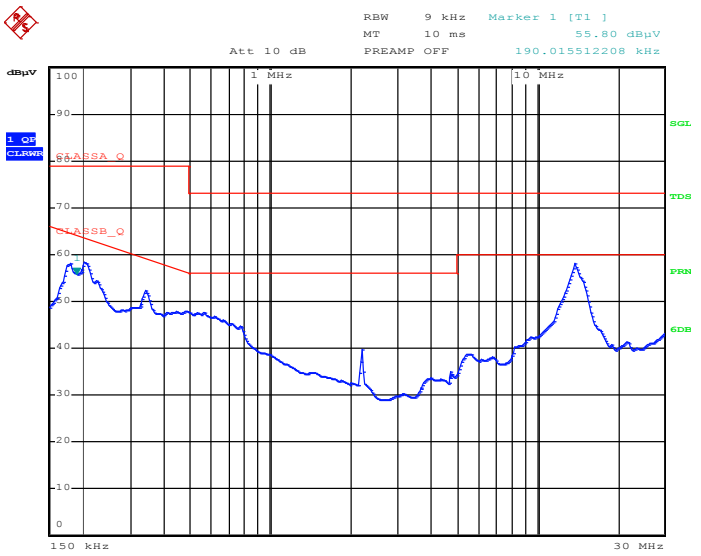
# Measurement Results I-(3)

- System Employing Electrolytic Capacitors as 1-Φ Power Pulsation Buffer

$P_{out}$= 400W




$P_{out}$= 2kW




- Compliant to All Specifications

# Little-Box Prototype II-(1)

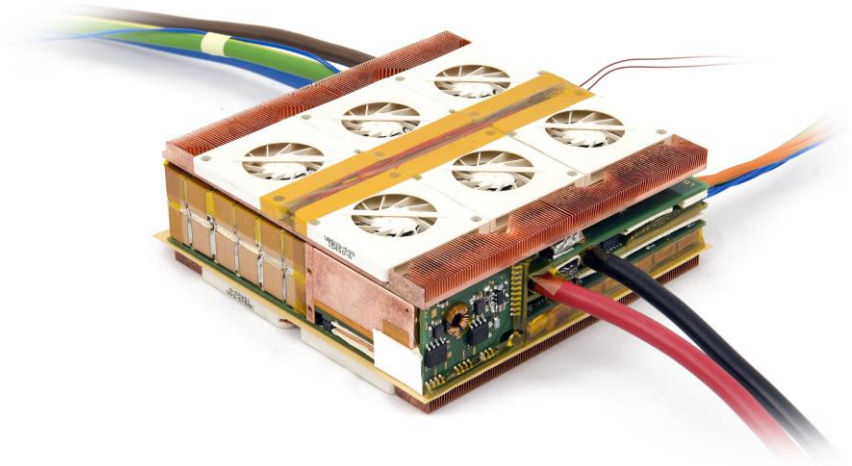
- System Employing Active 1-Φ Power Pulsation Buffer

243 cm³
8.2 kW/dm³
96,3% Efficiency @ 2kW
$T_c$=58°C @ 2kW

$\Delta u_{DC}$= 1.1%
$\Delta i_{DC}$= 2.8%
$THD+N_U$ = 2.6%
$THD+N_I$ = 1.9%

88.7mm x 88.4mm x 31mm (14.8in³)

★ 135 W/in³



- Compliant to All Specifications

# Little-Box Prototype II-(1)

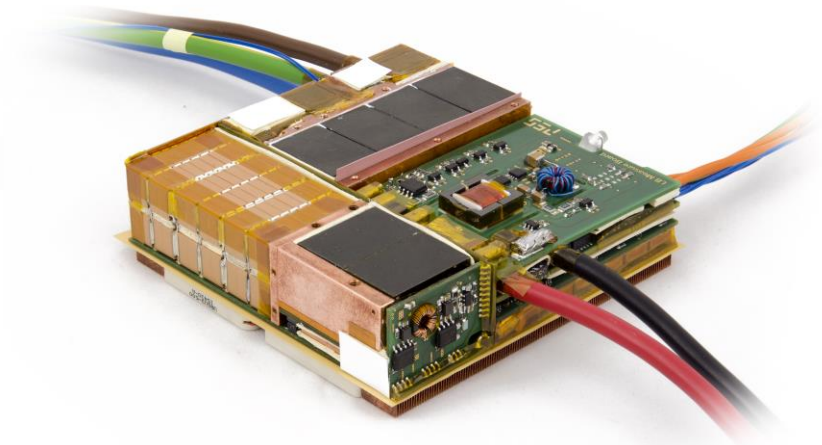
- System Employing Active 1-Φ Power Pulsation Buffer

243 cm³
8.2 kW/dm³
96,3% Efficiency @ 2kW
$T_c$=58°C @ 2kW

$\Delta u_{DC}$= 1.1%
$\Delta i_{DC}$= 2.8%
$THD+N_U$ = 2.6%
$THD+N_I$ = 1.9%

88.7mm x 88.4mm x 31mm (14.8in³)

★ 135 W/in³



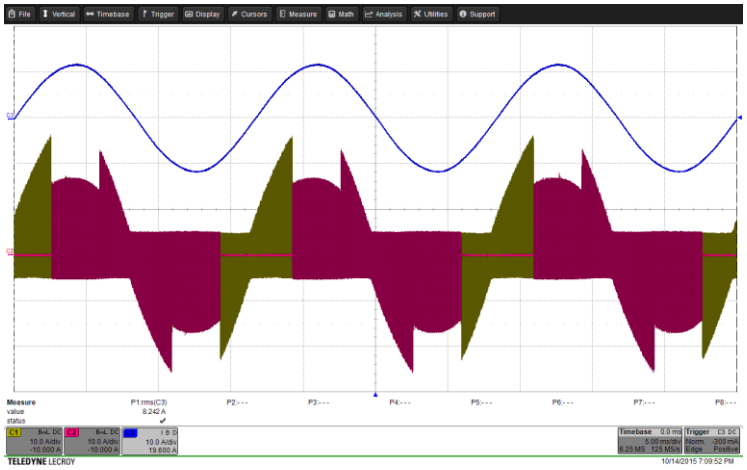
- Compliant to All Specifications

# Measurement Results II-(2)

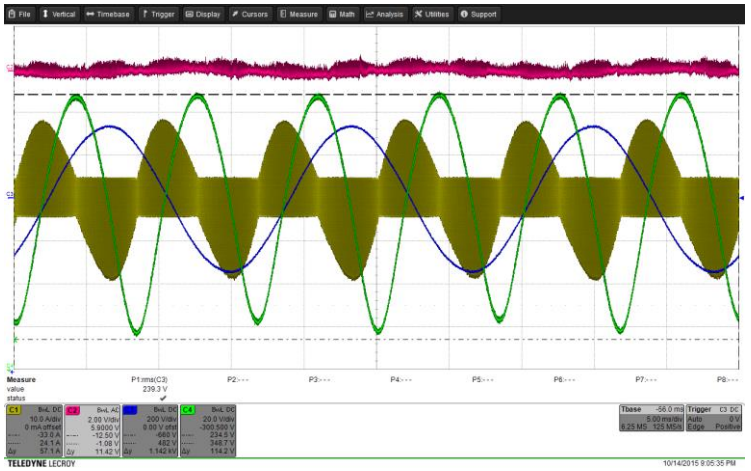
- System Employing Active 1-Φ Power Pulsation Buffer

- Ohmic Load / 2kW

Output Current
Inductor Current Bridge Leg 1-1
Inductor Current Bridge Leg 1-2



DC Link Voltage (AC-Coupl.)
Buffer Cap. Voltage
Buffer Cap. Current
Output Voltage

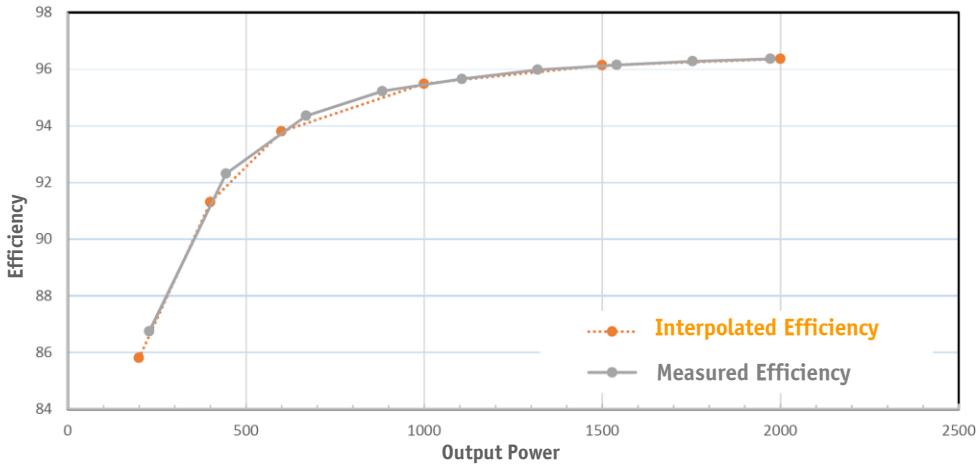


- Compliant to All Specifications

# Measurement Results II-(3)

- System Employing Active 1-Φ Power Pulsation Buffer

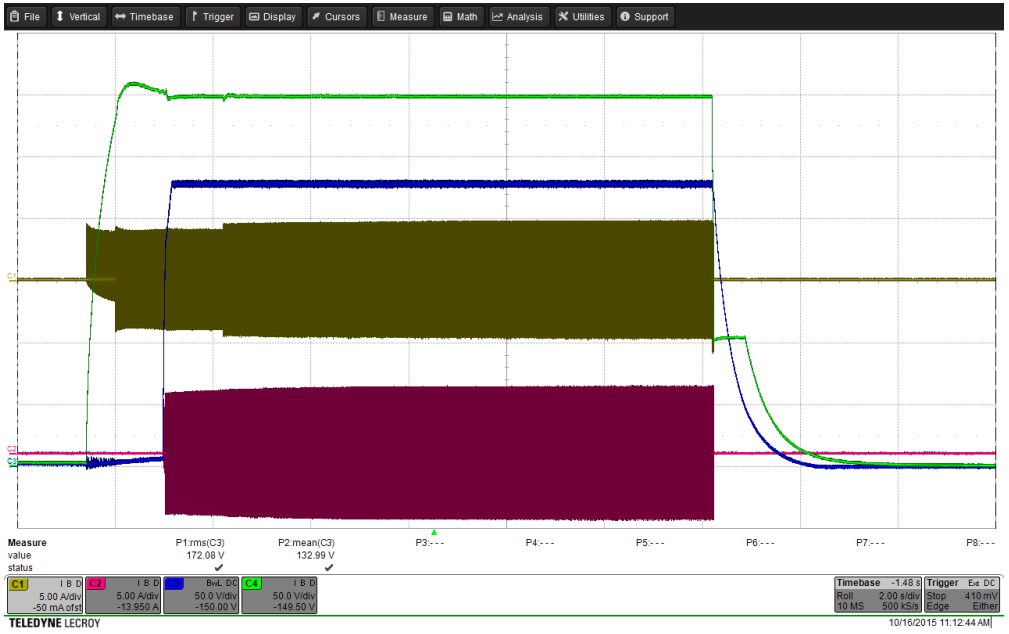
★ $\eta_w$=95.07% Weighted Efficiency




- Compliant to All Specifications

# Measurement Results II-(5)

- System Employing Active 1-Φ Power Pulsation Buffer




DC Link Voltage
Buffer Cap. Voltage
Buffer Cap. Current
Inductor Current Bridge Leg 1-1

- Start-up and Shut-Down (No Load Operation)

- ***Conclusions*** →

# Conclusions

- 2kVA 1-Φ Inverter @ 240cm³ (15in³) → 8kW/dm³ (135W/in³)
- 400...450VDC Input / 240VAC$_{rms}$ Output
- Efficiency > 95%
- Case Temp. < 60°C
- EMI FCC Part 15 B

- *100+ Teams*
- *3 Members / Team, 1 Year*
- *300 Man-Years*
- *3300 USD / Man-Year*

## Lessons Learned

- Upper Sw. Frequency Limit of ≈1MHz Due to Digital Control / i=0 Detection
- Integrated Gate Driver for Even Higher Power Density
- High Frequency Low Loss Magnetics are Key Issue
- Isol. Distance Requirements Difficult to Fulfill
- Losses of Ceramic Capacitors for Large AC Ripple
- Careful Mounting of Ceramic Caps.

- New U-I-Probes Required for Ultra-Compact Conv. R&D
- Convergence of Sim. & Measurem. Tools → Next Gen. Oscilloscope
- New Multi-Obj. Multi-Domain Simulation/Optim. Tools

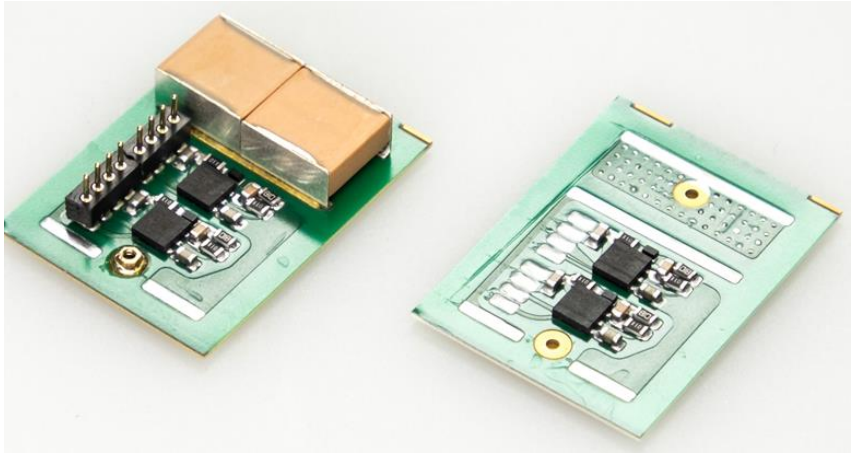
- Low Frequency (20kHz...120kHz) SiC vs. HF (200kHz...1.2MHz) GaN

# Outlook

- Embedded Switching Cell Package for Further Size Reduction
- Integr. Half Bridge Module incl. DC Link Caps and Drivers

- 2 Parallel Chips / Switch
- Embedded in PCB

- 8 mm Smaller than Conv. Design
- Extremely Low DC Link Indutance
- Driver Directly on Top of Switches
- Very Low Gate Inductance



# Thank You!

# Questions