Accurate Small-Signal Model for the Digital Control of an Automotive Bidirectional Dual Active Bridge

Florian Krismer, *Student Member, IEEE*, and Johann W. Kolar, *Senior Member, IEEE*

***Abstract*—The derivation of an accurate small-signal model for a galvanically isolated, bidirectional dc–dc converter and the implementation of a corresponding controller on a DSP as well as key methods and functions required for the digital implementation are detailed in this paper. The investigated dc–dc converter, an automotive dual active bridge (DAB) system, enables power transfer between a low-voltage port (ranging from 11 to 16 V) and an HV port (240 to 450 V). The nominal power rating is 2 kW. The developed small-signal model yields highly accurate results for the DAB system, but the proposed modeling procedure could also be applied to arbitrary resonant power converters with unidirectional or bidirectional power transfer.**

***Index Terms*—DC–DC power conversion, digital control, discrete-time systems, measurement, transient analysis.**

I. Introduction

LEGISLATION requiring lower CO_2 emissions, increasing fuel prices, and growing customer demands for increased vehicle performance present strong incentives for vehicle manufacturers to significantly improve their cars and, in particular, increase the efficiency and the performance of the vehicle drive trains. Current proposals support a hybrid electric vehicle drive train, where an electric motor and an internal combustion engine share the total provided traction power in such a way that the desired performance and/or efficiency characteristic is achieved [1]. With hybrid electric cars, zero local CO_2 emission is not feasible; this can be attained with electric vehicles and hydrogen powered fuel cell vehicles. Electric vehicles, however, require a considerably long time to recharge the battery and the cruising range is significantly below the range attained with hybrid electric vehicles. With a fuel cell car, both zero local CO_2 emission and a high cruising range can be achieved [2].

High-power requirements for the vehicle propulsion demand for an HV drive in order to obtain technically reasonable motor currents whereas the supply voltage for the motor drive is provided with an HVDC bus, e.g., according to the drive train architecture illustrated in Fig. 1. Besides, the conventional 14 V bus (the low-voltage (LV) dc bus), buffered with a 12 V battery, will still exist in future cars to supply conventional vehicle loads (e.g., lighting, electric-motor-driven fans, pumps, and compressors) [2]. In order to enable arbitrary electric power transfer between the HVDC bus and the 14 V bus, a bidirectional dc–dc converter (allows for buck and boost operation) is employed

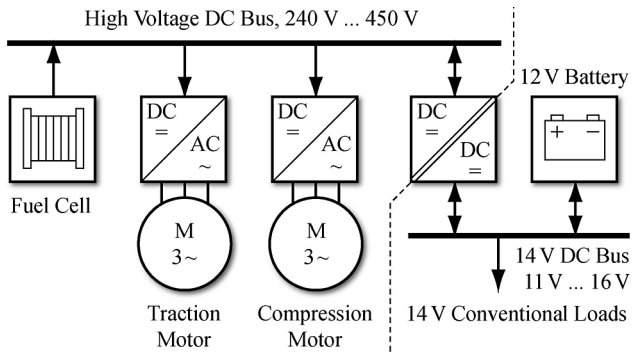


Fig. 1. Fuel cell car system architecture proposed in [3]; the fuel cell is directly connected to an HVDC bus and provides power to the traction motor and the fuel compression motor. A bidirectional dc–dc converter is employed to enable arbitrary power transfer between the HVDC bus and the conventional 14 V dc bus.

(Fig. 1). Boost operation (i.e., power is transferred to the HV port) is required to start the vehicle, and thereafter, during normal car operation, the dc–dc converter transfers power to the 14 V bus to charge the 12 V battery and to provide power to the conventional vehicle loads. For the 14 V bus (V_1), the considered voltage range is between 11 and 16 V. The supply voltage of the drive train (V_2) typically ranges between 240 and 450 V [3].[1] A maximum output power of 2 kW is specified over the given voltage ranges for buck and boost operation; accordingly, large dc currents of up to 200 A result on the LV side. In addition, due to high automotive safety standards and due to the HV ratio between V_1 and V_2, a transformer with galvanic isolation is required [4], [5]. For automotive applications, there is as well demand for a high converter efficiency (more than 90%), high reliability, and high power density [6].

A large number of different topologies of isolated bidirectional dc–dc converters exists. Most prominent are the isolated bidirectional full-bridge converter [7], the bidirectional current doubler (or L-type) converter topology [8], and the dual active bridge (DAB) converter [9]–[11]. For this application, the DAB topology (Fig. 2) was selected due to the following reasons.

1) The low number of passive components (transformer with integrated inductor L and two dc blocking capacitors): the use of large dc inductors is avoided.
2) A high potential regarding the optimization of efficiency or power density: reduced conduction losses, lower switching losses, reduced rms capacitor currents, and/or reduced

Manuscript received March 5, 2009; revised June 5, 2009. Current version published December 28, 2009. Recommended for publication by Associate Editor J. Jatskevich.

The authors are with the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology (ETH) Zurich, Zurich 8092, Switzerland (e-mail: krismer@lem.ee.ethz.ch; kolar@lem.ee.ethz.ch).

Digital Object Identifier 10.1109/TPEL.2009.2027904

[1] According to [3], V_1 may be as low as 8.5 V; for $V_1 < 11$ V, the presented converter (Fig. 2) can still be operated. However, the LV-side dc current is limited to 200 A.

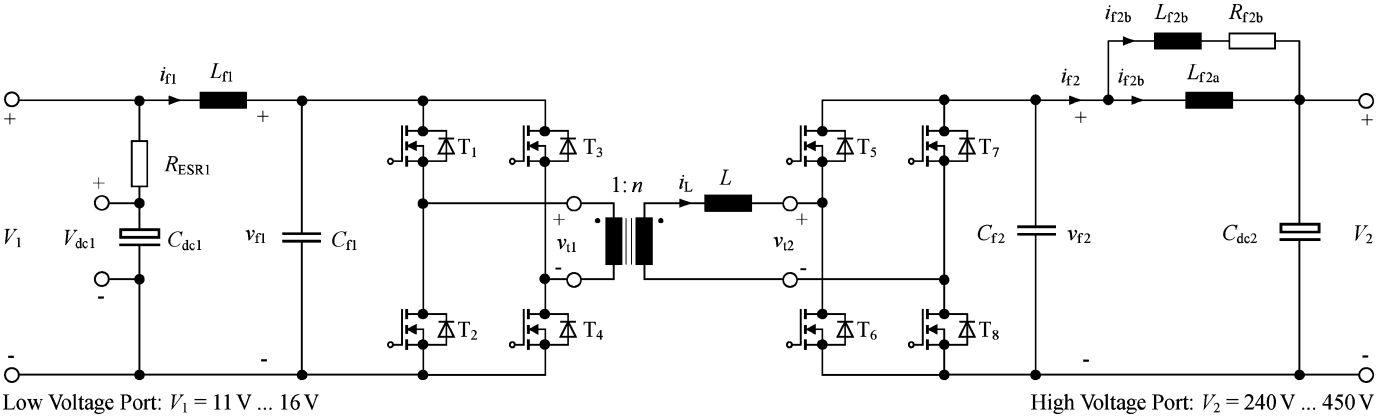


Fig. 2. DAB converter with EMI filters connected to the LV and the HV ports.

transformer core excitation can be achieved with an optimized transformer turns ratio n, an optimized inductance value L, and optimized modulation methods [10], [12]–[15].

3) The DAB employs soft-switching properties, and thus allows for the operation with high switching frequencies; therefore, a highly compact dc–dc converter is feasible.

In order for the presented converter to operate at a designated power level (inclusive of the desired direction of power transfer), a two-loop control structure is employed: the inner control loop adjusts the required current (e.g., on the HV side) and the superimposed voltage control loop regulates the respective output voltage.[2] However, the small-signal model of the DAB converter needs to be determined in order to enable the controller design.

First, small-signal models for switching power converters have been attained with averaged switched circuits [16]. There, a converter circuit diagram results, which partly consists of the original circuit (except for switches and diodes) and additional current sources or voltage sources or both that model the low-frequency system dynamics. It thus presents the effect of small-signal excitations on the system dynamics in a comprehensible way to the engineer. However, its construction requires circuit arrangements and is thus not accomplished in a straightforward way; with the introduction of state-space averaging [17], the automated derivation of small-signal transfer functions has been achieved. Both methods employ the average values of all independent system properties (e.g., inductor currents, capacitor voltages) and all input and output variables (e.g., actuating variable, output current) calculated over one switching period T_S in order to determine the desired transfer functions. A precise small-signal and continuous-time transfer function approximation is thus achieved for frequencies well below $1/T_S$ [16], [29] and well below the filter cutoff frequencies (negligible current and voltage ripples are assumed). These two methods presumably compute wrong transfer functions for the given DAB power converter (Fig. 2), since the assumption of negligible current ripple is not satisfied for the transformer and inductor current i_L. A very accurate, but discrete-time, small-signal model is obtained with the discrete modeling of switching regulators [18] that solely assumes a "small" input signal excitation about a steady-state value in order to reduce the nonlinear (exact) large-signal model to a linear small-signal model.

Today, many applications still employ continuous-time regulators, e.g., low-power and low-cost converters that are used for standard applications and where integrated regulators are available. There, the discrete-time nature of the transfer function obtained with [18] is considered disadvantageous, and thus, numerous extensions to the discrete-time modeling approach have been developed in order to achieve a highly accurate continuous-time small-signal converter model, for instance, the so-called sampled data modeling [19]. For many high-power converters, DSPs are increasingly employed, mainly because by now, a high computational performance is available at a comparably low cost. Advantages of a digital implementation are a considerably higher flexibility compared to analog electronics, a high electromagnetic interference (EMI) immunity, and the enhanced possibility of process and fault monitoring using an external interface or a network connection. Therefore, a digital control platform is employed for the control of the presented DAB, and thus, the discrete-time transfer function obtained with discrete modeling could be used readily for the controller design. However, in [18], only simple dc–dc converters (e.g., boost converter) operated with PWM modulation are focused. An extension to resonant power converters including modulator constraints is presented in [20] and a straightforward summary on the construction of a discrete-time small-signal model for arbitrary resonant converters is discussed in [21]. Merely, the time lag that arises due to software and A/D converter delay times is not considered in [21] and could be included using the procedure discussed in [22].

Up to now, no in-depth analysis on the dynamic properties of the DAB has been presented in the literature. In this paper, an exact discrete-time DAB model including input and output filter dynamics is developed and verified with results obtained from an experimental system. Moreover, a flexible

[2]For power being transferred from the HVDC bus to the 14 V dc bus, V_1 becomes the output voltage (cf., Fig. 2). Hence, the voltage control loop may become very sensitive due to the high electric storage capability of the 12 V battery and the voltage control loop may be simply replaced by a voltage inspection and battery charging algorithm.

TABLE 1
VALUES OF THE FILTER COMPONENTS IN FIG. 2 FOR PHASE-SHIFT MODULATION AND ALTERNATIVE MODULATION

Circuit Component	Value
C_{dc1}	200 mF
R_{ESR1}	4.6 mΩ
L_{f1}	100 nH
C_{f1}	1000 μF
n	24
L	31 μH (phase shift modulation [9]) or 20.6 μH (alternative modulation [13], [15])
R	1.0 Ω
C_{f2}	3.3 μF
L_{f2a}	20 μH
R_{f2a}	10 mΩ
L_{f2b}	10 μH
R_{f2b}	3.1 Ω
C_{dc2}	220 μF

Resistor R considers the DAB conduction losses and is connected in series to L [23]; resistor R_{f2a} is connected in series to L_{f2a} and models its copper losses. For C_{dc1}, a large capacitance of 200 mF is employed in order to decouple the LV port of the DAB and the LV supply line, since the impedance of the connecting cable to the LV supply considerably influences the resulting control-to-output transfer function if smaller capacitance values are used (e.g., for C_{dc1} = 20 mF).

control structure, which allows for optimized modulation and control algorithms, is proposed and detailed. The effect of time delays, mainly due to software processing time, is identified to be crucial with respect to a sufficiently large open-loop phase margin. The obtained results facilitate a significantly simplified construction of the DAB control-to-output transfer function, which can be universally employed to design the digital controllers.

In this paper, the DAB principle of operation as well as the design parameters of the experimental system are presented in Section II. The small-signal model is derived in Section III, the employed control loop is discussed in Section IV, and in Section V, the design of the digital current and voltage controllers is detailed. The results obtained from analytical investigations are verified with measured results in Sections IV and V as well.

II. CONVERTER

The investigated DAB converter in Fig. 2 consists of two full-bridge circuits, which are connected to a high-frequency transformer and a converter inductor L. EMI filters are included on the LV side as well as on the HV side in order to meet the specified EMI requirements; the component values are listed in Table I, and the employed switching frequency is $f_{\mathrm{S}} = 100$ kHz. The experimental system (Fig. 3) contains the two full bridges, the high-frequency transformer, the inductor L, the filter capacitors C_{f1} and C_{f2}, the digital control platform, and the auxiliary power supplies on the LV side and the HV side; the remaining filter components depicted in Fig. 2 are connected externally.

In order for the DAB to transfer power, time-varying voltages $v_{\mathrm{t}_1}(t)$ and $v_{\mathrm{t}_2}(t)$ must be provided from the full-bridge circuits to the high-frequency transformer and the converter inductor L.

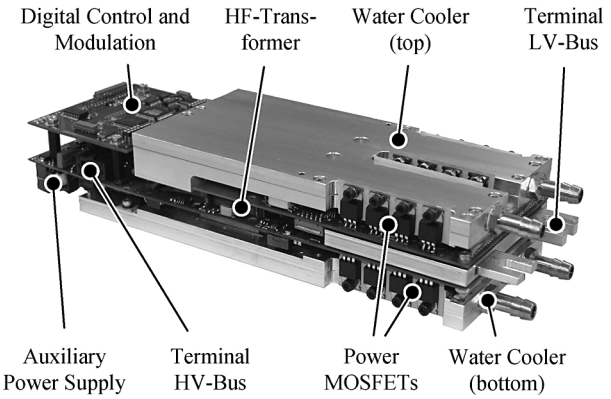


Fig. 3. Automotive DAB converter (273 mm × 90 mm × 53 mm).

Possible values for $v_{\mathrm{t}_1}(t)$ are

$$v_{\mathrm{t}_1}(t) = \begin{cases} +v_{\mathrm{f1}}(t), & \text{for } (\mathrm{T}_1, \mathrm{T}_4 \text{ ON}, \mathrm{T}_2, \mathrm{T}_3 \text{ OFF}) \\ 0, & \text{for } (\mathrm{T}_1, \mathrm{T}_3 \text{ ON}, \mathrm{T}_2, \mathrm{T}_4 \text{ OFF}) \text{ or } (\mathrm{T}_2, \mathrm{T}_4 \text{ ON}, \mathrm{T}_1, \mathrm{T}_3 \text{ OFF}) \\ -v_{\mathrm{f1}}(t), & \text{for } (\mathrm{T}_2, \mathrm{T}_3 \text{ ON}, \mathrm{T}_1, \mathrm{T}_4 \text{ OFF}) \end{cases} \tag{1}$$

(provided that the full bridges are ideal; dead time intervals and failure modes—e.g., bridge leg short circuits–are not considered). Similarly, $v_{\mathrm{t}_2}(t)$ is equal to one of $+v_{\mathrm{f2}}(t)$, 0, and $-v_{\mathrm{f2}}(t)$ depending on the switching states of T_5, T_6, T_7, and T_8. According to Fig. 2, the voltage difference between $nv_{\mathrm{t}_1}(t)$ and $v_{\mathrm{t}_2}(t)$ appears across L, which generates the current

$$i_{\mathrm{L}}(t_1) = i_{\mathrm{L}}(t_0) + \frac{1}{L}\int_{t_0}^{t_1} \left(nv_{\mathrm{t}_1}(t) - v_{\mathrm{t}_2}(t)\right) \mathrm{d}t, \qquad t_0 < t_1 \tag{2}$$

at the time t_1, starting with an initial current $i_{\mathrm{L}}(t_0)$ at time t_0. The expressions for the instantaneous power values on LV and HV sides are

$$p_1(t) = nv_{\mathrm{t}_1}(t) i_{\mathrm{L}}(t) \text{ and } p_2(t) = v_{\mathrm{t}_2}(t) i_{\mathrm{L}}(t) \tag{3}$$

for the DAB without EMI filters and when transformer magnetization current and DAB converter losses are neglected. The average power values over one switching cycle $T_{\mathrm{S}} = 1/f_{\mathrm{S}}$ are finally calculated with

$$P_1 = \frac{1}{T_{\mathrm{S}}}\int_{t_0}^{t_0+T_{\mathrm{S}}} p_1(t)\mathrm{d}t \quad \text{and} \quad P_2 = \frac{1}{T_{\mathrm{S}}}\int_{t_0}^{t_0+T_{\mathrm{S}}} p_2(t)\mathrm{d}t. \tag{4}$$

Three different parameters can be adjusted to control the DAB power level:

1) the phase shift φ between $v_{\mathrm{t}_1}(t)$ and $v_{\mathrm{t}_2}(t)$;
2) the duty ratios of $v_{\mathrm{t}_1}(t)$ and $v_{\mathrm{t}_2}(t)$ (cf., [10]);
3) the switching frequency.

The most common modulation principle, the so-called phase-shift modulation operates the DAB at constant switching frequency and only varies the phase shift φ in order to achieve the required output power [9]. For phase-shift modulation, maximum duty ratios are selected for $v_{\mathrm{t}_1}(t)$ and $v_{\mathrm{t}_2}(t)$; hence, $v_{\mathrm{t}_1}(t)$ is either $-v_{\mathrm{f1}}(t)$ or $v_{\mathrm{f1}}(t)$ and $v_{\mathrm{t}_2}(t)$ is either $-v_{\mathrm{f2}}(t)$ or $v_{\mathrm{f2}}(t)$. Typical waveforms for the inductor current and the transformer voltages during one switching period are depicted in Fig. 4

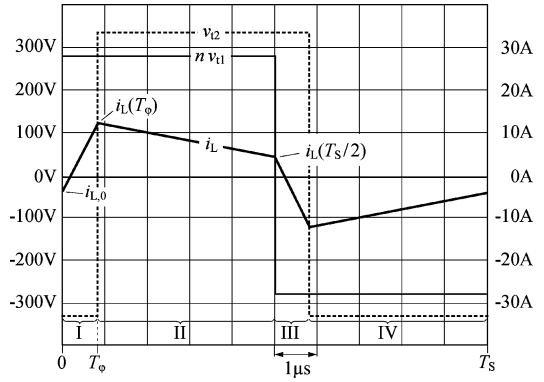


Fig. 4. Transformer voltages and inductor current for phase-shift modulation and nominal operation: $V_1 = 12$ V, $V_2 = 340$ V, and the HV port output power $P_2 = 2$ kW.

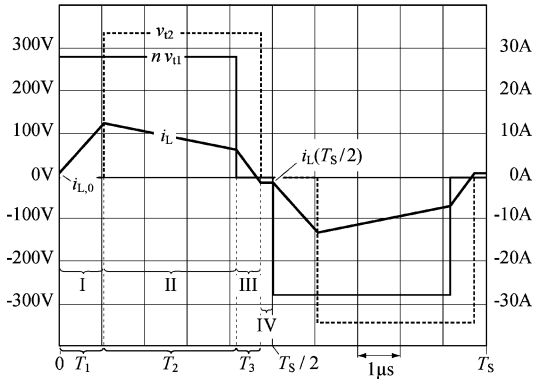


Fig. 5. Transformer voltages and inductor current for the alternative modulation and nominal operation with power transfer from the LV to the HV port ($V_1 = 12$ V, $V_2 = 340$ V, $P_2 = 2$ kW). The durations of the three time intervals I, II, and III are T_1, T_2, and T_3, respectively; the inductor current i_L is slightly negative during time interval IV in order to enable HV-side soft switching.

when the DAB transfers power from the LV port to the HV port at the nominal operating point ($V_1 = 12$ V, $V_2 = 340$ V, $P_2 = 2$ kW). Obviously, the average of the inductor current i_L, evaluated over one switching cycle T_S, is zero, which is required in order to avoid saturation of the high-frequency transformer. The inductor current repeats every half cycle with reversed sign $i_L(t + T_S/2) = -i_L(t)$, since the phase-shift time T_φ and the dc supply voltages V_1 and V_2 remain the same during the first and the second half cycles (time intervals I, II and III, IV in Fig. 4, respectively). Therefore, only the first half cycle (intervals I and II for phase-shift modulation) needs to be considered.

The great advantage of the phase-shift modulation is its simplicity: only a single control variable, the phase-shift angle φ, is required to arbitrarily transfer power according to

$$P_1 = P_2 = \frac{nV_1V_2\varphi(\pi - |\varphi|)}{2\pi^2 f_S L}, \qquad -\frac{\pi}{2} < \varphi < \frac{\pi}{2} \quad (5)$$

(on the assumption of a lossless converter; the derivation of (5) is outlined in [24]). Disadvantages of this modulation are the limited operating range where low switching losses occur (soft-switching range, see [9]) and a large amount of reactive power in the high-frequency transformer that may occur for certain working points when the DAB is operated within wide voltage ranges [15].

In order to increase the converter efficiency, the alternative modulation method discussed in [13] and [15] is employed. There, the phase shift between $v_{t_1}(t)$ and $v_{t_2}(t)$ and the respective duty ratios are adjusted. The resulting inductor current and the transformer voltages are depicted in Fig. 5 for the nominal operating point. This alternative modulation scheme enables considerably higher converter efficiency compared to phase-shift modulation for most operating points within the given voltage ranges. The cost for better converter utilization is mainly the higher complexity: now, a single half cycle consists of four different time intervals that are simultaneously adjusted with three timing parameters T_1, T_2, and T_3.

III. Small-Signal Model

The proposed control structure, depicted in Fig. 6, mainly consists of digital signal processing blocks: the voltage controller ($G_{C,V}$), the current controller ($G_{C,I}$), and the digital filters ($\mathbf{H_{Filter}}$, H_{Avg}) are fully implemented in a DSP; software and A/D converter time delays ($\mathbf{G_{Td,DSP}}$, $\mathbf{G_{Td,FPGA}}$, $\mathbf{G_{Td,meas}}$) are as well due to the digital implementation. Besides, the modulator function ($\mathbf{G_{Mod,PS}}$ or $\mathbf{G_{Mod,TT}}$) is realized in the DSP and determines the required timing values for the DAB [e.g., T_φ for phase-shift modulation based on (5)] with respect to the desired controller set value $I_{2,Mod}$ and the selected modulation scheme. Variations of these timing values dynamically alter the transferred power of the DAB power stage. The resulting changes of the filter currents $i_{f1}(t)$, $i_{f2}(t)$ and the filter voltages $v_{f1}(t)$, $v_{f2}(t)$ (cf., Fig. 2) are obtained from the DAB small-signal model $\mathbf{G_{PE}}$ (the voltages V_{dc1} and V_2 remain approximately constant during one switching period T_S, since very large filter capacitors C_{dc1} and C_{dc2} are considered).

The full control diagram (Fig. 6) indicates two transfer functions, which need to be determined in order to further investigate the control loop: the control-to-output transfer function $\mathbf{G_{PE}}$ of the DAB and the transfer function of the modulator.

A. DAB Power Stage, Phase-Shift Modulation

Phase-shift modulation is the most simple as well as the most common modulation method for the DAB. Therefore, the small-signal transfer function is first derived for this basic modulation scheme.

The small-signal calculation method outlined in [21] regards a single half cycle (e.g., $0 < t \le T_S/2$ in Fig. 4) and separately considers the time intervals between two switching events (time intervals I and II in Fig. 4). Within these time intervals, the time-domain expressions for all system state variables (i.e., all time-varying inductor currents and capacitor voltages) are required in order to determine their sensitivity on input signal variations. With the employed method, the state variables at the end of a half cycle are compared to the state variables at the beginning

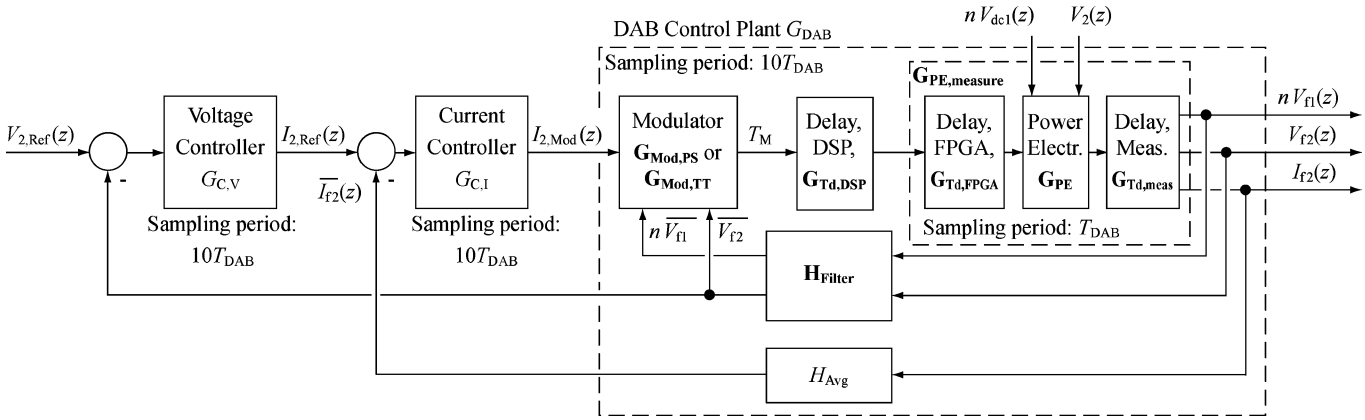


Fig. 6. Investigated control structure including voltage and current control loops for power transfer from the LV to the HV port as well as the modulator function that generates the required timing signals ($T_{\mathrm{M}} = T_\varphi$ for the phase-shift modulation or $\vec{T}_{\mathrm{M}} = (T_1,\, T_2,\, T_3)^{\mathrm{T}}$ for the alternative modulation); gate signal generation (FPGA) as well as power electronics and measurements are sampled with sampling time T_{DAB}, while the remaining transfer functions are sampled with $T = 10T_{\mathrm{DAB}}$ (due to computing time demands).

of the corresponding half cycle. This allows for the formulation of the control-to-output transfer function in the discrete-time domain.

Prior to the derivation of the transfer function, system inputs and outputs must be defined. Clearly, the timing parameter T_φ is an input to the dynamic system. Additionally, the voltages V_{dc1} and V_2 may be considered as inputs as well. The proposed system outputs are the filter current $i_{\mathrm{f2}}(t) = i_{\mathrm{f2a}}(t) + i_{\mathrm{f2b}}(t)$ and the filter voltages $n\,v_{\mathrm{f1}}(t)$, $v_{\mathrm{f2}}(t)$. Further, it is reasonable to collect the system state variables in a state vector

$$\vec{x} = \left(i_{\mathrm{L}} \;\; i_{\mathrm{f1}}/n \;\; i_{\mathrm{f2a}} \;\; i_{\mathrm{f2b}} \;\; nv_{\mathrm{f1}} \;\; v_{\mathrm{f2}}\right)^{\mathrm{T}}. \tag{6}$$

In a next step, the time-domain expressions for the system state variables need to be derived. These may change at each switching time instant, as indicated in Fig. 4. For the sake of clarity, the time-domain expressions during each time interval i are combined to one single function

$$\begin{aligned}\vec{\mathrm{f}}_{\mathrm{PS},i}(\vec{x}_{i-1}, \Delta t_i) = \big(&i_{\mathrm{L},i}(\vec{x}_{i-1}, \Delta t_i) \quad i_{\mathrm{f1},i}(\vec{x}_{i-1}, \Delta t_i)/n \\ &i_{\mathrm{f2a},i}(\vec{x}_{i-1}, \Delta t_i) \quad i_{\mathrm{f2b},i}(\vec{x}_{i-1}, \Delta t_i) \\ &nv_{\mathrm{f1},i}(\vec{x}_{i-1}, \Delta t_i) \quad v_{\mathrm{f2},i}(\vec{x}_{i-1}, \Delta t_i)\big)^{\mathrm{T}}. \end{aligned} \tag{7}$$

In (7), Δt_i denotes the time within the considered time interval (i.e., Δt_i is zero at the beginning of the ith time interval) and $\vec{x}_{i-1}$ contains the initial values, so $\vec{\mathrm{f}}_{\mathrm{PS},i}(\vec{x}_{i-1}, 0) = \vec{x}_{i-1}$; the index "PS" denotes the phase-shift modulation, and the index i specifies the considered time interval. The analysis considers two different time intervals for phase-shift modulation (Fig. 4)

$$\text{Interval I } (i = 1): \quad 0 < t \le T_\varphi \rightarrow \Delta t_1 = t \tag{8}$$

$$\text{Interval II } (i = 2): \quad T_\varphi < t \le T_{\mathrm{S}}/2 \rightarrow \Delta t_2 = t - T_\varphi. \tag{9}$$

The derivation of the time-domain expressions in $\vec{\mathrm{f}}_{\mathrm{PS},i}(\vec{x}_{i-1}, \Delta t_i)$ is associated with a considerable calculation effort and is preferably carried out with a mathematical software tool that allows for symbolic evaluation (e.g., Mathematica, Maple).

In steady state, the system state vector $\vec{x}_{\mathrm{St}}(t)$ (index "St" denotes "steady state") repeats cyclically every switching period. The steady-state values of $\vec{x}_{\mathrm{St}}(t)$ are obtained from

$$\vec{x}_{\mathrm{St}}\left(t + \frac{T_{\mathrm{S}}}{2}\right) = \begin{bmatrix} -1 & \mathbf{0}_{1\times 5} \\ \mathbf{0}_{5\times 1} & \mathbf{I}_{5\times 5} \end{bmatrix} \vec{x}_{\mathrm{St}}(t) = \mathbf{R}\vec{x}_{\mathrm{St}}(t) \tag{10}$$

since the DAB inductor current $i_{\mathrm{L}}(t)$ changes its sign every half cycle in steady state [21] whereas the signs of the filter inductor currents and capacitor voltages remain the same after one half cycle. In order to solve for $\vec{x}_{\mathrm{St}}(t)$ in (9), the time-domain expressions for $\vec{x}(t + T_{\mathrm{S}}/2)$ are required as a function of $\vec{x}(t)$. The derivation of these expressions is described based on the switching sequence shown in Fig. 4 and starts with the unknown values in $\vec{x}(t = 0)$. With (7), (8), and $i = 1$, the general expression for $\vec{x}(t)$ at $t = T_\varphi$ is equal to

$$\vec{x}(T_\varphi) = \vec{\mathrm{f}}_{\mathrm{PS},1}\big(\vec{x}_0, T_\varphi\big) \qquad \text{with } \vec{x}_0 = \vec{x}(0). \tag{11}$$

At $t = T_\varphi$ the switches T_5, T_6, T_7, and T_8 change and time interval II starts. Since capacitor voltages as well as inductor currents cannot change instantaneously, the initial conditions of time interval II are equal to the final state variable values of time interval I, $\vec{x}_1 = \vec{x}(T_\varphi)$. With the time-domain expressions for all state variables during time interval II, the state vector at the end of the half cycle (cf., Fig. 4) becomes

$$\begin{aligned}\vec{x}\left(\frac{T_{\mathrm{S}}}{2}\right) &= \vec{\mathrm{f}}_{\mathrm{PS},2}\left(\vec{x}_1, \frac{T_{\mathrm{S}}}{2} - T_\varphi\right) \\ &= \vec{\mathrm{f}}_{\mathrm{PS},2}\left(\vec{\mathrm{f}}_{\mathrm{PS},1}\big(\vec{x}(0), T_\varphi\big), \frac{T_{\mathrm{S}}}{2} - T_\varphi\right). \end{aligned} \tag{12}$$

The steady-state values are then obtained from the equation system (10) with (12), $\vec{x}_{\mathrm{St}}(t) = \vec{x}(t)$, and $t = 0$.

Besides for the calculation of the steady state, (11) forms the basis for the derivation of the discrete-time small-signal model with sampling time

$$T_{\mathrm{DAB}} = \frac{T_{\mathrm{S}}}{2} = 5\ \mu\mathrm{s}. \tag{13}$$

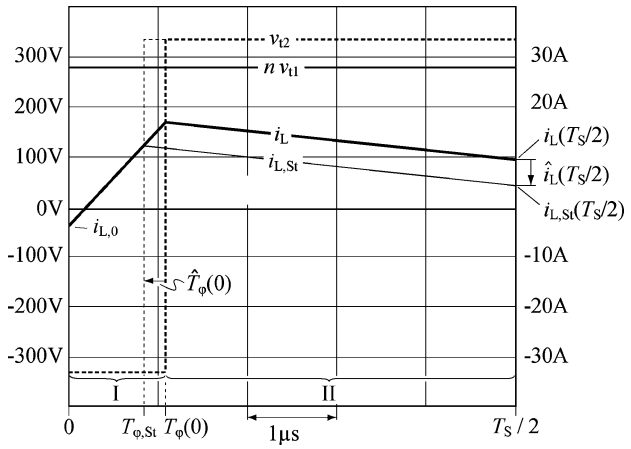


Fig. 7. Reaction of the DAB due to a phase-shift excitation $\hat{T}_\varphi(0)$ (thick lines): at the end of the half cycle $t = T_S/2$, the inductor current deviation $\hat{i}_L(T_S/2)$ results. The thin lines depict steady-state operation according to Fig. 4 (index "St" denotes "steady state"). The digital control electronics determines $T_\varphi(0)$ at $t = 0$, which is applied during $0 < t < T_S/2$.

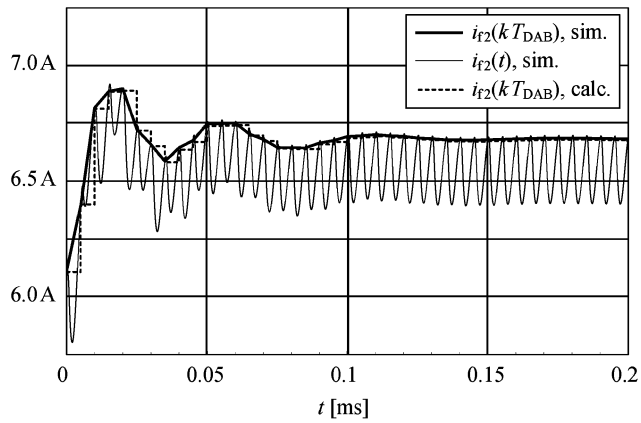


Fig. 8. Simulated step response (solid lines) and calculated step response (dashed line) of $i_{f2}(t)$ for phase-shift modulation, a time step of 100 ns, nominal operating point, and power being transferred from the LV to the HV port. The circuit simulator generates a continuous-time waveform $i_{f2}(t)$, which is sampled after every half cycle $t = kT_{DAB}$, in order to facilitate the comparison to the step response obtained from the discrete-time small-signal transfer function $G_{PE,PS,I_{f2}}$.

The proposed model considers small-signal deviations $\hat{\vec{x}}(t)$ of the system state variables $\vec{x}(t)$ about the steady state $\vec{x}_{St}(t)$

$$\hat{\vec{x}}(t) = \vec{x}(t) - \vec{x}_{St}(t) \tag{14}$$

(the symbol "$\hat{}$" denotes small-signal variables), because of three different kinds of excitations:

1) variations of the state variables due to prior excitations of input variables: $\hat{\vec{x}}_0 = \hat{\vec{x}}(0) = \vec{x}(0) - \vec{x}_{St}(0)$;
2) LV and HV voltage changes: $\hat{\vec{v}}_{g,0} = (n\hat{V}_{dc1}(0)\ \hat{V}_2(0))^T$;
3) excitation of the control input: $\hat{c}_{PS,0} = \hat{T}_\varphi(0)$.

It is important to note that the proposed discrete-time model considers an excitation of any of these variables exactly at the beginning of the half cycle and calculates the respective values of the system state variables at the end of the half cycle (Fig. 7). Consequently, all changes of the input variables $\hat{\vec{v}}_g(t)$ and $\hat{c}_{PS}(t)$ that occur for $0 < t \le T_{DAB}$ are not at all considered in $\hat{\vec{x}}(T_{DAB})$. This limitation only regards transfer functions with continuous-time input signals such as $V_{dc1}(t)$, $V_2(t)$. It does not affect the control-to-output transfer function in a digitally controlled system, provided that the digital controller is synchronized to the power electronics, so $T_\varphi(t)$ changes exactly at $t = kT_{DAB}$, $k \in \mathbb{N}_0$.

The small-signal deviations $\hat{\vec{x}}(T_{DAB})$ at the end of the half cycle are then obtained from a linear approximation [21]

$$\hat{\vec{x}}(T_{DAB}) \approx \mathbf{A}\hat{\vec{x}}_0 + \mathbf{B_{PS}}\hat{c}_{PS,0} + \mathbf{C}\hat{\vec{v}}_{g,0} \tag{15}$$

whereas the three terms $\mathbf{A}\hat{\vec{x}}_0$, $\mathbf{B_{PS}}\hat{c}_{PS,0}$, and $\mathbf{C}\hat{\vec{v}}_{g,0}$ express the small-signal deviations of the state variables at $t = T_{DAB}$ as a result of excitations in $\hat{\vec{x}}_0$, $\hat{c}_{PS,0}$, and $\hat{\vec{v}}_{g,0}$, respectively. The expressions for $\mathbf{A}$, $\mathbf{B_{PS}}$, and $\mathbf{C}$ are given in [25].

Expression (15) allows for the derivation of the required small-signal transfer functions: according to [21] and [25], the z-domain control-to-output transfer functions are calculated with

$$\underset{3\times1}{\mathbf{G}_{\mathbf{PE,PS}}} = \begin{bmatrix} G_{PE,PS,I_{f2}} \\ G_{PE,PS,V_{f1}} \\ G_{PE,PS,V_{f2}} \end{bmatrix} = \mathbf{E}^T(z_{DAB}\mathbf{I} - \mathbf{QRAQ})^{-1}\mathbf{QRB_{PS}} \tag{16}$$

$$\underset{6\times6}{\mathbf{Q}} = \begin{bmatrix} \operatorname{sgn}(i_{L,0}) & \underset{1\times5}{\mathbf{0}} \\ \underset{5\times1}{\mathbf{0}} & \underset{5\times5}{\mathbf{I}} \end{bmatrix} \quad \underset{6\times6}{\mathbf{R}} = \begin{bmatrix} -1 & \underset{1\times5}{\mathbf{0}} \\ \underset{5\times1}{\mathbf{0}} & \underset{5\times5}{\mathbf{I}} \end{bmatrix} \tag{17}$$

and $z_{DAB} = e^{sT_{DAB}}$. In order to collect the three control-to-output transfer functions with the output variables $I_{f2}(z_{DAB})$, $nV_{f1}(z_{DAB})$, and $V_{f2}(z_{DAB})$ in one matrix $\mathbf{G_{PE,PS}}$

$$\underset{3\times1}{\mathbf{G}_{\mathbf{PE,PS}}} = \left[\frac{I_{f2a}(z_{DAB}) + I_{f2b}(z_{DAB})}{T_\varphi(z_{DAB})} \quad \frac{nV_{f1}(z_{DAB})}{T_\varphi(z_{DAB})} \quad \frac{V_{f2}(z_{DAB})}{T_\varphi(z_{DAB})}\right]^T \tag{18}$$

the matrix $\mathbf{E}^T$ in (16) becomes

$$\mathbf{E}^T = \begin{bmatrix} 0 & 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}. \tag{19}$$

The small-signal transfer functions in (16) have been verified for various operating points with results from a circuit simulator (e.g., the control-to-output transfer function $G_{PE,PS,I_{f2}}$ in Fig. 8). Simulated and calculated results show very good agreement for all investigated operating points.

B. DAB Power Stage, Alternative Modulation

If the DAB converter is operated with phase-shift modulation within wide voltage ranges, its efficiency drops considerably for

certain operating points (i.e., for $V_2/V_1 \ll n$ or $V_2/V_1 \gg n$). The average DAB converter efficiency is substantially increased with an alternative modulation scheme [15], which is based on the modulation scheme with triangular and trapezoidal transformer current [13] (index "TT" denotes all variables regarding the alternative modulation).

The derivations of the small-signal transfer functions for phase-shift modulation and alternative modulation are very similar. However, phase-shift modulation requires only one control input T_φ whereas three control inputs T_1, T_2, and T_3 are needed for the alternative modulation.

Fig. 5 depicts typical voltage and current waveforms for the DAB with alternative modulation. Again, one single half cycle is segmented into the time intervals where no switching occurs

Interval I ($i = 1$): $0 < t \le T_1 \quad \rightarrow \Delta t_1 = t$

Interval II ($i = 2$): $T_1 < t \le T_1 + T_2 \rightarrow \Delta t_2 = t - T_1$

Interval III ($i = 3$): $T_1 + T_2 < t \le T_1 + T_2 + T_3$
$\rightarrow \Delta t_3 = t - (T_1 + T_2)$

Interval IV ($i = 4$): $T_1 + T_2 + T_3 < t \le \frac{T_\mathrm{S}}{2}$
$\rightarrow \Delta t_4 = t - (T_1 + T_2 + T_3)$.

This together with (6) and the time-domain expressions for all state variables within time interval i, $\vec{\mathrm{f}}_{\mathrm{TT},i}(\vec{x}_{i-1},\, \Delta t_i)$ [cf., (7)] facilitates the derivation of the system state values at the end of the half cycle (Fig. 5)

$$\vec{x}\left(\frac{T_\mathrm{S}}{2}\right) = \vec{\mathrm{f}}_{\mathrm{TT},4}\big(\vec{\mathrm{f}}_{\mathrm{TT},3}\big(\vec{\mathrm{f}}_{\mathrm{TT},2}\big(\vec{\mathrm{f}}_{\mathrm{TT},1}\big(\vec{x}(0),\, T_1\big),\, T_2\big),\, T_3\big),\, T_4\big) \tag{20}$$

whereas $T_4 = T_\mathrm{S}/2 - (T_1 + T_2 + T_3)$.

The solution to the equation system formed with (10) and (20) determines the steady-state values for $\vec{x}_{\mathrm{St}}(t) = \vec{x}(t)$ at $t = 0$.

Equation (20) also denotes the starting point for the small-signal transfer function derivation. In contrast to the phase-shift modulation, the control input variable is now vector-valued

$$\hat{\vec{c}}_{\mathrm{TT},0} = (\hat{T}_1(0) \quad \hat{T}_2(0) \quad \hat{T}_3(0))^\mathrm{T} \tag{21}$$

and the small-signal vectors $\hat{\vec{x}}_0$ and $\hat{\vec{v}}_{\mathrm{g},0}$ remain unchanged. Consequently, the system states at the end of the half cycle can be approximately calculated with

$$\hat{\vec{x}}(T_\mathrm{DAB}) \approx \mathbf{A}\hat{\vec{x}}_0 + \mathbf{B_{TT}}\hat{\vec{c}}_{\mathrm{TT},0} + \mathbf{C}\hat{\vec{v}}_{\mathrm{g},0} \tag{22}$$

($\mathbf{A}$, $\mathbf{B_{TT}}$, and $\mathbf{C}$ are derived in [25]). The control-to-output transfer functions are collected in the matrix

$$\underset{3\times3}{\mathbf{G}}_{\mathbf{PE,TT}} = \big[\, \vec{G}_{\mathrm{PE,TT},1} \quad \vec{G}_{\mathrm{PE,TT},2} \quad \vec{G}_{\mathrm{PE,TT},3} \,\big]$$

$$\vec{G}_{\mathrm{PE,TT},i} = \begin{pmatrix} \dfrac{I_{\mathrm{f2a}}(z_\mathrm{DAB}) + I_{\mathrm{f2b}}(z_\mathrm{DAB})}{T_i(z_\mathrm{DAB})} \\ \dfrac{nV_{\mathrm{f1}}(z_\mathrm{DAB})}{T_i(z_\mathrm{DAB})} \\ \dfrac{V_{\mathrm{f2}}(z_\mathrm{DAB})}{T_i(z_\mathrm{DAB})} \end{pmatrix} \tag{23}$$

($i = 1, 2, 3$), which is derived based on (22) with (17) and (19)

$$\underset{3\times3}{\mathbf{G}}_{\mathbf{PE,TT}} = \mathbf{E}^\mathrm{T}(z_\mathrm{DAB}\mathbf{I} - \mathbf{QRAQ})^{-1}\mathbf{QRB_{TT}}. \tag{24}$$

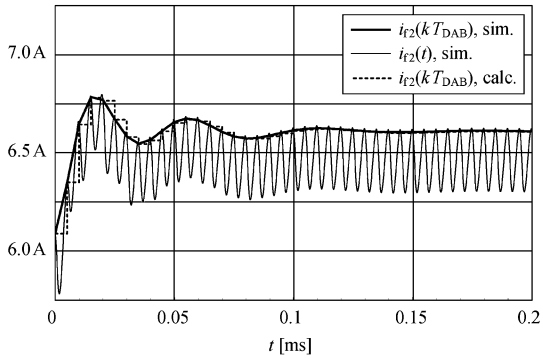


Fig. 9. Simulated step response (solid lines) and calculated step response (dashed line) of $i_{\mathrm{f2}}(t)$ when the alternative modulation is applied with a time step $\hat{T}_1 = 100$ ns $\sigma(t)$ and $\hat{T}_2 = \hat{T}_3 = 0$, nominal operation, and power being transferred from the LV to the HV port. The continuous-time waveform $i_{\mathrm{f2}}(t)$ is again sampled after every half cycle in order to facilitate the comparison to the step response obtained from the discrete-time small-signal model.

The small-signal transfer functions in (23) have been verified with a circuit simulator. Very good agreement between simulation and calculation has been obtained for all investigated operating points [e.g., for nominal operation in Fig. 9, which shows the step response of the control-to-output transfer function $G_{\mathrm{PE,TT},1,I_{\mathrm{f2}}}$ with input $T_1(z_\mathrm{DAB})$ and output $I_{\mathrm{f2}}(z_\mathrm{DAB})$].

C. Modulator

The modulator calculates the control variables depending on the applied modulation scheme, the set current $i_{2,\mathrm{Mod}}$, and the measured values $n\overline{v}_{\mathrm{f1}}$ and $\overline{v}_{\mathrm{f2}}$, obtained from nv_{f1} and v_{f2}. The modulator function for phase-shift modulation

$$c_\mathrm{PS} = T_\varphi = \mathrm{f}_{\mathrm{Mod,PS}}(i_{2,\mathrm{Mod}}(kT),\, n\overline{v}_{\mathrm{f1}}(kT),\, \overline{v}_{\mathrm{f2}}(kT)) \tag{25}$$

is derived in the time domain from (5) for a lossless DAB (the sampling time T is defined with (29), $k \in \mathbb{Z}$, and variables with lowercase letters denote time-domain functions, e.g., $i_{2,\mathrm{Mod}}(kT)$ is equal to the sum of the steady-state dc component $I_{2,\mathrm{Mod,St}}$ and the small-signal disturbance $\mathcal{Z}^{-1}\{I_{2,\mathrm{Mod}}(z)\}$: $i_{2,\mathrm{Mod}}(kT) = I_{2,\mathrm{Mod,St}} + \mathcal{Z}^{-1}\{I_{2,\mathrm{Mod}}(z)\}$). The expressions for the alternative modulation

$$\begin{aligned}\vec{c}_\mathrm{TT} &= (T_1 \;\; T_2 \;\; T_3)^\mathrm{T} \\ &= \vec{\mathrm{f}}_{\mathrm{Mod,TT}}(i_{2,\mathrm{Mod}}(kT), n\overline{v}_{\mathrm{f1}}(kT), \overline{v}_{\mathrm{f2}}(kT))\end{aligned} \tag{26}$$

become rather large; hence, their evaluation in the DSP is avoided. Instead, precalculated values stored in DSP memory tables are used together with the fast linear interpolation algorithm presented in [25].[3] Since the modulator function is static, the small-signal transfer function is simply determined with the respective derivatives at the operating point. Thus, the transfer functions for phase-shift modulation are

$$\underset{1\times3}{\mathbf{G}}_{\mathbf{Mod,PS}} = \begin{bmatrix} \dfrac{\partial \mathrm{f}_{\mathrm{Mod,PS}}}{\partial i_{2,\mathrm{Mod}}} & \dfrac{\partial \mathrm{f}_{\mathrm{Mod,PS}}}{\partial (n\overline{v}_{\mathrm{f1}})} & \dfrac{\partial \mathrm{f}_{\mathrm{Mod,PS}}}{\partial \overline{v}_{\mathrm{f2}}} \end{bmatrix} \tag{27}$$

[3]The use of tables also facilitates compensation of nonlinear effects due to losses (e.g., DAB model discussed in [23]) and due to deadband effects [11].

and for the alternative modulation

$$\underset{3\times 3}{\mathbf{G}_{\mathbf{Mod,TT}}} = \left[\frac{\partial \vec{\mathrm{f}}_{\mathrm{Mod,TT}}}{\partial i_{2,\mathrm{Mod}}} \quad \frac{\partial \vec{\mathrm{f}}_{\mathrm{Mod,TT}}}{\partial (n\overline{v}_{\mathrm{f1}})} \quad \frac{\partial \vec{\mathrm{f}}_{\mathrm{Mod,TT}}}{\partial \overline{v}_{\mathrm{f2}}} \right]. \quad (28)$$

$\mathbf{G_{Mod,PS}}$ and $\mathbf{G_{Mod,TT}}$ are evaluated at the operating point with the steady-state values of $i_{2,\mathrm{Mod}}$, $\overline{v}_{\mathrm{f1}}$, and $\overline{v}_{\mathrm{f2}}$.

IV. DAB Digital Control Loop

In the given laboratory setup, the average DAB output voltage is controlled (e.g., $\overline{V}_{\mathrm{f2}}$ in Fig. 6 for power transfer from LV to HV). The proposed control loop consists of an inner loop with a proportional–integral (PI) controller $G_{\mathrm{C,I}}$, which controls $\overline{I}_{\mathrm{f2}}(z)$, and an outer loop with another PI controller $G_{\mathrm{C,V}}$, which controls the output voltage. Depending on the power transfer direction, the average output voltage can be either $\overline{V}_{\mathrm{f2}}(z)$ for power transfer from the LV port to the HV port or $n\overline{V}_{\mathrm{f1}}(z)$ for the opposite direction.

According to Fig. 6, the current controller $G_{\mathrm{C,I}}$ outputs $I_{2,\mathrm{Mod}}(z)$ and connects to the modulator $\mathbf{G_{Mod}}$. The modulator then calculates the DAB timing parameters in order to achieve the required power transfer. Since the current controller solely operates on the difference between $\overline{I}_{\mathrm{f2}}(z)$ and $I_{2,\mathrm{ref}}(z)$, G_{DAB} is a single-input–single-output transfer function with set current input $I_{2,\mathrm{Mod}}(z)$ and HV-side current output $\overline{I}_{\mathrm{f2}}(z)$. However, there is internal feedback in the transfer function G_{DAB}, since $n\overline{V}_{\mathrm{f1}}(z)$ and $\overline{V}_{\mathrm{f2}}(z)$ are required for the modulator; this must be considered in order to determine G_{DAB}.

Except for the DAB small-signal transfer function matrix $\mathbf{G_{PE}}$ (equal to $\mathbf{G_{PE,PS}}$ or $\mathbf{G_{PE,TT}}$), all transfer functions in Fig. 6 are part of the digital system and either reside in the DSP or in the field-programmable gate array (FPGA). Relatively simple z-domain transfer functions result for the modulator $\mathbf{G_{Mod}}$ (Section III-C), the time delays $\mathbf{G_{Td,DSP}}$, $\mathbf{G_{Td,FPGA}}$, and $\mathbf{G_{Td,meas}}$, the moving average filters $\mathbf{H_{Filter}}$ and H_{Avg}, as well as for the controllers $G_{\mathrm{C,V}}$ and $G_{\mathrm{C,I}}$. This section focuses on these transfer functions in order to complete the derivation of G_{DAB}. The obtained transfer function is finally compared to a transfer function based on a simplified DAB model that allows for a significantly reduced calculation effort.

A. System Sampling Rate

The small-signal model of the power stage results in a z-domain transfer function with sampling time T_{DAB} [cf., (12)]. Due to the required DSP calculation time, the DAB timing parameters are only updated every $10\,T_{\mathrm{DAB}}$; therefore, the DSP sampling time is

$$T = 10\,T_{\mathrm{DAB}} = 50\ \mu\mathrm{s} \qquad z = \mathrm{e}^{sT}. \quad (29)$$

Hence, all transfer functions with faster update rate, such as $\mathbf{G_{PE}}$ and voltage and current measurements (Fig. 6), need to be resampled (e.g., with the method outlined in [25]).

B. Time Delays

The implemented software acquires three measurements during one calculation period T in order to achieve higher noise immunity. The resulting time delay in $\mathbf{G_{Td,meas}}$ is $10\,T_{\mathrm{DAB}}$ for the first measurement, $8\,T_{\mathrm{DAB}}$ for the second, and $6\,T_{\mathrm{DAB}}$ for the third measurement. The FPGA ($\mathbf{G_{Td,FPGA}}$) causes an additional time delay of $2T_{\mathrm{DAB}}$ in order to apply the new timing values to the power electronics. FPGA and measurement time delays sum up to a total time delay of $12\,T_{\mathrm{DAB}}$ for the first measurement, and $10\,T_{\mathrm{DAB}}$ and $8\,T_{\mathrm{DAB}}$ for the two subsequent measurements. The DSP calculates the average of the three measured values and

$$\mathbf{G_{PE,measure}}(z_{\mathrm{DAB}}) = \frac{z_{\mathrm{DAB}}^{-12} + z_{\mathrm{DAB}}^{-10} + z_{\mathrm{DAB}}^{-8}}{3} \mathbf{G_{PE}}(z_{\mathrm{DAB}}) \quad (30)$$

results for that part of G_{DAB} which is updated with the higher sampling rate T_{DAB} (Fig. 6). The sampling rate of this transfer function finally needs to be converted to the system sampling rate T (cf., [25])

$$\mathbf{G_{PE,measure}}(z_{\mathrm{DAB}}) \underset{\text{resample}}{\rightarrow} \mathbf{G_{r,PE,measure}}(z). \quad (31)$$

The DSP causes another time delay of T in order to carry out all calculations; therefore,

$$G_{\mathrm{Td,DSP,PS}}(z) = z^{-1} \quad (32)$$

$$\mathbf{G_{Td,DSP,TT}}(z) = \mathrm{diag}\left(z^{-1}, z^{-1}, z^{-1}\right) \quad (33)$$

for phase shift or alternative modulation, respectively.

C. Moving Average Filters

The z-domain transfer function of the implemented Nth order moving average filter

$$H_{\mathrm{Avg}}(z) = \frac{1}{N} \sum_{i=0}^{N-1} z^{-i} \quad (34)$$

calculates the average over N previously measured values $x(0)$, $x(T), \ldots, x((N-1)T)$; the present software implementation uses $N = 5$. The moving average filter is applied to $I_{\mathrm{f2}}(z)$, $nV_{\mathrm{f1}}(z)$, and $V_{\mathrm{f2}}(z)$. The filter regarding I_{f2} is included in G_{DAB} (Section IV-D), and the feedback transfer function $\mathbf{H_{Filter}}$ contains the remaining two filter functions

$$\mathbf{H_{Filter}}(z) = \mathrm{diag}\left(H_{\mathrm{Avg}}, H_{\mathrm{Avg}}\right). \quad (35)$$

D. DAB Control Plant G_{DAB}

The transfer function G_{DAB} is calculated according to [25, Appendix D]

$$G_{\mathrm{DAB}} = \frac{\overline{I}_{\mathrm{f2}}}{I_{2,\mathrm{Mod}}} = H_{\mathrm{Avg}}(G_{00} + \mathbf{G_{0r}}\mathbf{H}\left(\mathbf{I} - \mathbf{G_{sr}}\mathbf{H}\right)^{-1}\mathbf{G_{s0}}) \quad (36)$$

with G_{00}, $\mathbf{G_{0r}}$, $\mathbf{G_{sr}}$, and $\mathbf{G_{s0}}$ summarized in the matrix $\mathbf{G}$

$$\mathbf{G} = \begin{bmatrix} G_{00} & \underset{1\times n}{\mathbf{G_{0r}}} \\ \underset{m\times 1}{\mathbf{G_{s0}}} & \underset{m\times n}{\mathbf{G_{sr}}} \end{bmatrix} \quad (37)$$

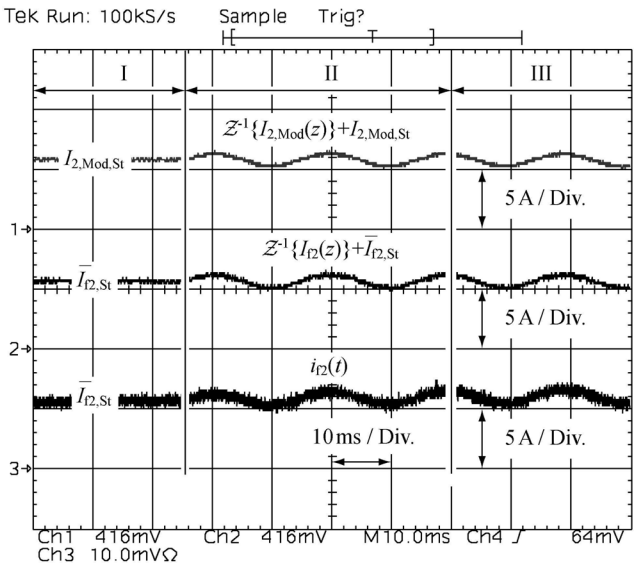


Fig. 10. Current waveforms for the proposed measurement of the control-to-output transfer functions: during time interval I, the converter settles the desired operating point, time interval II is used to avoid transient effects, and during time interval III gain and phase are measured (cf., Fig. 11). The converter is voltage and current controlled during time interval I and is operated in open loop during time intervals II and III with a sinusoidal waveform $\mathcal{Z}^{-1}\{I_{2,\mathrm{Mod}}(z)\}$ being superimposed on $I_{2,\mathrm{Mod,St}}$. The depicted example employs an excitation amplitude of 500 mA at a frequency of 51 Hz; nominal operation is selected (i.e., $V_1 = 12$ V, $V_2 = 340$ V, and the HV port output power is $P_2 = 2$ kW). The waveform $i_{\mathrm{f2}}(t)$ is measured with an analog current probe in order to allow for a comparison between digital and analog signals. Time interval III is not fully depicted; its duration is equal to 50 ms.

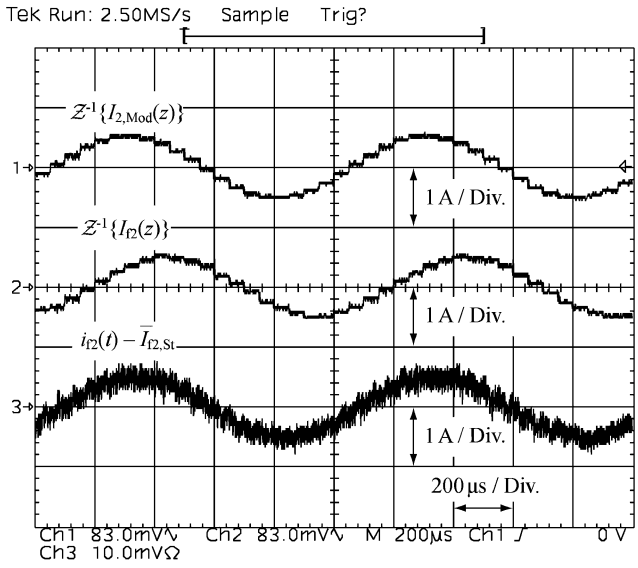


Fig. 11. Measurement method employed to determine the DAB transfer function: during time interval III (cf., Fig. 10), amplitude and phase of the generated sinusoidal time series $\mathcal{Z}^{-1}\{I_{2,\mathrm{Mod}}(z)\}$ are compared to amplitude and phase of the measured time series $\mathcal{Z}^{-1}\{I_{\mathrm{f2}}(z)\}$ in order to obtain gain and phase shift for one frequency of the control-to-output transfer function (for this, only ac components are regarded—the dc components $I_{2,\mathrm{Mod,St}}$ and $\overline{I}_{\mathrm{f2,St}}$ are not considered). The depicted example employs an excitation amplitude of 500 mA at a frequency of 1 kHz and nominal converter operation. The waveform $i_{\mathrm{f2}}(t)$ is measured with an analog current probe in order to allow for a comparison between digital and analog signals.

(cf., [25, eq. (56)]). According to [25, Fig. 12] and Fig. 6, $\mathbf{G}$ and $\mathbf{H}$ become

$$\mathbf{G} = \mathbf{G}_{\mathbf{r,PE,measure,PS}} G_{\mathrm{Td,DSP,PS}} \mathbf{G}_{\mathbf{Mod,PS}}$$
$$\mathbf{H} = \mathbf{H}_{\mathbf{Filter}} \tag{38}$$

for phase-shift modulation and

$$\mathbf{G} = \mathbf{G}_{\mathbf{r,PE,measure,TT}} \mathbf{G}_{\mathbf{Td,DSP,TT}} \mathbf{G}_{\mathbf{Mod,TT}}$$
$$\mathbf{H} = \mathbf{H}_{\mathbf{Filter}} \tag{39}$$

if the alternative modulation is employed.

E. Experimental Verification

The control-to-output transfer function $I_{\mathrm{f2}}/I_{2,\mathrm{Mod}}$ (cf., Fig. 6) is measured using a sinusoidal current sequence superimposed on the steady-state modulator current value $I_{2,\mathrm{Mod,St}}$ (Figs. 10 and 11). The proposed measurement sequence consists of three different time intervals (Fig. 10).

1) *Time interval I* is used to settle the desired converter operating point. Therefore, controlled converter operation is needed during time interval I.
2) At the beginning of *time interval II*, the steady-state value $I_{2,\mathrm{Mod,St}}$ is stored in the DSP, and thereafter, current and voltage controllers are turned off. Hence, the converter is operated in open loop during time interval II. The stored value $I_{2,\mathrm{Mod,St}}$ and a superimposed sinusoidal time series $\mathcal{Z}^{-1}\{I_{2,\mathrm{Mod}}(z)\}$, calculated in the DSP, with a given amplitude and the desired excitation frequency are used to generate a sinusoidal current excitation about the steady-state operating point. The DSP measures the current i_{f2}, which results in the time series $\overline{I}_{\mathrm{f2,St}} + \mathcal{Z}^{-1}\{I_{\mathrm{f2}}(z)\}$. During time interval II, however, the DSP discards the measured current values in order to eliminate transient effects.
3) During *time interval III*, the DSP continues to generate the dc shifted sinusoidal time series (Figs. 10 and 11) and stores the generated modulator current values $I_{2,\mathrm{Mod,St}} + \mathcal{Z}^{-1}\{I_{2,\mathrm{Mod}}(z)\}$ and the measured current values $\overline{I}_{\mathrm{f2,St}} + \mathcal{Z}^{-1}\{I_{\mathrm{f2}}(z)\}$ in an on-chip table; the measurement sequence completes after time interval III has elapsed. In a postprocessing pass, the tabulated current values are refined with a finite-impulse response (FIR) filter in order to suppress noise and accurately obtain gain and phase of the control-to-output transfer function at the employed excitation frequency. The outlined procedure is repeated for each data point depicted in Fig. 12.

The obtained results for phase-shift modulation [Fig. 12(a) and (b)] and for the alternative modulation [Fig. 12(c) and (d)] illustrate a very good match between calculated and measured transfer functions. A maximum difference of 2 dB between calculated and measured gain occurs for phase-shift operation at 9.75 kHz (almost equal to the Nyquist frequency of 10 kHz). For the results depicted in Figs. 12 and 14 and for frequencies below 8 kHz, a maximum gain difference of less than ± 0.7 dB is achieved; the phase differences are smaller than $\pm 10°$.

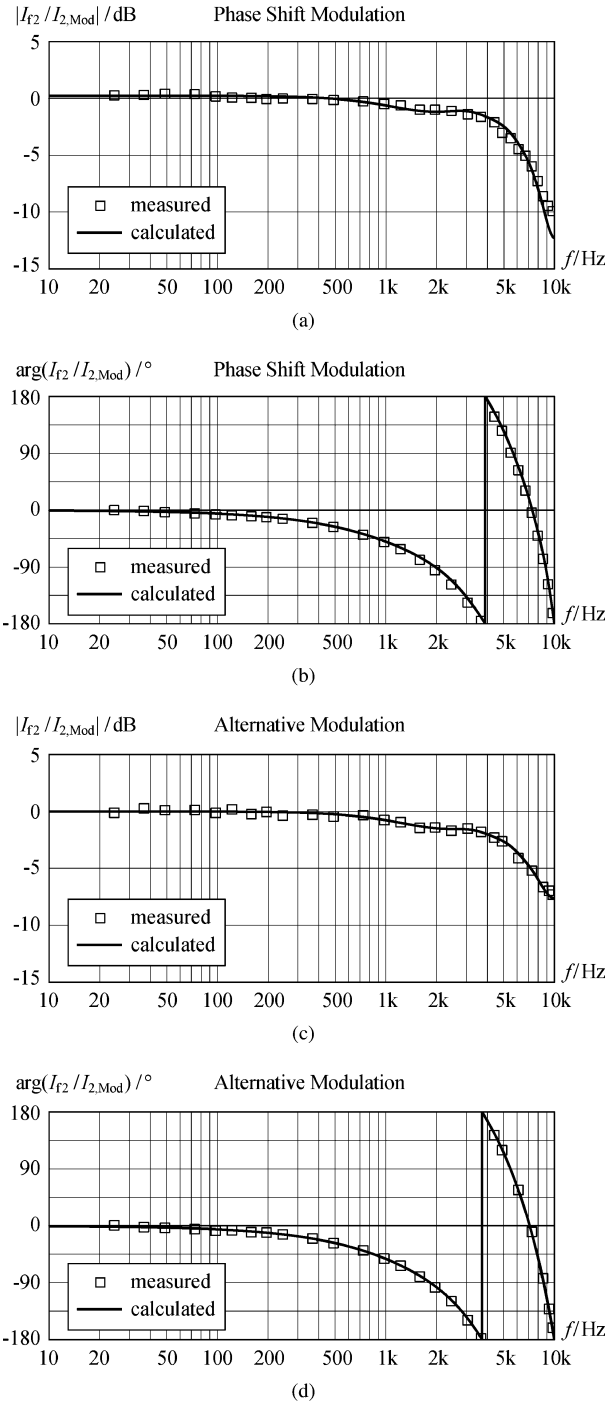


Fig. 12. Calculated and measured DAB frequency response for phase shift operation [(a) gain and (b) phase] and for the alternative modulation method [(c) gain and (d) phase]; the Nyquist frequency $1/(2T) = 10$ kHz limits the maximum possible frequency; the solid line denotes the calculated frequency response and the boxes mark the measured values. The DAB is operated with $V_1 = 12$ V, $V_2 = 340$ V, and with 2 kW output power at the HV port.

F. Derivation of a Simplified G_{DAB}

In the proposed system, all time constants of the EMI filters are significantly smaller than the time delay caused by the digital controller. The question may now arise whether a simple DAB converter model that neglects the couplings between the input filter, the output filter, and the DAB power stage itself would be sufficiently accurate in order to design current and voltage controllers. For steady-state operation, the employed modulator functions $\mathbf{G_{Mod,PS}}$ or $\mathbf{G_{Mod,TT}}$ already generate almost correct timing parameters, i.e., $I_{\mathrm{f2}} \approx I_{2,\mathrm{Mod}}$ and $I_{\mathrm{f1}} \approx I_{2,\mathrm{Mod}} V_2/V_1$ (on the assumption that $V_{\mathrm{f1}} \approx V_1$, $V_{\mathrm{f2}} \approx V_2$, and negligible losses; deviations may occur due to the table interpolation error and parasitic hardware components). Additionally, the total time delay G_{Td} (DSP, FPGA, and measurement) needs to be regarded according to (30), (32), and (33). Thus, the DAB converter in Fig. 2 may be replaced with the two current sources depicted in Fig. 13 (cf., [26]). However, the simplified model may fail when $I_{2,\mathrm{Mod}}$ changes, since the current I_{f2} depends on the actual values of $n\overline{V}_{\mathrm{f1}}$ and $\overline{V}_{\mathrm{f2}}$ as well (cf., Fig. 6).

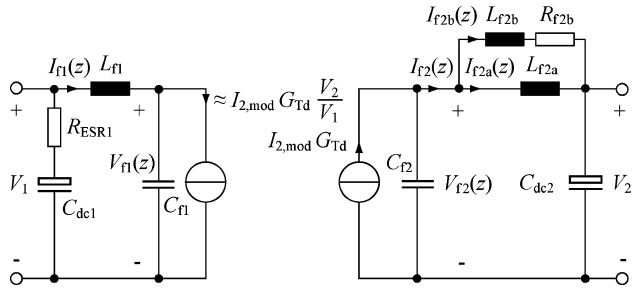


Fig. 13. Simplified circuit of the DAB: the two current sources replace the switches, inductor L, and transformer. For a lossless DAB, the accurate current for the source on the left-hand side would be equal to $\mathcal{Z}\{i_{2,\mathrm{Mod}}(kT)v_{\mathrm{f2}}(kT)/v_{\mathrm{f1}}(kT)\}G_{\mathrm{Td}}$, which is approximately equal to $I_{2,\mathrm{Mod}}(z)G_{\mathrm{Td}}V_2/V_1$ for constant voltages V_1, V_2 and if filter losses as well as variations of V_{f1} and V_{f2} are neglected. Since the simplified circuit contains no switches, it can directly be analyzed by means of Laplace- or Z-transform.

In Fig. 14, the frequency response of G_{DAB} (phase-shift modulation, nominal operation) is compared to the frequency response of the simplified transfer function $G_{\mathrm{DAB,simp}}$ derived from the circuit depicted in Fig. 13. Obviously, the frequency response obtained from the simplified model differs only little from the accurate model, which is mainly due to the digital controller's time delays. Thorough investigations have shown that the simplified model and the accurate model match very well for phase-shift modulation and alternative modulation as well as for all inspected operating points.

V. Current and Voltage Controllers

Due to the large capacitance values of C_{dc1} and C_{dc2}, constant input and output voltages V_1 and V_2 are assumed for the design of the current controller. Further, according to the considerations discussed in Section IV-F, the transfer function G_{DAB} is regarded to be independent of the actual operating point.

The proposed current controller in Fig. 6 is a discrete-time PI controller[4]

$$G_{\mathrm{C,I}} = K_{\mathrm{p,I}} \frac{z - (1 - T/T_{\mathrm{i,I}})}{z - 1} \tag{40}$$

[4]The digital PI controller is obtained from its continuous-time counterpart [27].

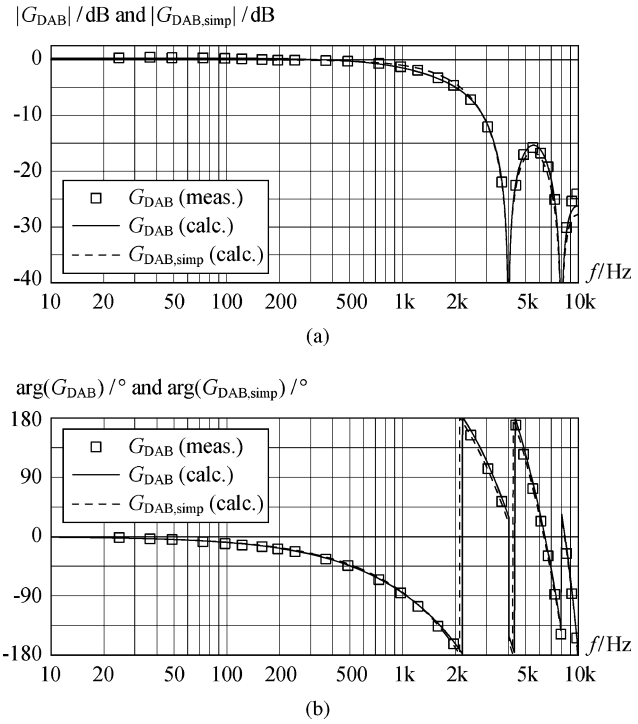


Fig. 14. Frequency response of the accurate transfer function G_{DAB} (solid lines) and the simplified transfer function $G_{\mathrm{DAB,simp}}$ (dashed lines). (a) Gain and (b) phase diagrams; the boxes mark measured values.

with gain $K_{\mathrm{p,I}}$ and cutoff frequency $\omega_{\mathrm{i,I}} = 1/T_{\mathrm{i,I}}$. Consequently, the open-loop transfer function

$$F_{\mathrm{o,I}} = G_{\mathrm{C,I}} G_{\mathrm{DAB}} \tag{41}$$

results. Due to the low-pass behavior of G_{DAB}, the following design method is proposed in order to achieve a high bandwidth of the closed current loop transfer function.

1) Calculation of the controller cutoff frequency such that $|G_{\mathrm{DAB}}|$ at $\omega_{\mathrm{i,I}}$ is 3 dB lower than the dc gain, i.e., $|G_{\mathrm{DAB}}(z_{\mathrm{i,I}})| = |G_{\mathrm{DAB}}(\mathrm{e}^{j0})|/\sqrt{2}$ with $z_{\mathrm{i,I}} = \mathrm{e}^{j\omega_{\mathrm{i,I}}T}$.
2) The controller gain $K_{\mathrm{p,I}}$ is determined in order to achieve a given phase margin Φ_{R}. First, the z-parameter $z_{\Phi_{\mathrm{R}}}$ needs to be determined where the open-loop phase is equal to $-180^\circ + \Phi_{\mathrm{R}}$, $\arg(F_{\mathrm{o,I}}(z_{\Phi_{\mathrm{R}}})/K_{\mathrm{p,I}}) = -180^\circ + \Phi_{\mathrm{R}}$. With this, the controller gain $K_{\mathrm{p,I}} = |1/F_{\mathrm{o,I}}(z_{\Phi_{\mathrm{R}}})|$ can be calculated.

With $\Phi_{\mathrm{R}} = 60^\circ$, the controller parameters $K_{\mathrm{p,I}} = 0.37$ and $T_{\mathrm{i,I}} = 113\ \mu$s result for the given system setup. The calculated and the measured step responses of the closed current control loop are depicted in Fig. 15: since the measured current signals are superimposed by noise, the average of 128 singular current step responses is shown; calculated and measured results match closely. The proposed current controller achieves the rise time $t_{\mathrm{r}} \approx 250\ \mu\mathrm{s} = 5T$ and the delay time $t_{\mathrm{d}} \approx 200\ \mu\mathrm{s} = 4T$ with a percentage overshoot of approximately 7% ($\Delta I_{\mathrm{f2,p}} \approx 70$ mA, $\hat{I}_{\mathrm{2,Ref}} = 1$ A). For the given application, a rise time of less than $500\ \mu$s and a delay time of less than $500\ \mu$s are required, which has been achieved with the given controller design. If a faster response is required, the DSP time delays should be reduced

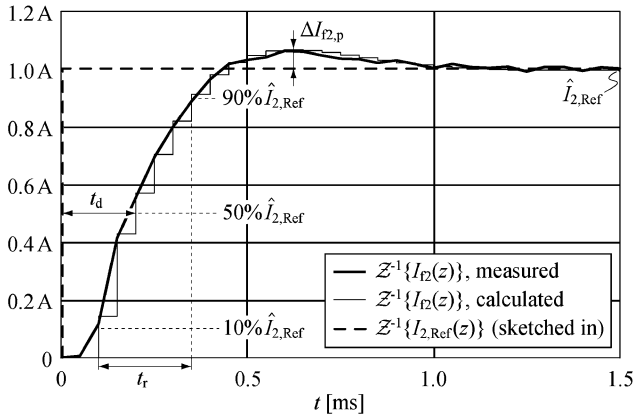


Fig. 15. Measured and calculated unity step response of the closed current control loop; a rise time t_{r} of approximately 250 μs and a delay time t_{d} of approximately 200 μs are achieved.

(optimized algorithm, faster DSP), instead of using a smaller phase margin, to obtain an adequate control performance (fast response and small overshoot), since the time delays caused by the digital controller account for the main part of the proposed converter's phase lag.

The direction of power transfer determines the voltage that needs to be controlled: this is V_1 for power transfer from the HV to the LV port and V_2 for the opposite direction. However, V_1 and V_2 are not measured in the given system, but only v_{f1} and v_{f2} (Fig. 2) are. Therefore, according to the direction of power transfer, either $\overline{V}_{\mathrm{f1}}$ or $\overline{V}_{\mathrm{f2}}$ is controlled and $V_1 \approx \overline{V}_{\mathrm{f1}}$ as well as $V_2 \approx \overline{V}_{\mathrm{f2}}$ is assumed. For the voltage controller, again, a PI controller with the transfer function

$$G_{\mathrm{C,V}} = K_{\mathrm{p,V}} \frac{z - (1 - T/T_{\mathrm{i,V}})}{z - 1} \tag{42}$$

is employed. For power being transferred from the LV to the HV port, the controlled current I_{f2} flows into the output capacitor C_{dc2} and the load. The plant transfer function for the voltage controller ($\overline{V}_{\mathrm{f2}}/I_{\mathrm{2,Ref}}$; cf., Fig. 6) therefore consists of the closed current loop transfer function, the filter impedances L_{f2a}, L_{f2b}, R_{f2b}, and C_{dc2} (Fig. 13), and the load connected to the HV port. When the direction of power transfer changes (HV to LV), then the current I_{f1}, which is not measured in the given system, flows into C_{dc1} and into the load connected to the LV port. However, I_{f1} can be approximated with $I_{\mathrm{f2}}V_2/V_1$ for control purposes, since losses are rather low and the capacitance C_{dc1} is comparably large. The transfer function of the closed current loop again exhibits low-pass characteristics but the output capacitor adds an integration stage to the plant. For this type of plant, the symmetric optimum design method [28] is selected in order to design the voltage controller (in the case of a resistive load, the no-load operation depicts the worst case for the voltage controller design). A phase margin of $\Phi_{\mathrm{R}} = 75^\circ$ leads to $K_{\mathrm{p,V}} = 130\ \mathrm{mA/V}$ and $T_{\mathrm{i,I}} = 14.7$ ms.

In Fig. 16, the measured and the calculated step responses of the voltage controlled system are shown for no-load and for a load resistance of $58\ \Omega \approx (340\ \mathrm{V})^2/2\ \mathrm{kW}$; again, a very good matching between measured and calculated results is achieved.

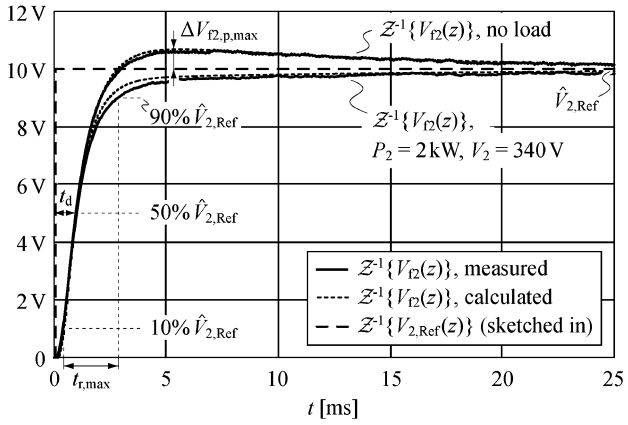


Fig. 16. Step response of the closed voltage control loop for no-load operation and for 2 kW output power at 340 V output voltage; the input voltage is 12 V and the output voltage step amplitude is 10 V.

Measurements, however, show that the capacitance of the employed electrolytic capacitor C_{dc2} is 186 μF instead of 220 μF due to capacitance tolerances. Therefore, $C_{\mathrm{dc2}} = 186\,\mu$F is used to calculate the depicted voltage step responses.

The proposed voltage controller achieves the rise time $t_{\mathrm{r}} \approx 2.5\ \mathrm{ms} = 50T$ and the delay time $t_{\mathrm{d}} \approx 1\ \mathrm{ms} = 20T$ with a maximum percentage overshoot of approximately 7% at no-load operation ($\Delta V_{\mathrm{f2,p,max}} \approx 0.7$ V, $\hat{V}_{2,\mathrm{Ref}} = 10$ V).

VI. Conclusion

To develop an accurate small-signal model for a DAB converter, a precise knowledge of the modulation method is required and the EMI filters need to be included in order to consider their interactions with the DAB. However, simplified converter models may be used in order to facilitate a less extensive controller design, since the time delay of a digitally controlled system causes a significant phase lag, which is considerably larger than the power converter's phase lag.

In this paper, the small-signal models for the DAB including EMI filter were derived for different modulation schemes. Further, the structure of the digital control system (including the most relevant algorithms), a simplified DAB model, and the controller design were detailed. The resulting control-to-output transfer functions are verified using measurements (obtained from an experimental setup), and a very good match between measured and calculated results was shown. Besides, in this paper, a measurement method to obtain the control-to-output transfer functions was proposed; this method may even be applied automatically in order to enable the autonomous calibration of the current and voltage controllers.

Even though the focus is on the DAB, the proposed small-signal model derivation method and the given digital control structure are easily extendable for resonant power converters with unidirectional and bidirectional power flow. For resonant power converters, however, increasing system orders result (e.g., order 8 for a bidirectional *LLC* converter with EMI filters according to Fig. 2), and therefore, the (offline) computing time increases considerably. Thus, future research may focus on the transfer functions of the converter core (e.g., the control-to-output transfer function of the DAB with surrounding filter capacitors C_{f1} and C_{f2}) and the interactions between the converter core and the surrounding power components (i.e., EMI filter components, supply line impedance, load impedance), which is similar to the analysis presented in [29], but in the discrete-time domain.

References

[1] A. Emadi, Y. J. Lee, and K. Rajashekara, "Power electronics and motor drives in electric, hybrid electric, and plug-in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 55, no. 6, pp. 2237–2245, Jun. 2008.

[2] A. Emadi, S. S. Williamson, and A. Khaligh, "Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems," *IEEE Trans. Power Electron.*, vol. 21, no. 3, pp. 567–577, May 2006.

[3] G. R. Flohr, "Performance considerations of a bi-directional DC/DC converter for fuel cell powered vehicles," presented at the SAE Future Car Congr., Arlington, VA, Jun. 2002.

[4] J.-S. Lai and D. J. Nelson, "Energy management power converters in hybrid electric and fuel cell vehicles," *Proc. IEEE*, vol. 95, no. 4, pp. 766–777, Apr. 2007.

[5] I. A. Khan, "DC-to-DC converters for electric and hybrid vehicles," in *Proc. IEEE Power Electron. Transp.*, Oct. 1994, pp. 113–122.

[6] S. Y. Kim, K. Nam, H.-S. Song, and H.-G. Kim, "Fault diagnosis of a ZVS DC–DC converter based on DC-Link current pulse shapes," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1491–1494, Mar. 2008.

[7] L. Zhu, "A novel soft-commutating isolated boost full-bridge ZVS-PWM DC–DC converter for bidirectional high power applications," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 422–429, Mar. 2006.

[8] H. Xiao and S. Xie, "A ZVS bidirectional DC–DC converter with phase-shift plus PWM control scheme," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 813–823, Mar. 2008.

[9] M. H. Kheraluwala, R. W. Gascoigne, D. M. Divan, and E. D. Baumann, "Performance characterization of a high-power dual active bridge dc-to-dc converter," *IEEE Trans. Ind. Appl.*, vol. 28, no. 6, pp. 1294–1301, Nov./Dec. 1992.

[10] H. Bai and C. Mi, "Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge DC–DC converters using novel dual-phase-shift control," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2905–2914, Nov. 2008.

[11] H. Bai, C. Mi, and S. Gargies, "The short-time-scale transient processes in high-voltage and high-power isolated bidirectional DC–DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 6, pp. 2648–2656, Nov. 2008.

[12] K. Vangen, T. Melaa, S. Bergsmark, and R. Nilsen, "Efficient high-frequency soft-switched power converter with signal processor control," in *Proc. 13th IEEE INTELEC*, Kyoto, Japan, Nov. 5–8, 1991, pp. 631–639.

[13] N. Schibli, "Symmetrical multilevel converters with two quadrant DC–DC feeding," Ph.D. dissertation, no. 2220, Ecole Polytechnique Federale de Lausanne (EPFL) Lausanne,, Switzerland, 2000.

[14] A. K. Jain and R. Ayyanar, "PWM control of dual active bridge: Comprehensive analysis and experimental verification," in *Proc. 34th IEEE IECON*, Orlando, FL, Nov. 10–13, 2008, pp. 1–7.

[15] F. Krismer, S. Round, and J. W. Kolar, "Performance optimization of a high current dual active bridge with a wide operating voltage range," in *Proc. 37th IEEE PESC*, Jeju, Korea, Jun. 18–22, 2006, pp. 909–915.

[16] G. W. Wester and R. D. Middlebrook, "Low-frequency characterization of switched dc–dc converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. AES-9, no. 3, pp. 376–385, May 1973.

[17] R. D. Middlebrook and S. Ćuk, "A general unified approach to modelling switching-converter power stages," in *Proc. IEEE PESC*, Cleveland, OH, Jun. 8–10, 1976, pp. 18–34.

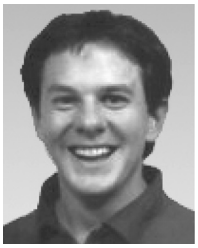
[18] D. J. Packard, "Discrete modeling and analysis of switching regulators," Ph.D. dissertation,, California Inst. Technol., Pasadena, 1976.

[19] A. R. Brown and R. D. Middlebrook, "Sampled-data modeling of switching regulators," in *Proc. IEEE PESC*, Boulder, CO, Jun. 29–Jul. 3, 1981, pp. 349–369.

[20] G. C. Verghese, M. E. Elbuluk, and J. G. Kassakian, "A general approach to sampled-data modeling for power electronic circuits," *IEEE Trans. Power Electron.*, vol. PE-1, no. 2, pp. 76–89, Apr. 1986.

[21] I. Batarseh and K. Siri, "Generalized approach to the small signal modeling of DC-to-DC resonant converters," *IEEE Trans. Aerosp. Electron. Syst.*, vol. 29, no. 3, pp. 894–909, Jul. 1993.

[22] D. Maksimovic and R. Zane, "Small-signal discrete-time modeling of digitally controlled PWM converters," *IEEE Trans. Power Electron.*, vol. 22, no. 6, pp. 2552–2556, Nov. 2007.
[23] S. Inoue and H. Akagi, "A bidirectional isolated DC–DC converter as a core circuit of the next-generation medium-voltage power conversion system," *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 535–542, Mar. 2007.
[24] R. W. A. A. De Doncker, D. M. Divan, and M. H. Kheraluwala, "A three-phase soft-switched high-power-density dc/dc converter for high-power applications,," *IEEE Trans. Ind. Appl.*, vol. 27, no. 1, pp. 63–73, Jan./Feb. 1991.
[25] F. Krismer and J. W. Kolar, "Accurate small-signal model for an automotive bidirectional dual active bridge converter," presented at the 11th IEEE COMPEL Workshop, Zürich, Switzerland, Aug. 2008.
[26] H. Tao, A. Kotsopoulos, J. L. Duarte, and M. A. M. Hendrix, "Transformer-coupled multiport ZVS bidirectional DC–DC converter with wide input range," *IEEE Trans. Power Electron.*, vol. 23, no. 2, pp. 771–781, Mar. 2008.
[27] G. F. Franklin, J. D. Powell, and M. L. Workman, *Digital Control of Dynamic Systems*, 3rd ed. Menlo Park, CA: Addison-Wesley/Longman, 1998.
[28] J. W. Umland and M. Safiuddin, "Magnitude and symmetric optimum criterion for the design of linear control systems: What is it and how does it compare with the others?" *IEEE Trans. Ind. Appl.*, vol. 26, no. 3, pp. 489–497, May/Jun. 1990.
[29] R. W. Erickson and D. Maksimović, *Fundamentals of Power Electronics*, 2nd ed. New York: Springer Science+Business Media, 2001.



Florian Krismer (S'05) received the M.Sc. degree (with honors) from Vienna University of Technology, Vienna, Austria, in 2004. He is currently working toward the Ph.D. degree at the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zurich, Zurich, Switzerland. He studied electrical engineering at Vienna University of Technology and at Lunds Tekniska Högskola (LTH), Sweden, majoring in automatic control systems.

His current research interests include the analysis, the design, and the optimization of high-current and high-frequency power converters.

Johann W. Kolar (S'89–M'91–SM'04) received the Ph.D. degree (*summa cum laude*) in industrial electronics from Vienna University of Technology, Vienna, Austria.

From 1984 to 2001, he was with Vienna University of Technology, where he was teaching and working in research in close collaboration with industry in the fields of high-performance drives, high-frequency inverter systems for process technology, and uninterruptible power supplies. Since 2001, he has been a Professor and the Head at the Power Electronic Systems Laboratory, Swiss Federal Institute of Technology Zurich, Zurich, Switzerland. His current research interests include novel ac–ac and ac–dc converter topologies with low effects on the mains for telecommunication systems, more-electric-aircraft applications, and distributed power systems utilizing fuel cells, and also the realization of ultracompact intelligent converter modules employing latest power semiconductor technology (SiC) and novel concepts for cooling and electromagnetic interference filtering. He has authored or coauthored more than 150 scientific papers in international journals and conference proceedings, and has filed more than 50 patents.

Prof. Kolar is a member of the Institute of Electrical Engineers of Japan and the Technical Program Committees of numerous international conferences. He is also the Director of the Power Quality Branch of the International Conference on Power Conversion and Intelligent Motion. From 1997 to 2000, he was an Associate Editor of the IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS. Since 2001, he has been an Associate Editor of the IEEE TRANSACTIONS ON POWER ELECTRONICS.