Comprehensive Comparison of Three-Phase AC-AC Matrix Converter and Voltage DC-Link Back-to-Back Converter Systems

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***Abstract*—This paper provides a comprehensive comparison of a Direct Matrix Converter, an Indirect Matrix Converter, and a Voltage DC-Link Back-to-Back Converter for a 15 kW permanent magnet synchronous motor drive. The comparison involves the investigation of the passive components including the EMI input filter, the required silicon chip area for a defined maximum admissible thermal loading of the power semiconductors, the total losses and achievable efficiency, and a prediction of the resulting volume of the passive components. With this comparative evaluation a systematic procedure is presented that ultimately allows for determining the application area of the considered converter topologies.**

***Index Terms*—Matrix converter, voltage dc-link back-to-back converter, comparative evaluation.**

I. Introduction

In academia, for a fairly long time Matrix Converters (MCs) have been considered as one of the future converter concept for variable speed drives (VSDs) for industry and more recently also for more electric aircraft or renewable energy applications. However, despite intensive research for the last three decades, MCs have until now only achieved low market diffusion. The industrially most widely used bidirectional, low-voltage ac-ac converter topology is the 2-level Voltage DC-Link Back-to-Back Converter (VLBBC), also known as Voltage Source Back-to-Back converter. The proponents of the MC technology argue that the direct ac-ac power converters without intermediate energy storage elements would not only allow for a more compact implementation, but also considerably increase the system lifetime due to the absence of the dc-link capacitor. On the contrary, the critics claim that MCs would not provide significant advantages that would compensate for their limitations, such as the lack of voltage step-up capability and/or the limited maximum output voltage of 86.6% of the input voltage.

The main objective of this paper is to describe the key criteria required for a systematic converter system evaluation. Based on this set of criteria, a comprehensive comparison of the Conventional (direct) Matrix Converter (CMC), the Indirect Matrix Converter (IMC), and the Voltage DC-Link Back-to-Back Converter (VLBBC), depicted in Fig. 1, is performed for a $15\,\mathrm{kW}$ Permanent Magnet Synchronous Motor (PMSM) drive.

Section II first summarizes the main properties of the MC and VLBBC and highlights the similarities and differences between the two converter concepts. Subsequently, a brief overview of the considered modulation schemes and the main converter control loops is provided. Therewith, the essential converter operating properties are defined and the key criteria required for a systematic comparison are identified. Section III is dedicated to the passive components and derives the basic relations between the volume and the weight of capacitors and inductors and their main lifetime limiting quantities. Based on these findings, in section IV, the design of the passive components including the EMI input filter components of the individual converter topologies is demonstrated. Section V briefly presents the main properties of the selected power semiconductor devices, which forms the starting point for a semiconductor area based comparison of the considered converter topologies. Based on the findings of the previous sections, ultimately, in section VI, the actual comparative evaluation of the CMC, IMC, and VLBBC is performed. This paper concludes with a compilation of the key findings.

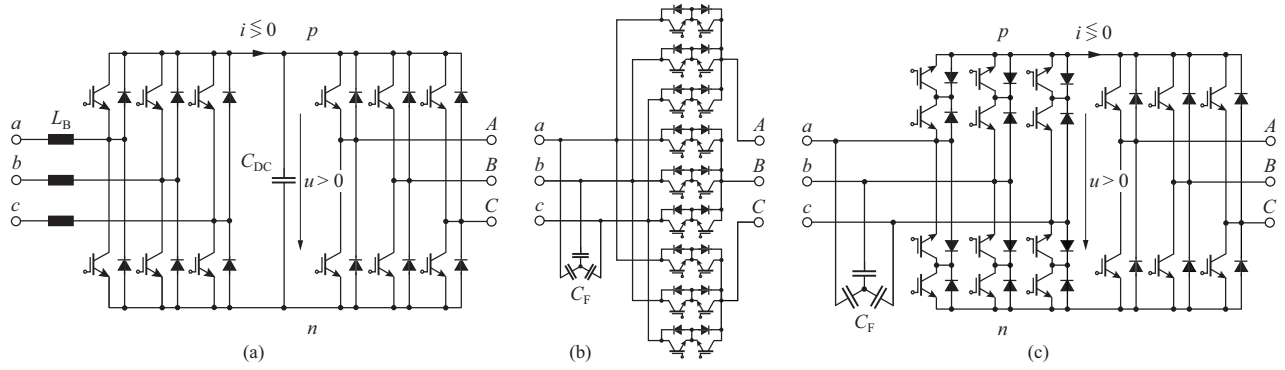

Fig. 1. Considered converter topologies, shown without input filter. (a) Voltage DC-Link Back-to-Back Converter (VLBBC), (b) Conventional (direct) Matrix Converter (CMC), and (c) Indirect Matrix Converter (IMC) with link voltage u and link current i.

II. Converter Properties

A. Circuit Topology

The VLBBC is a two-stage topology (Fig. 1(a)) that is formed by a back-to-back connection of a Voltage Source Rectifier (VSR) input stage and a Voltage Source Inverter (VSI) output stage, which are decoupled by the dc-link capacitor C_{DC}. The dc-link capacitor serves as an energy storage element and impresses a constant voltage across the dc-link. The inductors L_{B} enable input Power Factor Correction (PFC) under the restriction of boost operation of the input stage. Therefore, these inductors are in the following termed as boost-inductors.

Ac-ac converter topologies without any intermediate energy storage are referred to as Matrix Converters (MCs). They can provide simultaneous amplitude and frequency transformation of three-phase voltage-current systems. Their operating principle is based on the constant power flow in a symmetrical three-phase voltage-current system. The CMC (cf. Fig. 1(b)) performs the voltage and current conversion in one semiconductor stage. Alternatively, the IMC (cf. Fig. 1(c)) features a two-stage (indirect) power conversion. Regarding their basic functionality both MC topologies are equivalent. Their different physical implementation results in a different loading of the semiconductors and a different commutation scheme, which is going to be addressed in this paper.

B. Energy Storage

Concerning the energy flow, the dc-link capacitor C_{DC} of the VLBBC enables to decouple load variations from the mains input and to absorb the discontinuous (block-shaped) dc-link currents generated by the switching of the input and output stage. Correspondingly, the input capacitors C_{F} of the MC provide the major energy storage between the mains and the load and smooth the discontinuous input currents that are impressed by the load. Due to the absence of an intermediate energy storage the input capacitors are the key passive components that limit the feed-back of the load on the mains and determine the control behavior of a MC system. In analogy to the input capacitors of the MC, the boost inductors L_{B} of the VLBBC absorb the discontinuous (switched) voltages of the input stage and therewith enable continuous input currents. The stored energy in the boost inductors is low, compared with the dc-link capacitor. From a topological view it could hence be stated that in MCs the intermediate energy storage of the VLBBC has been shifted to the input filter and the load.

C. Control

The main control properties of the individual converter topologies are briefly discussed for a basic feed-back control scheme of a motor drive. From a control point of view there is no significant difference between the CMC and IMC. It is hence sufficient to restrict the considerations to MCs in general. In order to visualize the main control properties of the VLBBC and MC, in Fig. 2 their dc-dc converter equivalents are presented. Thereby L_1 represents the boost inductors L_{B} of the VLBBC and C_1 the dc-link capacitor C_{DC} of the VLBBC or the input capacitors C_{F} of the MC. The inductor L_2 models

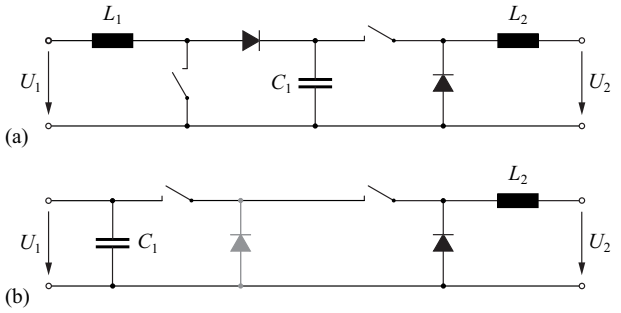

Fig. 2. Dc-dc converter equivalent circuits for (a) the VLBBC (boost-buck converter) and (b) the MC (buck-buck converter).

the stator inductance L_{S} of the motor. The VLBBC represents a series connection of a boost and a buck converter (cf. Fig. 2(a)) and thus features a boost-buck-type characteristic, whereas the dc-dc converter equivalent of a MC is a buck converter (cf. Fig. 2(b)) and thus features a buck-type characteristic.

For both converter concepts the motor control is identical and typically consists of an outer speed control loop and two inner current control loops for the d- and q-axis stator currents. The motor control actually is already the whole feed-back control required for a basic MC based drive system. The VLBBC requires another three control loops for its input stage: one outer control loop for the dc-link voltage and two inner loops for the d- and q- axis input currents that are impressed in the boost inductors.

D. Considered Modulation Schemes

The characteristics of the considered Space Vector Modulation (SVM) schemes are briefly described, starting with the VLBBC. For symmetry reasons it is sufficient to consider only one converter stage, in this case the output stage of the VLBBC. The switching state of the output stage (VSI), can be represented by a triple $(s_{\mathrm{A}}, s_{\mathrm{B}}, s_{\mathrm{C}})$ with $s_j = \{p, n\}$, which is formed by the switching functions of the three bridge-legs that are connected to the output phases A, B, and C. The switching state (pnn), for instance, means that the output phase A is connected to the positive dc-bus p, and the output phases B and C are connected to the negative dc-bus n. The corresponding space vector diagram is depicted in Fig. 3(b). The selected modulation scheme is a discontinuous SVM. Within a pulse period the desired output voltage space vector $\vec{u}_2^*$ is formed by two active voltage vectors and one zero vector. The resulting switching sequence for a phase angle $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$ of $\vec{u}_2^*$ equals to

$$\ldots \Big|_{0} (pnn) - (ppn) - (ppp) - (ppn) - (pnn) \Big|_{T_{\mathrm{P}}} \ldots \quad (1)$$

It has been already stated that the IMC topology can be conceived as a back-to-back connection of a CSR and VSI. This topological relationship forms the basis for the SVM of the IMC. For that purpose the switching states of the CSR are represented by a duplet $(s_{\mathrm{p}}, s_{\mathrm{n}})$ with $s_{\mathrm{p}} = \{a, b, c\}$ and $s_{\mathrm{n}} = \{a, b, c\}$. In analogy to the VSI, the switching state (ac), for example, means that the input phase a is connected to the positive bus p of the CSR and the input phase c is connected to its negative bus n (cf. Fig. 1). The corresponding space vector diagram of

the CSR is shown in Fig. 3(a). The resulting switching sequence of the IMC for a phase angle $\varphi_{\vec{i}_1^*} \in [0, \pi/6]$ and a $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$ is given by

$$\begin{aligned}\ldots \Big|_0 &(ac)(pnn)-(ac)(ppn)-(ac)(ppp)- \\ &(ab)(ppp)-(ab)(ppn)-(ab)(pnn)\Big|_{\frac{T_\mathrm{P}}{2}} \\ &(ab)(pnn)-(ab)(ppn)-(ab)(ppp)- \\ &(ac)(ppp)-(ac)(ppn)-(ac)(pnn)\Big|_{T_\mathrm{P}} \ldots \end{aligned} \quad (2)$$

As can be seen in (2), for a complete switching sequence of the input stage the switching sequence of the output stage is repeated for two different link voltage levels u. The advantage of this modulation scheme is that the switching state of the input stage can be changed during the free-wheeling state of the output stage, when no current flows in the link and thus no special commutation strategy is required for the IMC. Consequently, Zero-Current-Switching (ZCS) of the input stage is enabled, and therewith no switching losses occur in the input stage apart from losses due to component parasitics.

For the CMC a slightly different modulation scheme is selected than for the IMC, which is advantageous in terms of the CM voltage generation for the CMC. The switching states of the CMC are represented by the triple ($s_{i\mathrm{A}}$,$s_{i\mathrm{B}}$,$s_{i\mathrm{C}}$). The switching state (acc), for instance, means that the input phase a is connected to the output phase A, and the input phase c is connected to the output phases B and C. The resulting switching sequence of the CMC for a phase angle of $\varphi_{\vec{i}_1^*} \in [0, \pi/3]$ and a $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$ yields to

$$\begin{aligned}\ldots \Big|_0 &(acc)-(aac)-(aaa)-(aab)-(abb)\Big| \\ &(abb)-(aab)-(aaa)-(aac)-(acc)\Big|_{T_\mathrm{P}} \ldots \end{aligned} \quad (3)$$

Due to its topology, for the CMC a multi-step commutation strategy is required to guarantee safe commutation. In this work a conventional four-step commutation sequence is considered, which is based on the measured input voltages and the measured output currents. A more detailed description of all considered modulation and commutation scheme is provided in [1].

E. Voltage Step-up Capability

Output voltage step-up capability (boost operation) is a desirable feature of converter systems for drive applications, as it allows for a less conservative machine design. The VLBBC inherently provides voltage step-up functionality and thus is able to maintain the nominal output voltage also at reduced input voltages. For MCs the maximum output voltage is limited to 86.6% of the input voltage, and hence the control can only compensate for input voltage drops as long as the maximum modulation index $M_{12} = [0 \ldots 1]$ is not achieved [1].

F. Reactive Power Compensation

Another preferable characteristic of three-phase ac-ac converters is the capability to provide reactive input power in order to compensate the capacitive currents drawn by the input filter or to perform active damping. Assuming a proper design, the reactive power compensation capability of VLBBCs is primarily limited by the component ratings, whereas for MCs there are different restrictions imposed by the topology. For standard modulation schemes of MCs the formation of real input power P_1 and reactive input power Q_1 can be quantified by the subsequent equations, whereby the converter losses are neglected.

$$P_1 = \frac{3\sqrt{3}}{4} M_{12} \hat{U}_1 \hat{I}_2 \cos(\Phi_1^*) \cos(\Phi_2) \quad (4)$$

$$Q_1 = \frac{3\sqrt{3}}{4} M_{12} \hat{U}_1 \hat{I}_2 \sin(\Phi_1^*) \cos(\Phi_2) \quad (5)$$

$\hat{U}_1$ represents the amplitude of the input voltage, $\hat{I}_2$ the amplitude of the output current, M_{12} the modulation index, Φ_1^* the desired voltage-to-current displacement at the input and Φ_2 the apparent voltage-to-current phase displacement at the converter output. Thus, it appears that the formation of reactive input power is only possible if the real power flow is different from zero and that the maximum reactive input power decreases with an increasing displacement angle Φ_2.

Special, hybrid modulation schemes, suggested in [2] allow for decoupling the real power transfer from the reactive power transfer and hence enable the formation of reactive input power also for a purely reactive load ($\Phi_2 = \pm\pi/2$). However, if the instantaneous output currents of the MC equal to zero, no reactive input power can be provided at all, neither with standard nor with extended, hybrid modulation schemes.

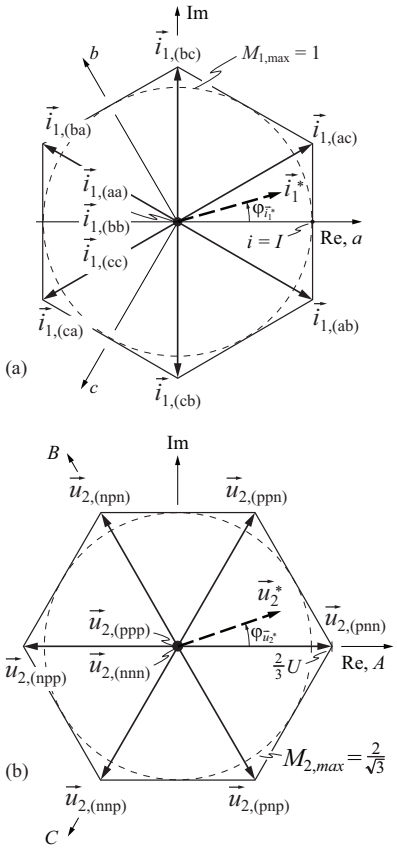

Fig. 3. (a) Space vector diagram of a CSR with the reference (desired) input current vector $\vec{i}_1^*$. (b) Space vector diagram of a VSI with the reference (desired) output voltage vector $\vec{u}_2^*$.

III. Passive Components

A. DC-Link and EMI Filter Capacitors

A frequently used argument in favor of the MC is that with the absence of the dc-link capacitor, a converter lifetime limiting component is implicitly omitted. With respect to state-of-the-art capacitor technologies this argument however seems to be inadequate. Additionally, it should be noted that also the input capacitors C_F of the MC suffer from an aging process. From this perspective the provided internal energy storage at a specified lifetime of the energy storage components or simply the lifetime of the energy storage components are more adequate criteria for comparing the MC with the VLBBC than the argument of "thermal aging of the dc-link capacitor" stated above.

In the following we restrict our considerations to polypropylene (PP) foil capacitors. Fig. 4 presents the two characteristic foil capacitor types that are utilized for ac-ac converters: dc-link and EMI suppression capacitors. In this comparison X2 and Y2 capacitors, both rated for a continuous rms voltage of $305\,\mathrm{V}$, are considered for EMI suppression.

The volume per capacitance scales with the rated voltage and the surge voltage capability. If the relation between volume and capacitance is evaluated for instance for the dc-link capacitors, it is found that the volume scales for a given rated voltage linearly with the capacitance and for a given capacitance with the square of the rated voltage, which is proportional to the stored energy.

$$V_\mathrm{C}(C,U) \propto C \text{ and } \propto U^2 \tag{6}$$

As can be seen in Fig. 4, the volume of the $1100\,\mathrm{V}$ dc-link capacitor ($1100\,\mathrm{V}$ at $70°\mathrm{C}$, $920\,\mathrm{V}$ at $85°\mathrm{C}$) scales similarly with the capacitance as for the considered X2 capacitors. The resulting mathematical relation, evaluated for an operating temperature of $70°\mathrm{C}$, yields to

$$V_\mathrm{C}(C) = 2.38\tfrac{\mathrm{cm}^3}{\mu\mathrm{F}}\,C + 6.45\,\mathrm{cm}^3 \qquad C \geq 0.68\,\mu\mathrm{F}\ . \tag{7}$$

This scaling law is used in the following to determine the volume of the dc-link and DM capacitors. By utilizing the average density of foil capacitors $\rho_\mathrm{C,avg}$ the resulting weight of the capacitors can be calculated.

$$m_\mathrm{C}(C) = \rho_\mathrm{C,avg} V_\mathrm{C}(C) \qquad \rho_\mathrm{C,avg} \approx 1.3\tfrac{\mathrm{g}}{\mathrm{cm}^3} \tag{8}$$

The Y-capacitors have a marginal impact on the filter volume as the maximum allowable capacitance is limited by the specified current in the Protective Earth (PE) conductor and is small compared to the required DM input capacitors. Assuming a maximum tolerable PE current of $I_\mathrm{CM,Y,max} \leq 3\,\mathrm{mA}$, for a $400\,\mathrm{V}\,/\,50\,\mathrm{Hz}$ mains system the maximum Y-capacitance value is then limited to

$$C_\mathrm{Y,max} \leq \frac{I_\mathrm{CM,Y,max}}{2\pi U_1 f_1} = 41.5\,\mathrm{nF}\ . \tag{9}$$

By inspection of the curves in Fig. 4, this Y-capacitance value hardly contributes to the overall filter volume and is accounted for with a default volume of $8.5\,\mathrm{cm}^3$ for the maximum Y-capacitance $C_\mathrm{Y,max}$.

The remaining dimension is the relation between the capacitor lifetime and the capacitance value. The capacitor losses scale with the volume of the dielectric material and therewith with the capacitance and with the resulting current ripple at a given operating voltage. For the specified operating temperature of $70\,°\mathrm{C}$ and by considering the loss and cooling properties of the capacitors this condition is used to determine the maximum current ripple of the dc-link capacitor such that a useful life of $100\,000\,\mathrm{h}$ can be achieved. Evaluated for a current ripple frequency of $10\,\mathrm{kHz}$ and an operating temperature of $70\,°\mathrm{C}$, the maximum tolerable rms ripple current $I_\mathrm{C,rms,max}$ can be expressed as a function of the capacitance and yields to

$$I_\mathrm{C,rms,max}(C) = 0.39\tfrac{\mathrm{A}}{\mu\mathrm{F}}\,C + 4.87\,\mathrm{A} \quad C \geq 2\,\mu\mathrm{F}\ . \tag{10}$$

The corresponding equations can be found in [3]. For polypropylene X-capacitors of typical input filters, the resulting losses are significantly lower than for an equally sized dc-link capacitor in a VLBBC as the voltage respectively the current ripple of the input filter capacitors is low. Thus, the losses are mainly determined by the reactive currents generated by the mains voltage and are uncritical for $50\,/\,60\,\mathrm{Hz}$ applications. An exception is provided by the input capacitors C_F of the MC as they absorb the block-shaped currents of the input stage. In terms of a worst case consideration (10) has to be considered as a constraint for the X2 input capacitors C_F of the MC. An additional important constraint for the X2 capacitors is given by the maximum voltage rise and fall time, which is inversely proportional to the lead spacing of the capacitors. With reference to [3], for the selected X2 capacitors it may hence be modeled as

$$\left|\frac{du_\mathrm{C}(C)}{dt}\right| \leq 2.3\tfrac{\mathrm{V}}{\mu\mathrm{F}\mu\mathrm{s}}C - 89\tfrac{\mathrm{V}}{\sqrt[3]{\mu\mathrm{F}}\mu\mathrm{s}}\sqrt[3]{C} + 252\tfrac{\mathrm{V}}{\mu\mathrm{s}}\ . \tag{11}$$

B. Differential Mode Inductors

DM inductors are required to implement the boost inductors of the VLBBC and obviously the DM filter inductors of all topologies. In this comparison toroidal powder core inductors are considered as they provide a good compromise between achievable inductance per volume, ac- and dc-magnetization properties, and feature a soft saturation curve, which is desirable regarding the converter control.

The core material selected is the High Flux HF 60 manufactured by Magnetics. The main inductor parameters are the inductance at zero current $L_\mathrm{DM,0}$, the inductance at the peak current value L_DM and the rms inductor current $I_\mathrm{L,rms}$ at a given frequency and temperature. Based on these quantities the inductors are designed such that the desired DM inductance L_DM is provided at the peak inductor current $\hat{I}_\mathrm{L} = \sqrt{2} I_\mathrm{L,rms}$ and the inductance value drops at the peak current to $\gamma_\mu = 80\%$ of its initial value a zero current.

The starting value of the wire diameter d_w (current conducting cross section) is selected such that a maximum rms current density $J_\mathrm{w,max}$ of $8\,\mathrm{A/mm}^2$ results. In order to minimize the parasitic winding capacitance, only single layer designs are considered. The resulting relation between the boxed inductor volume and the inductance is depicted in Fig. 5 as a function of the peak inductor

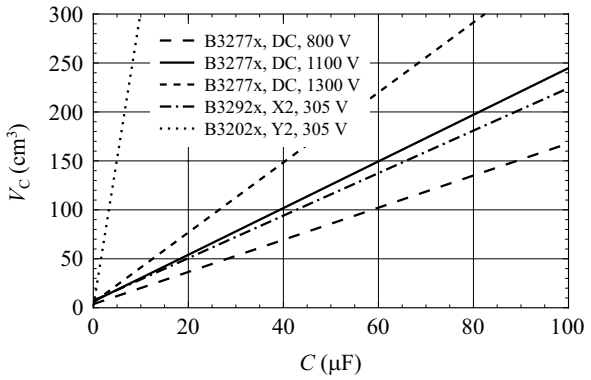

Fig. 4. Volume versus capacitance for polypropylene dc, X2, and, Y2 capacitors (B320xx-, B3277x-, and B3292x-series, EPCOS) at 70°C.

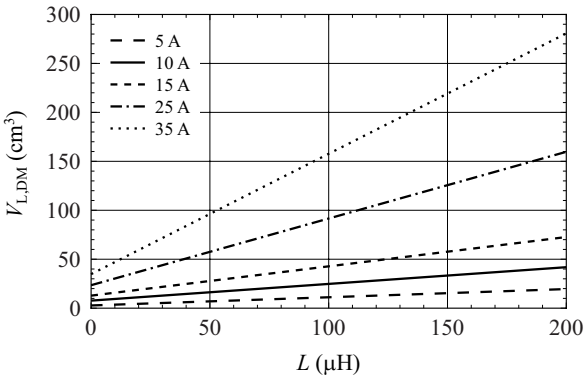

Fig. 5. Volume versus inductance for single layer, toroidal DM inductors based on HF 60 core material (Magnetics).

current and can be expressed as

$$V_{\mathrm{L_{DM}}}(\hat{I}_\mathrm{L}, L) = \left(k_{1,\mathrm{V},\mathrm{L_{DM}}}\hat{I}_\mathrm{L}^2 + k_{2,\mathrm{V},\mathrm{L_{DM}}}\hat{I}_\mathrm{L} + k_{3,\mathrm{V},\mathrm{L_{DM}}}\right)L + \left(k_{4,\mathrm{V},\mathrm{L_{DM}}}\hat{I}_\mathrm{L}^2 + k_{5,\mathrm{V},\mathrm{L_{DM}}}\hat{I}_\mathrm{L} + k_{6,\mathrm{V},\mathrm{L_{DM}}}\right) . \quad (12)$$

$$k_{1,\mathrm{V},\mathrm{L_{DM}}} = 1.99\cdot 10^3\,\tfrac{\mathrm{cm}^3}{\mathrm{A}^2\mu\mathrm{H}} \quad k_{2,\mathrm{V},\mathrm{L_{DM}}} = 3.11\cdot 10^2\,\tfrac{\mathrm{cm}^3}{\mathrm{A}\mu\mathrm{H}}$$
$$k_{3,\mathrm{V},\mathrm{L_{DM}}} = 5.82\cdot 10^4\,\tfrac{\mathrm{cm}^3}{\mu\mathrm{H}} \quad k_{4,\mathrm{V},\mathrm{L_{DM}}} = -1.06\cdot 10^{-2}\,\tfrac{\mathrm{cm}^3}{\mathrm{A}^2}$$
$$k_{5,\mathrm{V},\mathrm{L_{DM}}} = 1.13\,\tfrac{\mathrm{cm}^3}{\mathrm{A}} \quad k_{6,\mathrm{V},\mathrm{L_{DM}}} = -3.56\,\mathrm{cm}^3$$

For the above scaling factors $k_{i,\mathrm{V},\mathrm{L_{DM}}}$ the inductance value and the peak inductor current are restricted to

$$\hat{I}_\mathrm{L}L = [50\ldots4000]\,\mathrm{A}\mu\mathrm{H} \qquad \hat{I}_\mathrm{L} = [5\ldots35]\,\mathrm{A}\ .$$

In analogy to the capacitors, the inductor volume scales for a given peak current approximately linearly with the inductance and for a given inductance approximately with the square of the peak current, which again corresponds to the stored energy.

$$V_{\mathrm{L_{DM}}}(\hat{I}_\mathrm{L}, L) \propto L \text{ and } \propto \hat{I}_\mathrm{L}^2$$

The ratio between the mass of the core material and copper wire within the boxed inductor volume $V_{\mathrm{L_{DM}}}$ is obviously not constant. The weight of the inductor thus can be estimated by using an average density $\rho_{\mathrm{L_{DM},avg}}$.

$$m_{\mathrm{L_{DM}}}(\hat{I}_\mathrm{L}, L) = \rho_{\mathrm{L_{DM},avg}} V_{\mathrm{L_{DM}}}(\hat{I}_\mathrm{L}, L) \quad (13)$$
$$\rho_{\mathrm{L_{DM},avg}} \approx 3.0\,\tfrac{\mathrm{g}}{\mathrm{cm}^3}$$

The major loop core losses at the mains frequency, referred to as low-frequency core losses, are modeled with the standard Steinmetz equation according to

$$P_{\mathrm{c,LF},\mathrm{L_{DM}}}(B, f) = k\cdot B^\alpha\cdot f^\beta\ . \quad (14)$$

$$k = 2.57\cdot 10^{-6}\,\tfrac{\mathrm{mW}}{\mathrm{T}\,\mathrm{cm}^3\,\mathrm{s}} \quad \alpha = 2.56 \quad \beta = 1.23$$

The minor loop core losses due to the current ripple, referred to as high-frequency core losses, are more intricate to estimate, as the bias of the core varies with the mains frequency. The pragmatic approach, chosen here, is to perform core loss measurements with a square-wave voltage. The measurement results prove that for the chosen DM inductor design, the core losses hardly depend on the resulting dc-bias along the major loop and that the HF core losses can be approximated by the first five components of the Fourier-series of the resulting flux density. This quasi-linear loss behavior results from the selected core material and the applied inductor design, limiting the variation of the relative permeability.

The wire losses can be calculated by means of the wire resistance R_w, which is split into a dc (low-frequency) component $R_{\mathrm{w,DC}}$ and an ac (high-frequency) component $R_{\mathrm{w,AC}}$. Under the assumption that the wire diameter is significantly larger than the skin depth, the resulting wire resistance may be approximated by

$$R_\mathrm{w}(T, f, l_\mathrm{w}) = R_{\mathrm{w,DC}} + R_{\mathrm{w,AC}} \quad (15)$$
$$\frac{4\,l_\mathrm{w}}{\pi\,d_\mathrm{w}^2}\left(\rho_{\mathrm{Cu}}(T) + \sqrt{\frac{f\,\rho_{\mathrm{Cu}}(T)\,\mu_\mathrm{w}}{\pi}}\right) .$$

The temperature dependency of the specific dc resistance of copper ρ_{Cu} is modeled by

$$\rho_{\mathrm{Cu}}(T) = \rho_{\mathrm{Cu},20}\left(1 + \alpha_{\mathrm{Cu,T}}\,(T - 20)\right) . \quad (16)$$

$$\rho_{\mathrm{Cu},20} = 1.76\cdot 10^{-8}\,\Omega\mathrm{m} \quad \alpha_{\mathrm{Cu,T}} = 3.9\cdot 10^{-3}\,\tfrac{1}{^\circ\mathrm{C}}$$

The maximum average inductor temperature is limited to 100°. In free air and for a low-profile arrangement, the thermal resistance of the DM inductors varies within

$$R_{\mathrm{th},\mathrm{L_{DM}}} = [3\ldots32]\,\tfrac{\mathrm{K}}{\mathrm{W}} \qquad T_{\mathrm{L_{DM}}} - T_\mathrm{A} = 40\,\mathrm{K}\ . \quad (17)$$

The impact of the temperature on the lifetime of the considered inductors is significantly less critical compared to capacitors as for the selected HF 60 cores no temperature sensitive compound material is utilized. A temperature dependent variation of the core parameters is not required as within the specified temperature range the permeability of the HF 60 material changes only by 1%.

C. Common Mode Inductors

For the CM inductors of the input filter, toroidal cores from Vacuumschmelze are considered with a tape-wound core made of Vitroperm 500 F. The main design parameters of a CM inductor are the impedance $|\underline{Z}|$ (insertion loss) provided at a certain frequency, the CM saturation current respectively the corresponding voltage-time area product, and the rms inductor current. In order to minimize the parasitics, again a single layer design is assumed. The main design steps are similar to those shown for the DM inductors and therefore are not presented here. The

TABLE I
CONVERTER SPECIFICATION SUMMARY

Parameter	Value
Nominal rms input voltage	$3 \times 400\,\mathrm{V}$, $50\,\mathrm{Hz}$
Rated continuous output power at 90% of $U_{2,\max}$	$15\,\mathrm{kVA}$
Switching frequency	$8\,\mathrm{kHz}$, $32\,\mathrm{kHz}$
DC-link voltage of the VLBBC	$700\,\mathrm{V}$
PMSM phase inductance	$2.0\,\mathrm{mH} \ldots 3.0\,\mathrm{mH}$
Conducted emission EMC norm	Class B, CISRP 11
Maximum ambient temperature	$40°\mathrm{C}$

scaling law for the boxed CM inductor volume, evaluated at $100\,\mathrm{kHz}$, equals to

$$V_{\mathrm{L_{CM}}}(\hat{I}_{\mathrm{L}}, |\underline{Z}|) = \left(k_{1,\mathrm{V},\mathrm{L_{CM}}} \hat{I}_{\mathrm{L}}^2 + k_{2,\mathrm{V},\mathrm{L_{CM}}} \hat{I}_{\mathrm{L}} + k_{3,\mathrm{V},\mathrm{L_{CM}}}\right) |\underline{Z}| + \left(k_{4,\mathrm{V},\mathrm{L_{CM}}} \hat{I}_{\mathrm{L}}^2 + k_{5,\mathrm{V},\mathrm{L_{DM}}} \hat{I}_{\mathrm{L}} + k_{6,\mathrm{V},\mathrm{L_{CM}}}\right) . \quad (18)$$

$$k_{1,\mathrm{V},\mathrm{L_{CM}}} = 9.78 \cdot 10^{-5}\,\tfrac{\mathrm{cm}^3}{\mathrm{A}^2\Omega} \qquad k_{2,\mathrm{V},\mathrm{L_{CM}}} = 7.82 \cdot 10^{-4}\,\tfrac{\mathrm{cm}^3}{\mathrm{A}\Omega}$$
$$k_{3,\mathrm{V},\mathrm{L_{CM}}} = 5.85 \cdot 10^{-5}\,\tfrac{\mathrm{cm}^3}{\Omega} \qquad k_{4,\mathrm{V},\mathrm{L_{CM}}} = 1.48 \cdot 10^{-2}\,\tfrac{\mathrm{cm}^3}{\mathrm{A}^2}$$
$$k_{5,\mathrm{V},\mathrm{L_{CM}}} = 5.71 \cdot 10^{-1}\,\tfrac{\mathrm{cm}^3}{\mathrm{A}} \qquad k_{6,\mathrm{V},\mathrm{L_{CM}}} = 4.49\,\mathrm{cm}^3$$

IV. PASSIVE COMPONENT AND INPUT FILTER

A. Input and DC-Link Capacitor

In order to meet the dynamic requirements that are imposed by the load, for both converter concepts a minimum internal energy storage needs to be provided. For the VLBBC, the energy storage is implemented by the dc-link capacitor C_{DC}, whereas for the MC the internal energy storage is mainly provided by the input capacitors C_{F}. The worst case for the VLBBC occurs for an instantaneous load shedding at nominal motor operation, which is caused by the load and therefore cannot be precontrolled. In order to limit the relative overshoot of the dc-link voltage $\delta_{\mathrm{u_{DC}}} = \Delta u_{\mathrm{DC}}/U_{\mathrm{DC}}$, a minimal dc-link capacitance is required that can be calculated to

$$C_{\mathrm{DC}} \geq \frac{P_2}{18 U_{\mathrm{DC}}^2 \delta_{\mathrm{u_{DC}}}} \left(\frac{\sqrt{3} L_{\mathrm{B}} P_2 U_{\mathrm{DC}}}{U_1^2 \left(\sqrt{2} U_1 + \frac{U_{\mathrm{DC}}}{\sqrt{3}}\right)} + \frac{36}{f_{\mathrm{sw}}} \right) , \quad (19)$$

whereby regular sampling and a worst case dead time of two pulse periods ($2\,T_{\mathrm{P}} = 2\,f_{\mathrm{sw}}^{-1}$) are assumed.

A similar criterion can be derived for the input capacitors C_{F} of the MC by considering the input EMI filter depicted in Fig. 6. The design relevant operating condition occurs, when the current drawn from the input capacitors C_{F} is larger than the current supplied to them, and thus the capacitor voltage u_{C} drops. The voltage drop $\Delta u_{\mathrm{C,d}}$ depends on the DM inductance $L_{\mathrm{DM,2,tot}}$, the input capacitor C_{F}, and the variation of the load current. If the coupling between the d- and q- axis is neglected, which is allowable for the mains frequencies of $50\,/\,60\,\mathrm{Hz}$ and typical filter parameters, the voltage drop $\Delta u_{\mathrm{Cd}} = \delta_{\mathrm{u_C}} \hat{U}_1$ across the input capacitors is given by

$$\Delta u_{\mathrm{Cd}} = L_{\mathrm{res}} \frac{di_{\mathrm{2d}}}{dt} \left[\cos\left(\frac{t}{\sqrt{C_{\mathrm{F}} L_{\mathrm{res}}}} \right) - 1 \right] . \quad (20)$$

By inspection of (20), two cases for the duration of the current rise time t_{rise} have to be distinguished.

$$t_{\mathrm{rise}} < \pi \sqrt{C_{\mathrm{F}} L_{\mathrm{res}}} \quad \text{and} \quad t_{\mathrm{rise}} \geq \pi \sqrt{C_{\mathrm{F}} L_{\mathrm{res}}} \quad (21)$$

Mostly, the second case is design relevant, and therewith the capacitance of the filter capacitors only indirectly limits the voltage drop Δu_{Cd} across the input filter capacitors. The relative voltage drop is assumed with $\delta_{\mathrm{u_{DC}}} = \delta_{\mathrm{u_{Cd}}} = 10\%$ for both the VLBBC and the MC.

Besides the control based dimensioning criterion, for the MC also the voltage ripple across the input capacitors at the switching frequency needs to be considered. In order to enable safe operation, the maximum peak-to-peak voltage ripple $\Delta u_{\mathrm{C_F,pp}}$ across the input filter capacitors C_{F} is limited to $\delta_{\mathrm{u_{C,pp}}} = 10\%$ of the input voltage amplitude $\hat{U}_1$ and can be calculated to

$$\Delta u_{\mathrm{C_F,pp,max}} = \frac{\hat{I}_2}{4 C_{\mathrm{F}} f_{\mathrm{sw}}} = \delta_{\mathrm{u_C,pp}}\, \hat{U}_1 . \quad (22)$$

The maximum rms current $I_{\mathrm{C,rms,max}}$ of the input capacitors for MCs occurs at two-third of the maximum output voltage and $\Phi_2 = 0$ for the considered modulation schemes and may be written as

$$I_{\mathrm{C_F,rms,max}} \approx 0.41 \cdot \hat{I}_2 . \quad (23)$$

Assuming a center-aligned synchronization of the modulation of the input and output stage of the VLBBC, the maximum rms dc-link capacitor current equals to

$$I_{\mathrm{C_{DC},rms,max}} \approx 0.67 \cdot \hat{I}_2 . \quad (24)$$

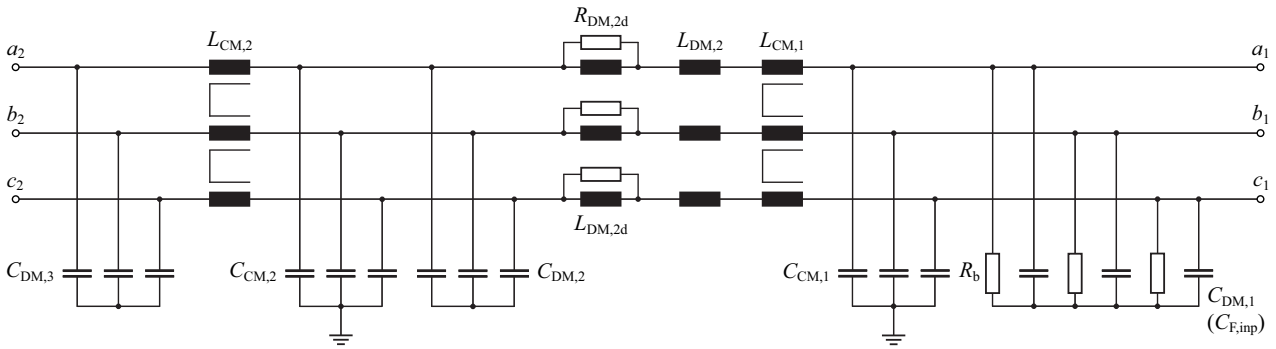

Fig. 6. Considered input EMI filter topology. $C_{\mathrm{DM,1}}$ corresponds to the input capacitors C_{F} of the MC. The boost inductors L_{B} of the VLBCC (not shown here) are connected to the terminals a_1, b_1, and c_1 and represent the DM filter inductors $L_{\mathrm{DM,1}}$ of the input filter.

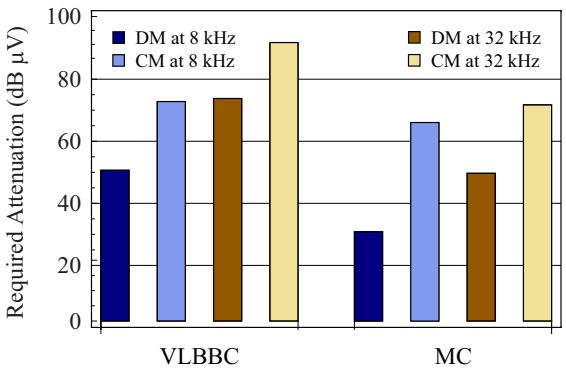

Fig. 7. Required DM and CM filter attenuation for the VLBBC and MC at a switching frequency of 8 kHz and 32 kHz.

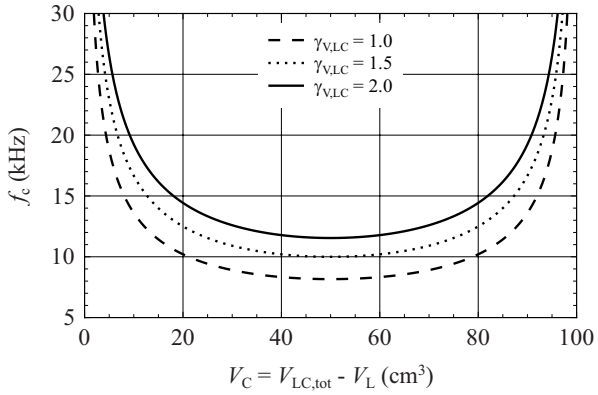

Fig. 8. Corner frequency f_c of an LC for a different partitioning of the total filter volume of 100 cm^3 between capacitors and inductors.

Ultimately, the energy storage density in a MC is compared with a VLBBC. Assuming a symmetrical three-phase mains system with a phase voltage U_1 and a dc-link voltage U_{DC}, the stored energy can be quantified by

$$W_{\mathrm{C_{DC}}} = \frac{1}{2} C_{\mathrm{DC}} U_{\mathrm{DC}}^2 \qquad W_{\mathrm{C_F}} = \frac{3}{4} C_{\mathrm{F}} \hat{U}_1^2 \,. \tag{25}$$

By determining the required volume using (7), it is found that for the considered capacitors and an input rms phase voltage of $U_1 = 230\,\mathrm{V}$, the energy storage density in a MC is three-times lower compared to a VLBBC with a dc-link voltage of $U_{\mathrm{DC}} = 700\,\mathrm{V}$.

B. Boost Inductors

The boost inductors L_{B} of the VLBBC are dimensioned based on the current ripple at the switching frequency. In analogy to the input capacitors of the MC, the boost inductors are designed for a maximum peak-to-peak current ripple $\Delta i_{\mathrm{L_B,pp,max}}$ of $\delta_{\mathrm{i_L,pp}} = 20\%$ of the input current amplitude $\hat{I}_1$.

$$\Delta i_{\mathrm{L_B,pp,max}} = \frac{1}{\hat{I}_1 f_{\mathrm{sw}} \delta_{\mathrm{i_L,pp}}} \left(U_1 - \frac{3U_1^2}{2U_{\mathrm{DC}}} \right) \tag{26}$$

C. EMI Input Filter Design

Although different advanced filtering concepts have been presented for ac-ac converters, as for instance in [4] for the CMC, in this comparison a conventional multi-stage LC filter topology is applied, in order to establish comparability with commercial EMI filters. The considered filter topology is presented in Fig. 6. The protection devices are not shown. Only the last capacitor stage ($C_{\mathrm{DM},1}$) is equipped with bleeding resistors R_{b}.

The first step in the filter design is to investigate the parameter variation of the passive components. The A_{L}-value respectively the permeability of the considered DM inductor material varies within $\pm 8\%$. For the Vitroperm 500 F material, which is utilized for the CM inductors, a permeability variation of $+45\%/-25\%$ is specified. The variation of the capacitance for the considered polypropylene foil capacitor technologies is limited to $\pm 10\%$. Consequently, the considered DM filter design margins are set to 6 dB for the DM attenuation and 10 dB for the CM attenuation. The next step is to design the input capacitors C_{F} and boost inductors L_{B} according to the ripple and control performance based criteria defined above. Therewith, all three converter topologies are operational and the required filter attenuation can be calculated. The filters are designed for nominal converter operation as specified in Tab. I to meet the CISPR 11 Class B Quasi-Peak (QP) level for conducted emission.

The actual filter design is performed with a custom developed, automated filter design software. For the DM filter design the impact of the load is marginal. However, for the CM filter design a first-order equivalent of the CM impedance $\underline{Z}_{\mathrm{m,CM}}$ of the motor load is utilized. The impedance is parameterized based on measurement results of PMSMs (LST-series, LTi Drives) including a 3 m long motor cable.

$$\underline{Z}_{\mathrm{m,CM}} = \frac{1}{j2\pi C_{\mathrm{m,CM}}} + j2\pi f L_{\mathrm{m,CM}} + R_{\mathrm{m,CM}} \tag{27}$$

$$C_{\mathrm{m,CM}} = 2\,\mathrm{nF} \quad L_{\mathrm{m,CM}} = 435\,\mathrm{nH} \quad R_{\mathrm{m,CM}} = 2.1\,\Omega$$

The impedance parameters are valid within the frequency range of 100 kHz to 8 MHz, which is required for the high-frequency CM filter design. In order to ensure that the CM-inductors do not saturate in the frequency range of the electrical input and output frequency of the converter, also a low-frequency equivalent impedance is needed, which is not shown here. In view of the wire losses of the CM inductors, their core losses are marginal for the considered switching frequency range of 8 kHz to 32 kHz and hence are neglected. For the considered modulation schemes the DM noise of the CMC and IMC are identical and the CM noise spectrum mainly differs in the low frequency range at multiples of the input and output frequencies. Thus, it is sufficient to consider the EMI filter requirements for MCs in general. The required DM and CM EMI filter attenuation values, are shown in Fig. 7.

The overall filter volume can mainly be minimized by an adequate design of the DM filter stages with regard to the volumetric scaling factors of the capacitors and inductors. The basic principle can be best explained by considering the corner frequency $f_{\mathrm{c,DM}}$ of a single LC filter stage (e.g. $C_{\mathrm{DM},2}$ and $L_{\mathrm{DM},2}$ in Fig. 6).

$$f_{\mathrm{c}} = \frac{1}{2\pi\sqrt{CL}} \tag{28}$$

The lower the corner frequency is, the higher is the filter attenuation. The linkage between the filter volume $V_{\mathrm{LC,tot}}$

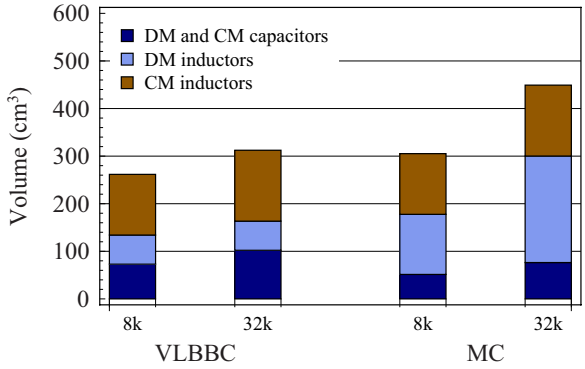

Fig. 9. Boxed volume of the EMI input filter components for the VLBBC and MC at a switching frequency of 8 kHz and 32 kHz.

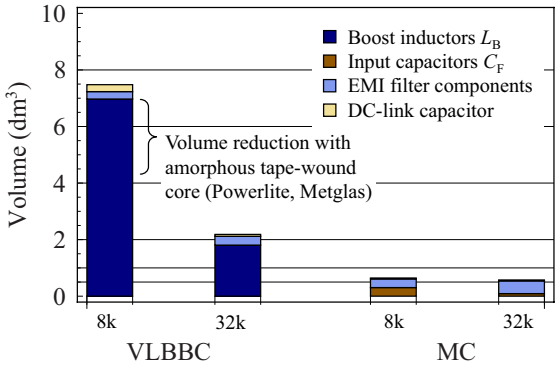

Fig. 10. Total boxed volume of the passives components of the VLBBC and MC at a switching frequency of 8 kHz and 32 kHz.

and the attenuation can be established by expressing the capacitance and inductance value as a function of the component volume.

$$C = \frac{V_\mathrm{C}}{\gamma_\mathrm{V,C}} \qquad L = \frac{V_\mathrm{L}}{\gamma_\mathrm{V,L}} \qquad \gamma_\mathrm{V,LC} = \frac{\gamma_\mathrm{V,L}}{\gamma_\mathrm{V,C}} \tag{29}$$

By substituting C and L in (28) with (29), the corner frequency is then given by

$$f_\mathrm{c} = \frac{1}{2\pi\sqrt{\frac{V_\mathrm{C}}{\gamma_\mathrm{V,C}}\frac{V_\mathrm{L}}{\gamma_\mathrm{V,L}}}} = \frac{\gamma_\mathrm{V,C}}{2\pi}\sqrt{\frac{\gamma_\mathrm{V,LC}}{V_\mathrm{C}\left(V_\mathrm{F,tot}-V_\mathrm{C}\right)}}\,. \tag{30}$$

f_c is minimal and thus the attenuation is maximum for

$$V_\mathrm{C,opt} = V_\mathrm{L,opt} = \frac{V_\mathrm{LC,tot}}{2}\,. \tag{31}$$

In other words, independent of the volumetric scaling $\gamma_\mathrm{V,LC}$ between the capacitors and inductors, the maximum attenuation of a single LC filter stage at a minimal filter volume is achieved if one half of the total filter volume is utilized for the capacitors and the other half for the inductors. This optimization approach was suggested in [5] for optimizing the drive train of an electric vehicle. In Fig. 8 the resulting corner frequency is plotted versus the partitioning of the capacitor and inductor volume for different scaling factors between the inductor volume and its inductance and the scaling of capacitors provided in (7). The implemented filter design algorithm additionally ensures that

- the filter resonances do neither occur at the switching frequency nor at the beginning of the EMI measurement range at 150 kHz,
- passive damping is provided for the resonances above the current control bandwidth of the converter,
- the output impedance of the filter is minimized,
- the lifetime based loading limits of the passive components (cf. section III) are fulfilled,
- the total reactive power of the filter including the input capacitors (C_F) is below 15% of the nominal converter output power, and
- an nominal efficiency of the EMI input filter of at least 99.6% is achieved.

The required boxed volume of the EMI filter components (without the boost inductors of the VLBBC and the input capacitors of the MC) is presented in Fig. 9. Ultimately, Fig. 10 shows the total boxed volume of the passive components.

V. Semiconductors

A. Semiconductor Selection

The considered power semiconductors are latest generation Trench and Field-Stop 1200 V silicon IGBT4 devices and EmCon4 diodes from Infineon that are rated for a maximum junction temperature of 175°C and packed in standard power modules with an Al_2O_3 ceramic substrate. Although, it is known, that CMCs are often implemented with Reverse-Blocking IGBTs (RB-IGBTs), in this comparison conventional IGBTs are utilized, as only a few manufacturers of RB-IGBTs exist and therewith only low component diversity would be given.

B. Required Semiconductor Chip Area

In order to provide a common basis for investigating the semiconductor requirements of the VLBBC, the CMC, and the IMC, a Semiconductor Area based Converter Comparison (SACC) is performed. The applied algorithm determines the minimum required semiconductor area for the individual IGBT and diode chips of all converters and at given operating points such that the average junction temperatures of the IGBTs and diodes $T_\mathrm{J,S/D}$ are equal or less than a predefined maximum value $T_\mathrm{J,max}$. The advantages of this consideration are as follows:

- The algorithm ensures an optimal partitioning of the semiconductor chip area and thus avoids a converter performance reduction due to an inadequate chip area selection.
- By adjusting the average junction temperature to a predefined maximum value, an essential precondition is provided for limiting the variation in the lifetime of the semiconductor modules of the individual converter topologies.

Different design relevant operating points in the torque-speed plane of bidirectional motor drives were identified.

- Motor operation (OP1) and generator operation (OP5) at nominal output current, nominal electrical output frequency $f_2 = 150$ Hz, and nominal output power of $P_\mathrm{2,nom} = 15$ kW.
- Motor operation (OP2) and generator operation (OP4) at an electrical output frequency equal to the input mains frequency $f_2 = f_1 = 50$ Hz.
- Motor operation (OP3) at electrical stand-still at the output $f_2 = 0$ Hz.

The current rating of transistors and diodes is proportional to the active chip area $A_{\mathrm{chip,act}}$, whereas the differential forward resistance $r_{\mathrm{S/D,F}}$ is inversely proportional to the active chip area $A_{\mathrm{chip,act}}$. The resulting thermal impedance between the junction and the heat sink $Z_{\mathrm{th,JS}}$ is inversely proportional to the total chip area $A_{\mathrm{chip}} > A_{\mathrm{chip,act}}$ and depends on the semiconductor module assembly and the cooling system.

$$I_{\mathrm{S/D,nom}} \propto A_{\mathrm{chip,act}} \qquad r_{\mathrm{S/D,F}} \propto {A_{\mathrm{chip,act}}}^{-1} \tag{32}$$

$$Z_{\mathrm{th,JS}} \propto {A_{\mathrm{chip}}}^{-1} \tag{33}$$

C. Cooling System

The cooling system design aims for a simple and compact construction with an average Cooling System Performance Index (CSPI) between $10\,\mathrm{W/(K\,dm^3)}$ to $12\,\mathrm{W/(K\,dm^3)}$. The demanded characteristics can be achieved with a forced air cooled, customized aluminum heat sink. For the heat sink a sub-optimum design, suggested in [6], is applied to simplify the manufacturing while still maintaining superior cooling performance. The thermal resistance of the cooling system between the heat sink and the ambient air $R_{\mathrm{th,CS}}$ is expressed as a function of the length $l_{\mathrm{CS}} \geq 160\,\mathrm{mm}$ and for a given width of $200\,\mathrm{mm}$ of the cooling system.

$$R_{\mathrm{th,CS}}(l_{\mathrm{CS}}) = k_{1,\mathrm{R_{CS}}} l_{\mathrm{CS}}^2 + k_{2,\mathrm{R_{CS}}} l_{\mathrm{CS}} + k_{3,\mathrm{R_{CS}}} \tag{34}$$

$$k_{1,\mathrm{R_{CS}}} = 7.50 \cdot 10^{-7} \tfrac{\mathrm{K}}{\mathrm{W\,mm^2}} \qquad k_{2,\mathrm{R_{CS}}} = -4.43 \cdot 10^{-4} \tfrac{\mathrm{K}}{\mathrm{W\,mm}}$$
$$k_{3,\mathrm{R_{CS}}} = 1.05 \cdot 10^{-1} \tfrac{\mathrm{K}}{\mathrm{W}}$$

The boxed volume of the cooling system V_{CS} yields to

$$V_{\mathrm{CS}}(l_{\mathrm{CS}}) = k_{1,\mathrm{V_{CS}}} l_{\mathrm{CS}} + k_{2,\mathrm{V_{CS}}} \,. \tag{35}$$

$$k_{1,\mathrm{V_{CS}}} = 9.20 \tfrac{\mathrm{cm^3}}{\mathrm{mm}} \qquad k_{2,\mathrm{V_{CS}}} = -3.36 \cdot 10^{1}\ \mathrm{cm^3}$$

D. Protection Concepts

All converters should enable a controlled emergency stop of the drive, even in case of mains phase loss. For that purpose the VLBBC requires only a brake chopper that is connected across the dc-link capacitor. For the CMC and IMC it is assumed that the auxiliary supply is implemented with a three-phase diode rectifier that is connected to the input phases and thus provides a dc-bus voltage of approximately $\sqrt{6}\,U_1$. In order to provide a path for the motor currents during mains phase loss, for the CMC an additional three-phase diode rectifier needs to be connected between the output phases and the (high-voltage) dc input of the auxiliary supply. For the IMC, only two additional power diodes are required, that connect the rails of the intermediate link to the dc input of the auxiliary supply.

VI. Comparison

A. Setup

All three drive systems are designed to operate on a balanced three-phase $50\,\mathrm{Hz}$ mains system with a nominal voltage of $400\,\mathrm{V}$ and to meet the CISPR 11 (Class B) EMC standard for conducted emission. The converters are controlled to provide unity power factor at the input. The dc-link voltage U_{DC} of the VLBBC is assumed with $700\,\mathrm{V}$. In order to enable a fair comparison, the rated voltages of the PMSMs are matched to the output voltage ranges of the VLBBC and MC such that at 90% of the maximum output voltage of the converter and at equal electrical output frequency of $150\,\mathrm{Hz}$ all drives deliver the same nominal shaft power.

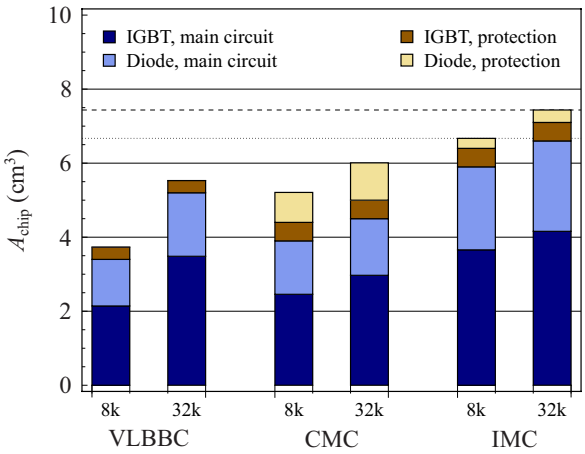

Fig. 11. Required minimum semiconductor chip areas for $T_{\mathrm{A}} = 40°\mathrm{C}$ such that at OP1 and OP5 $T_{\mathrm{J}} \leq 150°\mathrm{C}$ for all power semiconductors at a switching frequency of $8\,\mathrm{kHz}$ and $32\,\mathrm{kHz}$.

In this comparison, for all converter topologies the minimum semiconductor chip areas are determined such that $T_{\mathrm{J,max}}$ is equal or less than $150°\mathrm{C}$ for all semiconductor chips at the operating points OP1 and OP5 and at an ambient temperature T_{A} of $40°\mathrm{C}$. The required semiconductor chip areas are depicted in Fig. 11. A detailed description of the SACC is provided in [7].

B. Main Results

For the considered $15\,\mathrm{kW}$ drive system with PMSMs, both the CMC as well as the IMC enable a more compact implementation than the VLBBC. For the considered (identical) component selection and design and at a switching frequency of $8\,\mathrm{kHz}$, the MC concept allows for a reduction of the total volume of the passive components including the heat sink by a factor of 4, and at $32\,\mathrm{kHz}$ by a factor of 1.5 compared with the VLBBC. This volume reduction is mainly due to the absence of the boost inductors. For a switching frequency of $8\,\mathrm{kHz}$, laminated iron cores or amorphous tape-wound cores (e.g. Powerlite, Metglas) could be used for the boost inductors of the VLBBC instead of powder cores as considered. This would allow for reducing the volume of the boost inductors. Thus, the previously stated factor of 4 for the volume reduction between the VLBBC and the MC at $8\,\mathrm{kHz}$ would then be reduced to 2.5 (cf. Fig. 10). Unfortunately, the higher achievable power density of MCs is overshadowed by the lack of desirable, basic converter properties such as output voltage step-up capability, unconstrained reactive input power compensation, simple feed-back control of the input currents, and the possibility for single-phase operation.

The resulting total efficiency of all three converters for the considered worst case at an ambient temperature of $40°\mathrm{C}$, a junction temperature of $150°\mathrm{C}$, and for a minimum semiconductor chip area varies between 94.2% and 95.2% at $8\,\mathrm{kHz}$ and between 93.2% and 93.9% at

32 kHz. For switching frequencies above 20 kHz the semiconductor chip area (without the devices for protection) of the CMC is smaller than for the VLBBC. For the considered switching frequency range and semiconductor design the IMC always requires a larger chip area compared with the VLBBC and CMC. If the VLBBC and CMC are implemented (including the chopper IGBT and protection diodes) with the same total semiconductor area of $7.4\,\mathrm{cm}^3$, which is required by the IMC at 32 kHz, then at 32 kHz the CMC provides the highest semiconductor efficiency of 95.1%, whereas the VLBBC and the IMC allow for a semiconductor efficiency of 94.6%. The results of the comparative evaluation are compiled in Tab. II. For a commercial converter system typically more semiconductor chip area would be implemented and for the VLBBC more dc-link capacitance would be provided than the determined minimum value. Assuming a dc-link capactiance of $150\,\mu\mathrm{F}$ ($10\,\mu\mathrm{F/kVA}$), the volume of the passive component of the VLBBC would increase at 8 kHz by only 2% and at 32 kHz by 15%.

TABLE II
CONVERTER SYSTEM PARAMETER OVERVIEW

Parameter		VLBBC	CMC	IMC
Nominal output voltage		256 V	175 V	175 V
Nominal output current		19.6 A	28.6 A	28.6 A
Boost inductors L_B	8 k	2.0 mH	–	–
	32 k	0.5 mH	–	–
Input capacitors C_F	8 k	–	40 μF	40 μF
	32 k	–	10 μF	10 μF
DC-link capacitor C_DC	8 k	101 μF	5 μF	5 μF
($U_\mathrm{DC} = 700$ V)	32 k	25 μF	5 μF	5 μF
Passive components	8 k	8.4 dm^3	2.3 dm^3	1.9 dm^3
(including heat sink)	32 k	4.1 dm^3	2.9 dm^3	2.4 dm^3
Number of gate drivers		12	18	12
Semiconductor chip area	8 k	3.7 cm^2	5.2 cm^2	6.7 cm^2
($T_\mathrm{J} \leq 150°\mathrm{C}$)	32 k	5.5 cm^2	6.0 cm^2	7.4 cm^2
Semiconductor efficiency	8 k	96.7%	94.8%	95.6%
(OP1/OP5, $T_\mathrm{J} = 150°\mathrm{C}$)	32 k	94.4%	93.9%	94.6%
Total efficiency	8 k	95.2%	94.2%	94.9%
(OP1/OP5, $T_\mathrm{J} = 150°\mathrm{C}$)	32 k	93.3%	93.2%	93.9%

C. CMC versus IMC

The major difference is given by the fully symmetrical topology of the CMC compared to the IMC, which leads to an even loading of all semiconductors of the CMC. The simple commutation of the IMC due to its two-stage structure is achieved at the expense of more, potentially not evenly loaded power devices in the current path, which results in a higher semiconductor effort compared to the CMC. The CMC should hence be selected for applications, where the conduction losses are dominant. For high switching frequency MCs, where advanced (expensive) semiconductor devices are indispensable, the IMC should be considered, as it enables more degree of freedom regarding the combination of different semiconductors (e.g. SiC JBS diodes only in the output stage).

VII. CONCLUSIONS

The MC represents a converter concept that aims at minimizing the internal energy storage. This key converter system property should be considered as an assessment criteria on whether the MC matches well its intended application. This means that for ac-ac converter applications that require internal energy storage due to high-load dynamics, single-phase operation capability, extended ride-through capability, or unconstrained reactive power compensation, the MC does not provide the most appropriate solution. Another important aspect when considering the MC as an alternative converter topology is that there should be a certain degree of freedom on the system design level to adapt the overall drive system to the MC (e.g. motor voltage). A suitable load for a MC can be characterized in general as load with a high inertia and low dynamic performance requirements. Such "MC friendly" loads and operating conditions are found, for instance, for compressor, fan, or pump drives for 50 / 60 Hz mains application. For most of these applications, actually only unidirectional power flow is required and thus also an unidirectional MC, could be utilized. Under this restriction an unidirectional IMC, also known as Ultra-Sparse Matrix Converter (USMC) [1] could be applied. However, the strong competitor of the MC technology in this application area obviously is the VSI with a B6 diode bridge rectifier (B6-VSI), which is an industrially well established and reliable converter concept allowing for a high efficiency between 97% and 98%. Since the B6-VSI enables an input power factor above 0.9 and evidently also provides compliance to the considered Class B (CISPR 11) EMI standards, the main advantages of the USMC compared to the B6-VSI is its potential for reducing the volume of the passive components and the sinusoidal input currents.

Due to its multiple intrinsic limitations, the MC does not seem to be the appropriate topology for a general purpose, flexibly configurable, bidirectional, low-voltage ac-ac converter. For such requirements, the VLBBC clearly is the preferred choice. In conclusion, in the low-voltage and low-power ac-ac converter segment the MC technology is rather restricted to niche-applications.

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