The Essence of Three-Phase AC/AC Converter Systems

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***Abstract*— In this paper the well-known voltage and current DC-link converter systems, used to implement an AC/AC converter, are initially presented. Using this knowledge and their space vector modulation methods we show their connection to the family of Indirect Matrix Converters and then finally the connection to direct Matrix Converters. A brief discussion of extended Matrix Converter circuits is given and a new unidirectional three-level Matrix Converter topology is proposed. This clearly shows the topological connections of the converter circuits that directly lead to an adaptability of the modulation methods. These allow the reader who is familiar with space vector modulation of voltage and current DC-link converters to simply incorporate and identify new modulation methods. A comparison of the converter concepts, with respect to their fundamental, topology-related characteristics, complexity, control and efficiency, then follows. Furthermore, by taking the example of a converter that covers a typical operation region in the torque-speed plane (incl. holding torque at standstill), the necessary silicon area of the power semiconductors is calculated for a maximum junction temperature. This paper concludes with proposals for subjects of further research in the area of Matrix Converters.**

***Keywords*— AC/AC converter, matrix converter, voltage source converter, current source converter.**

I. Introduction

For conversion from a three-phase mains source to a three-phase voltage load with an arbitrary frequency and amplitude, e.g. variable speed drives, converter systems with either a voltage or current DC-link are mainly used today (Fig. 1). In the case of the voltage DC-link, the mains coupling can, in the simplest case, be implemented by a diode bridge. To accomplish braking operation of the load, a pulse-controlled braking resistor must be placed in the DC-link or an antiparallel thyristor bridge be provided on the mains side. The disadvantages are the relatively high mains distortion and high reactive power requirements, especially during inverter operation.

A mains-friendly AC/AC converter with bidirectional power flow can be implemented by coupling a PWM rectifier and a PWM inverter to the DC-link. The DC-link quantity is then impressed by an energy storage element that is common to both stages, i.e. a capacitor C for the voltage DC-link (U-BBC) or an inductor L for the current DC-link (I-BBC). The PWM rectifier is controlled such that a sinusoidal mains current is drawn that is in phase or anti-phase (energy feedback) with the corresponding mains phase voltage. For the realization of the AC/AC converter, 12 power transistors and 12 diodes are required, or in the future 12 reverse conducting IGBTs (RC-IGBTs) or 12 reverse blocking IGBTs (RB-IGBTs), since for the I-BBC the feedback of energy can be achieved only by the reversal of the DC-link voltage polarity because of the unidirectional current flow set by the power semiconductors.

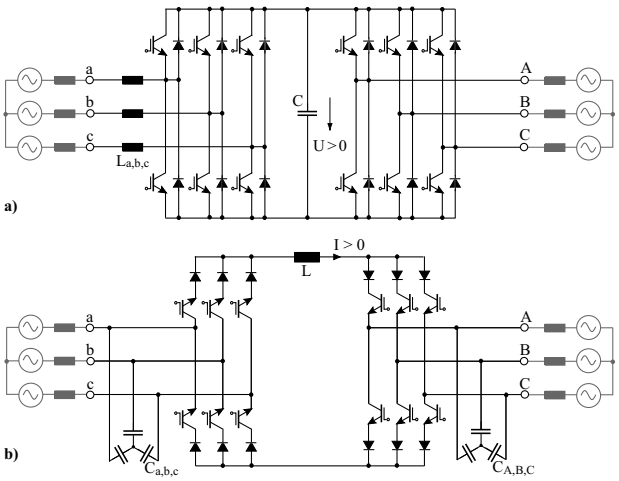

Figure 1: Three-phase AC/AC converter with a) voltage DC-link (U-BBC) and b) current DC-link (I-BBC).

Due to the DC-link storage element, there is the advantage that both converter stages are to a large extent decoupled for control purposes. Furthermore, a constant, mains independent input quantity exists for the PWM inverter stage, which results in high utilization of the converter's power capability. On the other hand, the DC-link energy storage element has a relatively large physical volume, and when electrolytic capacitors are used, in the case of a voltage DC-link, there is potentially a reduced system lifetime.

With the goal of higher power density and reliability, it is hence obvious to consider the so-called Matrix Converter concepts that achieve three-phase AC/AC conversion without any intermediate energy storage element. The physical basis of these systems is the constant instantaneous power produced by a symmetrical three-phase current-voltage system, which allows, for example, to directly provide the constant power consumption of an electrical machine generating constant torque and running at constant speed (Fig 2). Conventional direct Matrix Converters (CMC, Fig. 3a) carry out voltage and current conversion in one stage. Alternatively, there is the option of indirect conversion by means of an Indirect Matrix Converter (IMC, Fig. 3b). As with the U-BBC and I-BBC, separate stages are again provided for voltage and current conversion, but the DC-link has no intermediate storage element. Realization of

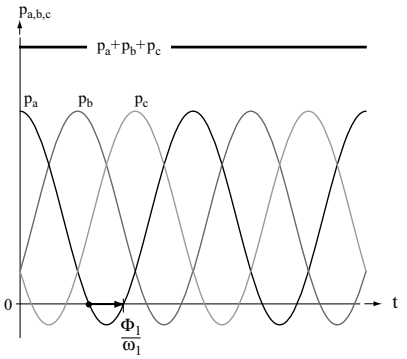

Figure 2: Instantaneous power $p_{a,b,c}(t)$ of the phases a, b, c of a symmetrical three-phase current-voltage system; also shown is the total power of the phases $p(t) = p_a(t) + p_b(t) + p_c(t) = P$.

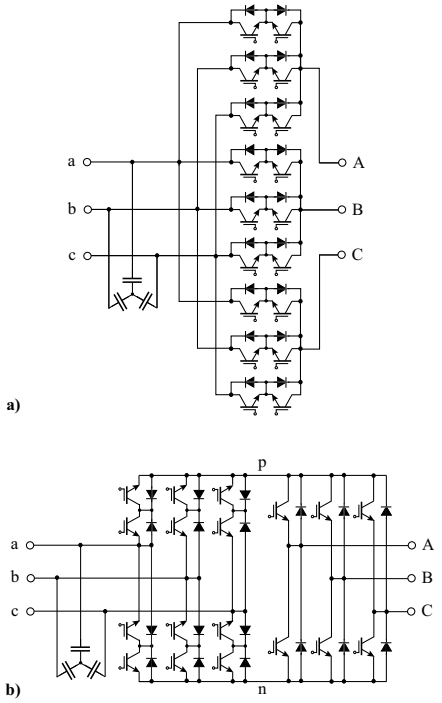

Figure 3: Basic Matrix Converters: a) Conventional (Direct) Matrix Converter (CMC), b) conventional Indirect Matrix Converter (IMC).

both converter systems requires in the basic configuration 18 IGBTs and 18 diodes, or 18 RB-IGBTs (CMC) or 12 RB-IGBTs and 6 RC-IGBTs (IMC): thus the storage element in the DC-link is eliminated at the cost of more semiconductors.

Matrix Converters are frequently seen as a future concept for variable speed drives technology, but despite intensive research over the decades they have until now only achieved low industrial penetration. The reason for this could be, apart from technical aspects, the more complex modulation and dimensioning calculations compared with DC-link converters and the high topological variations, especially with the introduction of the group of the Sparse Matrix Converters (SMC) and the Hybrid Matrix Converters (HMC), which is a mixture between matrix and DC-link converters. A classification of DC-link and Matrix Converter concepts presented up to now in the literature is shown (limited to forced commutated systems) in Fig. 4.

In this paper, starting from the well-known converter systems with voltage and current DC-links and their space vector modulation methods (Section II), a connection is made to the Indirect Matrix Converters (Section III) and finally to direct Matrix Converters (Section IV). A brief discussion of extended Matrix Converter circuits is given and a new unidirectional three-level Matrix Converter topology is proposed (Section V). This clearly shows the topological connections of the converter circuits that directly lead to an adaption of the modulation methods and allows the readers, who are familiar with space vector modulation of the voltage and current DC-link converters, to easily incorporate and identify the new modulation methods. Then a comparison of the converter concepts with respect to their fundamental, topology-related characteristics, complexity, control requirements and efficiency (Section VI) follows. Furthermore, taking the example of a converter that covers a typical operating region in the torque-speed plane (incl. holding torque at standstill), the necessary silicon area of the power semiconductor is calculated for maintaining a maximum junction temperature. This paper concludes with suggestions of subjects for further research in the field of Matrix Converters (Section VII).

II. AC/AC CONVERTERS WITH DC-LINK

In the following, the fundamentals of space vector modulation of PWM DC-link converters are briefly discussed and their functional equivalent circuit diagrams shown. For the U-BBC, the PWM inverter stage and for the I-BBC the PWM rectifier stage are considered. This allows the development of the IMC topology by simply combining the two subsystems, and the control of the IMC by connection and coordination of the subsystems' modulation methods.

A. Voltage DC-link PWM Inverter

The PWM inverter stage of the voltage DC-link AC/AC converter system shown in Fig. 1a is composed of three bridge legs where each exhibits the function of a switch that connects the output to either the positive or the negative DC bus, p and n.

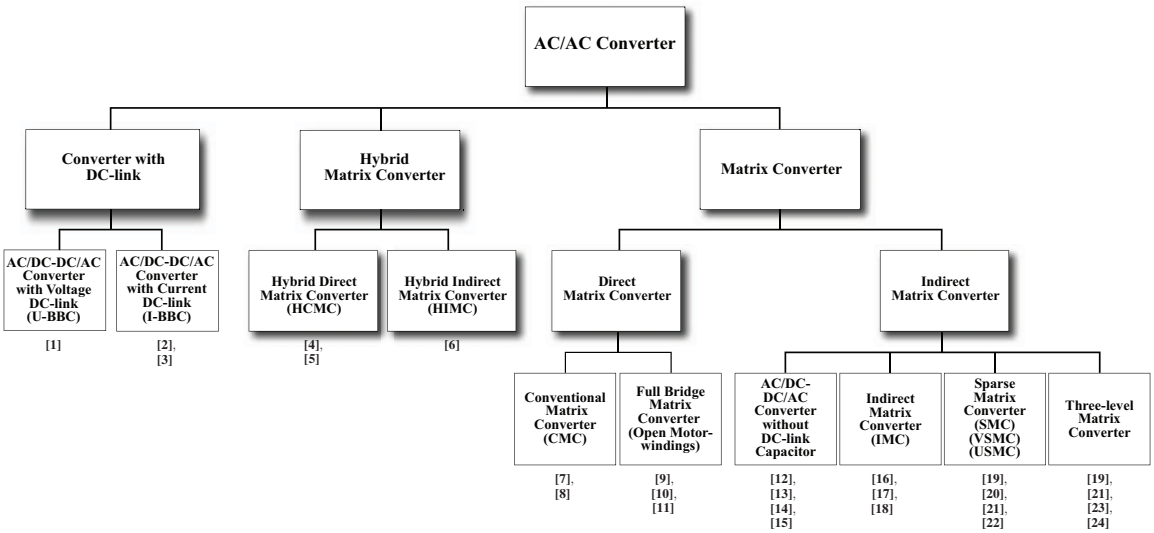

Figure 4: Classification of three-phase AC/AC converter circuits with chronologically ordered references to the technical literature.

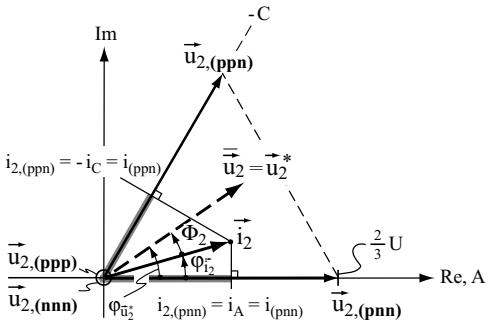

Figure 5: Voltage space vector sector for the U-BBC PWM inverter (output) stage. The DC-link current i (input current of the PWM inverter stage) can be determined by projection of the current space vector $\vec{i}_2$ onto the instantaneous voltage space vector $\vec{u}_{2,j}$.

The switching state of the inverter is defined by (xxx) where x is either p or n, for example (pnn) means that output A is connected to p, and outputs B and C are connected to n. Control of the switch is carried out such that over a pulse period T_P an average voltage space vector $\bar{\vec{u}}_2 = \vec{u}_2^*$ is formed at the output of the inverter, where $\vec{u}_2^*$ is the output voltage reference value and '$\bar{}$' is the local average value.

To form a steady-state three-phase voltage system

$$\vec{u}_2^* = \hat{U}_2^* \mathrm{e}^{j\varphi_{\vec{u}_2^*}} = \hat{U}_2^* \mathrm{e}^{j\omega_2^* t} \tag{1}$$

(with output voltage amplitude $\hat{U}_2^*$ and output frequency ω_2^*) in the simplest case, one must utilize the voltage space vectors closest to $\vec{u}_2^*$, i.e. two active switching states and the free-wheeling state. For the position of $\vec{u}_2^*$, as in Fig. 5, i.e. for $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$, there results the following possible switching state sequences

$$\ldots \left| \begin{matrix} (\underline{p}nn) - (\underline{p}pn) - (\underline{p}pp) \\ t_\mu = 0 \end{matrix} \right| \begin{matrix} (\underline{p}pp) - (\underline{p}pn) - (\underline{p}nn) \\ t_\mu = T_P/2 \end{matrix} \left| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \right. \tag{2}$$

$$\ldots \left| \begin{matrix} (pp\underline{n}) - (pn\underline{n}) - (nn\underline{n}) \\ t_\mu = 0 \end{matrix} \right| \begin{matrix} (nn\underline{n}) - (pn\underline{n}) - (pp\underline{n}) \\ t_\mu = T_P/2 \end{matrix} \left| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \right. \tag{3}$$

in order to achieve

$$\begin{aligned} \bar{\vec{u}}_2 = \frac{1}{T_P} \int_0^{T_P} \vec{u}_{2,j} \, \mathrm{d}t_\mu &= d_{(pnn)} \cdot \vec{u}_{2,(pnn)} + d_{(ppn)} \cdot \vec{u}_{2(ppn)} \\ &= d_{(pnn)} \frac{2}{3} U + d_{(ppn)} \frac{2}{3} U \mathrm{e}^{j\pi/3} \\ &= \vec{u}_2^* \end{aligned} \tag{4}$$

or the associated sequence of the DC-link current shown in Fig. 6. The DC-link current levels may be simply obtained via projection of the output current space vector $\vec{i}_2$ onto the instantaneous active voltage space vector. By restricting operation to a single free-wheeling state (c.f. (2) and (3)), one bridge leg remains clamped to p or n, and hence there are no switching losses in that bridge leg. It is advantageous to change the clamping between the phases in such a way that the phase carrying the highest current is not switched. With an approximately ohmic load (e.g. a permanent magnet synchronous machine), therefore for the angle $\varphi_{\vec{u}_2^*} \in [0, \pi/6]$ Phase A should be permanently connected to p and for $\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$ Phase C should be permanently connected to n.

Independent of the switching state sequence utilized, a fundamental amplitude of the output phase voltage can be formed without overmodulation, where the modulation index M_2 is

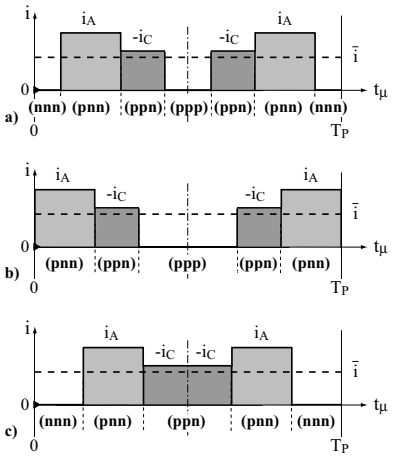

Figure 6: DC-link current i waveform for one pulse period a) switching state sequence (nnn)-(pnn)-(ppn)-(ppp), b) clamping pulse pattern (p̲nn)-(p̲pn)-(p̲pp), and c) clamping pulse pattern (nn̲n)-(pn̲n)-(pp̲n).

defined as

$$M_2 = \frac{\hat{U}_2^*}{U/2} = [0, 2/\sqrt{3}]. \tag{5}$$

The current conversion of the converter, i.e. the transformation of the output phase currents, is determined not only by the switching state, or the modulation index, but also by the phase angle Φ_2 between the output current $\vec{i}_2$ and $\vec{u}_2^*$. As clearly shown by Fig. 7, the average DC-link current, which is formed from the phase current blocks, shifts with increasing Φ_2 from the maximum value to a zero value. The local mean value of the DC-link current is thus given by

$$\bar{i} = I = \frac{3}{4} M_2 \hat{I}_2 \cos \Phi_2. \tag{6}$$

In summary, the output voltage $\hat{U}_2^*$ (and ω_2^*), is directly formed (i.e. load independent) from the DC-link voltage. In contrast, the backward current conversion is determined not only by the load amplitude $\hat{I}_2$ resulting from $\hat{U}_2^*$ and ω_2^*, but also by the phase angle of the load Φ_2.

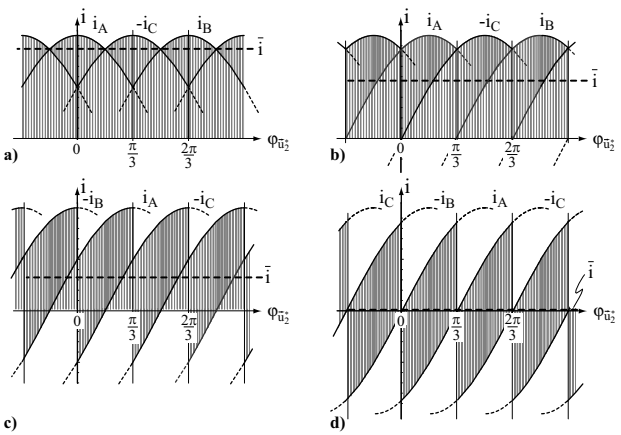

Figure 7: Simulation of the DC-link current waveform for characteristic load current phase angles Φ_2; a) $\Phi_2 = 0$, b) $\Phi_2 = \pi/6$ (ohmic-inductive load), c) $\Phi_2 = \pi/3$ and d) $\Phi_2 = \pi/2$ (purely inductive load). Assumes $M_2 = 2/\sqrt{3}$ and ripple-free phase currents.

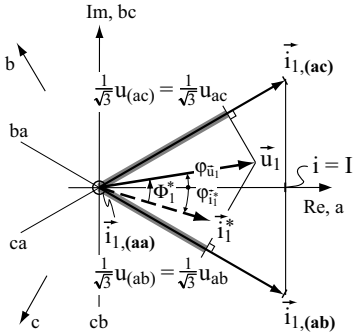

Figure 8: Current space vector sector for the I-BBC PWM rectifier (input) stage. Output voltage u waveform of PWM rectifier can be obtained by projection of the mains voltage space vector $\vec{u}_1$ onto the instantaneous input current space vector $\vec{i}_{1,k}$.

B. Current DC-link PWM Rectifier

The input stage of the current DC-link AC/AC converter has the basic functionality of a diode bridge with regard to the conducting state of the power transistors, which is independent of the filter capacitors' voltage magnitude on the mains side.

Control of the power transistors must be carried out such that a path is always available to the impressed DC-link current. At least one transistor of the positive and one transistor of the negative bridge halves must therefore always be held in the on-state.

If now a sinusoidal, symmetric input current system $\bar{\vec{i}}_1$ is to be formed after filtering of switching frequency spectral components

$$\bar{\vec{i}}_1 = \vec{i}_1^{\,*} = \hat{I}_1^* \mathrm{e}^{\,j\varphi_{\vec{i}_1^*}} = \hat{I}_1^* \mathrm{e}^{\,j(\omega_1 t - \Phi_1^*)} \tag{7}$$

with phase current amplitude $\hat{I}_1$, mains frequency ω_1 and mains current phase angle Φ_1^*, then in analogy to the considerations for the U-BBC, the switching states with the current space vectors closest to $\vec{i}_1^{\,*}$ must again be utilized. Thus for the sector $\varphi_{\vec{i}_1^*} \in [-\pi/6, +\pi/6]$ shown in Fig. 8, three possible switching state sequences may be employed

$$\ldots \left| \begin{matrix} (\underline{a}b) - (\underline{a}c) - (\underline{a}a) \\ t_\mu = 0 \end{matrix} \right| \begin{matrix} (\underline{a}a) - (\underline{a}c) - (\underline{a}b) \\ t_\mu = T_P/2 \end{matrix} \left| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \right. , \tag{8}$$

$$\ldots \left| \begin{matrix} (\underline{a}c) - (\underline{a}b) - (\underline{a}a) \\ t_\mu = 0 \end{matrix} \right| \begin{matrix} (\underline{a}a) - (\underline{a}b) - (\underline{a}c) \\ t_\mu = T_P/2 \end{matrix} \left| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \right. , \tag{9}$$

$$\ldots \left| \begin{matrix} (\underline{a}c) - (\underline{a}a) - (\underline{a}b) \\ t_\mu = 0 \end{matrix} \right| \begin{matrix} (\underline{a}b) - (\underline{a}a) - (\underline{a}c) \\ t_\mu = T_P/2 \end{matrix} \left| \begin{matrix} \ldots \\ t_\mu = T_P \end{matrix} \right. , \tag{10}$$

which differ regarding the commutation voltages that occur for the individual switching operations. Therefore, for a given Φ_1^* different switching losses result. The details of this can be found in [3], [25]. It is, however, important to note that in contrast to the converter with impressed DC voltage, the free-wheeling state can now also be placed between two active switching states. Starting from one of the two active states, this can be achieved by changing the state of only a single switch. It can be derived from the converter modulation function that a phase current amplitude equal to the magnitude of the DC-link current can be formed without overmodulation, the modulation index M_1 is

$$M_1 = \frac{\hat{I}_1^*}{I} \quad ; \quad M_1 \in [0, 1]. \tag{11}$$

The output voltage of the input stage for the individual switching states for one pulse period is shown in Fig. 9. As can be seen, the individual voltage levels may be simply obtained

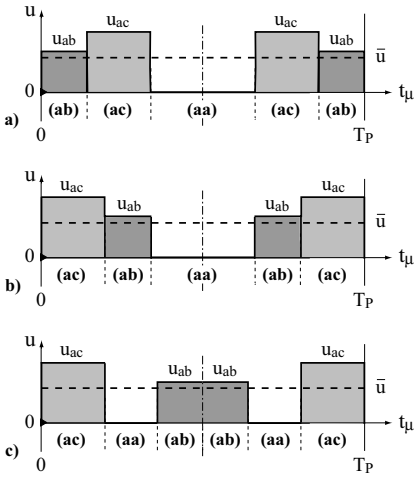

Figure 9: Input stage waveforms of the I-BBC for one pulse period; a) switching state sequence (ab)-(ac)-(aa); b) switching state sequence (ac)-(ab)-(aa); c) switching state sequence (ac)-(aa)-(ab).

by projecting the mains voltage space vector $\vec{u}_1$ onto the instantaneous active current space vector. The waveform of the output voltage is shown in Fig. 10. The current on the input side, i.e. in particular the resulting current amplitude, is determined by the nature of the converter and the output voltage formation is dependent on the (preselectable) mains current phase angle Φ_1^* in order to fulfil the power balance requirement. With increasing Φ_1^*, the mean output voltage

$$\bar{u} = \frac{3}{2} M_1 \hat{U}_1 \cos \Phi_1^* \tag{12}$$

decreases. Therefore, the instantaneous values of the mains line-to-line voltages become smaller and display positive and negative polarity (Fig. 10c, d), until finally for $\Phi_1^* = \pi/2$ or $\cos \Phi_1^* = 0$, i.e. for impression of a purely reactive current into the mains, $\bar{u} = 0$ results. A further increase of Φ_1^* leads to reversal of the polarity of the output voltage and hence the direction of the power flow. As we shall see later, this is of fundamental importance for the Matrix Converter.

It must be noted that the mains current amplitude $\hat{I}_1^*$ and the mains current phase angle Φ_1^* are predeterminable parameters.

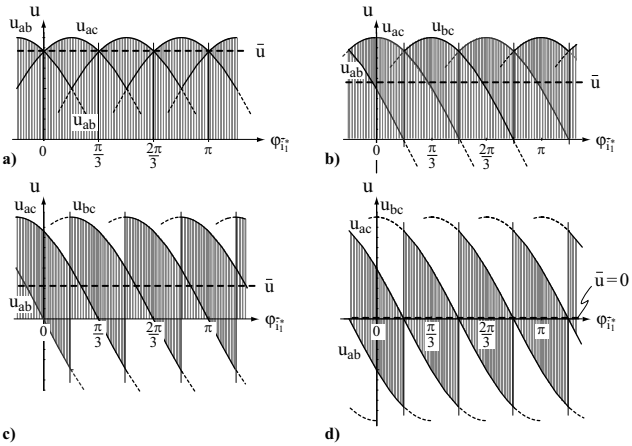

Figure 10: Simulation of the output voltage u waveforms of the I-BBC input stage for characteristic mains current phase angles Φ_1^*; a) $\Phi_1^* = 0$ (ohmic fundamental mains behavior) , b) $\Phi_1^* = \pi/6$, c) $\Phi_1^* = \pi/3$ and d) $\Phi_1^* = \pi/2$. Simulation assumes $M_1 = 1$ and ideal input voltages.

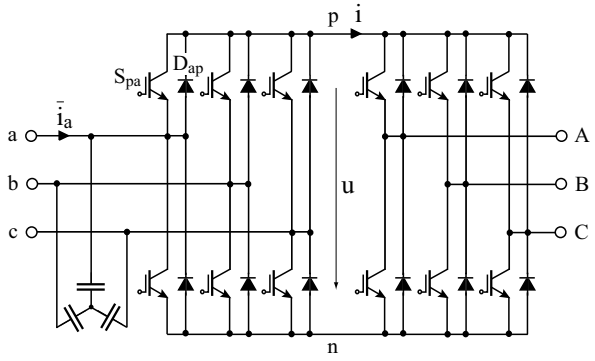

Figure 11: Indirect AC/AC converter with a voltage DC-link without energy storage.

Hence with a given mains voltage the mean value $\bar{u}$ of the output voltage is determined, whereby the maximum value of the output voltage is obtained only for $\Phi_1^* = 0$.

III. Indirect Matrix Converter

By considering the basic functionality and modulation of the AC/DC converter with impressed output current and the DC/AC converter with impressed input voltage, the basis is created for the analysis of Matrix Converter circuits. In the next step we develop the topology of the IMC, starting from the circuit of the U-BBC.

A. AC/AC converter with voltage DC-link without energy storage

In order to derive a Matrix Converter topology from the AC/AC converter with DC-link capacitor, it is obvious to first consider the case where the DC-link capacitor is omitted, or becomes the filter capacitors on the mains side (Fig. 11). Because of the impressed current on the load side, voltage impression must also be assured on the input side. Such a system was suggested in [12] and investigated in more detail in [13]–[15] and is in industrial use.

The input stage of the system in Fig. 11 represents a synchronous three phase rectifier. Its conductive state is directly defined by the mains voltage and cannot be influenced via the control. The load phase current segments in the DC-link, that are generated by the PWM inverter, must be supplied by the input stage through the diodes with the highest instantaneous mains phase-to-phase voltage across them. In order to avoid a mains phase short circuit, only the power transistors that are connected in anti-parallel to a conducting diode may be switched on. The transistors of the input stage thus have no influence on the formation of the DC-link voltage and only permit a reversal of the current flow direction. This is needed since negative components of the DC-link current occur for $\Phi_2 > \pi/6$ (Fig. 7) or for the case of energy feedback into the mains where a negative mean value of the DC-link current exists. The switching frequency of the input stage power transistors is equal to the mains frequency and has the advantage of conducting zero current within a free-wheeling interval of the PWM inverter stage. Thus in contrast to the conventional converter structure with DC-link storage (U-BBC), there are no switching losses of the input stage, hence the system has a higher energy conversion efficiency and still allows bidirectional power flow with the mains. However, the variation of the DC-link voltage with six times mains frequency represents a fundamental disadvantage. According to Fig. 12, a minimum DC-link voltage

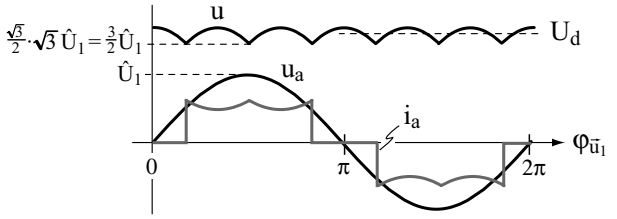

Figure 12: Waveforms of the mains phase voltage u_a, the associated input phase current $\bar{i}_a$ (with filtered switching frequency components) and the DC-link voltage u of the circuit in Fig. 11.

$$u_{\min} = \frac{3}{2}\hat{U}_1 \tag{13}$$

occurs, so that the amplitude of the output voltage fundamental is limited to

$$\hat{U}_2^* < \frac{2}{\sqrt{3}} \cdot \frac{1}{2} u_{\min} = \frac{\sqrt{3}}{2} \cdot \hat{U}_1 \approx 0.86\,\hat{U}_1 \tag{14}$$

when operated without overmodulation. We shall find the same limitation of the output voltage later for the IMC and CMC. Furthermore, for a constant power demand of the load, a variation of the local mean value of the DC-link current occurs that is inversely proportional to the variation of the DC-link voltage and appears in the two mains phases of the conducting diodes. The system thus exhibits a relatively high power factor of $\lambda \approx 0.95$, but because of the $\pi/3$-wide gap in the input phase currents, it also has relatively high harmonic current levels.

Hence to obtain a sinusoidal input current, the circuit in Fig. 11 has to be extended according to [26] in such a way that the conductive state of the input stage can be directly defined, i.e. independent of the mains voltage.

B. Indirect Matrix Converter

In order to be able to influence the conductive state of the input stage, it is first necessary to place a power transistor in series with each diode (e.g. $\mathrm{S_{ap}}$ and $\mathrm{D_{ap}}$ in Fig. 13). However, when this series transistor blocks, a forward voltage can occur that must not appear across the anti-parallel transistor $\mathrm{S_{pa}}$, which is used for the reverse power flow. This is achieved by adding the diode $\mathrm{D_{pa}}$ in series with $\mathrm{S_{pa}}$. Overall, the input side now has two mutually anti-parallel current link PWM rectifier stages. Together with the PWM inverter output stage, they form the topology of the Indirect Matrix Converter, IMC. The power transistor and diode combinations between the input phases and the DC-link bus bars form separately controllable four-quadrant switches, which could also be realized by the anti-parallel connection of RB-IGBTs.

The simultaneous turn-on of two four-quadrant switches of the upper or the lower bridge halves would lead to a short circuit

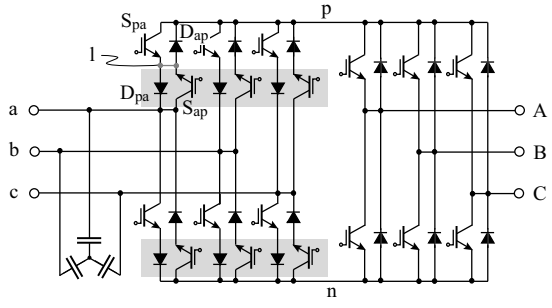

Figure 13: Development of the switching topology of the IMC via extension of the indirect AC/AC converter shown in Fig. 11.

of two mains phases and must therefore be avoided. The basic function of the input stage can thus be abstracted in the same way as for the input section of the I-BBC and can be represented by means of two single-pole, triple-throw switches. With regard to modulation, the IMC represents a combination of the input stage of the I-BBC, with the DC-link inductor shifted to the load side, and the output stage of the U-BBC, with the DC-link capacitor shifted to mains side (Fig. 14a).

The modulation of the system is carried out such that for a given input voltage $\vec{u}_1$ only positive mains line-to-line voltages are switched to the DC-link, and the desired output voltage $\underline{\vec{u}}_2 = \vec{u}_2^*$ is formed along with a sinusoidal mains current $\underline{\vec{i}}_1$ with a defined phase angle Φ_1^* relative to $\vec{u}_1$. On the input side, only the phase angle $\varphi^*_{\underline{\vec{i}}_1}$ can be predetermined, and not the amplitude of the mains current. The current amplitude adjusts itself via the load current segments, which reach the input via the DC-link, in such a way that the mains provides the real power required by the load.

Starting from, e.g., $\varphi_{\vec{u}_1} \in [0, \pi/6]$ (Fig. 14b), and projecting $\vec{u}_1$ onto the axes ab, ac and bc leads to positive DC-link voltages; correspondingly, the switching states (ab), (ac), (bc) of the input stage or the mains line-to-line voltages u_{ab}, u_{ac}, u_{bc} are permissible within the particular segment of $\varphi_{\vec{u}_1}$. For each of these DC-link voltages, the output stage can form a space vector hexagon. A total of 18 different active voltage vectors and a zero vector are possible, realizable both by the free-wheeling states (nnn) and (ppp) of the output stage and by the free-wheeling states (aa), (bb), (cc) of the input stage (Fig. 15b). The IMC thus exhibits a large variety of output voltage space vectors, similar to a three-level converter.

Considering the current transfer from the load side to the input, we can again limit ourselves to a $\pi/3$-wide interval (of the output period), e.g. $\varphi_{\vec{i}_2} \in [-\pi/6, +\pi/6]$ or $i_A > 0$, $i_B < 0$, $i_C < 0$ (Fig. 14c). For switching states (pnn), (ppn) and (pnp) the respective instantaneous positive DC-link currents $i_{(pnn)} = i_A$, $i_{(ppn)} = -i_C$, $i_{(pnp)} = -i_B$ occur. For the inverse switching states (npp), (nnp) and (npn) DC-link currents of the same absolute value, but of inverse polarity $i_{(npp)} = -i_A$, $i_{(nnp)} = +i_C$ and $i_{(npn)} = +i_B$ result. These DC-link currents are now translated into input current space vectors corresponding to the switching state of the input stage.

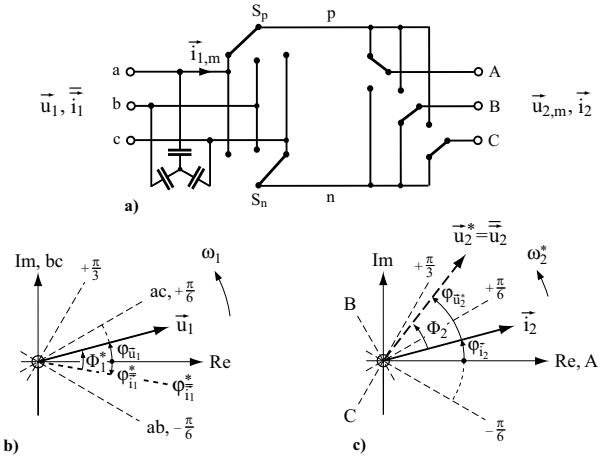

Figure 14: a) Idealized IMC circuit topology, b) mains voltage space vector $\vec{u}_1$ and reference phase angle $\varphi^*_{\underline{\vec{i}}_1} = \varphi_{\vec{u}_1} - \Phi_1^*$ of input current space vector $\underline{\vec{i}}_1$; c) reference output voltage space vector $\vec{u}_2^*$ and load current space vector $\vec{i}_2$ with angle $\varphi_{\vec{i}_2} = \varphi_{\vec{u}_2^*} - \Phi_2$.

As stated above, only the switching states (ab), (ac) and (bc) are permissible in order to provide a positive DC-link voltage.

If, for example, switching state (ac) of the input stage is present, we obtain three input current space vectors pointing in the direction (ac) according to the three DC-link instantaneous values (switching states (pnn), (ppn), (pnp)). Negative DC-link current values result for the inverse switching states and lead to input current space vectors $\vec{i}_{1,(ac)(npp)} = -\vec{i}_{1,(ac)(pnn)}$, $\vec{i}_{1,(ac)(nnp)} = -\vec{i}_{1,(ac)(ppn)}$, $\vec{i}_{1,(ac)(npn)} = -\vec{i}_{1,(ac)(pnp)}$ oriented in the opposite direction to (ac), i.e. in the direction (ca). Input current space vectors of the mutually inverse switching states of the input stage have the same absolute values

$$\begin{aligned} |\vec{i}_{1,(ac)(pnn)}| &= |\vec{i}_{1,(ac)(npp)}| = i_A, \\ |\vec{i}_{1,(ac)(ppn)}| &= |\vec{i}_{1,(ac)(nnp)}| = -i_C, \\ |\vec{i}_{1,(ac)(pnp)}| &= |\vec{i}_{1,(ac)(npn)}| = -i_B. \end{aligned} \tag{15}$$

During free-wheeling of the output stage, (nnn) or (ppp), no DC-link current occurs and hence no input current is formed. The same applies for the switching states (aa), (bb) and (cc) of the input stage, which close the DC-link current path without inclusion of the mains.

Through a suitable combination of switching states, a desired target value of the output voltage $\vec{u}_2^*$ and simultaneously desired

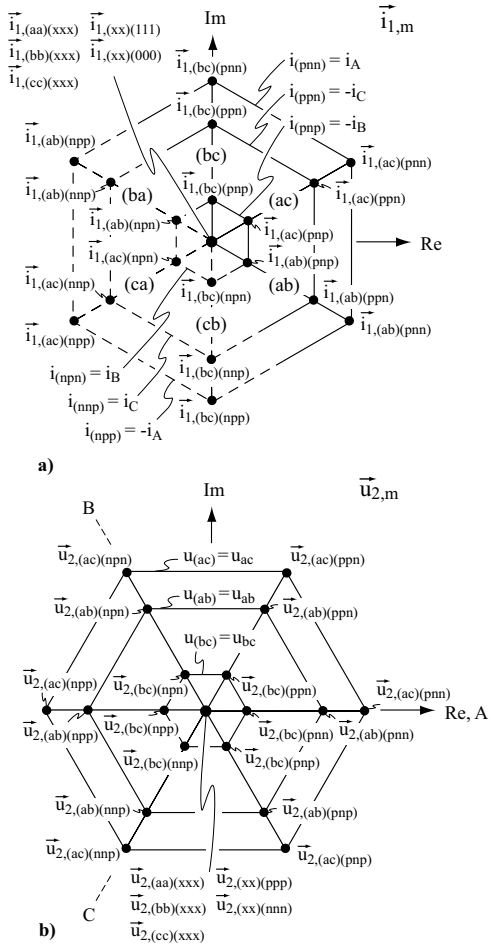

Figure 15: Current conversion a) and voltage conversion b) of the IMC for the input voltage and output current space vector $\vec{u}_1$ and $\vec{i}_2$ according to Fig. 14. To maintain $u > 0$, input current space vectors in the direction of (ca), (ba), (cb) (dotted) can only be formed by inversion of the DC-link current, i.e. inversion of the switching state of the output stage.

phase position $\varphi^*_{\vec{i}_1}$ of the mains current $\vec{i}_1$ must be formed, whereby $\varphi^*_{\vec{i}_1}$ is finally determined by the angular position $\varphi_{\vec{u}_1}$ of the input voltage space vector $\vec{u}_1$ and the desired phase shift Φ^*_1 of $\vec{i}_1$ with reference to $\vec{u}_1$, $\varphi^*_{\vec{i}_1} = \varphi_{\vec{u}_1} - \Phi^*_1$. Further considerations are based upon the condition shown in Fig. 16. For a given $\vec{u}_2^*$, the active switching states (pnn) and (ppn) of the output stage of the IMC should be employed.

The input stage supplies the DC-link voltage, which should be as large as possible in order to obtain the highest possible output voltage magnitude. Thus, operation is limited to the outermost voltage space vector hexagon (Fig. 15b) for the entire pulse period, i.e. the switching state (ac) of the input stage or the DC-link voltage $u_{(ac)} = u_{ac}$. As shown by inspection of the input current space vector diagram (Fig. 16a), this would, however, not allow to achieve the required $\varphi^*_{\vec{i}_1}$ to be set, since only two input phases, a and c, are connected to the DC-link and hence an input current space vector in the direction (ac) is formed over the full pulse period. The absolute value of the vector would be equal to the values $i_{1,(ac)(pnn)} = i_A$, $i_{1,(ac)(ppn)} = -i_C$ and $i_{1,(ac)(nnn)} = i_{1,(ac)(ppp)} = 0$, which is dependent of the switching state of the output stage. Viewed over the mains period, the current space vector would thus retain the direction of a line-to-line axis within $\pi/3$-wide segments, with a block-shaped mains current waveform, as for the circuit in Fig. 11.

In order to always obtain the desired position $\varphi^*_{\vec{i}_1}$, i.e. a continuous rotation of the current space vector $\vec{i}_1$ and hence a sinusoidal input current, it is mandatory to include a second active switching state of the input stage, in this case (ab), in the modulation method. This leads to a second DC-link voltage level $u_{(ab)} = u_{ab}$ and hence to a second output voltage space vector hexagon. For the modulation of the IMC, a switching state sequence must therefore be employed that combines active switching states $(ac)(ppn)$, $(ac)(pnn)$, $(ab)(ppn)$, $(ab)(pnn)$ and the free-wheeling states $(xx)(ppp)$ and $(xx)(nnn)$ or $(aa)(xx)$, $(bb)(xxx)$ and $(cc)(xxx)$.

1) Modulation Method 1: One method consists of leaving the input stage at first in the switching state (ac) while the output side cycles through the switching state sequence $(pnn) - (ppn) - (ppp)$. In this way, voltage space vectors pointing to the corners of the triangular segment of the space vector plane valid for $u = u_{ac}$ are generated, whereby the input current space vector in the direction (ac) is left in place. Next, the input stage changes to (ab) and consequently only input current space vectors oriented in the direction (ab) occur while the output stage repeats the switching state sequence, advantageously in reverse order $(ppp) - (ppn) - (pnn)$. However, the voltage space vectors magnitudes are now equal to $u = u_{ab}$. When the end of the first pulse half-period is reached the sequence is then immediately repeated again in the opposite direction.

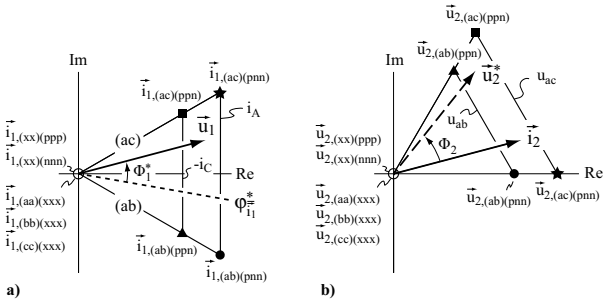

Figure 16: Sector of the space vector diagrams according to Fig. 15 and is relevant for $\varphi^*_{\vec{i}_1} \in [-\pi/6, +\pi/6]$ and $\varphi_{\vec{u}_2^*} \in [0, +\pi/3]$. Switching states for short voltage space vectors are omitted.

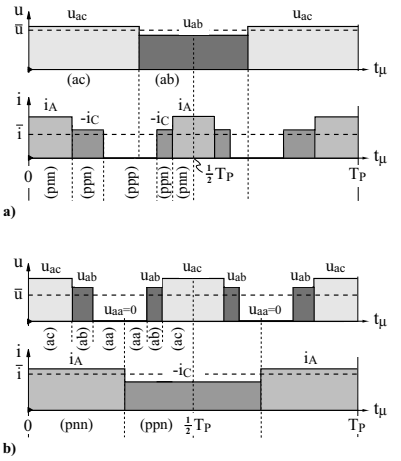

Figure 17: Waveforms of the DC-link voltage u and current i for one pulse period T_P for a) modulation method 1 and b) modulation method 2, assuming the current and voltage conditions in Fig. 14.

$$\begin{aligned} \ldots \big|_{t_\mu=0} \;& (ac)(pnn) - (ac)(ppn) - (ac)(ppp) \\ & -(ab)(ppp) - (ab)(ppn) - (ab)(pnn) \big|_{t_\mu=T_P/2} \\ & (ab)(pnn) - (ab)(ppn) - (ab)(ppp) \\ & -(ac)(ppp) - (ac)(ppn) - (ac)(pnn) \big|_{t_\mu=T_P} \ \ldots \end{aligned} \tag{16}$$

The third possible switching state of the input stage, (bc), can be omitted, i.e. the modulation can be limited in this case to those two switching states of the input stage which lead to the higher DC-link voltages and hence to the maximum possible output voltage ($u_{ac} > u_{ab} > u_{bc}$).

For the switching state sequences shown in (16), the switching cycle of the output stage is embedded in the switching cycle of the input stage; thus for a complete cycle of the current space vector triangle, the voltage space vector triangle is run through twice with different DC-link voltages. The switching state sequence basically exhibits the form given in (10) for the current DC-link rectifier. For the presented modulation method, the switching of the input stage occurs during the free-wheeling state of the output stage. It thus has the advantage that the change of the input stage switching state takes place when the DC-link current (Fig. 17a) is absent, so that no switching losses of the input stage occur.

2) Modulation Method 2: As an alternative to modulation method 1, a different switching state of the output stage, e.g. (pnn) can be assumed at the start of a pulse period, where the input stage cycles through the switching state sequence $(ac) - (ab) - (aa)$, i.e. with fixed output voltage space vectors, and a current space vector triangle is run through. After this, the output stage changes from (pnn) to (ppn), whereupon a new position of the discrete output voltage space vector results; the switching state sequence of the input stage is cycled through in reverse sequence, $(aa) - (ab) - (ac)$, and the first pulse half-period ends. During the second half period the entire sequence

is repeated in reverse order

$$\begin{aligned}\ldots \big|_{t_\mu=0}\ & (ac)(pnn)-(ab)(pnn)-(aa)(pnn)\\ & -(aa)(ppn)-(ab)(ppn)-(ac)(ppn)\big|_{t_\mu=T_P/2}\\ & (ac)(ppn)-(ab)(ppn)-(aa)(ppn)\\ & -(aa)(pnn)-(ab)(pnn)-(ac)(pnn)\big|_{t_\mu=T_P}\ \ldots\ .\end{aligned} \tag{17}$$

This switching state sequence is, in principle, known from the AC/AC converter with current DC-link (c.f. (9)), however to date it has not yet been described in the literature for the IMC. The switching sequence of the input stage is embedded in the switching sequence of the output stage. The switching state change of the output stage occurs within the freewheeling interval (aa) of the input stage, i.e. with DC-link voltage absent (Fig. 17b). In this way, switching losses of the output stage are avoided and all of the switching losses occur in the input stage.

Basically, $\vec{u}_2^*$ and $\varphi_{\vec{i}_1}^*$ may be set by modulation method 1 or 2. However, for modulation method 2, the change of the switching state of the input stage must be carried out at full DC-link current and hence, as later for the CMC (Section IV), a relatively complex multistage commutation sequence must be implemented, which avoids interruption of the DC-link current and a short-circuit of mains phases. In contrast, the conditions are extremely simple for modulation method 1. The four-quadrant switches of the input stage can be switched at zero current and only a small safety time is required to avoid the short circuiting of the mains phases. For a practical realization, therefore, modulation method 1 is clearly preferred to modulation method 2 and is therefore taken as the basis for further considerations.

It is also important to point out here that the voltage transfer ratio of the IMC is independent of the chosen modulation method, as for the AC/AC converter without DC-link capacitor, by

$$\hat{U}_{2,\max}^* \le \frac{\sqrt{3}}{2}\cdot\hat{U}_1 \tag{18}$$

(for $\cos\Phi_1^*=1$). For a general phase angle of the mains current

$$\hat{U}_{2,\max}^* \le \frac{\sqrt{3}}{2}\cdot\hat{U}_1\cos\Phi_1^* \tag{19}$$

applies.

As shown in Section II, the DC-link voltage formed decreases with increasing Φ_1^*, which results in a corresponding reduction of the achievable maximum output voltage.

C. Sparse Matrix Converter

As shown in Fig. 13, the input stage of the IMC is realized with four-quadrant switches and could in principle also be operated with a negative DC-link voltage. On the other hand, however, for the PWM inverter stage it is mandatory to maintain $u>0$. It is hence obvious to consider reduction of the number of switches by limiting the operating range of the PWM rectifier stage to a unipolar DC-link voltage that retains the option of bidirectional current flow.

The derivation of a simplified bridge branch structure of the IMC is shown in Fig. 18. If Phase a of the IMC (Fig. 18a) is connected bidirectionally with the positive DC-link bus p, i.e. if S_{pa} and S_{ap} are turned-on and S_{an} and S_{na} turned-off. The positive DC-link voltage will always appears as a blocking voltage over S_{an}. Thus, the function of S_{na} is limited to providing a current path from the negative DC-link bus n (via D_{na}) to the phase input terminal a. For this purpose, no direct connection of the emitter of S_{na} with a is required.

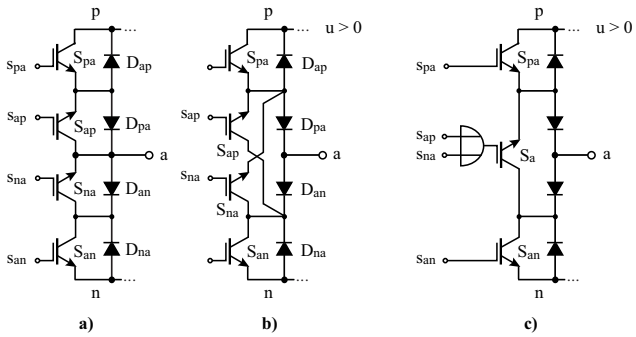

Figure 18: Derivation of the bridge branch topology c) of the SMC, starting from the circuit topology a) of the IMC.

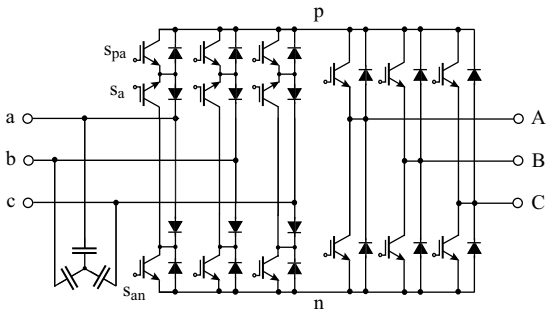

Figure 19: Circuit topology of the Sparse Matrix Converter (SMC, or *Swiss Matrix Converter*).

The return current feedback can be provided via S_{na} and D_{pa}. An analogous consideration for S_{ap} leads to the direct parallel connection of S_{na} and S_{ap} shown in Fig. 18b, which may be replaced by a single switch S_a (Fig. 18c). The effort for the realization of the IMC is thus reduced from 18 IGBTs and (18 diodes) to 15 IGBTs (and 18 diodes). The variant of an IMC shown in Fig. 19 is called a Sparse Matrix Converter (SMC, also known as the Swiss Matrix Converter) [19], [22].

A more comprehensive simplification of the circuit topology is possible by limiting the converter to unidirectional power flow. The transistors S_{pa} and S_{an} (Fig. 18c) only conduct for $i<0$, i.e. when current flows from the DC-link into the mains, and can thus be omitted when connected to passive (and mostly ohmic) loads. The resulting topology is the Ultra Sparse Matrix Converter (USMC, also known as the Unidirectional Swiss Matrix Converter, Fig. 20a). As is directly obvious with reference to Fig. 7 and Fig. 10, the operation of the converter is limited to

$$\Phi_1^*=\left[-\frac{\pi}{6},+\frac{\pi}{6}\right] \quad \text{and} \quad \Phi_2=\left[-\frac{\pi}{6},+\frac{\pi}{6}\right], \tag{20}$$

i.e. not restricted to a purely ohmic load ($\Phi_2=0$). This is explained by the absence of a connection between the mains star point, the DC-link and the load. Apart from the implementation shown in Fig. 20a, the USMC can also be realized with 6 IGBTs in the input stage (Fig. 20b). This circuit variant is obtained by simply omitting the current-carrying power semiconductor of the input stage of the IMC (Fig. 13) for $i<0$, and exhibits lower conduction losses but a greater realization effort. Finally we must mention a fully bidirectional variant of the IMC, the Very Sparse Matrix Converter (VSMC, [12], [19]) shown in in Fig. 21, whose four-quadrant switches cannot be controlled separately according to the current direction. This controllability is not required when using modulation method 1. As described in Section III-B, the switching of the transistors of the input

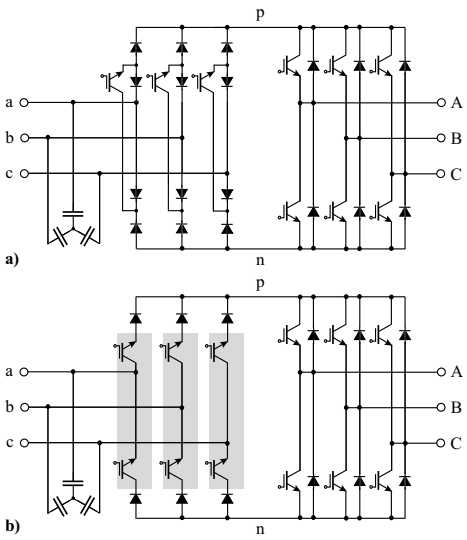

Figure 20: a) Circuit topology of the Unidirectional Ultra-Sparse Matrix Converter (USMC, or Unidirectional Swiss Matrix Converter), b) circuit variant with low conduction losses, which allows the use of PWM inverter half bridge modules (on gray background).

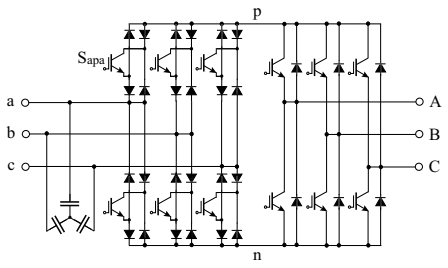

Figure 21: Very-Sparse Matrix Converter (VSMC) circuit topology.

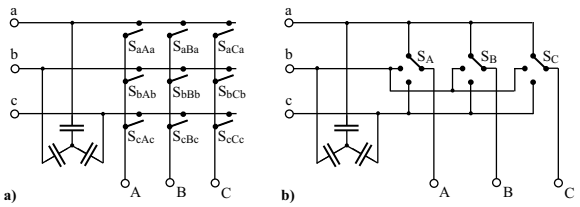

Figure 22: Idealized representation of the CMC as a) a switching matrix and b) in the form of a three-level converter

stage then takes place at zero current within the free-wheeling intervals of the inverter stage and thus only a safety interval is required between switch-off of one four-quadrant switch and the switch-on of the next four-quadrant switch.

IV. Direct Matrix Converter

In contrast to the IMC, for the CMC each of the input phases a, b, c can be directly connected with each output phase A, B, C via a four-quadrant switch and therefore be represented as a matrix (Fig. 22a). The four-quadrant switches, as for the input stage of the IMC, must be realized by the anti-series connection of IGBTs with antiparallel, free-wheeling diodes (an even better solution, with regard to the conduction losses, is by using an anti-series connection of RB-IGBTs).

To take into account an inductive load, it is mandatory to arrange the filter capacitors at the input of the CMC to enable free commutation of the current. The capacitors, in connection with the mains side series inductance, help filter the load current

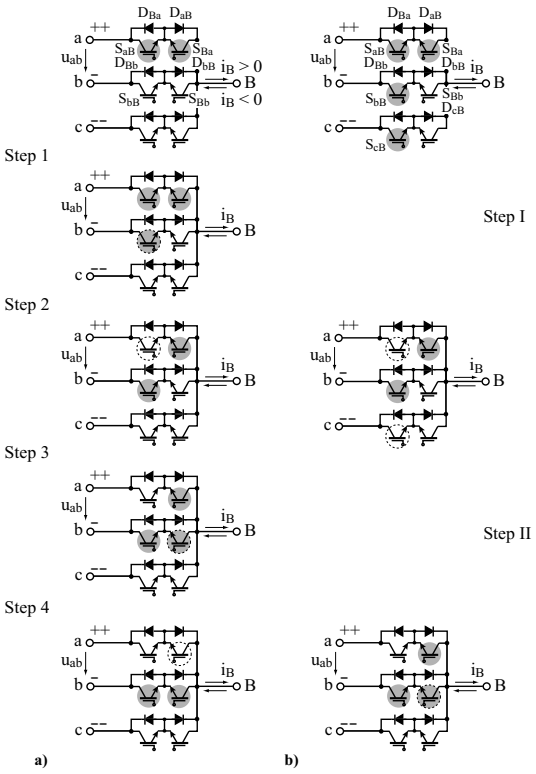

Figure 23: Switching states of the single-pole, triple-throw switch $B - a,\ b,\ c$ of the CMC for a) voltage dependent four-step commutation (Steps 1 – 4) of connection $B - a$ to $B - b$ and b) voltage dependent two-step commutation (Steps I and II); for the connected input phase voltages, $u_a > u_b > u_c$ and $u_a > 0$, $u_b,\ u_c < 0$ are assumed.

blocks on the input side in order to form a continuous mains current. To avoid a short circuit of the impressed input voltages, simultaneous connection of two input phases to the same output phase must be strictly avoided. On the other hand, because of the impressed load current, one output phase must in any case be connected to one input, whereby it is also permissible to connect all outputs to the same input.

The basic functionality of the Matrix Converter can thus be represented by three single-pole, triple-throw switches whose poles are connected to the outputs (Fig. 22b). The obtained circuit topology clearly shows the strong similarity of the CMC to a three-level voltage DC-link PWM inverter and thus makes it clearer why the Matrix Converter has a greater functionality than the two-level PWM inverter.

The change of the switching state of the CMC must be carried out considering the impressed load current and the impressed input voltage. Suitable multi-step commutation strategies were first described in [27] and [28]. The commutation is thereby carried out depending on the sign of the current in the output phase that is to be connected to another input phase, or, as shown in Fig. 23, with dependence on the sign of the voltage difference of those input phases between which the commutation is carried out. In the case under consideration, u_{ab} must be taken into account.

Fig. 23a depicts the multi-step commutation strategy. There, transistors on a grey background are in the on-state and those surrounded by a dashed line indicate that a change of the switching state has happened in the present commutation step. Prior to transistor turn-off, a transistor of the branch that will take over the current has to be switched on in order to always

Table I: Classification of the switching states of the CMC.

Group I	(aaa)	(bbb)	(ccc)	
Group II	(cca)	(ccb)	(aab)	$\} u_{AB} = 0$
	(aac)	(bbc)	(bba)	
	(acc)	(bcc)	(baa)	$\} u_{BC} = 0$
	(caa)	(cbb)	(abb)	
	(cac)	(cbc)	(aba)	$\} u_{CA} = 0$
	(aca)	(bcb)	(bab)	
Group IIIa	(abc)	(cab)	(bca)	
Group IIIb	(acb)	(cba)	(bac)	

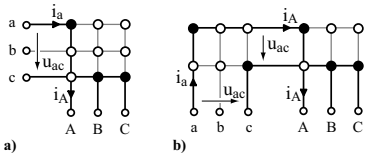

Figure 24: a) Conduction state of the CMC for switching state (acc) and b) associated switching state $(ac)(pnn)$ of the IMC.

provide a current path. The transistor to be turned on is selected such that no input phase short circuit occurs for the given commutation voltage, i.e. its series diode blocks the commutation voltage. Consequently, two possible current paths exist for one load current direction, and therefore the remaining transistor of the branch handing over the current can be turned off.

As proposed in [29] and [30], the four-step commutation strategy (Fig. 23a) can also be reduced to two steps (Fig. 23b). For this purpose, as many transistors as possible are always held in the on-state, so that when a commutation is required, fewer steps have to be executed. However, it must be noted that commutation of the CMC in all cases demands that the four-quadrant switches can be separately controlled according to their current direction.

The CMC has a total of $3^3 = 27$ possible switching states, which may be arranged in three groups according to Tab. I. For Group I all output phases are connected to the same input phase, and for Group II two outputs in each case are connected to the same input. The third output is switched to one of the remaining inputs, whereby a total of 18 possibilities exist. Finally, with Group III six further switching states are found where each output phase is connected to a different input phase which generates rotating output voltage or input current space vectors.

The use of rotating space vectors has been widely discussed when the concept of the CMC was first introduced [31] but it has lost considerable importance, therefore we shall in the following limit ourselves exclusively to the switching states of the Groups I and II. This type of output and input connection is also known from the IMC. According to Fig. 3b each connection between the output and the input phases is made via the DC-link rails p and n, whereas only two choices exist for the outputs. The control of the CMC can then be considered simply with reference to a (fictitious) IMC, i.e. obtained by recoding its switching states (Fig. 24). For example, the switching state $(ac)(pnn)$ of the IMC corresponds to the switching state (acc) of the CMC. In both cases the same output and input current space vectors are applied:

$$\begin{aligned} \vec{u}_{2,(acc)} &= \vec{u}_{2,(ac)(pnn)}, \\ \vec{i}_{1,(acc)} &= \vec{i}_{1,(ac)(pnn)}. \end{aligned} \tag{21}$$

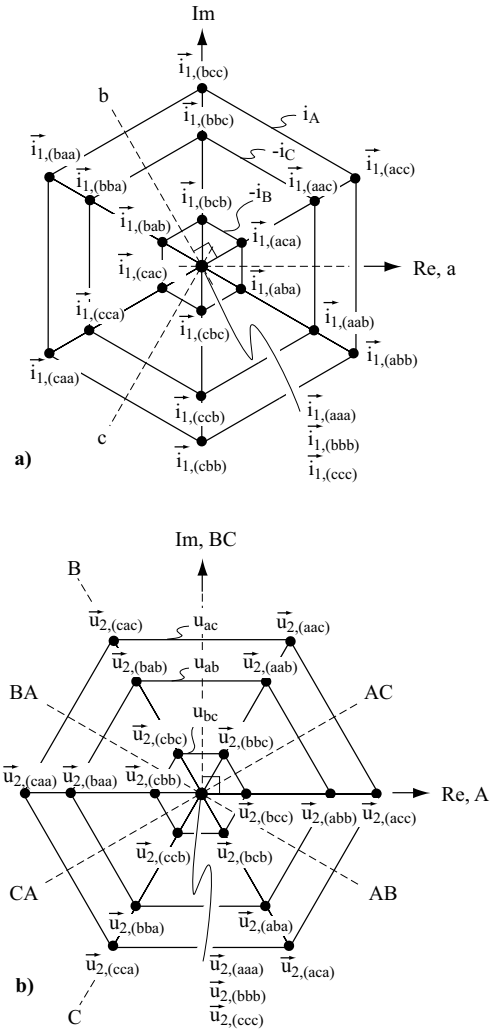

Figure 25: Input current space vector a) and output voltage space vector b) of the CMC for switching states of Groups I and II (Tab. I) assuming the input voltage and output current, $\vec{u}_1$ and $\vec{i}_2$, in Fig. 14.

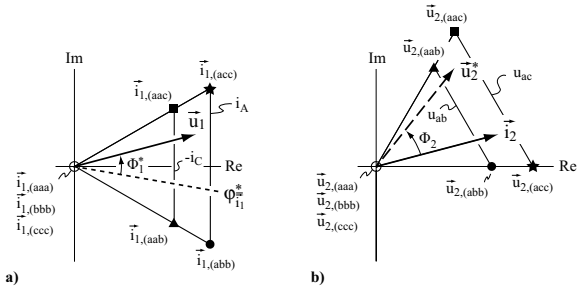

Figure 26: Relevant sectors of the space vector diagrams in Fig. 25 for $\varphi^*_{\vec{i}_1} \in [-\pi/6, +\pi/6]$ and $\varphi_{\vec{u}_2^*} \in [0, +\pi/3]$. Switching states leading to short length voltage space vectors are omitted.

For the given input voltage and load current vectors, $\vec{u}_1$ and $\vec{i}_2$, the CMC and IMC show the same space vector diagrams (cf. Fig. 25 and Fig. 15). By considering the change in coding of the switching states or taking into account the equivalence of the space vector diagrams Fig. 16 and Fig. 26, the switching state sequence of the IMC in (16) changes into the switching state sequence

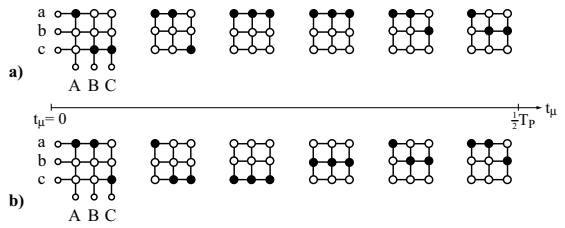

Figure 27: Switching state sequence of the CMC within a half pulse period with a) control in (22) and b) control in (24).

$$\begin{aligned}\ldots|_{t_\mu=0}\ & (\underline{a}cc)-(\underline{a}ac)-(\underline{a}aa)\\ & -(\underline{a}aa)-(\underline{a}ab)-(\underline{a}bb)|_{t_\mu=T_P/2}\\ & (\underline{a}bb)-(\underline{a}ab)-(\underline{a}aa)\\ & -(\underline{a}aa)-(\underline{a}ac)-(\underline{a}cc)|_{t_\mu=T_P}\ \ \ldots\end{aligned} \tag{22}$$

for the CMC. For the IMC in the angular range $\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$ the clamping of Phase C to n brings a greater reduction in the switching losses than the clamping of Phase A to p. This results in a new switching state sequence,

$$\begin{aligned}\ldots|_{t_\mu=0}\ & (ac)(ppn)-(ac)(pnn)-(ac)(nnn)\\ & -(ab)(nnn)-(ab)(pnn)-(ab)(ppn)|_{t_\mu=T_P/2}\\ & (ab)(ppn)-(ab)(pnn)-(ab)(nnn)\\ & -(ac)(nnn)-(ac)(pnn)-(ac)(ppn)|_{t_\mu=T_P}\ \ \ldots\end{aligned} \tag{23}$$

For the associated switching state sequence of the CMC, however, this leads to

$$\begin{aligned}\ldots|_{t_\mu=0}\ & (aac)-(acc)-(ccc)\\ & -(bbb)-(abb)-(aab)|_{t_\mu=T_P/2}\\ & (aab)-(abb)-(bbb)\\ & -(ccc)-(acc)-(aac)|_{t_\mu=T_P}\ \ \ldots,\end{aligned} \tag{24}$$

i.e. in each pulse half-period there is a commutation of all output phases from input c to input b (Fig. 27b). To avoid such commutations with the CMC a clamping of the input phase, which is not switched in the considered angular range, must be implemented. Thus in the present case, the clamping to Phase a or the free-wheeling state (aaa) (free-wheeling state (ppp) of the IMC) must also be retained for $\varphi_{\vec{u}_2^*} \in [\pi/6, \pi/3]$, so the switching state sequence in (22) or Fig. 27a must be used within the entire angular interval $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$. It is an advantage that all commutations always take place between input voltages with large voltage difference, so that high commutation reliability is assured.

It is also advantageous for the IMC to retain the switching state sequence (16) over the entire angular range $\varphi_{\vec{u}_2^*} \in [0, \pi/3]$. Hence, the DC-link bus that is used for clamping the output stage remains permanently connected to an input terminal (via the input stage) during one pulse period. It can be shown that the free-wheeling state used for the output stage is repeated with six times the mains frequency and not with six times the output frequency. In this way, at low output frequencies, a more even loading of the power semiconductors (inherently given by the CMC topology) of the output stage can be attained. This allows for a higher standstill torque being produced for a variable speed drive.

V. Extended Matrix Converter topologies

Within the last few years especially, numerous extensions of the basic forms of the CMC and IMC have been given in literature that aim to

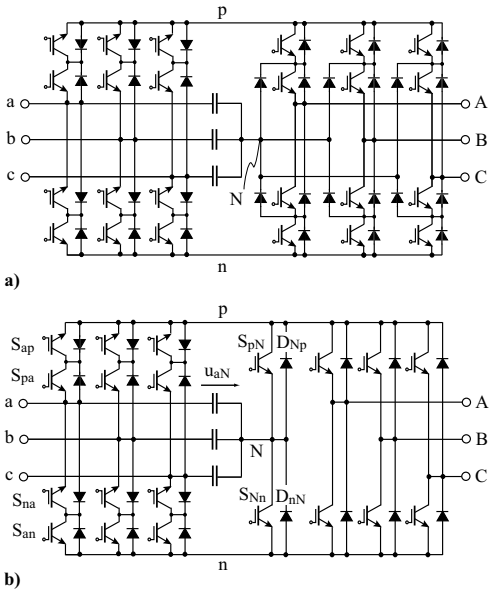

Figure 28: a) IMC with three-level PWM inverter output stage; b) IMC with a further bridge branch that also allows the mains phase voltages to switch directly or inverted into the DC-link and thus attain the functionality of a).

- reduce the load current switching frequency harmonics, or
- operate the IGBTs with low switching losses (e.g. ZCS), or
- realize the converters with conventional power semiconductor modules, or
- increase the voltage control range, or
- reduce or avoid common-mode output voltages.

In the following, only the circuit topologies of the individual systems are briefly discussed; a detailed description of the functionality can be found in the associated literature.

A. Indirect Three-level Matrix Converter

For the IMC, the output stage is a two-level PWM inverter (Fig. 14a). To reduce the switching frequency harmonics of the output voltage or of the load current, it is thus obvious to employ an inverter stage with a three-level characteristic (Fig. 28a). Such a topology with the star point of the mains-side filter capacitors as the voltage center point was proposed in [19] and later designated as SMC3. The space vector modulation for the system is described in [23].

The circuit topology, given in Fig. 28a, enables the line-to-line voltages together with the input phase voltages to form the output voltage. The same functionality can be achieved with Fig. 28b [24], which has the advantage of having a reduced number of switches.

A considerable simplification of the indirect three-level Matrix Converter circuits is possible by restricting the systems to unidirectional power flow (Fig. 29, [21]). The input stage of this new topology exhibits the structure of a Vienna Rectifier [32], [33], i.e. requires only 3 IGBTs, and is thus with regard to complexity of the input stage comparable to a USMC. Hence the abbreviation USMC3 has been agreed for further reference. It should be emphasized that on the input side, the transistors are only switched with twice the mains frequency, i.e. show very low switching losses.

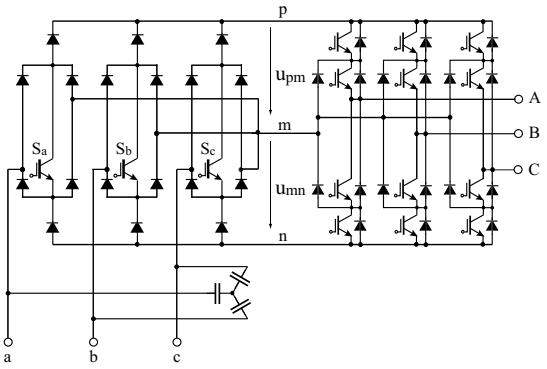

Figure 29: Unidirectional IMC with three-level input stage according to the concept of the Vienna Rectifier and three-level PWM inverter output stage. By switching-on of a transistor in the input stage, the mains phase voltage having the smallest absolute value is connected to the center point of the three-level output stage.

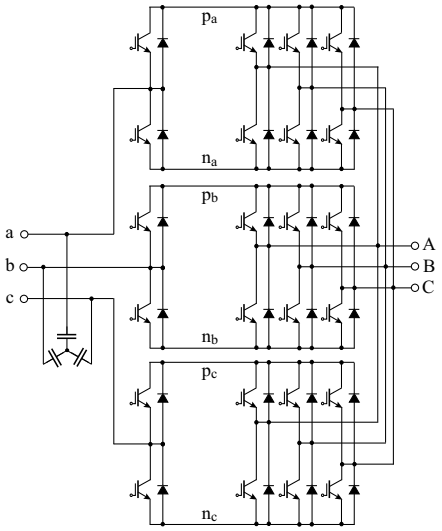

Figure 30: Indirect Matrix Converter with separate sections of a double converter for the individual mains phases.

B. IMC with DC-Links Separated According to Input Phases

In Section III-A, a U-BBC without DC-link storage was examined as an example of a very simple circuit topology of a bidirectional IMC. Because of the lack of controllability of the rectifier stage due to the diodes, zero-current intervals and thus relatively high low-frequency harmonics of the mains current occur.

A sinusoidal shape of the mains current can be achieved with the circuit modification suggested in [34], i.e. by arrangement of an explicit DC-link or a separate input stage for each phase (Fig. 30). However, the system has 24 IGBTs and results in a relatively high component expenditure compared to the IMC with the same functionality. According to [34], a reduction of the switching stress of the IGBTs can be easily achieved. The circuit can be realized with commercially available semiconductor modules.

C. Matrix Converter with Full Bridge Circuit

CMC can be constructed in a half bridge topology (Fig. 3a) or, as with cycloconverter, with a full bridge topology. The latter (Fig. 31) requires open motor windings and 36 instead of 18 IGBTs. With the goal of minimal realization effort, the half bridge topology is often emphasized in technical papers. An

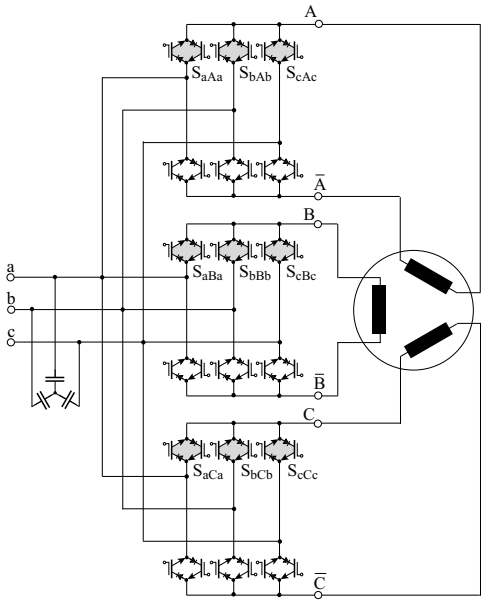

Figure 31: Full bridge CMC topology realized by four-quadrant switches with RB-IGBTs connected in antiparallel. Circuit formed by two CMCs with a half bridge topology, which feed the start A, B, C and end ($\bar{A}$, $\bar{B}$, $\bar{C}$) open windings of an AC machine.

exception is e.g. [9] where in the full bridge topology of the CMC shown in Fig. 31, a control procedure is suggested that achieves a low stress on the insulation of the motor windings, a maximum output voltage of

$$\hat{U}_{2,\max} = \frac{3}{2}\hat{U}_1 \tag{25}$$

(instead of $\hat{U}_{2,\max} = \sqrt{3}/2\hat{U}_1$), and ohmic fundamental mains behavior. Thus, the topology is of interest especially for high power variable speed drives. However, 6 instead of 3 motor feeds and terminals are necessary for the system.

A reduction of the realization effort of the full bridge topology to 24 power transistors is possible with the variant shown in Fig. 32, i.e. using two PWM inverter output stages I and II in combination with an IMC input stage (Fig. 12 in [9]). When the associated motor terminals are driven in opposition, an output voltage range of

$$\hat{U}_{2,\max} = 2\frac{\sqrt{3}}{2}\hat{U}_1 = \sqrt{3}\hat{U}_1 \tag{26}$$

is thus available.

D. Hybrid Matrix Converter

The limited voltage control range of the simple Matrix Converters (IMC or CMC) – where an output voltage of approximately only 86% of the mains voltage can be formed without overmodulation – is a significant disadvantage compared to converters with DC-link storage (U-BBC or I-BBC). In the literature, therefore, combinations of CMC and U-BBC, so-called hybrid Matrix Converters have been described that overcome this limitation. However, these converter topologies again have energy storage elements (e.g. electrolytic capacitor) and require a great realization effort.

If the four-quadrant switches in a CMC are replaced by cascaded H-bridge circuits with output capacitors (similar to PWM inverters with cascaded bridge circuits), then the hybrid CMC topology (HCMC, [4]) results as shown in Fig. 33. This enables step-up or step-down converter operation. With an adequate

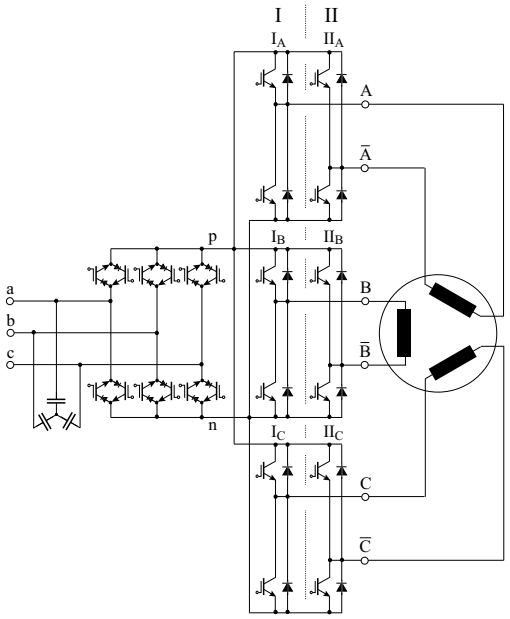

Figure 32: IMC-Topology extended on the output side for the supply of an AC machine with open windings.

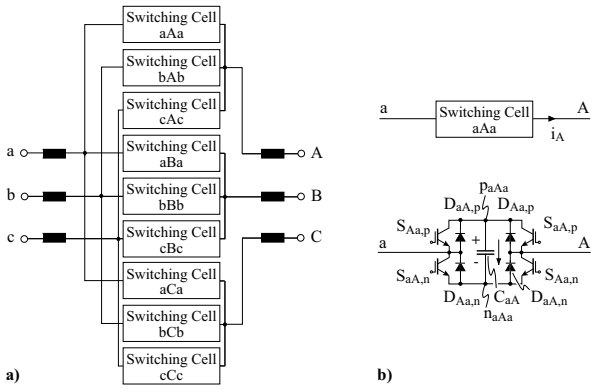

Figure 33: Hybrid CMC (HCMC); also possible is a cascading of several H-bridges in each connection of an input and output.

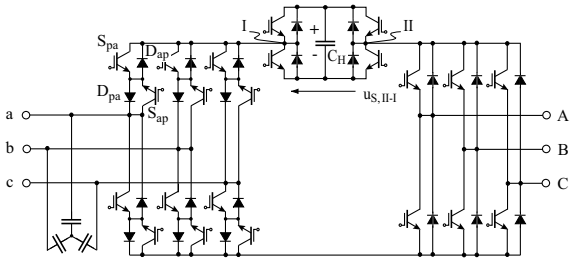

Figure 34: Hybrid IMC with a series voltage source $u_{S,II\text{-}I}$ in the DC-link; this voltage coupling topology is also known from AC/AC converters with an input diode bridge, which simulates a DC-side filter inductor.

modulation scheme, no external supply of the switching cells is required. In contrast to all previously discussed topologies, for the HCMC both the input and the output currents are impressed and can be managed according to [4] via control of always 5 half-bridges.

Transferring the concept of the HCMC to the IMC (HIMC) requires in the simplest case only one H-bridge in the DC-link [6] (Fig. 34). In the voltage step-up mode, i.e. providing a voltage $u_{S,II\text{-}I}$ with non-zero mean value, a voltage supply of the capacitor C_H is necessary.

In summary, hybrid concepts enable an enlargement of the voltage control range and also offer advantages in the management of mains asymmetries [35]. To obtain these advantages, however, there is a higher complexity of the power stages and of their control.

VI. Comparison and Evaluation of DC-link and Matrix Converters

Up until now the fundamentals, topologies and control techniques of the IMC and CMC, as well as the modifications and extensions of the circuit topologies have been discussed. We will now conclude by giving a rough qualitative comparison of the converter concepts. All systems have in common

- sinusoidal mains currents (with the exception of the AC/AC converter without energy storage in the DC-link, Section III-A),
- supply of the load with sinusoidal currents, and
- the possibility of bidirectional power transfer (with the exception of the USMC), i.e. in particular feedback of braking energy into the mains.

The converter concepts thus differ not with regard to the basic functionality but in respect of the possible operating range, in particularly the output voltage range, the behavior in characteristic points of the speed-torque plane, of the complexity, of the realization effort, and the physical volume.

To illustrate the differences, we intend in the following to briefly examine the Matrix Converters including CMC and IMC (MC) and standard solution topologies, i.e. provide a comparison of the U-BBC, the CMC, and IMC.

A. Output Voltage Range

The limited output voltage range of the MC represents a clear disadvantage and requires an electrical machine with an adapted nominal voltage. Such a matching of the converter and the machine is possible, especially for niche applications, e.g. for elevator drives. For the U-BBC, on the other hand, the DC-link voltage is freely selectable and thus is highly flexible and a wide control range exists or a broad speed range is covered. Also for the I-BBC, a step-up of the output voltage over the mains voltage can take place via the boost function of the output stage.

Furthermore, mains voltage unbalances directly effect the MC and pulsating load currents are passed through the input filter, with some attenuation, to the mains.

B. DC-link Capacitor and EMC Filter

For the MC, the DC-link capacitor of the U-BBC (an electrolytic capacitor is often used) is omitted but instead filter capacitors (foil capacitor) are required at the mains input. However, a foil capacitor may also be employed in the DC-link of the U-BBC, whereby a similar capacitance value is required to limit the voltage ripple and the voltage change for a step change of the energy flow direction, i.e. on sudden change from motor to generator operation. There is thus no significant difference between the two converter concepts.

For the U-BBC, limiting mains overvoltages or overvoltages caused by the load, e.g. on emergency stop of the drive, may be simply achieved with varistors in the DC-link or pulse-controlled emergency braking resistors integrated in the heat sink. For the CMC, an explicit clamp circuit must be provided.

Both for the U-BBC and for the MC, a multi-stage EMC filter must be provided on the mains side to comply with radio

interference regulations. The input inductors of the U-BBC may be regarded as a part of this EMC filter. They cause an increase in apparatus size and hence a reduction in the power density of the converters. However, the input current of the U-BBC is sinusoidal through the use of closed-loop current control. The mains side filter capacitors have values that are significantly lower than those used in the MC. Therefore, the resonance circuit formed between filter capacitors and the input inductors (plus mains impedance) is simpler to damp for the U-BBC.

C. Space Vector Modulation and Commutation

Space vector modulation of the MC is considerable more complex than for the U-BBC. Despite numerous publications by the industry, the often missing knowledge of the modulation details may be one of the reasons that hinder industrial use of the MC today. The space vector modulation of the MC is developed in a stepwise manner, in this paper, from the widely known modulation concepts of the U-BBC and I-BBC in order to provide a better understanding of the MC.

If the modulation of the CMC is chosen such that the commutation always takes place between mains phases with highest voltage difference and two-step commutation is employed, a similar commutation reliability is achieved as for the U-BBC. There are slightly higher switching losses, which can be justified due to the higher system reliability, with this modulation method compared to modulation schemes that are optimized for low switching losses (i.e. schemes that favor commutations between phases of low voltage difference).

For the IMC, the commutation of the input stage takes place during free-wheeling of the output stage. Furthermore, only high mains line-to-line voltages with clearly defined polarity are switched into the DC-link. The commutation strategy of the IMC is thus easier to implement and at least equal to the CMC in respect of reliability.

D. Control

For the MC, the machine currents are impressed by the drive control whereas the mains currents are formed by open-loop control, i.e. not set by a control loop. The system, which is composed of the machine and mains filter, exhibits a relatively high order and has to be controlled by the motor controller. Therefore, especially at low switching frequencies, i.e. close to the mains and output frequencies, the system is difficult to control.

For the U-BBC, the motor currents, DC-link voltage and mains currents are controlled by separate control loops, i.e. the system is broken up into subsystems of lower order. Considering the U-BBC as a virtual MC, regarding mains current and filter capacitor voltage, the input filter can be operated under closed-loop control. Then, generally, the U-BBC offers higher degrees of freedom with its control and therefore the U-BBC offers a more robust control solution.

E. Efficiency and System Volume

The input stage of the IMC, because of the zero-current commutation, exhibits no switching losses. The switching losses of the output stage corresponds, to a first approximation, to those of the output stage of an U-BBC, which works with higher voltage but lower currents. However, the input stage of the U-BBC generates switching losses, so that in total there are higher switching losses and above switching frequencies of approximately $10\,\mathrm{kHz}$ a lower efficiency results. With the use of SiC diodes, this limit is shifted to higher frequencies, whereby for the IMC it is an advantage that SiC diodes are only necessary in the output stage.

The conduction losses of the CMC depend only on the load current amplitude and not on the phase angle of the output current or the voltage modulation index. For the IMC and the U-BBC, the output stage, at low output voltage, will work mainly in freewheeling mode, so that for each phase only one conducting IGBT or diode causes the loss. Furthermore, there exists a low input power and hence a low current through the input stage. Therefore low conduction losses occur both in the input and in the output stages. In respect of conduction losses, there is an advantage for the CMC only at higher speeds.

Apart from power semiconductors or power modules, signal processing and sensors, and the EMC filter, the heat sink occupies a significant fraction of the physical volume of the converter. As shown by a detailed analysis, a $10-20\%$ smaller volume of the heat sink and hence a correspondingly higher power density is to be expected on account of the lower losses of the MC as against the U-BBC at medium switching frequencies.

F. Semiconductor Area Based Converter Topology Assessment

The crucial question often raised is which of these converter topologies CMC, IMC, U-BBC, or I-BBC would be the most advantageous for a state-of-the-art motor drive. To select the best converter topology the application's requirements (control dynamics, input and output power quality, overall volume, etc.) and the drive's mission profile must be considered. Therefore a new concept is required to assess and comparing different converter topologies and is introduced in this section.

The core components of three-phase AC/AC converter systems are the power semiconductors, including their packaging. They do not only determine the key performance figures such as efficiency, power density, and allowable switching frequency range, but also contribute to the overall converter costs by approximately 25%. Therefore, any converter comparison should comprise of data for the selected power semiconductors.

The approach is to provide a common basis for comparison by considering the required semiconductor chip area of the individual converter topologies for a given motor drive application profile. For that purpose, in a first step the motor drive requirements defined by its mission profile are mapped to the torque-speed ($M-n$) plane, as depicted in Fig. 35. Then, the motor type (ASM, PMSM) and possibly a gear system need to be selected and suitably matched to the converter output voltage range and the mission profile. Based on that, the required electrical specifications, the semiconductor technology, and the switching frequency are determined. With this information the semiconductor losses can be calculated. Finally, the required semiconductor chip area is determined, according to (27), where the resulting semiconductor junction temperature T_J is equal or less than a selected maximum value $T_{J,max}$ for all power IGBT and diode chips. This automatically leads to minimum semiconductor usage and an optimal partitioning between the IGBT and diode chip area. For this calculation a heat sink temperature T_S, a thermal resistance between junction and sink $R_{th,JS}$, and the overall semiconductor chip losses $P_{L,Chip}$ must be given.

$$T_{J,max} \geq T_J = T_S + R_{th,JS} \cdot P_{L,Chip} \tag{27}$$

The prerequisite for any semiconductor chip area based comparison is a sufficiently accurate semiconductor model. The individual semiconductor parameters can be derived based on statistical analysis of power module data sheets and should

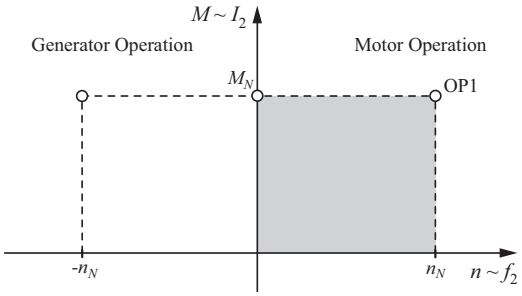

Figure 35: Motor drive requirements represented in the torque-speed plane for an elevator drive example with 2-quadrant operation.

ideally be verified with chip manufacturer data and switching loss measurements of a few selected components.

As an example, the chip area based comparison approach is presented for operating point 1 (OP1 in Fig. 35, nominal motor operation) for the U-BBC, the I-BBC, and the IMC, using latest generation Trench and Field Stop IGBT 4 and diode technology. All of the these converter topologies have in common that they feature a physically dedicated input and output stage but are different regarding their DC-link energy storage elements. The U-BBC, I-BBC, and IMC are designed for a nominal apparent output power $S_{2,N} = 30\,\mathrm{kVA}$, a switching frequency $f_S = 8\,\mathrm{kHz}$, and a heat sink temperature $T_S = 80^{\circ}\mathrm{C}$ for a RMS phase-to-phase input voltage of $400\,\mathrm{V}$. In this comparison the individual power converters supply a PMSM load machine, optimally matched to the converter output voltage range, such that they can provide a nominal output power of $P_{2,N} = 30\,\mathrm{kW}$ for OP1 with the junction temperature of all IGBT and diode chips limited to $T_J = 150\,^{\circ}\mathrm{C}$.

The most economical topology regarding semiconductor usage is the U-BBC with a minimal chip area of roughly $6.5\,\mathrm{cm}^2$, where a DC-link voltage of $750\,\mathrm{V}$ has been assumed. The IMC and the I-BBC in contrast typically need a 60% larger chip area in the range of $10.5\,\mathrm{cm}^2$. In terms of efficiency the U-BBC and IMC are similar ($\eta_{OP1} \approx 96\%$), whereas the I-BBC achieves an efficiency of only $\eta_{OP1} \approx 94\%$ due to the comparably high conduction losses.

The new chip area based procedure does not only provide a distinct criterion for assessment and comparison but ultimately enables the determining of the semiconductor costs ($€/\mathrm{cm}^2$) for a given motor drive application for different converter topologies. Nevertheless, as defined by the drive's requirements, other benefits such as converter compactness may outweigh the higher semiconductor costs resulting from the use of larger chip areas as for MCs.

VII. Future research

As shown in Section VI, the CMC and IMC exhibit in contrast to U-BBC a potential for reduction of the losses and the physical volume. An exact statement is only possible with a detailed knowledge of the operating range to be covered and of the motor characteristic of the drive. In each case it makes sense for all converters, MC, U-BBC and I-BBC, to carry out an optimization, taking into account the operating conditions, of the total silicon area distribution used for the semiconductors of the converter topology.

However, MCs are overall in a more difficult competitive position compared to the widespread introduction of a more standard solution, in the form of the U-BBC, and can only offer advantages for special application profiles or ranges, e.g. elevators and escalators. Furthermore, mains feedback or sinusoidal input current is only necessary for a small fraction of industrial drives.

Fundamentally, there still exists no clear picture in the technical literature, i.e. no comprehensive quantitative comparison of the advantages and disadvantages of MC, U-BBC and I-BBC for specific applications. Future scientific work should therefore pay more attention to the comprehensive comparison of the converter concept, whereby the advantages of new semiconductor technologies, e.g. SiC, should also taken be into account and special attention paid to the obtainable energy conversion efficiency.

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