Novel Concept for Mains Voltage Proportional Input Current Shaping of a VIENNA Rectifier Eliminating Controller Multipliers

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***Abstract*—This paper proposes a novel mains voltage proportional input current control concept eliminating the multiplication of the output voltage controller output and the mains ac phase voltages for the derivation of mains phase current reference values of a three-phase/level/switch pulsewidth-modulated (VIENNA) rectifier system. Furthermore, the concept features low input current ripple amplitude as, e.g., achieved for space-vector modulation, a low amplitude of the third harmonic of the current flowing into the output voltage center point, and a wide range of modulation. The practical realization of the analog control concept as well as experimental results for application with a 5-kW prototype of the pulsewidth-modulated rectifier are presented. Furthermore, a control scheme which relies only on the absolute values of the input phase currents and a modified control scheme which does not require information about the mains phase voltages are presented.**

***Index Terms*—AC–DC power conversion, analog multipliers, cascade control, harmonic distortion, power supplies, pulsewidth-modulated (PWM) power converters, three-level rectifier, three-phase PWM rectifier, VIENNA Rectifier.**

I. Introduction

THE control of three-phase three-level pulsewidth-modulated (PWM) rectifier systems is realized in a two-loop structure [1] where the outer loop controls the total value of the output voltage and provides a balancing of the partial output voltages, and the inner current control loop ensures a mains voltage proportional guidance of the input phase currents and/or unity power factor operation.

The current control and/or the determination of the rectifier switching state sequence can basically be performed with reference to space vector calculus in rotating dq coordinates defined by the mains voltage [2], [3] or in phase quantities [1]. Space-vector control shows a relatively high complexity and realization effort, but does not provide a lower input current ripple or a higher control bandwidth ([4, p. 413]) and is not applicable for two-phase operation which is frequently required for high reliability three-phase power supply systems [5]. Accordingly, phase-oriented concepts have been considered for industrial realizations where a hysteresis phase current control [1] seems attractive but exhibits the disadvantage of a not constant switching frequency (resulting in an involved electromagnetic compatibility (EMC) filter design) and a missing natural stability of the output voltage center point [6]. Therefore, e.g., in [7] the application of carrier based average phase current mode control has been analyzed where a standard low-cost integrated control circuit known from single-phase power-factor correction has been employed in each phase. As compared to a control employing a common triangular carrier signal for all phases this, however, results in a significantly higher input current ripple due to the missing synchronization and the sawtooth shape of the phase carrier signals [8]. Accordingly, the control circuit has to be realized by discrete components where the realization effort should be minimized and all possibilities for cost savings should be utilized.

Conventional single-phase and three-phase power-factor-correction systems employ analog multipliers for the generation of the input current reference values for the current-mode controllers. These analog multipliers do contribute to a large portion of the cost of the control circuit. However, as shown in [9]–[12] ohmic mains behavior can be achieved for single-phase boost-type PWM rectifier systems in continuous conduction mode (CCM) without measurement of the input voltage and without a multiplication in the output voltage feedback loop.

In this paper this basic control concept shall now be applied and investigated in modified form [13] in connection with a three-phase/switch/level PWM (VIENNA) rectifier (cf. Fig. 1 [1]), which already is well established in the industry for three-phase power-factor correction in telecommunication power supply modules and industrial process technology power supplies such as the boost-type power-factor corrector for single-phase applications. Advantages of the system are a low blocking voltage stress on the power semiconductors (i.e., fast switching 600-V semiconductor devices can be used for 800-V output voltage) resulting in a high efficiency in addition to a low ripple with switching frequency of the sinusoidal mains current.

In Section II, after a brief discussion of the basics of multiplier-free current control, the three-phase realization of the control circuit in analog technique is described. In Section III, a modification of the proposed control concept which does not require a sensing of the mains phase voltages and, therefore, is ideally suited as a basis for the development of an integrated control circuit for three-phase power-factor correction is proposed; furthermore, a control scheme relying on the absolute values $|i_{N,i}|$ of the input phase currents is discussed. Section IV shows the experimental investigation of the control concepts in connection with a 5-kW prototype of the PWM rectifier. There,

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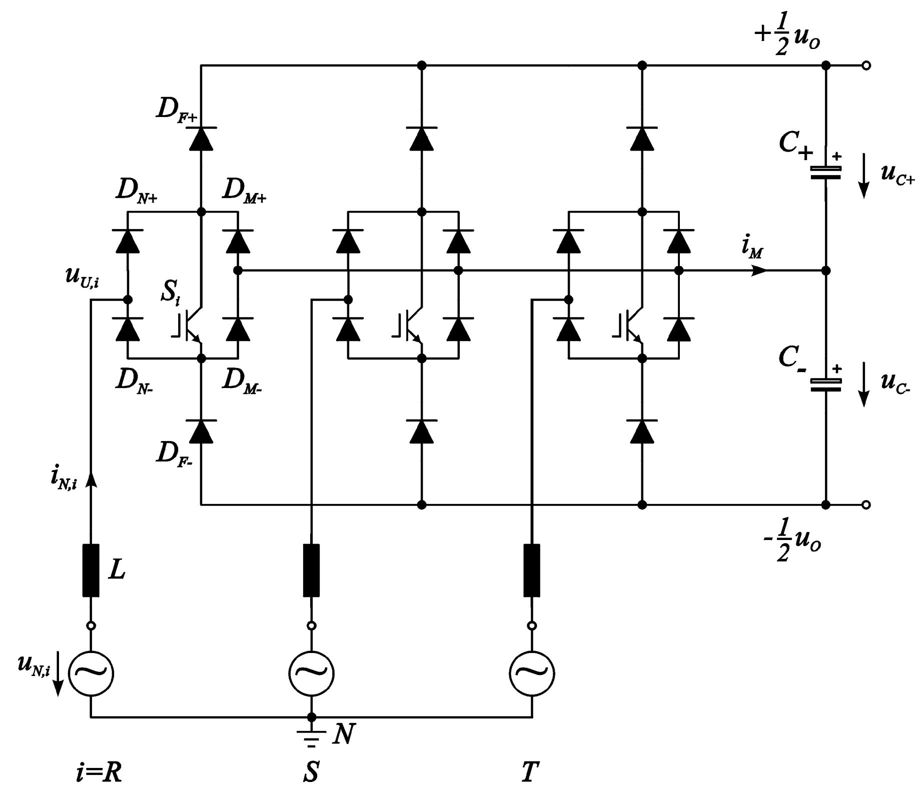

Fig. 1. Structure of the power circuit of the PWM (VIENNA) rectifier system.

special attention is paid to the quality of the guidance of the input currents in the vicinity of the zero crossings and at light load [resulting in discontinuous conduction mode (DCM)].

II. Multiplier-Free Current Control

In the following, the basic concept of multiplier-free average current-mode control of single-phase unity-power-factor rectifiers is briefly summarized in order to provide a theoretical basis for the description of the operating behavior of the new multiplier-free current control concept for three-phase PWM rectifiers proposed in Section II-B.

A. Single-Phase AC–DC Converter Control

According to the control concepts proposed in [11] and [12] the relative off-time $d'T_P$ of the power transistor S of the boost stage of a single-phase power-factor corrector (cf. Fig. 2(a), input diode bridge omitted) without multiplier for input current reference generation is defined by comparing the actual input current with a carrier signal with switching frequency $f_P = 1/T_P$. For given amplitude $\hat{I}_D$ of the sawtooth-shaped carrier signal and neglection of the ripple component of the input current, i.e.,

$$\overline{i}_N = \frac{1}{T_P}\int_0^{T_P} i_N dt \approx i_N \tag{1}$$

one receives

$$\frac{i_N}{\hat{I}_D} = d'. \tag{2}$$

Under consideration of the stationary equilibrium of the input voltage u_N and the local average value $\overline{u}'$ of the voltage u' across the power transistor

$$u_N = \overline{u}' = d'u_O \tag{3}$$

as valid for CCM, in case the output voltage ripple is neglected, i.e., $u_O \approx \overline{u}_O$ is assumed, this results in a proportionality of i_N and u_N,

$$u_N = i_N \frac{u_O}{\hat{I}_D} \tag{4}$$

and can be described by an equivalent input resistance of

$$R_N = \frac{u_O}{\hat{I}_D}. \tag{5}$$

Consequently, the input current and/or the power consumption of the system can easily be adjusted by the output voltage control by changing the amplitude of the carrier signal $\hat{I}_D$. A lower amplitude of the carrier signal leads to $d' = u_N/u_O$ at smaller values of the input current, cf. $i_{N,2}$ in Fig. 2(b). This system function can be realized without a multiplier in the control circuit (cf., e.g., [12, Fig. 10]).

The dynamic behavior of the system corresponds in the first approximation (for neglection of the low-frequency output ripple voltage due to the pulsation of the output power level with twice the mains frequency) to a first-order delay [12]

$$i_N(s) = \frac{u_N(s)}{R_N}\frac{1}{1 + s\frac{L}{R_N}}. \tag{6}$$

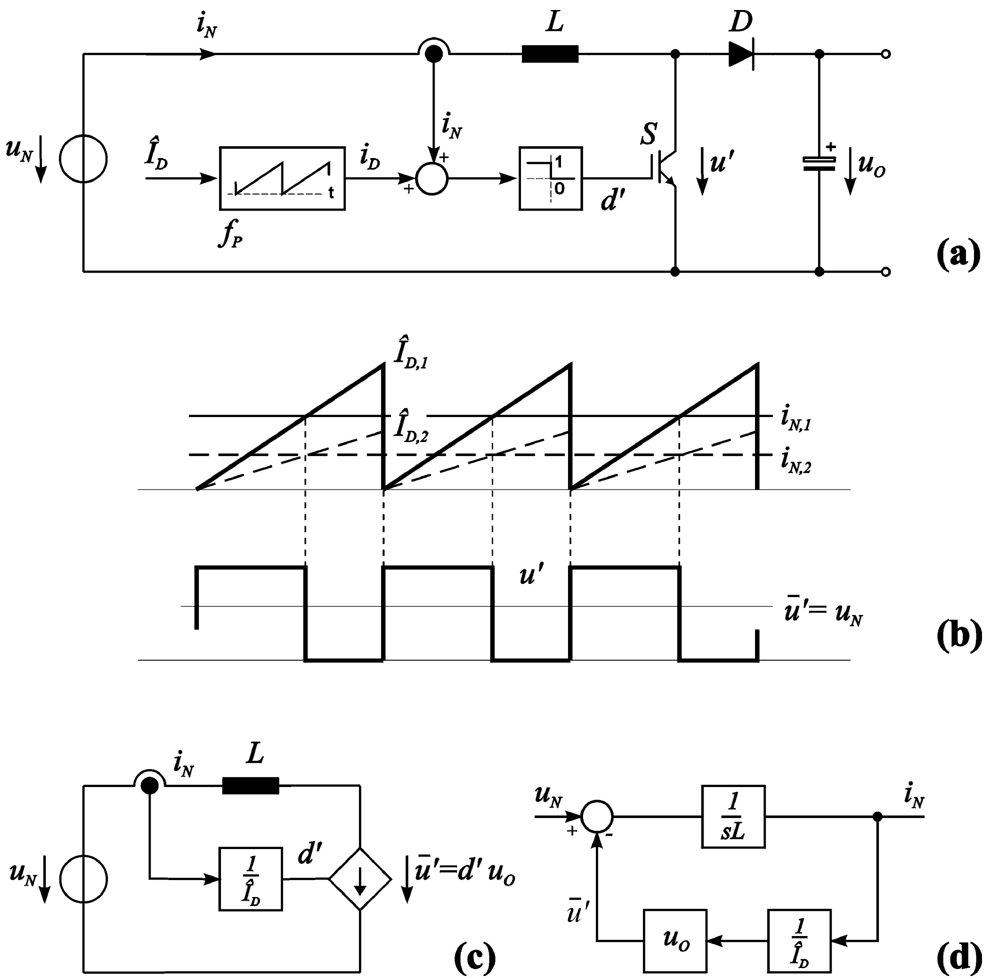

Fig. 2. Basics of an input voltage proportional guidance of the input current i_N of a PWM boost converter system by means of a proportional relationship of the turn-off interval d' of the power transistor and i_N. (a) Structure of the power circuit and block diagram of the control, (b) detailed time behavior of the input current i_N, of the carrier signal i_D and of the resulting power transistor voltage u' (the drive signal d' is inverse to u' and not shown), (c) equivalent circuit of the input stage, and (d) control-oriented block diagram.

This can be clearly explained by the negative feedback of the integration element $1/sL$ formed by the input inductor via the modulation stage [an increase of the input current i_N results in an increase of d' and/or of the voltage $\overline{u}'$ resulting in a decrease of the voltage $u_N - \overline{u}'$ which is applied to the inductor L, cf. Fig. 2(b) and (c)]. Fig. 2(d) can be interpreted as a control loop having u_N as reference value. As shown in [12] the unity gain bandwidth of the control loop results for common dimensioning of the system typically in $f_P/30$, hence, the considerations for processes with mains frequency can be in a quasi-stationary manner; therefore, the input current of the system is guided directly proportional to the input voltage without the requirement of an analog or digital multiplier for generating reference current waveforms.

B. Three-Phase AC–DC Converter Control

The block diagram of the two-loop control of the VIENNA Rectifier incorporating the proposed multiplier-free input phase current control concept [13] in the inner loop is shown in Fig. 3. The outer loop controls the total value of the output voltage u_O by means of a proportional-plus-integral (PI)-type controller $F(s)$ to a constant value by proper adjustment of the amplitude of the carrier signal $\hat{I}_D$ and balances the values of the two partial output voltages by means of the second PI-type controller $F_d(s)$ which outputs a zero-sequence current component i_0.

The basic operating behavior of the inner current control loop is identical to single-phase power-factor correction when adding a connection between the output voltage center point and the mains star point which would result in a decoupling of the phases.

Then, for positive mains phase voltages the (single-phase) boost converter topology shown in Fig. 1(a) is formed by the input inductor L (with series diode D_{N+}), the power transistor S_i (with series diode D_{M-}), the freewheeling diode D_{F+}, and the output capacitor C_+ (cf. Fig. 2); for negative mains phase voltages the boost structure is formed by the input inductor L (with D_{N-}), S_i (with D_{M+}), D_{F-}, and C_-. However, due to deriving the off-time of the power transistors directly from the ac input current $i_{N,i}$ (instead of taking the absolute values) one now has to shift the triangular carrier signal by $+\hat{I}_D$ for positive phase current, and $-\hat{I}_D$ for negative phase current. Due to the above-described changeover of the topology for negative input voltages , furthermore, an inversion of the switching decisions s'_i of the modulator stages in dependency of the signs of the input

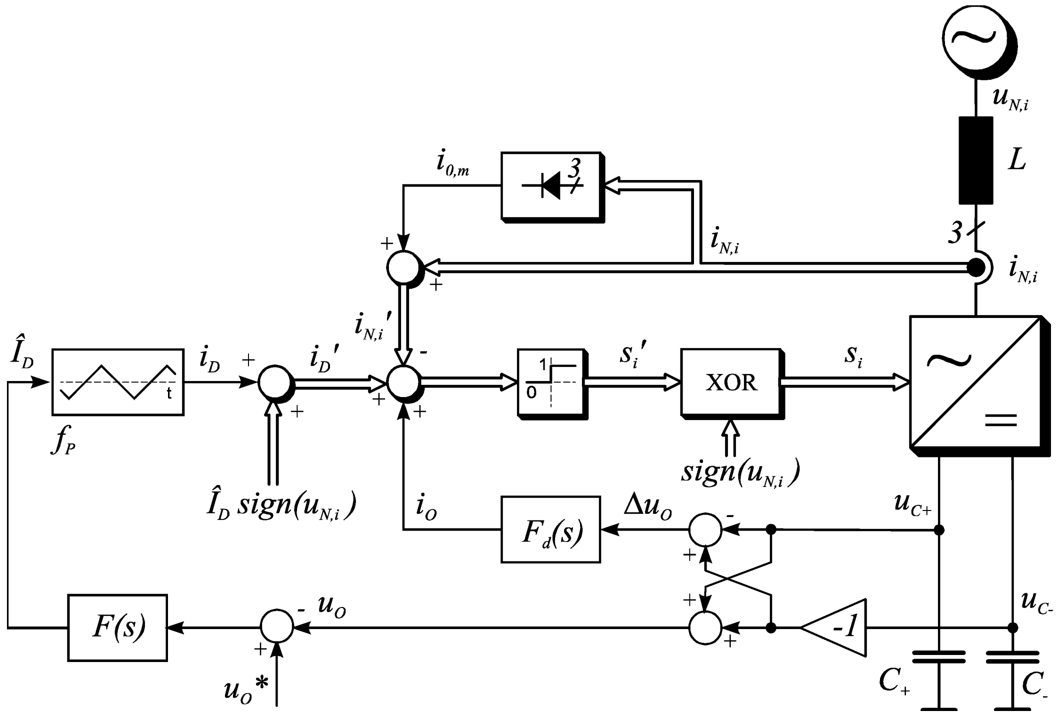

Fig. 3. Structure of the proposed multiplier-free current control concept [13]. Signal paths being equal for different phases are shown by double lines.

phase currents $i_{N,i}$ and/or of the input phase voltages $u_{N,i}$ ($u_{N,i}$ proportional to $i_{N,i}$) has to be performed by a controlled inverter realized by an exclusive OR (XOR) Gate.

Because the actual system does not show a connection between the mains neutral point and the capacitive rectifier output voltage center point a coupling of the phases must be taken into consideration. According to

$$i_{N,R} + i_{N,S} + i_{N,T} = 0 \tag{7}$$

and/or

$$\frac{\mathrm{d}i_{N,R}}{\mathrm{d}t} + \frac{\mathrm{d}i_{N,S}}{\mathrm{d}t} + \frac{\mathrm{d}i_{N,T}}{\mathrm{d}t} = 0 \tag{8}$$

the change of a switching state of a rectifier bridge leg and/or the change of a phase current takes influence also on the currents of the two other phases. Therefore, the switching decisions of the phases should advantageously be coordinated by using a single carrier signal i_D with triangular shape for all three phases as, e.g., for ramp comparison current control (regarding the drawbacks of a sawtooth-shaped carrier signal compared to a triangular shaped carrier please refer to [8]). The system in this case advantageously has the property of a natural stability of the partitioning of the total output voltage u_O to u_{C+} and u_{C-}. However, in order to ensure high system reliability, additionally an active symmetry control of the partial output voltages is provided by offsetting all measured phase currents by i_0. As shown in [1], i_0 directly results in a global average value I_M of the center point current i_M and, therefore, can be used for guaranteeing $u_{C+} = u_{C-} = 1/2u_O$.

Using directly the actual sinusoidal and/or mains voltage proportional input phase current for the PWM modulator stage would allow the formation of a fundamental of the maximum rectifier input phase voltage of only $\hat{U}_{N,max} = u_O/2$. Therefore, besides low-pass filtering for suppression of the switching frequency ripple the measured actual phase currents $i_{N,i}$ are extended by a zero-sequence component $i_{0,m}$ with three times the mains frequency [13] (cf. Fig. 4), ($i'_{N,i} = i_{N,i} + i_{0,m}; i = R, S, T$). This increases the modulation limit to $\hat{U}_{N,\max} = (2/\sqrt{3})(u_O/2)$, and results in a significant reduction of the input current ripple amplitude and of the amplitude of the third harmonic of the center-point current i_M (as compared to purely sinusoidal modulation). Despite the addition of $i_{0,m}$ the phase current waveforms are still guided sinusoidally, i.e., proportional to the phase voltages as $i_{0,m}$ only leads to the formation of a zero-sequence component of the rectifier input voltage which according to (7) does not result in a current flow.

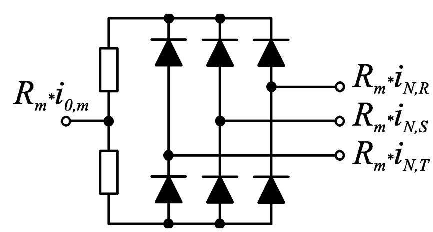

Fig. 4. Principle of generation of the zero-sequence component $i_{0,m}$ with a pronounced third harmonic from the measured input phase currents. In the practical realization the diodes are replaced by ideal diodes realized by means of operational amplifiers.

III. Three-Phase Multiplier-Free Current Control Without Input Voltage Sensing

The disadvantage of the realization shown in Fig. 3 is the need of the determination of the sign of the input phase voltages for

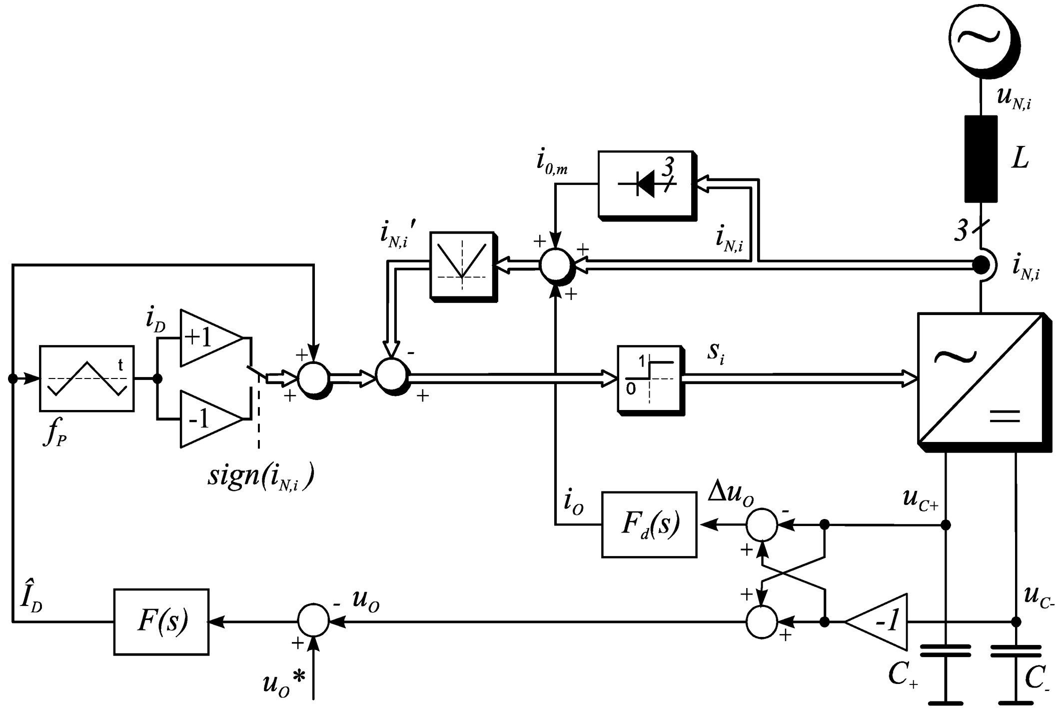

Fig. 5. Structure of a multiplier-free current control concept which relies on the absolute values $|i_{N,i}|$ of the input phase currents and which does not require a detection of the sign of the input phase voltages. Signal paths being equal for different phases are shown by double lines.

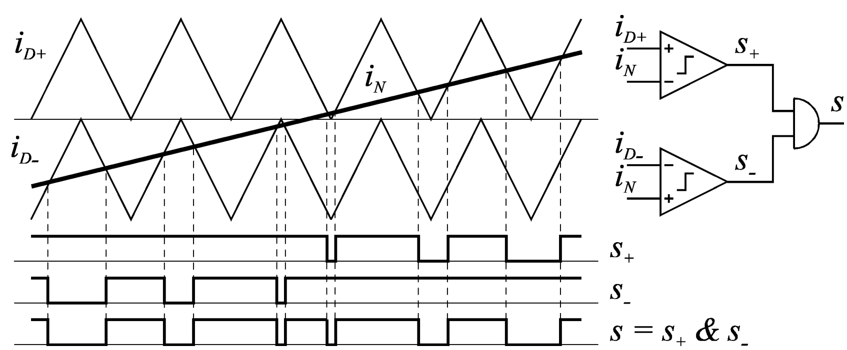

Fig. 6. Generation of phase-switching functions by intersection of the corresponding phase current i_N with a positive carrier signal i_{D+} and a negative carrier signal i_{D-}. The carrier signals i_{D+} and i_{D-} are common for all three phases.

shifting the triangular-shaped carrier signal and for the inversion of the switching signals s_i' with line frequency. Therefore, a realization of a control concept which relies only on the absolute values $|i_{N,i}|$ of the input phase currents would be of special interest. A block diagram of a possible realization is given in Fig. 5.

However, in this case, unfortunately, the triangular-shaped carrier signal $\hat{I}_D$ needs to be shifted by 180° in switching frequency (inverted) in case of negative input phase voltages and/or negative input phase currents $(sign(i_{N,i}))$ for a minimization of the input current ripple and/or of the size of the input inductors as has been proven by theoretical considerations referring to the space vectors employed for the current control. This again gives a reason for detecting the signs of the input phase voltages or the signs of the input phase currents where the latter could cause problems with light loads and/or in idle mode. However, advantageously, the total realization effort is comparably low.

An alternative is to generate not only a single triangular carrier signal i_D which is adjustable in amplitude but to generate a positive and a negative carrier with adjustable amplitude $\hat{I}_D$ where both signals are synchronized and in phase. These two signals i_{D+} and i_{D-} are compared with the measured (bipolar) input phase currents $i'_{N,i} = i_{N,i} + i_{0,m} + i_0$ by separate comparators. The switching signals s_i then can be derived by a simple combinatorial logic out of the signals s_+ and s_-, i.e. dependent on the sign of the comparison and the type of transistor drive circuit (high or low active) by an AND gate, Fig. 6. This allows for operation of the whole control circuit without a detection of the sign of the input voltage and/or a derivation of the sign information from the input current (cf. Fig. 7). It should be pointed out that there is also no need of a detection of sectors of the mains period defined by a combination of signs of the mains phase voltages as described in [15] for an alternative multiplier free current control concept ([15, Fig. 7]) or as required for space-vector modulation which could probably cause problems in case of heavily unbalanced mains and/or in case of a failure of a mains phase (phase loss). The proposed control technique does not rely on any input voltage information, which re-

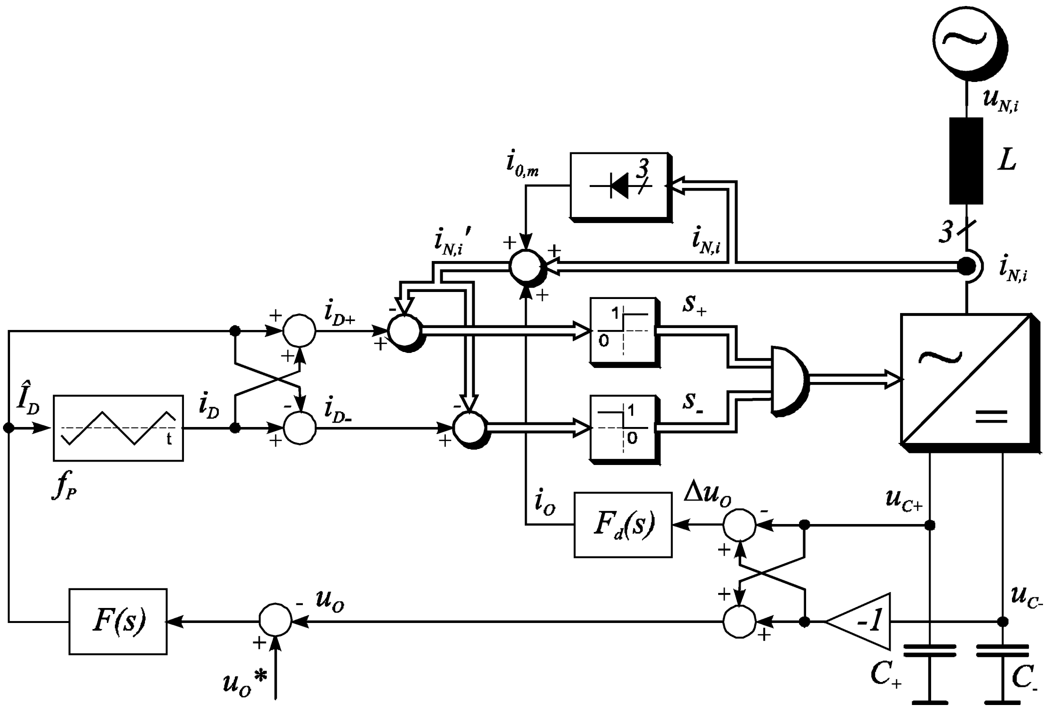

Fig. 7. Structure of a multiplier-free current control concept employing two unipolar carrier signals i_{D+} and i_{D-} where no information about the sign of the input voltages or currents is required.

sults in reliable and robust operation also for unbalanced mains conditions.

Remark: An alternative elegant current control approach requiring no multipliers for a scaling of the current references according to the output power and no input voltage sensors has been described by other authors in [16]. However, as compared to the proposed control concept [13] this scheme relies on a full-wave rectification of the phase currents and does not allow a full utilization of the modulation range due to the missing extension of the measured phase currents with a zero-sequence component $i_{0,m}$, but could also operate by sensing the switching currents instead of the inductor currents.

TABLE I
LIST OF COMPONENTS EMPLOYED IN THE VIENNA RECTIFIER PROTOTYPE

Part	Type / Value
S	Int. Rect. IRG4PC50W
D_F	Int. Rect. HFA15TB60
D_N, D_M	Semikron SKB26/08
C	2x 470µF / 450V
L	500µH, iron powder core

IV. Experimental Results

The experimental investigation was performed based on a prototype of the VIENNA Rectifier (cf. Fig. 1) with the following ratings:

output power $P_O = 5$ kW;
input voltage $U_N = 400$ $\mathrm{V_{rms}}$ (line to line);
output voltage $U_O = 675$ V;
Switching frequency $f_P = 25$ kHz.

The main power components of the system are listed in Table I. The investigation of the multiplier-free control concept was done in the first step for the control structure shown in Fig. 3 for two different load conditions (cf. Table II(a) for full load and Table II(b) for half the nominal load) in order to show the basic performance of the concept. In Fig. 8(a) and (d) one of the three mains ac phase voltages $u_{N,R}$ and the corresponding converter input inductor current $i_{N,R}$ (recorded in peak detection mode for the demonstration of the ripple of the inductor current) are depicted; furthermore, $i_{N,R}$ is recorded in high-resolution mode in order to show the current in the mains resulting after adequate EMI filtering. In Fig. 8(b) and (e) the modulating input current $i'_{N,R}$ (zero-sequence component $i_{0,m}$ added to the low-pass filtered actual current $i_{N,R}$), the triangular carrier signal i'_D shifted according to $\mathrm{sign}(u_{N,R})$ and the switching signal s'_R of the PWM stage for one fundamental period are depicted. Fig. 8(c) and (f) shows the time behavior in the vicinity of the zero-crossing of a phase current.

These results lead directly to the control concept according to Fig. 6 (no need of input phase voltage detection), which is investigated in Fig. 9 for full-load conditions as detailed in Table III.

Fig. 10 depicts the input phase voltage $u_{N,R}$ and the corresponding input inductor current recorded in peak detection mode (in order to show the input current ripple) and the operating behavior for partial DCM occurring at very light loads ($P_O = 366$ W). The local average value of the input current is still of approximately sinusoidal shape (and/or proportional to the phase voltage) with a total harmonic distortion of $THD\_A = 11.2\%$ and a power factor of $\lambda = 0.986$. Therefore, although the theory compiled in Section I does not hold in DCM

TABLE II
OPERATING PARAMETERS FOR THE EXPERIMENTAL INVESTIGATIONS (cf. FIG. 8) OF THE MULTIPLIER-FREE CONTROL SYSTEM ACCORDING TO FIG. 3 FOR TWO DIFFERENT INPUT POWER LEVELS

	$U_{N,rms}$ [V]	I_N [A]	P_N [kW]	λ	THD V [%]	THD A [%]	U_O [V]	I_O [A]	P_O [kW]	η [%]
(a)	400	7.68	5.30	1.000	2.7	3.2	676	7.60	5.14	97.0
(b)	400	3.59	2.47	0.999	2.7	3.2	677	3.55	2.40	97.3

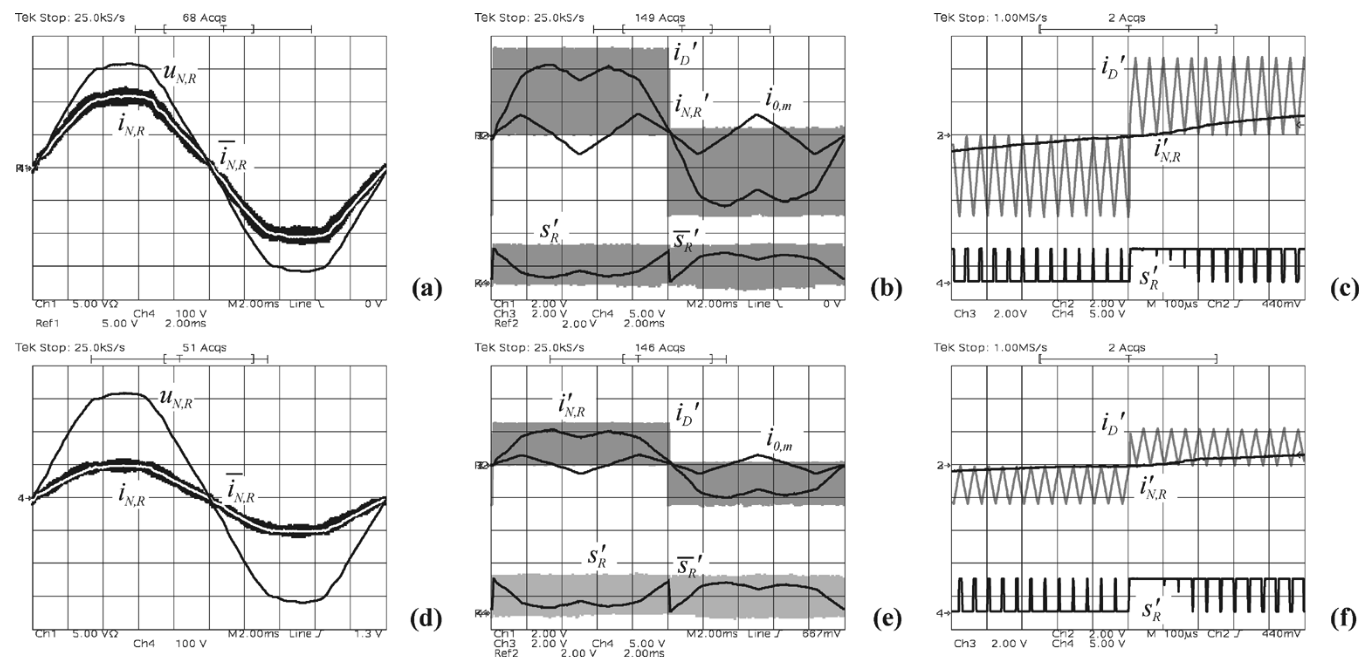

Fig. 8. Experimental analysis of the control concept according to Fig. 3 in connection with a 5-kW prototype of the VIENNA Rectifier. Operating parameters: $U_{N,\mathrm{rms}} = 400$ V (line-to-line voltage), $U_O = 675$ V, output power $P_O = 5.14$ kW for (a)–(c) and $P_O = 2.40$ kW, for (d)–(f). (a), (d) Mains ac phase voltage $u_{N,R}$ and corresponding input current $i_{N,R}$ (recorded in peak detection mode and in high resolution mode in order to attenuate the switching frequency ripple, 5 A/div). (b), (e) Modulating input current $i'_{N,R}$ (zero-sequence component current $i_{0,m}$ added to the low-pass filtered actual current $i_{N,R}$), triangular carrier signal i'_D shifted according to $sign(u_{N,R})$ and switching signal s'_R of the PWM stage for one fundamental period. (c), (f) Details of waveforms shown in (b) and (e) in the vicinity of the zero crossings of the phase current.

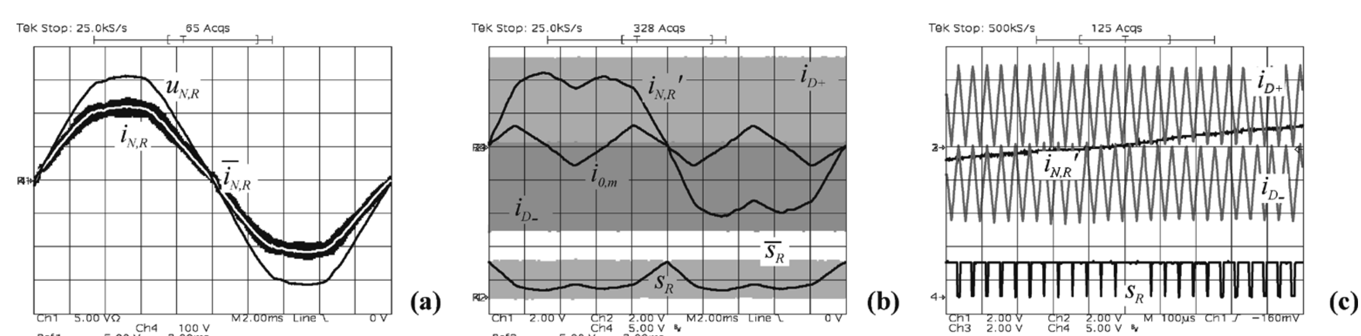

Fig. 9. Experimental analysis of the control concept according to Fig. 7 in connection with a 5-kW prototype of the VIENNA Rectifier. Operating parameters: $U_{N,rms} = 400$ V (line-to-line voltage), $U_O = 675$ V, output power $P_O = 5.11$ kW. (a) Mains ac phase voltage $u_{N,R}$ and corresponding input current $i_{N,R}$ (recorded in peak detection mode and in high resolution mode in order to attenuate the switching frequency ripple, 5 A/div). (b) Modulating input current $i'_{N,R}$ (zero-sequence component $i_{0,m}$ added to the low-pass filtered actual current $i_{N,R}$), triangular carrier signals i_{D+} and i_{D-} and switching signal s_R of the PWM stage for one mains period. (c) Details of waveforms shown in (b) in the vicinity of the zero crossings of the phase current.

the system shows a relatively good performance at light loads. A reason for this also is the nonlinearity of the iron powder cores employed for the input inductors which show the highest inductance values at zero and/or small current values, correspondingly the systems enters into DCM only at relatively light loads. Furthermore, if one of the input currents is in the vicinity of a zero crossing and, therefore, discontinuous, the other two phases show according to (7) current values different from zero

TABLE III
(a) OPERATING PARAMETERS FOR THE EXPERIMENTAL INVESTIGATIONS (cf. FIG. 9) OF THE MULTIPLIER-FREE CONTROL SYSTEM ACCORDING TO FIG. 7. (b) DCM CORRESPONDING TO FIG. 10

	$U_{N,rms}$ [V]	I_N [A]	P_N [kW]	λ	*THD* V [%]	*THD* A [%]	U_O [V]	I_O [A]	P_O [kW]	η [%]
(a)	400	7.60	5.25	0.999	2.7	3.1	675	7.57	5.11	97.3
(b)	400	0.56	0.389	0.986	2.7	11.2	677	0.54	0.366	94.0

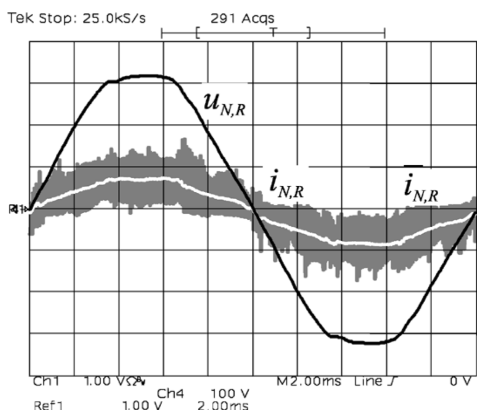

Fig. 10. Input inductor current $i_{N,R}$ (1 A/div) recorded in peak detection mode and the corresponding average value $\bar{i}_{N,R}$ (recorded using high-resolution mode) in partly DCM (light load) according to Table III(b).

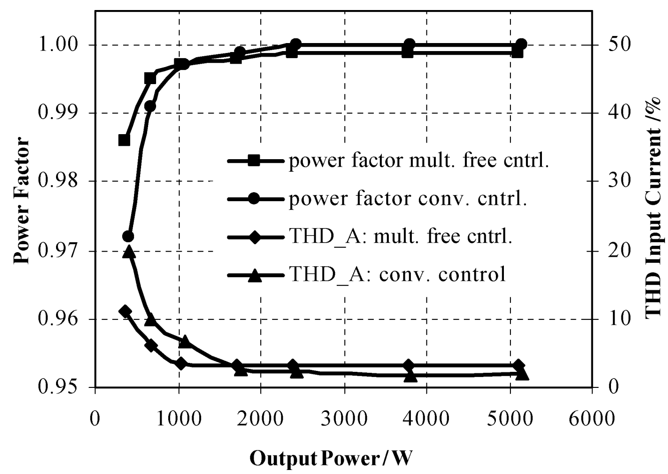

Fig. 11. Total harmonic distortion of the input currents (THD_A) and of the power factor λ for the conventional and for the multiplier-free control concept in dependency on the rectifier output power.

and, therefore, still stay in CCM (for operating conditions as shown in Fig. 10). Since the three phases are not decoupled this ensures an approximately voltage proportional guidance of all three input phase currents. The input current would become discontinuous within the whole mains period for low input current amplitudes, but in the realization at hand the converter enters a hickup mode below a defined input power level in order to control the output voltage to a constant value also in idle mode (at no load every single pulse would increase the output voltage). The behavior of the system in DCM could be further improved by increasing the switching frequency at light loads as proposed in [17].

The dependency of the total harmonic distortion of the input currents (THD_A) and of the power factor λ on the output power is given in Fig. 11. There, the performance of the multiplier free control concept is higher as compared to the conventional multiplier-based average current mode control for low output power levels ($P_O < 1.6$ kW). This is due to slight inaccuracies of the detection of the sign of the input phase voltages required for conventional control for the inversion of the switching signals for negative phase current (cf. [4, Fig. 7]). The opposite is true for higher output power, but, considering the limited accuracy of the measurement equipment the performance is about equal for both concepts. The efficiency of the converter system is not influenced by the control method.

V. CONCLUSION

This paper has presented a novel concept for mains voltage proportional input current shaping which eliminates analog or digital multipliers in the current control loop. The concept features a wide modulation range comparable to space-vector modulation by extending the modulating phase current values by a zero-sequence component with a significant third harmonic content. Besides a basic theoretical analysis an experimental verification of the concept was given in connection with a 5-kW prototype of the PWM VIENNA Rectifier for symmetric three-phase input. Also, a modified control scheme which relies on the absolute values of the input phase currents and a modified control scheme which directly employs the input phase currents as modulating signals and does not rely on information about the signs of the input phase currents and/or mains phase voltages were presented and the latter was verified experimentally also for DCM.

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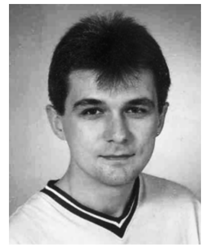

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