Novel Three-Phase AC-DC-AC Sparse Matrix Converter

Part I: Derivation, Basic Principle of Operation, Space Vector Modulation, Dimensioning

J.W. Kolar, M. Baumann*, F. Schafmeister, H. Ertl*

ETH Zurich
Power Electronic Systems Laboratory
ETH Zentrum/ETL H22
Physikstr. 3, CH-8092 Zurich/Switzerland
kolar@lem.ee.ethz.ch

*Vienna University of Technology
Dept. of Electrical Drives
Gusshausstr. 27/E 372
A-1040 Vienna/Austria
martina.baumann@tuwien.ac.at

Abstract. A novel three-phase AC-DC-AC Sparse Matrix Converter (SMC) having no energy storage elements in the DC link and employing only 15 IGBTs as opposed to 18 IGBTs of a functionally equivalent conventional AC-AC matrix converter (CMC) is proposed. It is shown that the realization effort could be further reduced to only 9 IGBTs (Ultra Sparse Matrix Converter, USMC) in case the phase displacement of the fundamentals of voltage and current at the input and at the output is limited to $\pm\pi/6$. The dependency of the voltage and current transfer ratios of the systems on the operating parameters is analyzed and a space vector modulation scheme is described in combination with a zero current commutation procedure. Furthermore, a safe multi-step current commutation concept is treated briefly. Conduction and switching losses of the SMC and USMC are calculated in analytically closed form. Finally, the theoretical results are verified in Part II of the paper by digital simulations and results of a first experimental investigation of a 10kW/400V SMC prototype are given.

I. INTRODUCTION

Three-phase matrix converters are capable of providing simultaneous amplitude and frequency transformation of a three-phase voltage system and do need only small switching frequency ac filter components as opposed to conventional two-stage AC/DC/AC conversion by back-to-back connection of current or voltage DC link PWM converter systems. Furthermore, matrix converters are inherently bi-directional and therefore can regenerate energy back into the mains from the load side where the mains current is sinusoidal and the displacement factor seen by the mains can be adjusted by proper modulation irrespective of the type of load. In consequence matrix converters show a high power density and due to lacking electrolytic capacitors a potentially high reliability. Accordingly, there is considerable interest in the application of matrix converters for the realization of highly compact three-phase AC drives [1] for industrial and military marine and avionics systems.

A conventional matrix converter does employ 9 bidirectional bipolar (four-quadrant) switches which, based on available power semiconductor technology have to be formed by 18 unipolar turn-off power semiconductors (IGBTs) and 18 diodes as shown in **Fig.1(a).** The combination of 2 IGBTs and 2 anti-parallel diodes per four-quadrant switch does allow a selective turn-on of the switch for each current direction as required for the implementation of a safe multi-step commutation strategy avoiding the short circuiting of an input line-to-line voltage or an abrupt interruption of an output phase current [2, 3].

Research on the matrix converter so far has been mainly focused on modulation schemes and digital generation of the PWM switching patterns. The derivation of alternative topologies showing identical functionality but a lower count of unipolar turn-off power semiconductors has not been paid much attention.

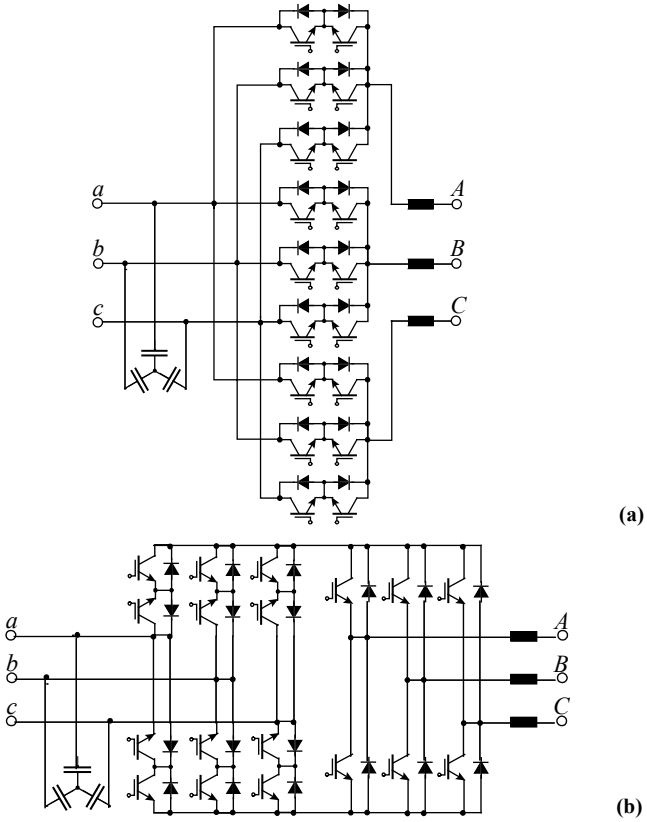


Fig. 1: (a): Conventional matrix converter (CMC) shown for common emitter arrangement of the power transistors of a four quadrant switch cell; a common collector arrangement does allow to reduce the number of isolated gate drive power supplies from nine to six (cf. Tab.1) and therefore is employed in a new matrix converter power module [4],[5]. **(b):** indirect matrix converter (IMC) as proposed in [6] and also analyzed in [7].

In this paper novel matrix-equivalent three-phase AC-DC-AC converter topologies are developed based on the structure of an indirect matrix converter (IMC, cf. Fig.1(b)) which has been proposed in [6] (cf. **Section II**). The novel converter topologies do show a reduced number of power transistors as compared to the CMC or IMC and are therefore denoted as *Sparse Matrix Converter* (SMC) and/or *Ultra Sparse Matrix Converter* (USMC). In **Section III** a safe multi-step commutation concept for the SMC is treated and a zero current commutation procedure featuring low complexity is described. In **Section IV** a space vector modulation scheme is proposed which naturally does provide zero current commutation and ohmic fundamental mains behavior. Furthermore, in **Section V** the operating range of the SMC and of the USMC is analyzed and the dependency of the current and voltage transfer ratio of a matrix

converter on the phase displacement of voltage and current fundamentals at the input and at the output side is clarified. In **Section VI** the average and rms current stress on the IGBTs and diodes as required for the dimensioning of the power circuit of the SMC and of the USMC are calculated for ohmic fundamental mains behavior in dependency on the modulation depth and on the load power factor. In **Section VII** the theoretical considerations are verified by digital simulations and in **Section VIII** results of a first experimental investigation of the reduced complexity matrix converter are presented. There, the theoretical considerations are verified by digital simulations and do provide the basis for the dimensioning of a 10kW/400V_{rms} line-to-line input SMC prototype supplying a passive load. Finally, in **Section IX** topics of the continuation of the research are identified and a novel three-level output stage SCM (SMC3) is proposed.

II. Derivation of the SMC Topology

In the following the derivation of the circuit topology of the SMC and the equivalence to the CMC concerning controllability and/or modulation range shall be treated. The topology of the CMC is shown in Fig.1(a) where, with reference to a three-phase AC motor drive application the converter input voltages and the output currents are assumed to be impressed. Modulation schemes for the CMC as given in the literature can be classified in direct frequency conversion schemes [8, 9] and indirect frequency conversion schemes [10, 2]. For the indirect frequency conversion scheme the CMC is fictitiously divided into a voltage-fed rectifier input stage and an inverter output stage with impressed output currents which are directly connected on the DC side (see Fig.2 in [2]). The physical implementation of this basic idea does result in the converter topology depicted in Fig.1(b) [6] which is functionally equivalent to a CMC and will be denoted as indirect matrix converter (IMC) in the following (cf. **Fig.2**).

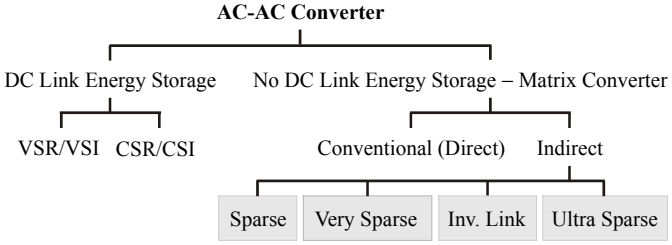


Fig. 2: Classification of AC-AC converter topologies. Systems pointed out are treated in more detail in this paper.

For the IMC a conventional (two-quadrant switch) voltage-source-type inverter is fed by a four-quadrant switch current-source-type rectifier which is able to operate with positive *and* negative DC current for *unipolar* DC link voltage as required by the inverter stage. There, the input capacitor of the inverter has to be thought to be realized by the AC-side (voltage impressing) filter capacitors of the rectifier stage and the output inductor of the rectifier is realized by the current-impressing inductance of the load. The IMC does employ 18 unipolar turn-off power semiconductors and 18 diodes (cf. **Tab.1**) and therefore basically shows the same realization effort as the CMC. However, the inverter stage could be realized by a conventional six-pack power module what slightly reduces the realization effort as compared to a fully discrete realization of a CMC.

Converter Type	Transistors	Diodes	Isolated Driver Potentials
CMC	18	18	6
IMC	18	18	8
SMC	15	18	7
VSMC	12	30	10
USMC	9	18	7

Table I: Realization effort of different matrix converter topologies (for VSMC see Section III.).

The DC link voltage of the IMC shows a fixed polarity, but the IMC four-quadrant switch current-source-type rectifier could operate with both DC link voltage polarities. Therefore, it is near at hand to consider ways of reducing the rectifier stage circuit complexity. The actual possibility of a reduction of the number of unipolar turn-off power semiconductors of the current-source-type rectifier stage is verified step-by-step in **Fig.3** for a single bridge leg.

For s_{pa}=s_{ap}=1 (a switching function s_i=1 does denote a turn-on state of the corresponding power transistor S_i, s_i=0 does denote the turn-off state) for the bridge leg topology Fig.3(a) input *a* is connected bidirectionally to *p*. There, in case of u_{pn}>0 transistor S_{an} is blocking voltage, a voltage u_{pn}<0 is taken over by S_{na}. Restricting the operation to u_{pn}>0, therefore a blocking of S_{na} within the turn-on interval of S_{ap} is not required and both transistors could be combined in a single transistor S_a (cf. Fig.3(b)) which has to be turned on for connection of *a* to *p* as well as for connecting *a* to *n*. However, the resulting bridge leg topology (cf. Fig.3(c), [11],[12]) for u_{pn}>0 still does provide the independent controllability of both current directions as required for the implementation of a safe commutation strategy [3]. Consequently, for u_{pn}>0 the functionality of an IMC and/or CMC can be realized by the novel converter topology depicted in **Fig.4(a)** which does employ only 15 IGBTs as opposed to 18 IGBTs of the IMC and does require a lower number of isolated gate drive power supplies and therefore shall be denoted as *Sparse Matrix Converter* (SMC) in the following.

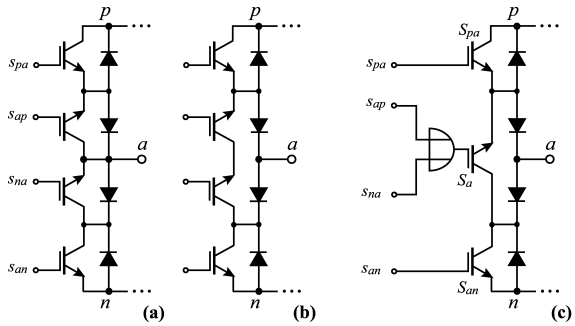


Fig. 3: Modification of the structure of a bridge leg of the current-source-type rectifier input stage of the IMC **(a)** (cf. Fig.1(b)) into the SMC bridge leg topology **(c)** (cf. Fig.4(a)).

The functional equivalence of CMC/IMC and SMC are proven by **Tab.2** [2] and **Tab.3** where the CMC and SMC line-to-line output voltages and input phase currents resulting for the different switching state combinations are compiled. In case, e.g., u_{ab}>0, u_{bc}, u_{ca} < 0 (as given in a π/3-wide interval of a mains period) is valid, due to the restriction u_{pn}>0 the SMC switching states pointed out in Tab.3 are not available. However, the remaining switching states to be employed for space vector modulation [2] are identical to the

switching states of the CMC concerning output voltage and input current formation (cf. Tab.2). Therefore, the controllability and the operating range of the SMC is not restricted as compared to the CMC despite the reduced number of unipolar turn-off power semiconductors. As a result the SMC represents a highly interesting alternative to the CMC for industrial applications.

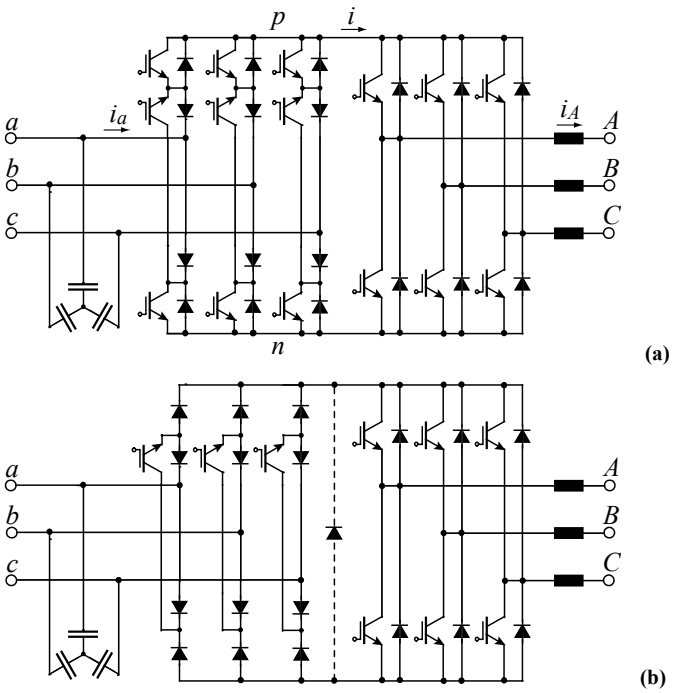


Fig. 4: Proposed Matrix Converter Topologies; **(a):** Sparse Matrix Converter (SMC), **(b):**Ultra Sparse Matrix Converter (USMC).

No.	*A*	*B*	*C*	s_{Aa}	s_{Ab}	s_{Ac}	s_{Ba}	s_{Bb}	s_{Bc}	s_{Ca}	s_{Cb}	s_{Cc}	u_{AB}	u_{BC}	u_{CA}	i_a	i_b	i_c
1	*a*	*a*	*a*	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0
2	*b*	*b*	*b*	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0
3	*c*	*c*	*c*	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0
4	*a*	*c*	*c*	1	0	0	0	0	1	0	0	1	$-u_{ca}$	0	u_{ca}	i_A	0	$-i_A$
5	*b*	*c*	*c*	0	1	0	0	0	1	0	0	1	u_{bc}	0	$-u_{bc}$	0	i_A	$-i_A$
6	*b*	*a*	*a*	0	1	0	1	0	0	1	0	0	$-u_{ab}$	0	u_{ab}	$-i_A$	i_A	0
7	*c*	*a*	*a*	0	0	1	1	0	0	1	0	0	u_{ca}	0	$-u_{ca}$	$-i_A$	0	i_A
8	*c*	*b*	*b*	0	0	1	0	1	0	0	1	0	$-u_{bc}$	0	u_{bc}	0	$-i_A$	i_A
9	*a*	*b*	*b*	1	0	0	0	1	0	0	1	0	u_{ab}	0	$-u_{ab}$	i_A	$-i_A$	0
10	*c*	*a*	*c*	0	0	1	1	0	0	0	0	1	u_{ca}	$-u_{ca}$	0	i_B	0	$-i_B$
11	*c*	*b*	*c*	0	0	1	0	1	0	0	0	1	$-u_{bc}$	u_{bc}	0	0	i_B	$-i_B$
12	*a*	*b*	*a*	1	0	0	0	1	0	1	0	0	u_{ab}	$-u_{ab}$	0	$-i_B$	i_B	0
13	*a*	*c*	*a*	1	0	0	0	0	1	1	0	0	$-u_{ca}$	u_{ca}	0	$-i_B$	0	i_B
14	*b*	*c*	*b*	0	1	0	0	0	1	0	1	0	u_{bc}	$-u_{bc}$	0	0	$-i_B$	i_B
15	*b*	*a*	*b*	0	1	0	1	0	0	0	1	0	$-u_{ab}$	u_{ab}	0	i_B	$-i_B$	0
16	*c*	*c*	*a*	0	0	1	0	0	1	1	0	0	0	u_{ca}	$-u_{ca}$	i_C	0	$-i_C$
17	*c*	*c*	*b*	0	0	1	0	0	1	0	1	0	0	$-u_{bc}$	u_{bc}	0	i_C	$-i_C$
18	*a*	*a*	*b*	1	0	0	1	0	0	0	1	0	0	u_{ab}	$-u_{ab}$	$-i_C$	i_C	0
19	*a*	*a*	*c*	1	0	0	1	0	0	0	0	1	0	$-u_{ca}$	u_{ca}	$-i_C$	0	i_C
20	*b*	*b*	*c*	0	1	0	0	1	0	0	0	1	0	u_{bc}	$-u_{bc}$	0	$-i_C$	i_C
21	*b*	*b*	*a*	0	1	0	0	1	0	1	0	0	0	$-u_{ab}$	u_{ab}	i_C	$-i_C$	0
22	*a*	*b*	*c*	1	0	0	0	1	0	0	0	1	u_{ab}	u_{bc}	u_{ca}	i_A	i_B	i_C
23	*a*	*c*	*b*	1	0	0	0	0	1	0	1	0	$-u_{ca}$	$-u_{bc}$	$-u_{ab}$	i_A	i_C	i_B
24	*b*	*a*	*c*	0	1	0	1	0	0	0	0	1	$-u_{ab}$	$-u_{ca}$	$-u_{bc}$	i_B	i_A	i_C
25	*b*	*c*	*a*	0	1	0	0	0	1	1	0	0	u_{bc}	u_{ca}	u_{ab}	i_C	i_A	i_B
26	*c*	*a*	*b*	0	0	1	1	0	0	0	1	0	u_{ca}	u_{ab}	u_{bc}	i_B	i_C	i_A
27	*c*	*b*	*a*	0	0	1	0	0	1	1	0	0	$-u_{bc}$	$-u_{ab}$	$-u_{ca}$	i_C	i_B	i_A

TABLE II. Switching states and corresponding line-to-line output voltages and input phase currents of the CMC.

No.	*A*	*B*	*C*	s_{pa}	s_{pb}	s_{pc}	s_{an}	s_{bn}	s_{cn}	s_A	s_B	s_C	u_{AB}	u_{BC}	u_{CA}	u	i_a	i_b	i_c
1	*p*	*p*	*p*	X	X	X	X	X	X	1	1	1	0	0	0	-	0	0	0
10	*n*	*n*	*n*	X	X	X	X	X	X	0	0	0	0	0	0	-	0	0	0
19	X	X	X	1	0	0	1	0	0	X	X	X	0	0	0	0	0	0	0
25	X	X	X	0	1	0	0	1	0	X	X	X	0	0	0	0	0	0	0
31	X	X	X	0	0	1	0	0	1	X	X	X	0	0	0	0	0	0	0
37	*a*	*c*	*c*	1	0	0	0	0	1	1	0	0	$-u_{ca}$	0	u_{ca}	$-u_{ca}$	i_A	0	$-i_A$
38	*a*	*c*	*c*	0	0	1	1	0	0	0	1	1	$-u_{ca}$	0	$-u_{ca}$	u_{ca}	i_A	0	$-i_A$
39	*b*	*c*	*c*	0	1	0	0	0	1	1	0	0	u_{bc}	0	$-u_{bc}$	u_{bc}	0	i_A	$-i_A$
40	*b*	*c*	*c*	0	0	1	0	1	0	0	1	1	u_{bc}	0	$-u_{bc}$	$-u_{bc}$	0	i_A	$-i_A$
41	*b*	*a*	*a*	0	1	0	1	0	0	1	0	0	$-u_{ab}$	0	u_{ab}	$-u_{ab}$	$-i_A$	i_A	0
42	*b*	*a*	*a*	1	0	0	0	1	0	0	1	1	$-u_{ab}$	0	u_{ab}	u_{ab}	$-i_A$	i_A	0
43	*c*	*a*	*a*	0	0	1	1	0	0	1	0	0	u_{ca}	0	$-u_{ca}$	u_{ca}	$-i_A$	0	i_A
44	*c*	*a*	*a*	1	0	0	0	0	1	0	1	1	u_{ca}	0	$-u_{ca}$	$-u_{ca}$	$-i_A$	0	i_A
45	*c*	*b*	*b*	0	0	1	0	1	0	1	0	0	$-u_{bc}$	0	u_{bc}	$-u_{bc}$	0	$-i_A$	i_A
46	*c*	*b*	*b*	0	1	0	0	0	1	0	1	1	$-u_{bc}$	0	u_{bc}	u_{bc}	0	$-i_A$	i_A
47	*a*	*b*	*b*	1	0	0	0	1	0	1	0	0	u_{ab}	0	$-u_{ab}$	u_{ab}	i_A	$-i_A$	0
48	*a*	*b*	*b*	0	1	0	1	0	0	0	1	1	u_{ab}	0	$-u_{ab}$	$-u_{ab}$	i_A	$-i_A$	0
49	*c*	*a*	*c*	1	0	0	0	0	1	0	1	0	u_{ca}	$-u_{ca}$	0	$-u_{ca}$	i_B	0	$-i_B$
50	*c*	*a*	*c*	0	0	1	1	0	0	1	0	1	u_{ca}	$-u_{ca}$	0	u_{ca}	i_B	0	$-i_B$
51	*c*	*b*	*c*	0	1	0	0	0	1	0	1	0	$-u_{bc}$	u_{bc}	0	u_{bc}	0	i_B	$-i_B$
52	*c*	*b*	*c*	0	0	1	0	1	0	1	0	1	$-u_{bc}$	u_{bc}	0	$-u_{bc}$	0	i_B	$-i_B$
53	*a*	*b*	*a*	0	1	0	1	0	0	0	1	0	u_{ab}	$-u_{ab}$	0	$-u_{ab}$	$-i_B$	i_B	0
54	*a*	*b*	*a*	1	0	0	0	1	0	1	0	1	u_{ab}	$-u_{ab}$	0	u_{ab}	$-i_B$	i_B	0
55	*a*	*c*	*a*	0	0	1	1	0	0	0	1	0	$-u_{ca}$	u_{ca}	0	u_{ca}	$-i_B$	0	i_B
56	*a*	*c*	*a*	1	0	0	0	0	1	1	0	1	$-u_{ca}$	u_{ca}	0	$-u_{ca}$	$-i_B$	0	i_B
57	*b*	*c*	*b*	0	0	1	0	1	0	0	1	0	u_{bc}	$-u_{bc}$	0	$-u_{bc}$	0	$-i_B$	i_B
58	*b*	*c*	*b*	0	0	1	0	1	0	1	0	1	u_{bc}	$-u_{bc}$	0	u_{bc}	0	$-i_B$	i_B
59	*b*	*a*	*b*	1	0	0	0	1	0	0	1	0	$-u_{ab}$	u_{ab}	0	u_{ab}	i_B	$-i_B$	0
60	*b*	*a*	*b*	0	1	0	1	0	0	1	0	1	$-u_{ab}$	u_{ab}	0	$-u_{ab}$	i_B	$-i_B$	0
61	*c*	*c*	*a*	1	0	0	0	0	1	0	0	1	0	u_{ca}	$-u_{ca}$	$-u_{ca}$	i_C	0	$-i_C$
62	*c*	*c*	*a*	0	0	1	1	0	0	1	1	0	0	u_{ca}	$-u_{ca}$	u_{ca}	i_C	0	$-i_C$
63	*c*	*c*	*b*	0	1	0	0	0	1	0	0	1	0	$-u_{bc}$	u_{bc}	u_{bc}	0	i_C	$-i_C$
64	*c*	*c*	*b*	0	0	1	0	1	0	1	1	0	0	$-u_{bc}$	u_{bc}	$-u_{bc}$	0	i_C	$-i_C$
65	*a*	*a*	*b*	0	1	0	1	0	0	0	0	1	0	u_{ab}	$-u_{ab}$	$-u_{ab}$	$-i_C$	i_C	0
66	*a*	*a*	*b*	1	0	0	0	1	0	1	1	0	0	u_{ab}	$-u_{ab}$	u_{ab}	$-i_C$	i_C	0
67	*a*	*a*	*c*	0	0	1	1	0	0	0	0	1	0	$-u_{ca}$	u_{ca}	u_{ca}	$-i_C$	0	i_C
68	*a*	*a*	*c*	1	0	0	0	0	1	1	1	0	0	$-u_{ca}$	u_{ca}	$-u_{ca}$	$-i_C$	0	i_C
69	*b*	*b*	*c*	0	0	1	0	1	0	0	0	1	0	u_{bc}	$-u_{bc}$	$-u_{bc}$	0	$-i_C$	i_C
70	*b*	*b*	*c*	0	1	0	0	0	1	1	1	0	0	u_{bc}	$-u_{bc}$	u_{bc}	0	$-i_C$	i_C
71	*b*	*b*	*a*	1	0	0	0	1	0	0	0	1	0	$-u_{ab}$	u_{ab}	u_{ab}	i_C	$-i_C$	0
72	*b*	*b*	*a*	0	1	0	1	0	0	1	1	0	0	$-u_{ab}$	u_{ab}	$-u_{ab}$	i_C	$-i_C$	0

TABLE III. Switching states and corresponding line-to-line output voltages and input phase currents of the CMC. The switching states pointed out are not available for $u_{ab}>0$, u_{bc}, $u_{ca}<0$ due to the restriction $u_{pn}>0$ given by the SMC inverter output stage. The switching state of a bridge leg of the input stage is denoted by switching functions s_{pi} and s_{in}, $i=a,b,c$, only, switching functions s_i are omitted for the sake of brevity and redundancy.

With reference to an unidirectional buck-type PWM rectifier system as described in [13] and [14] one now could further reduce the realization effort of the SMC by omitting the power transistors S_{pi} and S_{in} in each bridge leg $i=a,b,c$, which do provide a reversibility of the DC link current.

This basically does restrict the circuit operation to unidirectional power flow ($u_{pn}>0$, $i>0$). As a more detailed analysis shows (cf. Section V) the controllability of the phase displacement of input voltage and input current fundamental then is limited to $\pm\pi/6$. Furthermore, the phase displacement of load current and load voltage fundamental is not allowed to exceed $\pm\pi/6$. However, due to the low number of power transistors the novel circuit topology which is denoted as *Ultra Sparse Matrix Converter* (USMC) in the following is of high interest and will be treated in detail in a future paper.

III. COMMUTATION SCHEME

A. Multi-Step Commutation

For a given switching state of the rectifier input stage the commutation of the inverter output stage has to be performed identical to the commutation of a conventional voltage DC link converter where a dead time between turn-off and turn-on of the power transistors of a bridge leg has to be considered in order to avoid a short circuit of the DC link voltage.

For the changing of the switching state of the SMC rectifier input stage for given inverter switching state one has to ensure that no bidirectional connection between two input lines, i.e. not short-circuiting of an input line-to-line voltage does occur. There, multi-step commutation schemes, i.e. voltage independent and current independent commutation as known for the CMC (cf. e.g. [3]) can be employed (cf. **Fig. 5**). Both commutation strategies have been analyzed extensively in the literature (cf. e.g. [15-17]), we therefore would like to omit a detailed description here for the sake of brevity.

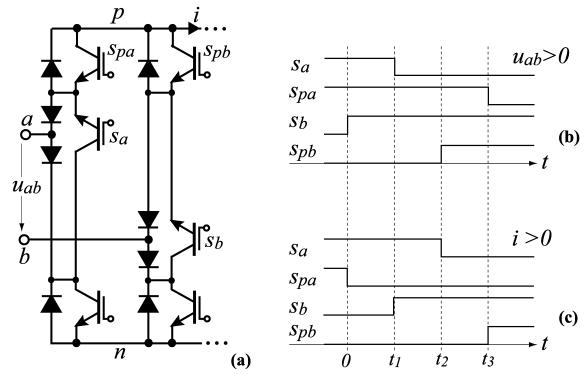


Fig. 5: Application of multi-step commutation to the SMC rectifier input stage; **(a):** Basic structure of the commutating bridge legs; switching state sequence given for changing the connection of the positive DC link voltage bus *p* from input *a* to input *b*, **(b):** voltage independent commutation assuming a positive DC link current, i.e. $i>0$, **(c):** current independent commutation assuming $u_{ab}>0$.

B. Zero DC Link Current Commutation

The obvious drawback of multi-step commutation is complexity. However, AC-DC-AC (two-stage) matrix converters do provide a degree of freedom for control which is not available for the CMC and can be utilized for alleviating the commutation problem. As proposed in [18], in advance to rectifier stage commutation the inverter stage could be switched into free-wheeling operation and the rectifier stage then could commutate at zero DC link current, i.e. no continuity of the DC link current flow during commutation has to be considered and the switching losses of the input stage are reduced. One only has to ensure that no overlapping of turn-on intervals of power transistors in a bridge half does occur which would result in a short circuit of an input line-to-line voltage (cf. **Fig. 6**). All further considerations in this paper will be restricted to this straightforward and potentially more reliable commutation concept.

It is interesting to note that for employing the zero DC link current commutation strategy the topology of the IMC could be reduced to the circuit structure shown in **Fig.7**(a) which will be denoted as *Very Sparse Matrix Converter* (VSMC [19, 20]) in the following.

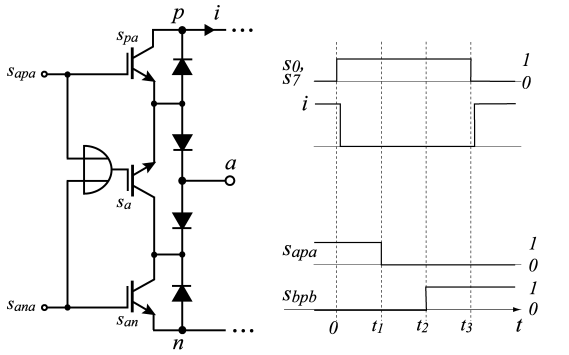


Fig. 6: Zero current commutation of indirect matrix converter topologies shown for the SMC. **(a):** Control of the power transistors of a bridge leg of the SMC, for the VSMC (cf. Fig.7(a)) the switching functions have to be applied directly to the corresponding power transistors (e.g. s_{apa} has to be connected to the gate terminal of switch S_{apa}). **(b):** Switching state sequence (s_0,s_7=1 does indicate a free-wheeling operation of the inverter stage) and DC link current *i* for changing the connection of the positive DC link voltage bus *p* from input *a* to input *b*.

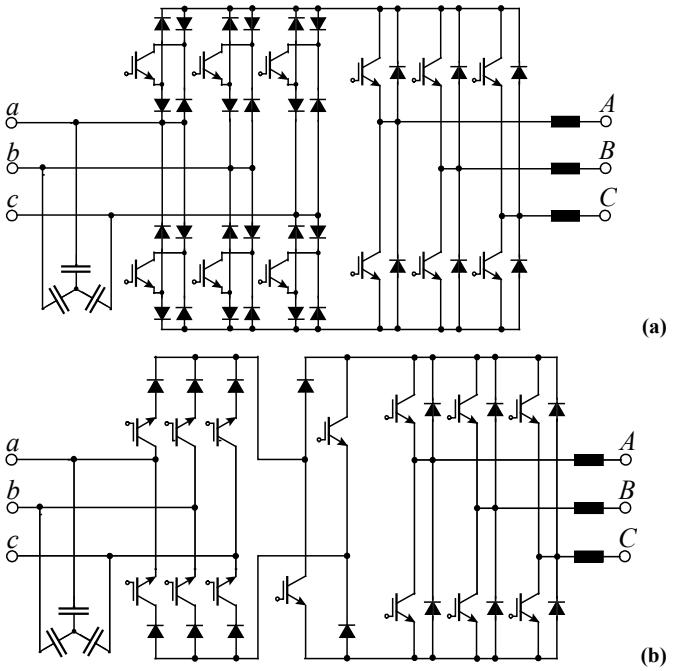


Fig. 7: Topology of the *Very Sparse Matrix Converter* (VSMC) **(a)** and of the *Inverting Link Matrix Converter* (ILMC) **(b)**.

Zero DC link current commutation also would allow employ the circuit topology shown in Fig.7(b) for three-phase AC-AC power conversion. There, the bidirectional current carrying capability of the input stage is achieved by combining a conventional current DC link rectifier and a voltage and/or current inverting switching section formed, e.g., by two power transistors and two diodes [21]. Accordingly, this converter shall be denoted as *Inverting Link Matrix Converter* (ILMC). As compared to the SMC, the ILMC does show an about equal number of power transistors. However, the inversion of the inverter output stage input current has to be performed with switching frequency for a phase displacement of load current and load voltage fundamental larger than $\pm \pi/6$ what does result in high

switching losses and complex control. Therefore, the ILMC will not be considered in more detail in this paper.

Finally, it should be pointed out that the commutation of the USMC can be performed irrespective of the switching state of the output stage in case a free-wheeling diode is provided in the DC link (cf. Fig.4(b)). However, commutating the input stage at non-zero DC link current does cause additional switching losses. Therefore, a coordination of the switching state changes of the input and output stage is advantageous also in this case. Employing a free-wheeling diode also for zero current commutation does potentially increase the circuit reliability because a path for the DC link current is provided in case of missing turn-on of an input stage power transistor, e.g. due to an gate drive failure. As is obvious from Fig.6(a), the switching function of the power transistors of the USMC can be derived from the switching functions of the power transistors of a bridge leg of the SMC by an OR gate.

IV. Space Vector Modulation

The modulation concept derived in the following should be applicable to the SMC, VSMC and USMC, i.e. should facilitate zero DC link current commutation of the rectifier (input) stage. In order to make a maximum voltage available for the formation of the output voltage, a phase input is clamped to the positive or negative DC link bus in $\pi/3$-wide intervals when the corresponding phase voltage does show the highest absolute value (cf. **Tab.4** and **Fig.8**). Thereby, the required operating condition $u_{pn}>0$ of the SMC, VSMC, and USMC is inherently satisfied.

$\varphi_1=\omega_1 t$	u_p	u_n	u
0 ... $\pi/6$	u_a	u_b, u_c	u_{ab}, u_{ac}
$\pi/6$ ... $\pi/2$	u_a, u_b	u_c	u_{ac}, u_{bc}
$\pi/2$ ... $5\pi/6$	u_b	u_a, u_c	u_{ba}, u_{bc}
$5\pi/6$ ... $7\pi/6$	u_b, u_c	u_a	u_{ba}, u_{ca}
$7\pi/6$ ... $3\pi/2$	u_c	u_a, u_b	u_{ca}, u_{cb}
$3\pi/2$ ... $11\pi/6$	u_a, u_c	u_b	u_{ab}, u_{cb}
$11\pi/6$ ... 0	u_a	u_b, u_c	u_{ab}, u_{ac}

Table IV. Intervals of an input voltage period, and corresponding potentials of the positive and negative DC link bus u_p and u_n (given with reference to the mains star point) and DC link voltage levels u; clamping of a phase input to p or n is pointed out by a dotted area.

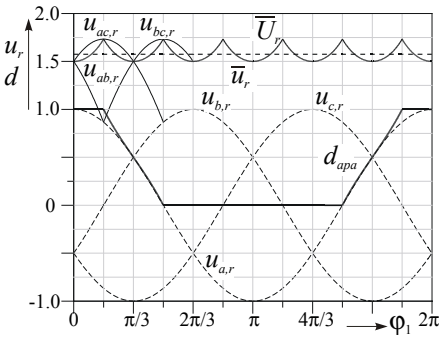


Fig. 8: Time behavior of the input phase voltage u_a, u_b, u_c, and of the local average $\bar{u}$ of the DC link voltage u; $\bar{U}$ does denote the global average value of u; voltages are normalized (index r) to the phase voltage amplitude $\hat{U}_1$. Furthermore shown: Duty cycle d_{apa} of power transistor S_{apa}, where for the clamping of phase a to p, $d_{apa}=1$ is valid.

With reference to the symmetry of the circuit topology and an assumed symmetry of the three-phase input voltage system,

$$u_a = \hat{U}_1 \cos(\omega_1 t)$$
$$u_b = \hat{U}_1 \cos(\omega_1 t - 2\pi/3) \qquad (1)$$
$$u_c = \hat{U}_1 \cos(\omega_1 t + 2\pi/3)$$

we will limit our considerations in the following to $\varphi_1 = 0...\pi/6$ where phase a remains clamped to the positive DC bus p. Furthermore, we assume a constant average value i of the DC link current i for each rectifier switching state. The formation of i and $\bar{i}$ within a pulse period $t_\mu=0...T_P$ (t_μ denotes a local time running within a pulse period) will be treated in detail, once the converter modulation scheme has been defined.

The DC link voltage u is defined by segments of the input line-to-line voltages u_{ab} and u_{ac} according to the rectifier switching state. Therefore, the voltage employed by the inverter for output voltage formation does show two different levels within each pulse half period (cf. **Fig.9**). In case the switching of rectifier and inverter stage is coordinated as shown in Fig.9 the switching over of the rectifier always does occur in the free-wheeling interval of the inverter and zero DC link current commutation is naturally achieved.

A free-wheeling of the rectifier stage, which could be realized by turning on the power transistors of a bridge leg simultaneously, e.g. $s_{apa}=s_{ana}=1$, would be equivalent to an inverter free-wheeling state concerning the formation of the input currents i_a, i_b, i_c and the formation of the output voltages u_A, u_B, u_C; in both cases $i_a=i_b=i_c=0$ and $u_{AB}=u_{BC}=u_{CA}=0$ is given. Therefore, aiming for a modulation scheme of low complexity (each change of the rectifier switching state is linked to switching the inverter into free-wheeling mode), free-wheeling operation is limited to the inverter stage, i.e.

$$d_{ab} + d_{ac} = 1. \qquad (2)$$

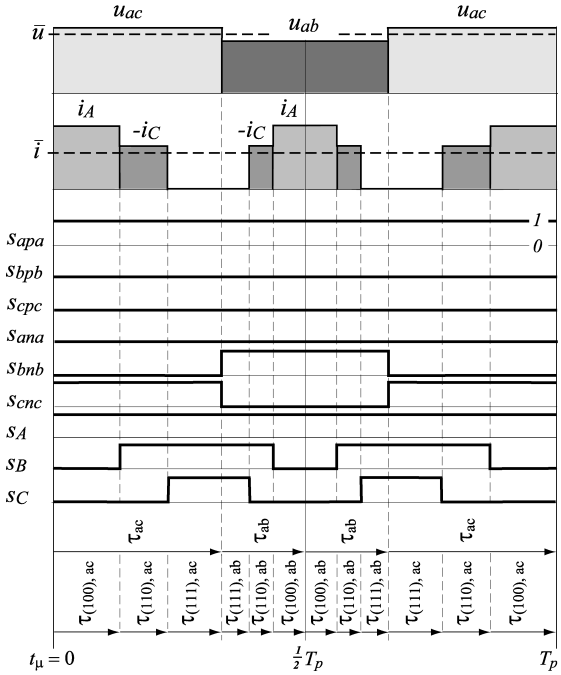


Fig. 9: Formation of the DC link voltage u and DC link current i within a pulse period and corresponding switching functions of the rectifier and inverter stage being characteristic for $\varphi_1 \in (0...\pi/6)$. Switching state changes of the input stage do occur at zero DC link current. The DC link current does show a constant average value i within τ_{ac} and τ_{ab}. The switching frequency ripple of the input line-to-line voltages u_{ac} and u_{ab} and of the output phase currents i_A and i_C is neglected for the sake of clarity.

Therefore, we have in the considered interval $\varphi_1= 0...\pi/6$ in which input a is clamped to the positive DC link bus

$$\bar{i}_a = (d_{ab} + d_{ac})\,\bar{i}, \qquad \bar{i}_b = d_{ab}\,\bar{i}, \qquad \bar{i}_c = d_{ac}\,\bar{i} \qquad (3)$$

where d_{ab} and d_{ac} do denote the relative on-time of the switching states being characterized by $u=u_{ab}$ and $u=u_{ac}$. In order to achieve an ohmic fundamental input behavior of the rectifier,

$$\cos\Phi_1 = 1 \tag{4}$$

we now have to guarantee a proportional relationship between the local average value (related to a pulse period) of an input phase current and the corresponding input phase voltage

$$\bar{i}_a \sim u_a; \qquad \bar{i}_b \sim u_b; \qquad \bar{i}_c \sim u_c \tag{5}$$

what does result in

$$d_{ac} = -\frac{\bar{i}_c}{\bar{i}_a} = -\frac{u_c}{u_a}; \qquad d_{ab} = -\frac{\bar{i}_b}{\bar{i}_a} = -\frac{u_b}{u_a} \tag{6}$$

where $u_a+u_b+u_c = 0$ has been considered.

At the inverter output a voltage space vector $\underline{u}_2$ of given absolute value $|\underline{u}_2|$ and given phase $\varphi_2 = \omega_2 t$ has to be formed in the average over half a pulse period $\frac{1}{2}T_P$ (reference values are denoted by a superscript *). For analyzing the voltage formation we will limit our considerations to $\varphi_2 = \omega_2 t = 0...\pi/6$. Based on this the relations for further intervals of the output period can be derived by symmetry considerations.

In $\varphi_2 = 0...\pi/6$ the formation of the output voltage is by the active voltage space vectors $\underline{u}_{2,(100)}$ and $\underline{u}_{2,(110)}$ and by the free-wheeling state (111) or (000), where $\underline{u}_{2,(111)} = \underline{u}_{2,(000)} = 0$ is valid. (The inverter output voltage space vectors are denominated by the corresponding combinations ($s_A s_B s_C$) of the bridge leg switching functions.)

In the time intervals $\tau_{ac} = d_{ac}T_P/2$ and $\tau_{ab} = d_{ab}T_P/2$ we have for the DC link voltage $u = u_{ac}$ and/or $u = u_{ab}$, accordingly the absolute value of the inverter output voltage space vector will show a different value. In order to fully utilize the voltages u_{ac} and u_{ab} for the formation of u_2 the output voltage space vectors have to show identical phase in τ_{ac} and τ_{ab} (cf. **Fig. 10**), what is achieved by identical values of the duty cycle of the active switching states (100) and (110) in τ_{ac} and τ_{ab}.

$$\delta_{(100),ac} = \frac{\tau_{(100),ac}}{\tau_{ac}} = \delta_{(100),ab} = \frac{\tau_{(100),ab}}{\tau_{ab}} = \delta_{(100)} \tag{7}$$

$$\delta_{(110),ac} = \frac{\tau_{(110),ac}}{\tau_{ac}} = \delta_{(110),ab} = \frac{\tau_{(110),ab}}{\tau_{ab}} = \delta_{(110)}\,. \tag{8}$$

With $\underline{u}_{(100)} = \frac{2}{3}u$ and $\underline{u}_{(110)} = \frac{2}{3}ue^{j\frac{\pi}{3}}$ for DC link voltage u we then have for the voltage space vector formed in the average over $\frac{1}{2}T_P$

$$\underline{u}_2^* = \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{(100),ac} + u_{ab}\tau_{(100),ab} + u_{ac}e^{j\frac{\pi}{3}}\tau_{(110),ac} + u_{ab}e^{j\frac{\pi}{3}}\tau_{(110),ab}) \tag{9}$$

and considering Eq.(7) and Eq.(8)

$$\begin{aligned}\underline{u}_2^* &= \frac{\frac{2}{3}}{\frac{T_P}{2}}(u_{ac}\tau_{ac}\delta_{(100)} + u_{ab}\tau_{bc}\delta_{(100)} + u_{ac}\tau_{ac}\delta_{(110)}e^{j\frac{\pi}{3}} + u_{ab}\tau_{bc}\delta_{(110)}e^{j\frac{\pi}{3}} \\ &= \tfrac{2}{3}(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P})\delta_{(100)} + \tfrac{2}{3}(u_{ac}\frac{\tau_{ac}}{\frac{1}{2}T_P} + u_{ab}\frac{\tau_{ab}}{\frac{1}{2}T_P})e^{j\frac{\pi}{3}}\delta_{(110)} \\ &= \tfrac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})\delta_{(100)} + \tfrac{2}{3}(u_{ac}d_{ac} + u_{ab}d_{ab})e^{j\frac{\pi}{3}}\delta_{(110)}.\end{aligned} \tag{10}$$

With the local average value $\bar{u}$ of the DC link voltage

$$\bar{u} = u_{ab}d_{ab} + u_{ac}d_{ac} \tag{11}$$

this results in

$$\underline{u}_2^* = \tfrac{2}{3}\bar{u}\delta_{(100)} + \tfrac{2}{3}\bar{u}e^{j\frac{\pi}{3}}\delta_{(110)}\,. \tag{12}$$

Therefore, for calculating the on-times of the active switching states we could directly refer to the local average value $\bar{u}$ of the DC link voltage and could omit the detailed consideration of the line-to-line input voltages u_{ac} and u_{ab} in τ_{ac} and τ_{ab}. We then have

$$\begin{aligned}\delta_{(100)} &= \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\cos(\varphi_2^* + \tfrac{\pi}{6}) \\ \delta_{(110)} &= \frac{\sqrt{3}}{2}\frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}}\sin\varphi_2^*\end{aligned} \tag{13}$$

and, therefore for the *absolute* turn-on times $\tau_{(100),ac}$ $\tau_{(100),ab}$ and $\tau_{(110),ac}$ $\tau_{(110),ab}$ of the output voltage space vectors $\underline{u}_{2,(100)}$ and $\underline{u}_{2,(110)}$ in τ_{ac} and τ_{ab}.

$$\begin{aligned}\tau_{(100),ac} &= -\tfrac{2}{3\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_c\cos(\varphi_2^* + \tfrac{\pi}{6}) \\ \tau_{(100),ab} &= -\tfrac{2}{3\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_b\cos(\varphi_2^* + \tfrac{\pi}{6}) \\ \tau_{(110),ac} &= -\tfrac{2}{3\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_c\sin\varphi_2^* \\ \tau_{(110),ab} &= -\tfrac{2}{3\sqrt{3}}T_P\frac{\hat{U}_2^*}{\hat{U}_1^2}u_b\sin\varphi_2^*\end{aligned} \tag{14}$$

As can be seen from Eq.(11) the local average value $\bar{u}$ of the DC link voltage shows a variation with six times the input frequency

$$\bar{u} = \tfrac{3}{2}\hat{U}_1\frac{1}{\cos(\omega_1 t)} \tag{15}$$

(cf. Fig.8) and a minimum of

$$\bar{u}_{\min} = 3/2\,\hat{U}_1 \tag{16}$$

(cf. Fig. 10). This does allow the formation of an output phase voltage system

$$\begin{aligned}u_A^* &= \hat{U}_2^*\cos(\omega_2 t + \varphi_0) \\ u_B^* &= \hat{U}_2^*\cos(\omega_2 t - \tfrac{2\pi}{3} + \varphi_0) \\ u_C^* &= \hat{U}_2^*\cos(\omega_2 t + \tfrac{2\pi}{3} + \varphi_0)\end{aligned} \tag{17}$$

($\varphi_0 = 0$ is selected here for the sake of simplicity what, however, does not restrict the general validity of the analysis) having a maximum fundamental amplitude $\hat{U}_2^*$ of $\sqrt{3}/2\,\hat{U}_1$. Therefore, we have the relation for the voltage transfer ratio M of the matrix converter as also known, e.g. from [2]

$$M = \frac{\hat{U}_2^*}{\hat{U}_1} \le \frac{\sqrt{3}}{2}\,. \tag{18}$$

For given constant output voltage amplitude $\hat{U}_2^*$ and/or given absolute value $|\underline{u}_2^*| = \hat{U}_2^*$ of the output voltage space vector the variation of $\bar{u}$ does make necessary a variation of the inverter modulation index,

$$m_2 = \frac{|\underline{u}_2^*|}{\frac{1}{2}\bar{u}} = \frac{4}{3}\frac{\hat{U}_2^*}{\hat{U}_1}\cos(\omega_1 t)\,. \tag{19}$$

In order to ensure, that the free-wheeling state of the inverter does remain for a minimum time τ_{min} (in $\varphi_2^* = 0...\pi/6$ we have $\tau_{min} = \min(\tau_{(111),ac} + \tau_{(111),ac})$, as required for changing the rectifier switching state at zero DC link current, the modulation index of the inverter and/or the output voltage reference amplitude has to be limited to

$$\hat{U}_2^* \le \frac{\sqrt{3}}{2}\hat{U}_1(1-4\frac{\tau_{\min}}{T_P}) \,. \tag{20}$$

Therefore, the achievable maximum system voltage transfer ratio will be slightly lower than the theoretical maximum $M_{\max} = \sqrt{3}/2$ (cf. Eq.(18)).

For the sake of minimizing the inverter switching losses, in $\varphi_2^* = 0...\pi/6$ only the free-wheeling state (111) is incorporated into the switching state sequence. Accordingly, output phase A remains clamped within the whole interval to the positive DC link bus (cf. Fig.19). The clamping intervals of all phases over an output voltage period can be seen in **Tab.5**. Each output phase remains clamped within a $\pi/3$–wide interval which is arranged symmetrically in time around the maxima and minima of the corresponding phase voltage. Accordingly, minimum switching losses will result for ohmic load.

In case the system is supplying an inductive load, the phase currents and the corresponding phase voltages will show a phase displacement Φ_2,

$$\begin{aligned} i_A &= \hat{I}_2 \cos(\omega_2 t + \Phi_2) \\ i_B &= \hat{I}_2 \cos(\omega_2 t - \tfrac{2\pi}{3} + \Phi_2) \,. \\ i_C &= \hat{I}_2 \cos(\omega_2 t + \tfrac{2\pi}{3} + \Phi_2) \end{aligned} \tag{21}$$

The clamping intervals then should be shifted accordingly in order to maintain low switching losses. E.g., phase A then should be clamped in $\varphi_2 = 0...\pi/3$ (clamping of A to p) and $\varphi_2^* = \pi...4\pi/3$ (clamping of A to n). A detailed analysis of minimum switching loss clamping of DC voltage link inverters has been given in [22]. We therefore would like to omit here a further discussion for the sake of brevity.

In connection with the formation of the input current (cf. Eq.(3)) we still have to prove that the local average $\bar{i}$ of the DC link current i shows a constant value. With Eqs.(7) and (8) we have

$$\bar{i}_{ac} = \tfrac{1}{\tau_{ac}}(i_A\delta_{(100),ac}\tau_{ac} - i_C\delta_{(110),ac}\tau_{ac}) = i_A\delta_{(100)} - i_C\delta_{(110)} \tag{22}$$

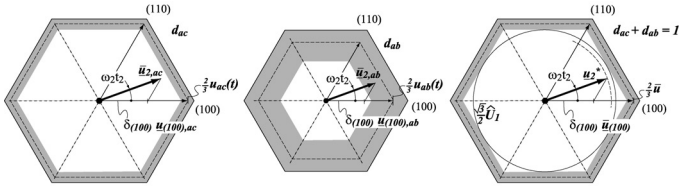
and

$$\bar{i}_{ab} = \tfrac{1}{\tau_{ab}}(i_A\delta_{(100),ab}\tau_{ab} - i_C\delta_{(110),ab}\tau_{ab}) = i_A\delta_{(100)} - i_C\delta_{(110)} \tag{23}$$

Accordingly, in τ_{ac} and τ_{ab} an equal average value

$$\bar{i} = \bar{i}_{ac} = \bar{i}_{ab} = \tfrac{3}{4}m_2\hat{I}_2\cos\Phi_2 = \hat{I}_2\frac{\hat{U}_2^*}{\hat{U}_1}\cos\Phi_2\cos(\omega_1 t) \tag{24}$$

of i is available for input current formation as assumed in Eq.(3). The variation of $\bar{i}$ is inverse to the variation of $\bar{u}$ what does result in a constant local average value of the DC link power flow $\bar{p} = \bar{u}\,\bar{i}$, and or of the power taken from the input and/or supplied to the load.



(a) **(b)** **(c)**

Fig. 10: Inverter output voltage space vectors $\underline{u}_{(100)}$ and $\underline{u}_{(110)}$ and average output voltage vector in τ_{ac} **(a)** and τ_{ab} **(b)** (the range of variation of and u_{ac} and u_{ab} is shown by a dotted area). Furthermore shown: Formation of the inverter output voltage space vector reference value $\underline{u}_2^*$ based on the average value $\bar{u}$ of the DC link voltage u over half a pulse period **(c)**. The minimum value of $\bar{u}$ does define a maximum available inverter output phase voltage amplitude of $\sqrt{3}/2\,\hat{U}_1$.

Analogous to referring the analysis of the formation of the inverter output voltage to the local average value $\bar{u}$ of the DC link voltage, one could give a description of the rectifier input current formation based on the local average value $\bar{i}$ of the DC link current.

There, the variation of $\bar{i}$ results in a variation of the diameter of the hexagon which is defined by the input current space vectors resulting for the different rectifier switching states. For controlling the rectifier according to Eq.(2) the tip of the input current space vector $\underline{\bar{i}}_1$ being formed in the average over a pulse period will move along the side μ of the hexagon (cf. **Fig.11**). In the interval $\varphi_1 = 0...\pi/6$ considered, this results in a variation of the modulation index of the rectifier

$$m_1 = \frac{|\underline{\bar{i}}_1|}{\bar{i}} = \frac{1}{\cos\omega_1 t} \,, \tag{25}$$

i.e. would not lead to a space vector $\underline{\bar{i}}_1$ of constant absolute value $|\underline{\bar{i}}_1|$ and constant angular frequency ω_1 and/or to sinusoidally shaped local average values of the input phase currents for a constant value of $\bar{i}$. However, due to the variation of $\bar{i}$ according to Eq.(24) the hexagon diameter does change such that the tip of $\underline{\bar{i}}_1$ actually does move along a circular trajectory and/or sinusoidal local average values of the input phase currents are generated,

$$\begin{aligned} \bar{i}_a &= \hat{I}_1\cos(\omega_1 t) \\ \bar{i}_b &= \hat{I}_1\cos(\omega_1 t - \tfrac{2\pi}{3}) \\ \bar{i}_c &= \hat{I}_1\cos(\omega_1 t + \tfrac{2\pi}{3}) \end{aligned} \tag{26}$$

This can be verified immediately by combining Eqs.(24) and (25)

$$|\underline{\bar{i}}_1| = \bar{i}\,m_1 = \hat{I}_2\frac{\hat{U}_2^*}{\hat{U}_1}\cos\Phi_2\cos(\omega_1 t)\frac{1}{\cos\omega_1 t} = \hat{I}_1 \,. \tag{27}$$

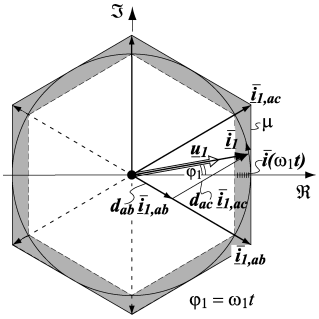


Fig.11: Rectifier input current space vectors resulting in the average over a pulse half period and trajectory of the space vector $\underline{\bar{i}}_1$ within the input voltage fundamental. The diameter of the space vector hexagon is determined by the local DC link current average value $\bar{i}$ varying over the fundamental period. The considerations are limited to $\varphi_1 = 0...\pi/6$. The range of variation of the hexagon is shown by a dotted area.

$\varphi_2 = \omega_2 t$	u_A	u_B	u_C
0 ... $\pi/6$	u_p	u_p, u_n	u_p, u_n
$\pi/6$ ... $\pi/2$	u_p, u_n	u_p, u_n	u_n
$\pi/2$ ... $5\pi/6$	u_p, u_n	u_p	u_p, u_n
$5\pi/6$ ... $7\pi/6$	u_n	u_p, u_n	u_p, u_n
$7\pi/6$ ... $3\pi/2$	u_n, u_p	u_p, u_n	u_p
$3\pi/2$ ... $11\pi/6$	u_n, u_p	u_n	u_p, u_n
$11\pi/6$ ... 0	u_p	u_n, u_p	u_p, u_n

TABLE 5. Intervals of an output voltage period, and corresponding potentials of the inverter output phases; clamping of an output phase to the positive DC bus p (potential u_p) or to the negative DC bus n (potential u_n) is pointed out by a dotted area.

As is clear form Fig. 9, the inverter switching frequency is two times the rectifier switching frequency,

$$f_{P,1} = 2f_{P,2} \,, \tag{28}$$

as a full switching cycle of the inverter is contained in each rectifier pulse half interval. Basically, also a different ratio of the pulse frequency could be selected as long as it is ensured that the commutation of the rectifier stage is at zero DC link current, i.e. is placed in the inverter free-wheeling interval.

V. Operating Range of SMC, VSMC and USMC

In the following we will briefly show which space vectors are available for output voltage and input current formation for the SMC, VSMC and USMC and/or which restrictions of the operating range have to be accepted in consequence of a simplification of the circuit structure.

A. Admissible Converter Switching States

A.1 SMC and VSMC

For space vector description of input voltage and input current we have for the instantaneous active power supplied to the DC link

$$p = \tfrac{3}{2}\Re\{\underline{u}_1^* \underline{i}_1(n)\} = u\, i \tag{29}$$

($\underline{u}_1^*$ does denote the complex conjugate of $\underline{u}_1$). The DC link current i as impressed by the inverter does define the absolute value of the input current space vectors $\underline{i}_1(n)$ resulting for the different rectifier switching states n. The voltage $u(n)$ occurring at the rectifier output then can be determined with reference to Eq.(29) by projection of the current space vectors along the input voltage space vector $\underline{u}_1$ (cf. **Fig.12**(a), [18]). The condition $u(n)>0$ there is met only by such switching states for which the corresponding current space vector shows a component in the direction of $\underline{u}_1$ and/or is located in the half-plane defined by the direction of $\underline{u}_1$. Therefore, three switching states are not available as they would result in a negative DC link voltage.

If now i does change its sign what could be achieved by inverting the switching state of the output stage, e.g., by changing form (100) to (011), such switching states and/or current space vectors $\underline{i}_1(n)$ are admissible which do result negative DC link power, $p<0$, i.e. do show a negative projection onto $\underline{u}_1$. As by changing the sign of i also the current space vectors are inverted, such switching states are identical to admissible switching states for $i>0$. In summary, all current space vectors available for the CMC can be formed also by the SMC or VSMC despite always only three out of six active rectifier switching states are employed (cf. also Tab.3, lines 37 - 72).

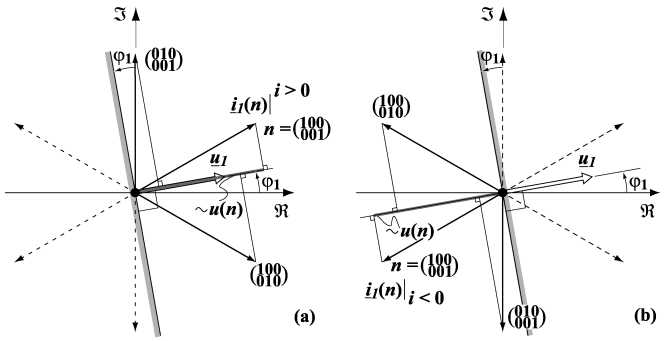


Fig.12: Input current space vectors and/or rectifier switching states admissible for a given angular position φ_1 of the input voltage space vector $\underline{u}_1$. Current space vectors not available are shown by broken lines. The rectifier switching states n are denoted by a combination of transistors switching functions in matrix form, where each row does characterize the switching state of a bridge leg. **(a):** DC link current $i>0$, **(b):** DC link current $i < 0$.

A.2 USMC

For the USMC besides the restriction $u>0$ according to the unidirectional connection of the input stage bridge legs to the DC bus also $i > 0$ has to be guaranteed. Therefore, as shown in Section A.1 for the formation of the input current only three space vectors are available which are defined by the instantaneous angular position of $\underline{u}_1$ (cf. Fig. 12(a)). As can be seen immediately, therefore, the phase displacement of the input current fundamental $\bar{\underline{i}}_1$ and of the input voltage $\underline{u}_1$ is limited to

$$\Phi_1 \in (-\tfrac{\pi}{6}, +\tfrac{\pi}{6}) . \tag{30}$$

For the formation of an input current of higher phase displacement current space vectors would not be continuously available over the fundamental period. However, this restriction is of low importance as in most cases ohmic mains behavior will be required and Eq.(30) will allow a compensation of the capacitive reactive power of the input filter capacitors at rated load.

However, as will be shown in the following, by $i > 0$ also the admissible load power factor is restricted. We have for the inverter stage in analogy to Eq.(29)

$$p = \tfrac{3}{2}\Re\{\underline{u}_2^*(m)\, \underline{i}_2\} = u\, i \tag{31}$$

where $\underline{u}_2^*(m)$ does denote the complex conjugate of the output voltage space vector being present for a switching state m. In order to ensure $i(m)>0$, only output voltage space vectors and/or switching states m are admissible which are located in the half-plane defined by the output current space vector $\underline{i}_2$ (cf. **Fig.13**). We therefore have for the output stage analogous to the input stage the requirement

$$\Phi_2 \in (-\tfrac{\pi}{6}, +\tfrac{\pi}{6}) \tag{32}$$

(cf. **Fig.14**). For supplying heavily inductive loads this limitation could be satisfied by compensating capacitors.

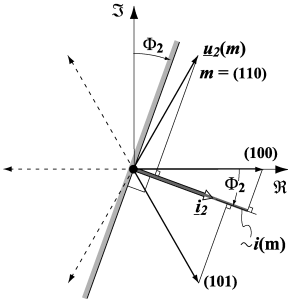


Fig.13: Output voltage space vectors and/or inverter switching states admissible for the USMC for a given angular position $\varphi_2^*+\Phi_2$ of the output current space vector $\underline{i}_2$. Voltage space vectors not available are shown by broken lines. The inverter switching states m are denoted by the combination of the bridge leg switching functions.

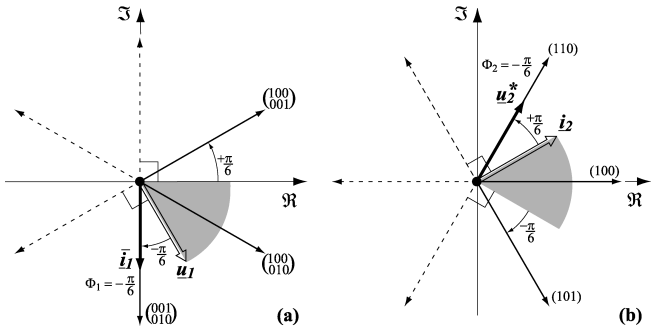


Fig.14: Input current space vectors **(a)** and output voltage space vectors **(b)** available for the USMC for $u_a>0$, u_b, $u_c<0$ (corresponding angular interval of $\underline{u}_1$ pointed out by a dotted area) and $i_a>0$, i_b, $i_c<0$ (corresponding angular interval of $\underline{i}_2$ pointed out by a dotted area). Only current space vectors showing a phase displacement Φ_2 of less than $\pi/6$ to the input voltage can be formed; furthermore, the voltage space vectors $\underline{u}_2^*$ to be formed at the output have to remain within $\pm\pi/6$ phase displacement to the output current $\underline{i}_2$ in order not to generate a negative DC link current.

B. Voltage and Current Transfer Ratio

With reference to Eqs.(19), (24), and (25) we have for the amplitude of the input current fundamental

$$\hat{I}_1 = m_1 \bar{i} = \tfrac{3}{4} m_1 m_2 \hat{I}_2 \cos\Phi_2 \tag{33}$$

and accordingly for the current amplitude transfer ratio of the matrix converter

$$\frac{\hat{I}_1}{\hat{I}_2} = \tfrac{3}{4} m_1 m_2 \cos\Phi_2 \,. \tag{34}$$

Considering the input and output power balance

$$\tfrac{3}{2}\hat{U}_1\hat{I}_1 = \bar{u}\,\bar{i} = \tfrac{3}{2}\hat{U}_2^*\hat{I}_2 \cos\Phi_2 \,, \tag{35}$$

where losses are neglected and $\cos\Phi_1 = 1$ is assumed, there follows for the voltage amplitude transfer ratio

$$\frac{\hat{U}_2^*}{\hat{U}_1} = \frac{\hat{I}_1}{\hat{I}_2}\frac{1}{\cos\Phi_2} = \tfrac{3}{4} m_1 m_2 \,. \tag{36}$$

Voltage and current transfer of the system therefore are characterized by a transfer ratio

$$M = \tfrac{3}{4} m_1 m_2 \tag{37}$$

where $M \in (0, \sqrt{3}/2)$; introducing Eq.(37) into Eqs.(34) and (36) there follows

$$\begin{aligned} \hat{U}_2^* &= M\,\hat{U}_1 \\ \hat{I}_1 &= M\hat{I}_2 \cos\Phi_2 \end{aligned} \tag{38}$$

(cf. Eq.(18)).

The basic function of the system concerning the conversion of voltage and current can be shown with reference to the amplitudes $\hat{U}_1$, $\hat{U}_2$ of the input voltage and of the output reference voltage and the amplitudes $\hat{I}_1$, $\hat{I}_2$ of the input current fundamental and the output current (phase difference $\cos\Phi_2$) as depicted in **Fig.15.**

In case a phase difference Φ_1 of input current and voltage would be set by proper control of the input stage we would have

$$\begin{aligned} \hat{U}_2^* &= M\,\hat{U}_1 \cos\Phi_1 \\ \hat{I}_1 &= M\hat{I}_2 \cos\Phi_2 \end{aligned} \tag{39}$$

It is important to point out that therefore the maximum voltage transfer ratio $(\hat{U}_2^*/\hat{U}_1)_{\max} = \sqrt{3}/2$ is only available for $\cos\Phi_1 = 1$.

Another interesting property of the matrix converter is that the formation of an output voltage, i.e. $\hat{U}_2^*/\hat{U}_1 \neq 0$ is not connected to the formation of an input current fundamental, i.e. $\hat{I}_1/\hat{I}_2 = 0$ could be valid. This can be explained by the fact that only active power is transferred via the DC link, accordingly, for a fundamental displacement factor of the output current of $\cos\Phi_2 = 0$ in the average of a pulse period no current flow does occur in the DC link, i.e. $\bar{i} = 0$, where a finite value of $\bar{i}$ is a requirement for the formation of an input current.

On the other hand, $\hat{U}_2^*/\hat{U}_1 = 0$ is possible for $\hat{I}_1/\hat{I}_2 \neq 0$ in case the control of the input stage is according to $\cos\Phi_1 = 0$ where the segments of the line-to-line input voltages occurring at the rectifier output do not form a local average value $\bar{u}$ of the DC link voltage and therefore no voltage is available for a formation of an output voltage fundamental, i.e. $\hat{U}_2^* = 0$.

Furthermore, we would like to note that input and output side are basically decoupled concerning the formation of fundamental reactive power, however, the generation of reactive power at the input side is possible only in case active power is transferred to the output, i.e. for $\bar{i} \neq 0$ and could be limited by the required voltage transfer ratio. Based on Eqs.(37) and (39) there follows for the maximum admissible phase displacement

$$\cos\Phi_{1,\max} = \tfrac{2}{\sqrt{3}} M \qquad M \le \sqrt{3}/2 \tag{40}$$

and/or

$$\Phi_1 \le \arccos(\tfrac{2}{\sqrt{3}} M) \,. \tag{41}$$

Accordingly, with reference to

$$Q_1^2 = (\tfrac{3}{2}\hat{U}_1\hat{I}_1)^2 - P^2 \tag{42}$$

where P denotes the active power, we have for the maximum fundamental reactive power Q_1 which could be generated at the input

$$Q_{1,\max} = P\sqrt{\frac{3}{4M^2} - 1} \,. \tag{43}$$

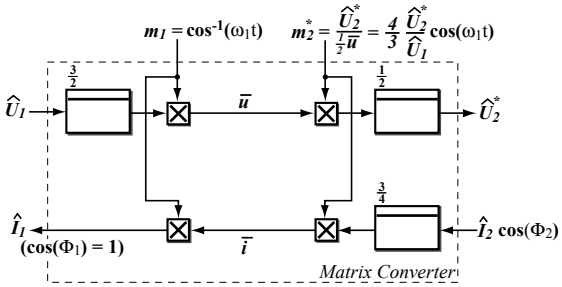


Fig. 15: Voltage and current transfer of a matrix converter shown with reference to the amplitudes of the fundamentals of the input and output voltages and currents.

VI. GUIDELINES FOR DIMENSIONING OF THE SMC, VSMC AND USMC

In the following analytical formulae for the current stresses on the power semiconductors will be derived. There, the basic idea is to define an average modulation index of the output stage and/or a global average value $\bar{U}$ of the DC link voltage. Thereby, the matrix converter is transferred into a constant DC link voltage system and the relation of input and output frequency is not longer of importance. Considering the limited range of variation of the local average value $\bar{u}$ of the DC link voltage (cf. Fig. 8) we could expect a sufficiently accurate approximation of the actual circuit behavior despite this drastic simplification.

The current stresses will be given for $\Phi_2 \in (0...\pi/2)$. Based on this, stresses on the components occurring for other phase displacement values can be determined by symmetry considerations.

A. Global Average Modulation

Based on Eq.(15) we have for the global average value of the DC link voltage

$$\bar{U} = \tfrac{9}{\pi}\ln(\sqrt{3})\hat{U}_1 \,. \tag{44}$$

As is immediately clear, the current stress on the input stage power semiconductors is determined by the DC link current average and rms value. We therefore will calculate the characteristic DC link current values in the following.

Corresponding to Eq.(24), the global average value of the DC link current results in

$$\bar{I} = \tfrac{3}{4} M_2 \hat{I}_2 \cos\Phi_2 \tag{45}$$

(output current ripple neglected) where

$$M_2 = \frac{\bar{U}_2}{\frac{1}{2}\bar{U}} \tag{46}$$

does define a global average modulation index. With reference to [23] we furthermore have for the global rms value of the DC link current

$$I_{rms}{}^2 = \frac{\sqrt{3}}{\pi} M_2 \hat{I}_2{}^2 (\tfrac{1}{4} + \cos^2 \Phi_2) \,. \tag{47}$$

The DC link current i is determined by the output phase currents and by the inverter switching state and/or switching functions

$$i = i_A s_A + i_B s_B + i_C s_C \,. \tag{48}$$

In the angle interval $\varphi_2 = \omega_2 t = 0...\pi/3$ the active switching states $s_{ABC} = (100)$ and (110) are employed where the DC link current is

$$i = \begin{cases} +i_A & \text{for} \quad s_{ABC} = (100) \\ i_A + i_B = -i_C & \text{for} \quad s_{ABC} = (110). \end{cases} \tag{49}$$

Accordingly, for $\Phi_2 = \pi/6...\pi/2$ the DC link current i will show a negative component due to $i_A < 0$ for $\varphi_2 \in (\pi/2 - \Phi_2 ... \pi/3)$ (cf. Eq.(21)) in the interval $\varphi_2 = 0...\pi/3$ which is considered in the following. The sign of i is of importance for splitting the DC link current to the respective power semiconductors of the input stage which are denominated as given in **Fig.16.**

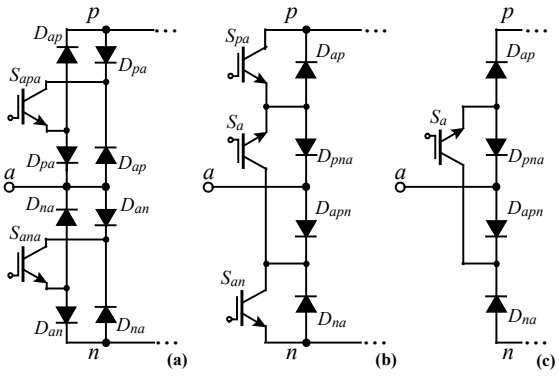


Fig.16: Structure of a bridge leg of the VSMC **(a)**, SMC **(b)** and USMC **(c)** and denomination of the diodes and power transistors. Identical denomination of components for the different bridge leg topologies does indicate an equal current stress, e.g. the average and rms current stress of diode D_{pa} of the VSMC is identical to the current stress on diode D_{pa} of the USMC.

A.1 Global DC Link Current Average Value

All findings described in the following are shown in graphical form in **Fig. 17**.

A.1.1 PHASE DISPLACEMENT $\Phi_2 \in (0...\pi/6)$

For $\Phi_2 \in (0...\pi/6)$ the DC link current is comprised of only positive components and/or output current segments, i.e. we have within the whole pulse period $i > 0$, accordingly

$$\bar{I}_+ = \bar{I} \;\text{ and }\; \bar{I}_- = 0 \tag{50}$$

is valid ($\bar{I}_+$ does denote the global average value of the positive components i_+ of i, i_- does denote the negative components). Due to $i>0$ the diodes D_{ap} will not be involved in the current conduction.

A.1.2 PHASE DISPLACEMENT $\Phi_2 \in (\pi/6...\pi/2)$

For the global average value of the positive DC link current component i_+ which is carried by the diodes D_{ap} we have

$$\begin{aligned} \bar{I}_+ &= \tfrac{3}{\pi}\Big[\int_0^{\pi/3} (-i_C)\delta_{(110)} d\varphi_2 + \int_0^{\pi/2-\Phi_2} i_A \delta_{(100)} d\varphi_2\Big] = \\ &= \tfrac{3}{4} M_2 \hat{I}_2 [\cos\Phi_2 + \tfrac{\sqrt{3}}{\pi}((\tfrac{\pi}{6} - \Phi_2)\sin(\tfrac{\pi}{3} + \Phi_2) + \sin(\Phi_2 - \tfrac{\pi}{6}))] \end{aligned} \tag{51}$$

and for the global average value of the negative component i_- (cf. Fig. 16)

$$\begin{aligned} \bar{I}_- &= \tfrac{3}{\pi} \int_{\pi/2-\Phi_2}^{\pi/3} (-i_A)\delta_{(100)} d\varphi_2 = \\ &= \tfrac{3\sqrt{3}}{4\pi} M_2 \hat{I}_2 [(\tfrac{\pi}{6} + \sqrt{3} - \Phi_2)\sin(\Phi_2 + \tfrac{\pi}{3}) - 2\cos\Phi_2] \end{aligned} \tag{52}$$

where

$$\bar{I} = \bar{I}_+ - \bar{I}_- \tag{53}$$

is valid.

A.2 Global DC Link Current RMS Value

A.2.1 PHASE DISPLACEMENT $\Phi_2 \in (0...\pi/6)$

As is immediately clear from the considerations in Section VI.A.1.1 we have for the global rms value of the DC link current components

$$I_{rms}{}^2 = I_{+,rms}{}^2 \tag{54}$$

and

$$I_{-,rms}{}^2 = 0 \tag{55}$$

A.2.2 PHASE DISPLACEMENT $\Phi_2 \in (\pi/6...\pi/2)$

In analogy to Section VI.A.2.1 we have

$$\begin{aligned} I_{+,rms}{}^2 &= \tfrac{3}{\pi}\Big[\int_0^{\pi/3} i_C{}^2 \delta_{(110)} d\varphi_2 + \int_0^{\pi/2-\Phi_2} i_A{}^2 \delta_{(100)} d\varphi_2\Big] = \\ &= \tfrac{\sqrt{3}}{\pi} M_2 \hat{I}_2{}^2 [\sin(\Phi_2 + \tfrac{\pi}{3}) - \tfrac{\sqrt{3}}{4}\sin(2\Phi_2 - \tfrac{\pi}{3})] \end{aligned} \tag{56}$$

$$\begin{aligned} I_{-,rms}{}^2 &= \tfrac{3}{\pi} \int_{\pi/2-\Phi_2}^{\pi/3} i_A{}^2 \delta_{(100)} d\varphi_2 = \\ &= \tfrac{\sqrt{3}}{\pi} M_2 \hat{I}_2{}^2 [\tfrac{3}{4} + \tfrac{1}{4}\sin(2\Phi_2 + \tfrac{\pi}{6}) - \sin(\Phi_2 + \tfrac{\pi}{3})] \end{aligned} \tag{57}$$

where

$$I_{rms}{}^2 = I_{+,rms}{}^2 + I_{-,rms}{}^2 \tag{58}$$

is valid due to the fact that i_+ and i_- do not overlap in time.

B. Stresses on the Components of the Output Stage

As given in [23] we have for the current stresses on the output stage power transistors and diodes

$$\begin{aligned} \bar{I}_{SA} &= \tfrac{1}{2}\hat{I}_2(\tfrac{1}{\pi} + \tfrac{1}{4} M_2 \cos\Phi_2) \\ \bar{I}_{DA} &= \tfrac{1}{2}\hat{I}_2(\tfrac{1}{\pi} - \tfrac{1}{4} M_2 \cos\Phi_2) \\ I_{SA,rms}{}^2 &= \hat{I}_2{}^2(\tfrac{1}{8} + \tfrac{1}{3\pi} M_2 \cos\Phi_2) \\ I_{DA,rms}{}^2 &= \hat{I}_2{}^2(\tfrac{1}{8} - \tfrac{1}{3\pi} M_2 \cos\Phi_2). \end{aligned} \tag{59}$$

C. Stresses on the Power Semiconductors of the Input Stage

C.1 Phase Displacement $\Phi_2 \in (0...\pi/6)$

C.1.1 CURRENT AVERAGE VALUES

Due to the symmetric average distribution of the DC link current i to the rectifier bridge legs we have

$$\begin{aligned} \bar{I}_{Dap} &= \tfrac{1}{3}\bar{I} = \tfrac{1}{4} M_2 \hat{I}_2 \cos\Phi_2 \\ \bar{I}_{Sapa} &= \bar{I}_{Dpna} = \bar{I}_{ap} \\ \bar{I}_{Sa} &= 2\bar{I}_{Dap}. \end{aligned} \tag{60}$$

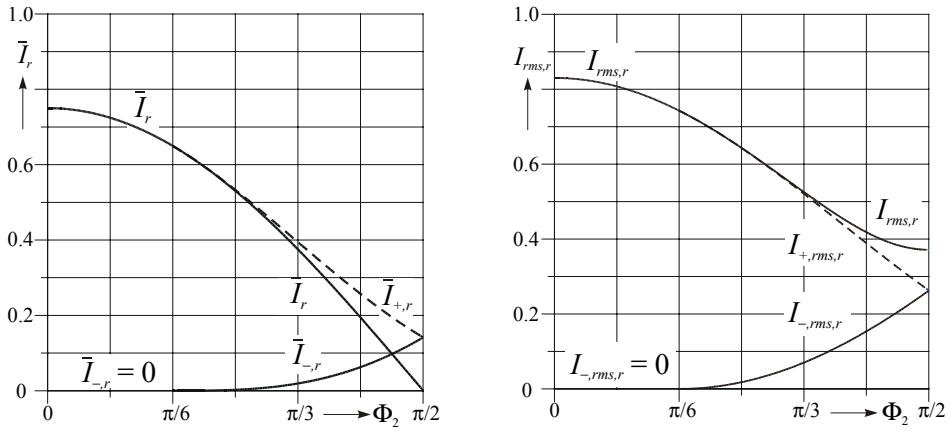


Fig. 17: Graphical representation of the normalized (index *r*) dependency of **(a):** the global average value of the DC link current *i* and of the current components i_+ and i_- (cf. Section VI.A.1) on the output current phase displacement Φ_2; normalization basis: $M_2\hat{I}_2$; and **(b):** the global rms value of the DC link current *i* and of the current components i_+ and i_- (cf. Section VI.A.2) on the output current phase displacement Φ_2; normalization basis $\sqrt{M_2\hat{I}_2}$.

According to $i>0$ the diodes D_{pa}, D_{an} and the switches S_{pa}, S_{an} do not participate in the current conduction, i.e. $i_{Dpa} = i_{Spa} = 0$ and/or

$$\bar{I}_{Dpa} = \bar{I}_{Spa} = 0 . \tag{61}$$

is valid.

C.1.2 CURRENT RMS VALUES

In analogy to Section VI.C.1.1 we have

$$\begin{aligned} I_{Dap,rms}{}^2 &= \tfrac{1}{3} I_{rms}{}^2 = \tfrac{1}{\sqrt{3}\pi} M_2 \hat{I}_2{}^2 (\tfrac{1}{4} + \cos^2 \Phi_2) \\ I_{Sapa,rms}{}^2 &= I_{Dpna,rms}{}^2 = I_{Dap,rms}{}^2 \\ I_{Sa,rms}{}^2 &= 2 I_{Dap,rms}{}^2 \end{aligned} \tag{62}$$

and

$$I_{Dpa,rms} = I_{Spa,rms} = 0 . \tag{63}$$

C.2 Phase Displacement $\Phi_2 \in (\pi/6...\pi/2)$

C.2.1 CURRENT AVERAGE VALUES

Positive components i_+ of *i* are carried by diodes D_{ap}, negative components i_- of *i* are taken over by diodes D_{pa}. Accordingly, there results for the global average current stress on the devices

$$\begin{aligned} \bar{I}_{Dap} &= \tfrac{1}{3}\bar{I}_+ = \\ &= \tfrac{1}{4} M_2 \hat{I}_2 [\cos\Phi_2 + \tfrac{\sqrt{3}}{\pi}((\tfrac{\pi}{6} - \Phi_2)\sin(\tfrac{\pi}{3} + \Phi_2) + \sin(\Phi_2 - \tfrac{\pi}{6}))] \\ \bar{I}_{Dpa} &= \tfrac{1}{3}\bar{I}_- = \tfrac{\sqrt{3}}{4\pi} M_2 \hat{I}_2 [(\tfrac{\pi}{6} + \sqrt{3} - \Phi_2)\sin(\Phi_2 + \tfrac{\pi}{3}) - 2\cos\Phi_2] \\ \bar{I}_{Sapa} &= \bar{I}_{Dpna} = (\bar{I}_{Dap} + \bar{I}_{Dpa}) \\ \bar{I}_{Sa} &= 2\bar{I}_{Dap} \\ \bar{I}_{Spa} &= \bar{I}_{Dpa} \end{aligned} \tag{64}$$

C.2.2 CURRENT RMS VALUES

In analogy to Section VI.C.2.1 we have

$$\begin{aligned} I_{Dap,rms}{}^2 &= \tfrac{1}{3} I_{+,rms}{}^2 = \tfrac{1}{\sqrt{3}\pi} M_2 \hat{I}_2{}^2 [\sin(\Phi_2 + \tfrac{\pi}{3}) - \tfrac{\sqrt{3}}{4}\sin(2\Phi_2 - \tfrac{\pi}{3})] \\ I_{Dpa,rms}{}^2 &= \tfrac{1}{3} \bar{I}_{-,rms} = \tfrac{1}{\sqrt{3}\pi} M_2 \hat{I}_2{}^2 [\tfrac{3}{4} + \tfrac{1}{4}\sin(2\Phi_2 + \tfrac{\pi}{6}) - \sin(\Phi_2 + \tfrac{\pi}{3})] \\ I_{Sapa,rms}{}^2 &= (I_{Dap,rms}{}^2 + I_{Dpa,rms}{}^2) = \tfrac{1}{3} I_{rms}{}^2 = \tfrac{\sqrt{3}}{\pi} M_2 \hat{I}_2{}^2 (\tfrac{1}{4} + \cos^2 \Phi_2) \\ I_{Spa,rms}{}^2 &= I_{Dpa,rms}{}^2 \\ I_{Sa,rms}{}^2 &= I_{Dpa,rms}{}^2 . \end{aligned} \tag{65}$$

D. Comparison to Digital Simulation

The analytical expressions given in Sections VI.C and VI.D have been verified with excellent consistency by digital simulations (cf. Section VII.) irrespective of the relation of input and output frequency, output stage modulation index and output current phase displacement. The simulation results are compiled in **Fig. 18** where results of the analytical approximation are shown in brackets.

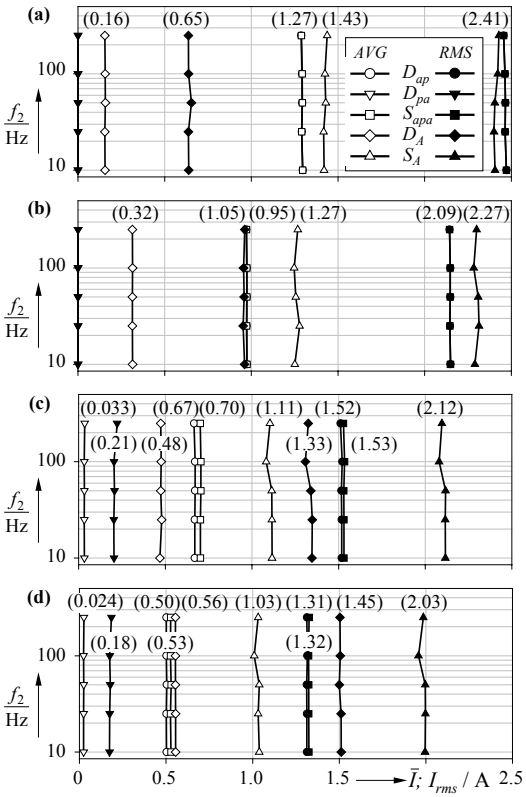


Fig.18: Average and rms current stresses on the power semiconductors as determined by simulations and analytical approximations (shown in brackets): Modulation index $M = 0.8$ in **(a)**, **(c)** and $M = 0.6$ in **(b)**, **(d)**; output phase displacement $\Phi_2 = 0$ in **(a)**, **(b)** and $\Phi_2 = \pi/3$ in **(c)**, **(d).** Input frequency $f_1 = 50$ Hz; amplitude of the output current fundamental $\hat{I}_2 = 5$ A, input line-to-line voltage $U_{1,l\text{-}l} = 400$ V.