Optimal Design of a Two-Winding Inductor Bouncer Circuit

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***Abstract*—In many pulsed-power applications, the flatness of the output pulse is an important characteristic to enable proper system operation, whereas a pulse flatness within less than a few percent has to be achieved. In power modulators based on capacitor discharge, this voltage droop is mainly defined by the input capacitance. In order to overcome this problem, in power modulator systems, compensation circuits are added, whereby in spite of a smaller storage capacitor, a flat pulse top is achieved. Depending on the pulse duration, different approaches for voltage droop compensation exist. For short pulse durations, in the range of several microseconds, only passive solutions or bouncer circuits are applicable. In this paper, the design and optimization of a two-winding inductor bouncer circuit are presented in order to achieve an output voltage droop of less than 1%. Due to the realized galvanic isolation, a new degree of freedom is obtained, which allows an adaptation of the bouncer circuit's voltage and current ratings to standard semiconductor switches. With an optimal design of the two-winding inductor bouncer circuit for the existing system, the volume of the input capacitor is reduced by a factor of 10.5, and the stored energy is decreased by a factor of 24 compared to a system without a bouncer circuit.**

***Index Terms*—Compensation circuit, pulse transformer, solid state modulator.**

I. Introduction

In MANY pulsed-power applications, like driving klystrons, the flatness of the output pulse is an important characteristic to enable proper system operation. Often, a pulse flatness within less than a few percent has to be achieved. In power modulators based on capacitor discharge, for example, as shown in Fig. 1, this results in a relatively large capacitor bank. There, the voltage droop is mainly defined by the input capacitance C_{in}, the pulse duration, and the output power. In the considered application, with the specifications given in Table I, where the voltage droop Δ is limited to less than 1% due to the proper operation of the klystron, the stored energy E_{Cin} in the input capacitor C_{in} would exceed the pulse energy E_p by more than 50 times in order to guarantee the specifications

$$\frac{E_p}{E_{\mathrm{Cin}}} = \frac{\frac{1}{2}C_{\mathrm{in}}\left(V_{\mathrm{Cin}}^2 - (1-\Delta)V_{\mathrm{Cin}}^2\right)}{\frac{1}{2}C_{\mathrm{in}}V_{\mathrm{Cin}}^2} = \frac{1}{2\Delta+\Delta^2}. \quad (1)$$

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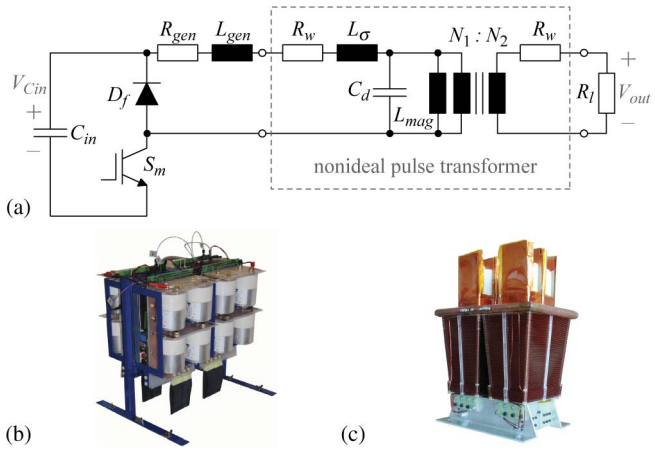

Fig. 1. (a) Schematic of the transformer-based 20-MW 5-μs solid-state power modulator without any droop compensation. (b) Pictures of the realized pulse generator unit with four parallel-connected IGBT modules. (c) Step-up pulse transformer.

TABLE I
Specifications of the Realized Klystron Power Modulator

DC link voltage V_{Cin0}	1000 V
Output voltage V_{out}	170 kV
Pulse duration T_p	5 µs
Peak output power P_{out}	20 MW
Repetition frequency f_{rep}	200 Hz
Output voltage droop Δ	$< 1\,\%$
Turns ratio N_1:N_2	1 : 170

Therefore, on the one hand, the capacitor bank will get bulky and expensive, and on the other hand, a lot of energy is stored in the system, which could be a problem concerning safety aspects during a system fault. Furthermore, in the case of a transformer-based power modulator (cf. Fig. 1), the magnetizing inductance L_{mag}, the leakage inductance L_σ, the distributed capacitance C_d, and the winding resistances R_w of the pulse transformer, as well as other parasitic components, like the pulse generator's internal resistance R_{gen} or inductance L_{gen}, lead to an additional voltage droop [1].

In order to overcome the problem of a large storage capacitor, compensation circuits are used, which enable a flat pulse top in spite of a small storage capacitor. Depending on the pulse duration, different approaches for droop compensation exist. For long-pulse modulators based on multistage modulators, like Marx generators, the voltage droop can be incrementally corrected by successively turning on additional stages during the pulse [2], [3]. Another possibility is to add a switched-mode

power supply to the modulator, which compensates the voltage droop [4]. Due to the high resulting switching frequency for pulse durations in the range of a few microseconds, switched-mode compensation circuits are not suitable due to the high switching losses. Therefore, usually, passive solutions or bouncer circuits are applied. The LR network is the simplest way to compensate the voltage droop, but the additional losses can become significant [1], [5] so that this circuit is not very attractive.

Alternatively, with a resonant LC bouncer circuit, a pulse flatness within $\pm 0.5\%$ over several microseconds to milliseconds can be achieved [2], [6], [7]. The bouncer produces an almost linearly decreasing voltage and compensates the approximately linear voltage droop of the storage capacitor. However, usually, the bouncer is connected in series to the main pulse generation unit, and through the resonant bouncer flows a current higher than the nominal pulse current. Additionally, for transformer-based power modulators, where a low primary voltage is used (cf. Table I, $V_{\mathrm{Cin}} = 1$ kV), the voltage across the bouncer switch is not adequate for existing semiconductors. Even if the bouncer circuit is placed on the secondary of a transformer, the voltage droop, which has to be compensated, would not be suitable for modern power semiconductors as it is in the range of several kilovolts.

Therefore, a two-winding inductor bouncer circuit is presented in this paper, which allows an adaptation of the bouncer circuit's voltage and current ratings to standard semiconductor switches, like IGBT modules for traction applications.

First, in Section II, the functionality of the conventional bouncer circuit is explained in detail, which is the basis for the new two-winding inductor bouncer circuit. In the new bouncer circuit, the galvanic isolation results in a new degree of freedom, which enables an optimal design of the bouncer circuit with respect to voltage and current ratings of the semiconductors. In Section III, a mathematical description of the two-winding inductor bouncer circuit is derived, and based on these equations, the two-winding inductor bouncer circuit is designed and optimized for the given modulator specifications in Section IV. In the optimization, the bouncer circuit is designed regarding a minimum overall volume of the power modulator system. However, with the presented procedure, an optimization also concerning other criteria, like losses or stored energy, is possible.

Based on the optimization procedure, a bouncer circuit is designed, and in Section V, simulation results are presented, validating the design, which results in a more than ten times smaller volume and 24 times less stored energy. There, the influence and dependence also of parameter tolerances, as well as of additional system parasitics, are considered.

II. Operation of Bouncer Circuit

The conventional LC bouncer circuit, as shown in Fig. 2(a), consists of capacitor C_c, which has to be charged to the voltage V_{Cc0} before a pulse is generated, inductor L_c, and switch S_b. The bouncer circuit is either directly connected in series to the load R_l or to the primary winding of the pulse transformer. Therefore, during the pulse duration T_p, when both switches

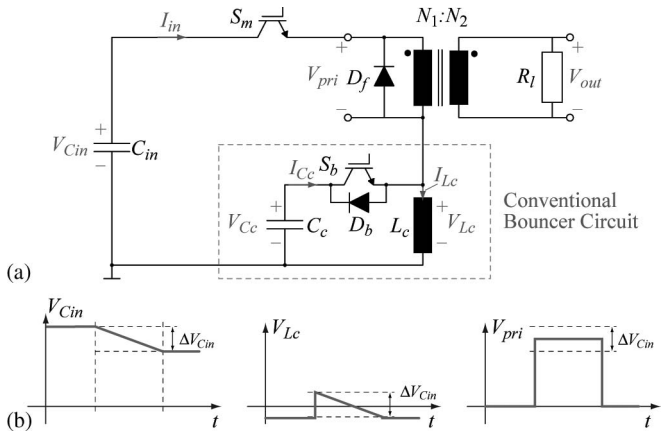

Fig. 2. (a) Series connection of the transformer-based power modulator with the conventional bouncer circuit. (b) Voltages V_{Cin} and V_{Lc} (equal to V_{Cc} when S_b is closed) to achieve a constant output voltage $V_{\mathrm{out}} = (N_2/N_1)V_{\mathrm{pri}}$.

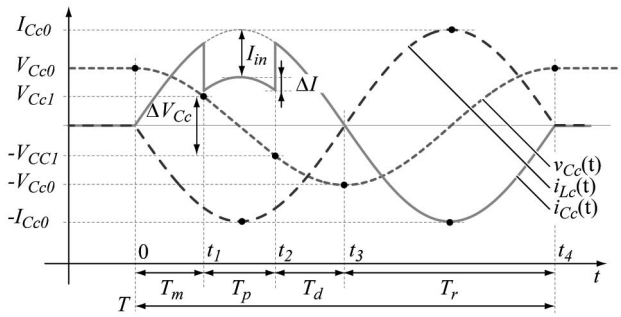

Fig. 3. Waveforms of the bouncer voltage v_{Cc}, the capacitor current i_{Cc}, and the inductor current i_{Lc} during one period T.

S_m and S_b are turned on and voltage drops across any parasitics or the switches are neglected, the output voltage is equal to the difference of the input voltage $v_{\mathrm{Cin}}(t)$ and the voltage at the bouncer capacitor $v_{Cc}(t)$. Consequently, the input voltage droop ΔV_{Cin} has to be the same as the voltage droop of the bouncer capacitor C_c [cf. Fig. 2(b)] so that the difference and, therewith, the output voltage V_{out} is constant.

The voltage droop at the bouncer capacitor C_c is generated by the current $i_{Lc}(t)$ and the load current I_{in} referred to the primary. In order to obtain an equal voltage droop at C_{in} and C_c, a current

$$i_{Lc}(t) = i_{\mathrm{in}}(t) + i_{Cc}(t) \tag{2}$$

which is equal to the sum of the load current $i_{\mathrm{in}}(t)$ and the bouncer current $i_{Cc}(t)$, has to be built up in the inductor L_c before the main pulse is generated. The current $i_{Lc}(t)$ is built up by closing switch S_b during the magnetizing interval T_m before the main pulse, i.e., S_m is open. With S_b closed, an LC oscillation with sinusoidal currents and voltages is started [cf. Figs. 3 and 4(a)]. As soon as the current in the inductor L_c exceeds a defined value or the bouncer capacitor C_c is discharged to a voltage V_{Cc1}, the main pulse is generated by closing switch S_m at t_1. According to Kirchhoff's current law, during the pulse interval T_p, an almost constant pulse current I_{in} starts to flow through the bouncer inductor L_c, whereas the current $i_{Cc}(t)$ immediately decreases by the same amplitude I_{in} [cf. Fig. 4(b)]. Consequently, also the rate of discharge of the

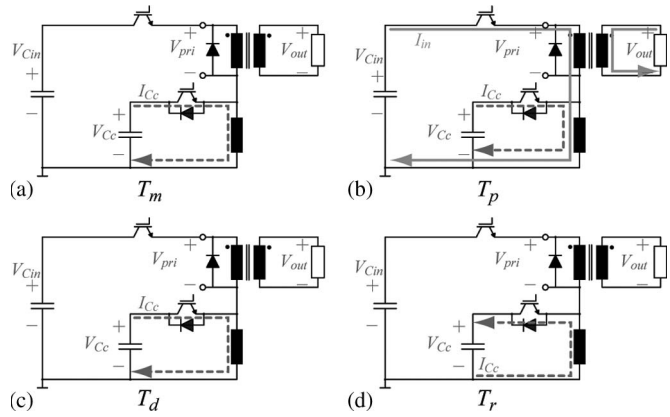

Fig. 4. Voltages and current paths during (a) the magnetizing interval T_m (S_m off, S_b on), (b) the pulse interval T_p (S_m and S_b on), (c) the demagnetizing interval T_d (S_m off, S_b on), and (d) the recovery interval T_r (S_b and S_m off).

bouncer capacitor C_c is decreased (cf. Fig. 3). With a correctly designed bouncer circuit, an equal voltage droop at $C_{\rm in}$ and C_c is achieved during the pulse interval T_p, which results in a constant output voltage $V_{\rm out}$. Depending on the design and timing of the bouncer circuit, the capacitor voltage $v_{Cc}(t)$ can also reach values below 0 V at the end of the pulse interval T_p, when S_m is turned off (cf. Fig. 3). This, for example, enables a compensation of twice the voltage droop for a given capacitor voltage V_{Cc0} assuming that $v_{Cc}(t)$ varies from $+V_{Cc0}$ to $-V_{Cc0}$.

After the pulse, when S_m is opened, the capacitor current $i_{Cc}(t)$ increases again by $I_{\rm in}$ and is equal to i_{Lc} [cf. Fig. 3 and (2)]. Capacitor C_c is further discharged during the demagnetizing interval T_d until the bouncer current reaches 0 A [cf. Fig. 4(c)].

In the recovery interval T_r after the demagnetization, the negative capacitor voltage $v_{Cv}(t)$ leads to a negative current i_{Lc} in L_c and recharges the bouncer capacitor C_c [cf. Figs. 3 and 4(d)]. Moreover, during T_r, soft switching can be achieved by opening switch S_b, while the current i_{C_c} flows in the diode D_b, and it is also possible to use a pulse thyristor to obtain a large current capability and low conduction losses.

If the described LC bouncer circuit is connected to the primary of the considered power modulator, where an input voltage droop of $\Delta V_{\rm Cin} = 100$ V $(= 10\%)$ is assumed, the capacitor voltage V_{Cc} would be around 200–300 V, and the peak current in the bouncer circuit would reach values about 30–50 kA. On the other hand, if the circuit is inserted on the secondary, the capacitor voltage V_{Cc} would be around 17–30 kV with a current of 300–400 A.

In both cases, due to the high current or the high voltage, no existing semiconductor switches can be employed without connecting several switches in parallel or in series.

To overcome this problem, a second winding is added to the inductor L_c. This extension leads to the two-winding inductor bouncer circuit, which allows an adaptation of the bouncer circuit's voltage $v_{Cc}(t)$ and current ratings $i_{Cc}(t)$ to standard semiconductor switches (cf. Fig. 5).

The two-winding inductor acts like a transformer of a flyback converter with a step-up ratio of $N_{b1} : N_{b2}$, whereas the magnetizing inductance is equal to inductance L_c (cf. Fig. 5). As with the conventional bouncer circuit, the additional transformer is connected in series to the existing system and has to be magnetized before the output pulse is generated. However, in contrast to the conventional bouncer circuit, the voltage pulse during T_m, which premagnetizes the two-winding inductor, is also transformed to the secondary and therefore is applied to the load in the reverse direction. According to the considered klystron load, the reverse voltage should not exceed 50 kV.

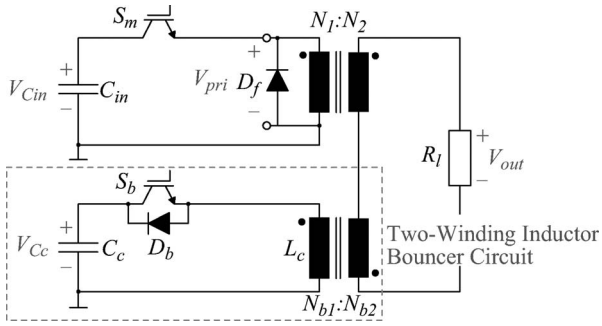

Fig. 5. Schematic of the transformer-based power modulator with the proposed two-winding inductor bouncer circuit.

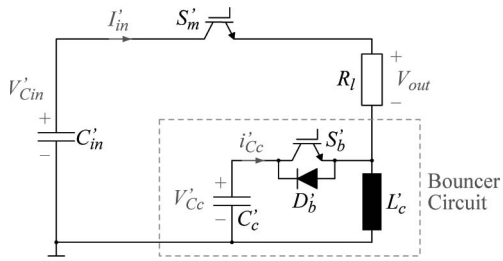

Fig. 6. Schematic of the power modulator and the bouncer circuit without galvanic isolation. All values are referred to the secondary.

In order to optimize the design of the bouncer circuit so that a minimum volume or a maximum efficiency results, an analytic model of the circuit and an optimization procedure is required. The analytic equations of the bouncer circuit are derived in the next section.

III. Mathematical Description

The operating principle of the two-winding inductor bouncer circuit is basically the same as that of the conventional bouncer circuit without galvanic isolation. As will be shown in Sections V and VI, the parasitics of the two-winding inductor bouncer circuit do not have an influence on the pulse performance of the power modulator. Therefore, in order to simplify the considerations, the parasitics of the bouncer circuit can be neglected, and the mathematical equations can be derived with the simple circuit schematic shown in Fig. 6. In this figure, all circuit values are referred to the secondary of the pulse transformer.

The insertion of the two-winding inductor only results in a transformation of the calculated bouncer circuit parameters depending on the turns ratio $N_{b1} : N_{b2}$ (cf. Fig. 2). In order to achieve a constant output voltage $V_{\rm out}$, the droop of the bouncer capacitor voltage $\Delta V'_{Cc}$ has to be equal to the input voltage droop $\Delta V'_{\rm Cin}$. In this case, the output voltage is equal to the

difference of the two initial voltages $V'_{\mathrm{Cin}0}$ and V'_{Cc0}, which results in a constant load current I'_{in}

$$I'_{\mathrm{in}} = \frac{V'_{\mathrm{Cin}0} - V'_{Cc0}}{R_l} = \text{constant}. \tag{3}$$

Neglecting the parasitics, like the magnetizing inductance or winding/interconnection resistances, the constant load current I'_{in} leads to a linear input voltage droop $\Delta V'_{\mathrm{Cin}}$

$$\Delta V'_{\mathrm{Cin}} = \frac{I'_{\mathrm{in}} T_p}{C'_c} \tag{4}$$

in contrast to an exponential voltage droop $\Delta V'_{\mathrm{Cin,exp}}$

$$\Delta V'_{\mathrm{Cin,exp}} = V'_{\mathrm{Cin}0} \cdot \left(1 - e^{-T_p/(C'_{\mathrm{in}} R_l)}\right) \tag{5}$$

without a bouncer circuit.

Consequently, the bouncer capacitor voltage V'_{Cc} also has to droop linearly with the same amplitude $\Delta V'_{Cc}$ in order to achieve a constant output voltage V_{out}. However, since the bouncer is basically a resonant circuit, the current $i'_{Cc}(t)$

$$i'_{Cc}(t) = I'_{Cc0} \cdot \sin(\omega t) - I'_{\mathrm{in}}, \quad \text{with} \quad \omega = \frac{1}{\sqrt{L'_c C'_c}} \tag{6}$$

in the bouncer capacitor C'_c has a sinusoidal run, as shown in Fig. 3. Additionally, the sine curve is shifted by the load current I'_{in} (cf. Fig. 3) during the pulse.

However, assuming a relatively long period $T = 2\pi/\omega$ of the resonance circuit compared to the pulse duration T_p, an almost constant current $i'_{Cc}(t)$ with only a small deviation

$$\begin{aligned} \Delta I'_{Cc} &= i'_{Cc}(T/4) - i'_{Cc}(T/4 \pm T_p/2) \\ &= k_1 \cdot (I'_{Cc0} - I'_{\mathrm{in}}), \quad \text{with} \quad k_1 = 0, \ldots, 1 \end{aligned} \tag{7}$$

can be obtained around the peak current I_{Cc0} at $t = T/4$ (cf. Fig. 3), where k_1 is a proportionality factor between the current deviation $\Delta I'_{Cc}$ and the bouncer capacitor's peak current at $t = T/4$. From (7), it follows that a small deviation $\Delta I'_{Cc}$ is obtained, if a small k_1 is selected. Consequently, by selecting a specific k_1, also the current amplitudes at $T/4$

$$i_{Cc}(T/4)' = I'_{Cc0} - I'_{\mathrm{in}} \tag{8}$$

and at $T/4 - T_p/2$

$$i_{Cc}(T/4 - T_p/2)' = I'_{Cc0} - I'_{\mathrm{in}} - \Delta I'_{Cc} \tag{9}$$

are defined. Thus, the needed resonance frequency

$$\begin{aligned} \omega &= \frac{2}{T_p} \arccos\left(\frac{i_{Cc}(T/4 \pm T_p/2)}{i_{Cc}(T/4)}\right) \\ &= \frac{2}{T_p} \arccos\left(\frac{I'_{Cc0} - k_1 \cdot (I'_{Cc0} - I'_{\mathrm{in}})}{I'_{Cc0}}\right) \end{aligned} \tag{10}$$

of the bouncer circuit can directly be deduced based on the two current amplitudes at $T/4$ and at $T/4 - T_p/2$ or based on k_1.

To simplify the calculation of ω for small k_1, the cosine can be approximated by a second-order Taylor series

$$\cos(\omega t) \approx 1 - \left(\frac{\omega t}{2}\right)^2. \tag{11}$$

Accordingly, by placing the pulse interval T_p symmetrically around the peak current at $t = T/4$, which means from $T/4 - T_p/2$ to $T/4 + T_p/2$, the most uniform capacitor current i'_{Cc} is achieved. For a small deviation $\Delta I'_{Cc}$, this results in an almost linear voltage droop $\Delta V'_{Cc}$ during T_p, whereas the bouncer's capacitor voltage V'_{Cc} is symmetrically changing from V_{cc1} to $-V_{cc1}$ (cf. Fig. 3).

Due to the constraint of the same voltage droop at C'_{in} and C'_c, the bouncer's capacitor voltage $V'_{Cc}(t_1) = V'_{cc1}$ is directly defined by the input voltage droop $\Delta V'_{\mathrm{Cin}}$

$$2 \cdot \Delta V'_{Cc1} = \Delta V'_{\mathrm{Cin}}. \tag{12}$$

Additionally, the bouncer's voltage droop of $2 \cdot \Delta V'_{cc1}$ during T_p can be expressed by the current $i'_{Cc}(t)$, which is approximately $(I'_{Cc0} - I'_{\mathrm{in}}) \cdot \sin(\omega t)$, respectively, by its average value $\bar{I}'_{Cc,Tp}$ during the pulse duration T_p

$$2 \cdot \Delta V'_{\mathrm{Cin}} = \frac{1}{C'_c} \int_{T/4-T_p/2}^{T/4+T_p/2} i'_{Cc}(t)dt = \frac{\bar{I}'_{Cc,Tp} \cdot T_p}{C'_c} \tag{13}$$

with

$$\bar{I}'_{Cc,Tp} = (I'_{Cc0} - I'_{\mathrm{in}}) \frac{\sqrt{k_1(2-k_1)}}{\arccos(1-k_1)}.$$

During T_m, a current $i_{Cc}(T/4 - T_p/2)' = I'_{Cc0} - \Delta I'_{Cc}$ has to be built up in the bouncer inductor L'_c before the pulse is generated, whereas the stored energy in the inductor at $i_{Cc}(T/4 - T_p/2)'$ is completely delivered from C'_c. Therefore, the required initial capacitor voltage V'_{Cc0} can be deduced from the energy balance

$$\frac{1}{2} C'_c \left(V^2_{Cc0} - V^2_{Cc1}\right) = \frac{1}{2} L'_c \left(I'_{Cc0} - \Delta I'_{Cc}\right)^2. \tag{14}$$

From (3) to (14), the circuit parameters of the conventional bouncer circuit can be calculated in dependence of the maximum allowed output voltage droop $\Delta_{\max}$. Thereafter, the real circuit values of the two-winding inductor bouncer result by selecting a proper turns ratio $N_{b1} : N_{b2}$

$$N_{b1} : N_{b2} = V'_{Cc0} : V_{Cc0} \tag{15}$$

which enables the application of commercial semiconductors with a voltage and a current rating of V_{Cc0} and I_{Cc0}, respectively.

IV. Design and Optimization

Based on the design equations, an optimization procedure is presented in the following. With this procedure, the bouncer circuit could be optimized for different quality criteria, for example, volume, losses, or the stored energy in the system.

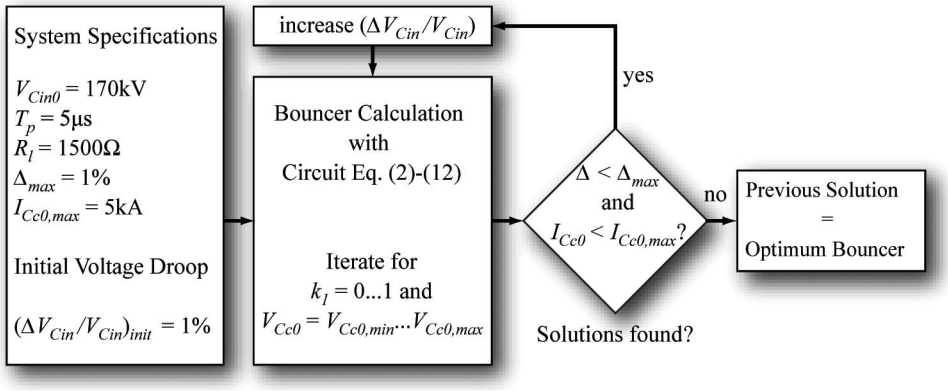

Fig. 7. Iterative workflow for optimizing the overall volume Vol_{tot} of the input capacitor and the bouncer circuit using the analytical equations.

Here, the focus is put on the volume, where on the one hand, the volume of the bouncer circuit can be optimized for an existing system with a given input voltage droop ΔV_{Cin}, or on the other hand, the whole system volume can be optimized regarding the overall volume, i.e., the input capacitor's volume and the volume of the bouncer. Considering the value of the input capacitor, the optimization results also in a reduction of the input capacitance C_{in} and the stored energy in the system, while the first approach only optimizes the volume of the bouncer circuit for a given input capacitor C_{in}.

In the following, the two-winding inductor bouncer circuit is designed and optimized regarding the overall volume

$$\begin{aligned} Vol_{\mathrm{tot}} &= Vol_{\mathrm{Cin}} + Vol_{\mathrm{bouncer}} \\ &= Vol_{\mathrm{Cin}} + Vol_{Cc} + Vol_{Lc} + Vol_{\mathrm{switch}} \end{aligned} \tag{16}$$

of the existing system (cf. Fig. 1 and Table I).

In addition to $\Delta_{\max}$, also constraints like maximum switched voltage and/or current of S_b are considered in the optimization. The initial capacitor voltage of the two-winding bouncer circuit is set to $V_{Cc0} = 1$ kV, which is equal to the modulator's input voltage V_{Cin0}. Consequently, for C_c, capacitors of the same type as for C_{in} can be used, as long as the current i_{Cc} does not exceed the current rating of the capacitors. Additionally, the power supply of the bouncer circuit has the same voltage, which allows a reduction of the power supply's complexity. Finally, for S_b, the same IGBT module (FZ3600R17KE3 from EUPEC) as for the existing power modulator is applied. In the following design, the peak current of S_b is limited to $I_{Cc0} = 5$ kA, and the volume of the IGBT module is fixed to $Vol_{\mathrm{switch}} = 0.9$ l.

In order to calculate Vol_{tot}, a proportionality

$$\begin{aligned} Vol_{\mathrm{Cin}} + Vol_{Cc} &= g_1 \cdot \frac{1}{2}\left(C_{\mathrm{in}} V_{\mathrm{Cin0}}^2 + C_c V_{Cc0}^2\right) \\ &= g_1 \cdot \frac{1}{2}(C_{\mathrm{in}} + C_c) V_{\mathrm{Cin0}}^2 \end{aligned} \tag{17}$$

of the stored energy in the capacitors C_{in} and C_c, respectively, and the capacitor's volume is assumed. For the employed capacitors (HDMKP series from Vishay), this assumption was empirically verified, whereas the proportionality factor is $g_1 = 9.5$ l/kJ.

Due to the dependence of the two-winding inductor's volume Vol_{Lc} on the number of turns, the air gap length, the turns ratio, and the isolation distances, the volume of the inductor is calculated for each operating point (L_C, I_{Cc0}) individually for the optimization.

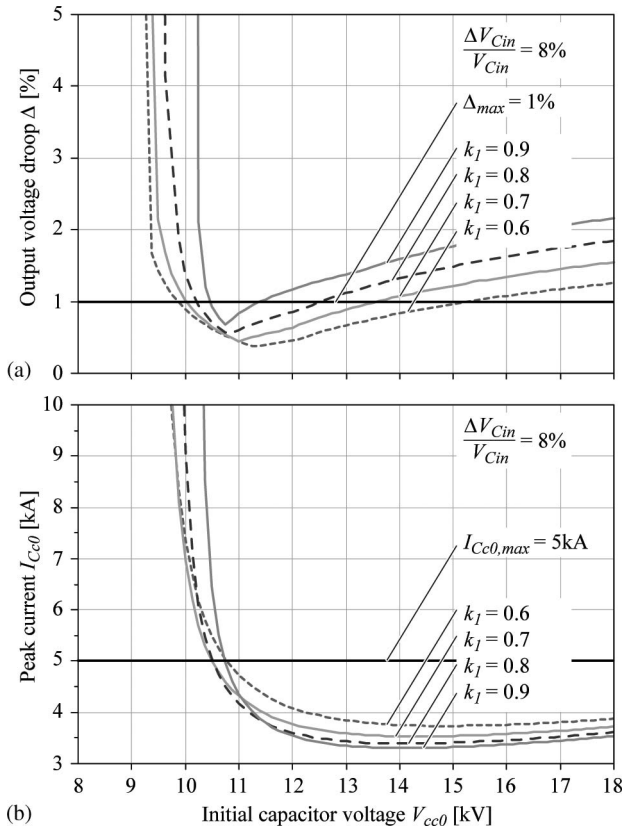

Fig. 8. (a) Output voltage droop Δ and (b) peak current I_{Cc0} depending on V_{Cc0} for different values of k_1 with $\Delta V_{\mathrm{Cin}}/V_{\mathrm{Cin}} = 8\%$.

Using the equations in Section III, the missing circuit parameters for the conventional bouncer (C_c, L_c, I_{Cc0}, ΔI_{Cc}, V_{Cc1}, ω, and $N_{b1} : N_{b2}$) can be calculated depending on k_1, $\Delta V_{\mathrm{Cin}}/V_{\mathrm{Cin}}$, and V_{Cc0}. By variation of these three parameters, the optimal circuit values resulting in a minimum overall system volume and an output voltage droop of less than $\Delta = 1\%$ can be calculated (cf. Fig. 7).

In Fig. 8, the resulting output voltage droop Δ and the peak current I_{Cc0} depending on the initial capacitor voltage V_{Cc0} are shown for different values of k_1 with $\Delta V_{\mathrm{Cin}}/V_{\mathrm{Cin}} = 8\%$.

As expected, in order to achieve a lower output voltage droop Δ, a smaller value of k_1 has to be selected, which results in a smaller deviation ΔI_{Cc} and leads to a more uniform current in the bouncer capacitor C_c during the pulse duration T_p [cf. Fig. 3 and (7)]. Unfortunately, a smaller value of k_1 also results in a higher initial capacitor voltage V_{Cc0} and in a larger peak current I_{Cc0} [cf. Fig. 8(b)]. Additionally, according to (10), a smaller value of k_1 leads to a lower resonance frequency ω and, therefore, also to larger capacitor and inductor values.

In the optimization procedure of the bouncer circuit, the boundary conditions given by the maximum switching current $I_{Cc0,\max}$, the maximum switch operating voltage $V_{Cc0,\max}$, and the maximum output voltage droop $\Delta_{\max}$ have to be fulfilled, whereas the switch operating voltage can be kept below the maximum switching voltage by selecting a proper turns ratio $N_{b1} : N_{b2}$. Therefore, in the optimization procedure, only the constraints for the maximum switching current $I_{Cc0,\max}$ and the maximum output voltage droop $\Delta_{\max}$ have to be met.

In Fig. 9, the output voltage droop Δ, the peak current I_{Cc0}, and the overall volume $Vol_{\rm tot}$ are shown as a function of the initial capacitor voltage V_{Cc0} for different values of input voltage droop $\Delta V_{\rm Cin}/V_{\rm Cin}$ with $k_1 = 0.6$. Additionally, for $\Delta V_{\rm Cin}/V_{\rm Cin} = 11\%$, the allowed design range is highlighted, which is limited by the mentioned boundary conditions $I_{Cc0,\max}$ and $\Delta_{\max}$.

As can be seen in Fig. 9(c), an increasing input voltage droop $\Delta V_{\rm Cin}/V_{\rm Cin}$ leads to a decreasing overall volume $Vol_{\rm tot}$, since the volume of the input capacitor $C_{\rm in}$ is decreasing, due to the increasing input voltage droop, while the volume of the bouncer circuit, due to the limited peak current I_{Cc0} and the slightly increasing inductor value L_c, is only slowly increasing.

Therefore, considering the dependences in Figs. 8 and 9, for the optimization of the bouncer circuit, the input voltage droop $\Delta V_{\rm Cin}/V_{\rm Cin}$ has to be increased as long as the boundary conditions $I_{0,\max}$ and $\Delta_{\max}$ can be fulfilled. For the considered power modulator, this leads to a maximum input voltage droop of $\Delta V_{\rm Cin}/V_{\rm Cin} = 14.3\%$ with a minimum overall volume of $Vol_{\rm tot} = 6.57$ l.

The resulting circuit parameters for the bouncer and the input capacitor $C_{\rm in}$ are listed in Table II.

In Fig. 10, the comparison of the overall volume with and without the bouncer circuit is shown. Without the bouncer circuit and by neglecting system parasitics, like the magnetizing inductance or series resistances, a minimum input capacitance of $C_{\rm in} = 15$ mF is required to limit the output voltage droop to 1%, which results in a capacitor volume of 70 l.

With the bouncer circuit, a volume reduction by a factor of 10.5 to 6.57 l is possible. Additionally, the stored energy in the input capacitor $C_{\rm in}$ and the bouncer capacitor C_c is reduced by a factor of 24 to 319.4 J, which is only 3.2 times of the pulse energy compared to 50 times of the pulse energy for the system without the bouncer circuit. Therefore, concerning volume and safety aspects, the proposed bouncer circuit should be employed even if the complexity of the system is increasing.

In comparison with the conventional bouncer circuit, a commercial IGBT module can be used for the two-winding inductor bouncer circuit. In the conventional bouncer, the switch S_b would have to handle a peak current of $I_{Cc0} = 230$ A and a capacitor voltage of $V_{Cc0} = 22$ kV.

Due to the insertion of the two-winding inductor, the total leakage inductance of the power modulator is increased, which could result in a degradation of the pulse performance.

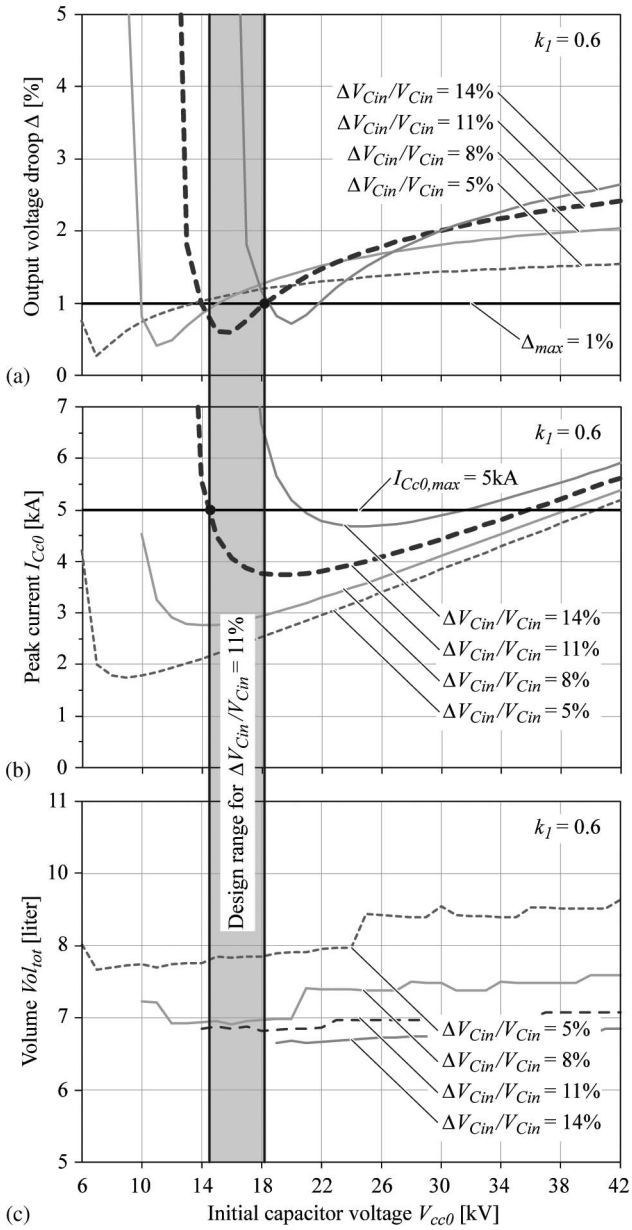

Fig. 9. (a) Output voltage droop Δ, (b) peak current I_{Cc0}, and (c) overall volume $Vol_{\rm tot}$ depending on V_{Cc0} and $\Delta V_{\rm Cin}/V_{\rm Cin}$ for $k_1 = 0.6$.

TABLE II
OPTIMAL CIRCUIT PARAMETERS OF THE TWO-WINDING INDUCTOR BOUNCER CIRCUIT FOR A MINIMAL SYSTEM VOLUME. THE LISTED VALUES ARE REFERRED TO THE PRIMARY OF THE BOUNCER CIRCUIT

Bouncer input voltage V_{Cc0}	1 kV
Turns ratio $N_{b1} : N_{b2}$	1 : 22
Peak current I_{Cc0}	5 kA
Bouncer capacitor C_c	13.8 µF
Bouncer inductor L_C	567 nH
Input capacitor C_{in}	625 µF

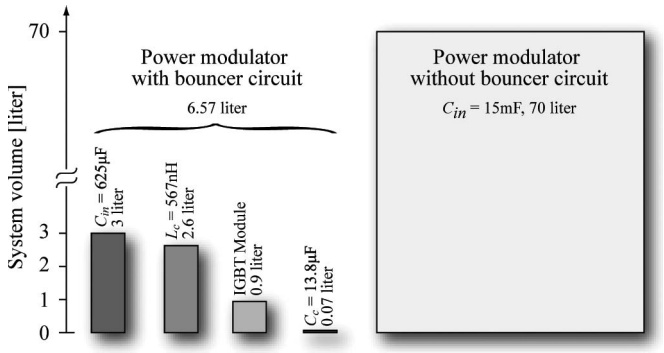

Fig. 10. Comparison of the total volume Vol_{tot} for a power modulator with and without the bouncer circuit, where the volume and the stored energy are reduced by a factor of 10.5 and 24, respectively.

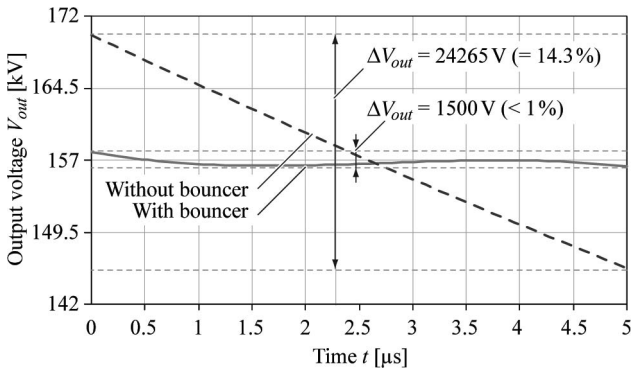

Fig. 11. Simulated output voltages $v_{\mathrm{out}}(t)$ of the power modulator with and without the optimized bouncer circuit (SIMPLORER).

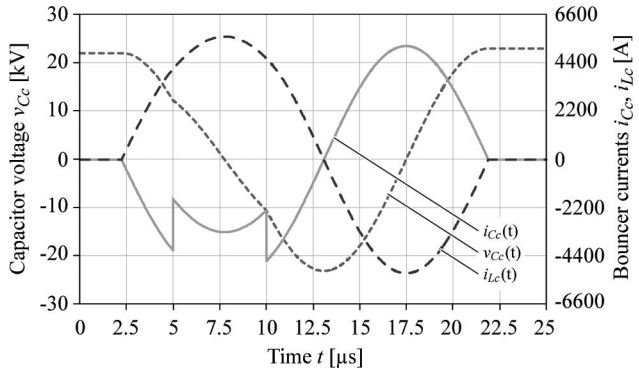

Fig. 12. Simulated voltage and current waveforms $v_{Cc}(t)$, $i_{Cc}(t)$, and $i_{Lc}(t)$ of the optimized bouncer circuit (SIMPLORER).

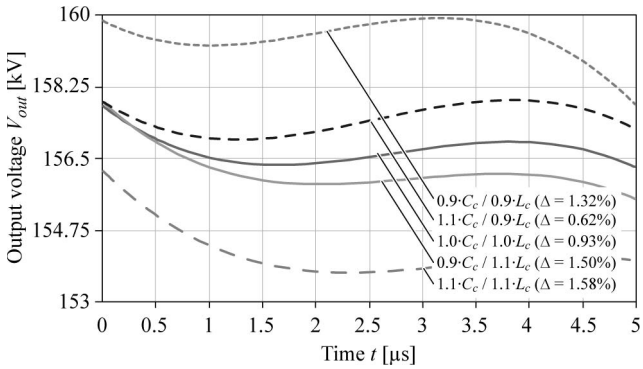

Fig. 13. Influence of tolerances in C_c and L_c. Output voltage waveforms for a variation of C_c and L_c by $\pm 10\%$ (SIMPLORER).

However, for the optimal two-winding inductor, the primary leakage inductance is only $L_{\sigma,b2} = 5.4$ nH. This corresponds to a leakage inductance of $L_\sigma = 3$ μH on the secondary of the power modulator, which is negligible compared to the leakage of approximately 350 μH of the modulator. Consequently, the insertion of the conventional bouncer on the primary or secondary would result in an even stronger degradation of the pulse performance.

V. Verification by Simulation

In the analytical optimization procedure of the bouncer circuit for each operating point, the output voltage droop Δ, shown in Figs. 8(a) and 9(a), has always been calculated based on the precise output voltage waveform $v_{\mathrm{out}}(t)$, which is derived by Laplace transformation. Due to this accurate description, the calculated waveform is equal to the simulated output voltage $v_{\mathrm{out}}(t)$ (cf. Fig. 11). As expected, the output voltage droop Δ can be kept below 1%. Additionally, for the same input capacitor value C_{in}, the output voltage of the power modulator without the bouncer is shown in Fig. 11.

In Fig. 12, the simulated voltage and current waveforms $v_{Cc}(t)$, $i_{Cc}(t)$, and $i_{Lc}(t)$ of the optimized bouncer circuit are shown. Due to the approximation of the cosine by its second-order Taylor series and the use of the average current value $\bar{I}_{Cc,Tp}$, the simulated peak current I_{Lc0} in the inductor exceeds the specified value $I_{Cc0,\max}$ during the pulse interval by approximately 10%. As a consequence of this, the pulse interval T_p is not symmetrically around $T/4$, which can be corrected by a small time shift of the pulse interval T_p. Due to the approximations, this can also lead to a smaller output voltage droop Δ in some cases, as shown in Fig. 13.

Furthermore, in the simulation, the influence and dependence of parameter tolerances, as well as additional system parasitics, like the magnetizing inductance and series resistances, were determined. There, for the circuit values C_c and L_c, a variation of $\pm 10\%$ was assumed. In Fig. 13, the output voltage waveforms of the calculated bouncer circuit and of the cases in which a variation of C_c and L_c by $\pm 10\%$ is assumed are shown.

The maximum output voltage droop of 1.58% results if both the values of C_c and L_c are increased by 10%. By a proper time shift of T_p and slightly changing the initial bouncer capacitor voltage V_{Cc0}, the output voltage droop Δ can be reduced. For the mentioned worst case, the output voltage droop can be reduced below 1% if V_{Cc0} is increased to 1068 V and the pulse interval is shifted in time by 240 ns. However, the constraint for the capacitor voltage of 1 kV is now exceeded.

As shown in Fig. 13, the minimum output voltage droop is achieved for 90% of C_c and 110% of L_c and not for the calculated bouncer circuit, which is due to the used approximations.

The influence of the main pulse transformer parasitics on the output voltage droop is shown in Fig. 14. The simulation includes the leakage inductance L_σ, the magnetizing inductance L_{mag}, the distributed capacitance C_d, and the winding resistances R_w shown in Fig. 1. According to the simulation results, the combination of all parasitics causes the shown

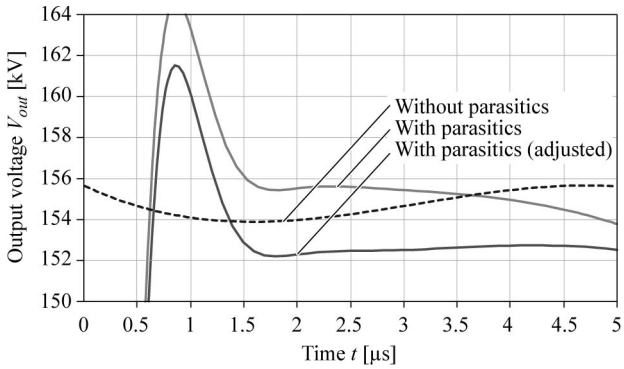

Fig. 14. Influence of the transformer parasitics ($L_{\mathrm{mag}} = 72$ mH, $L_\sigma = 180$ μH, and $C_d = 140$ pF—value referred to the secondary) of the pulse transformer on the voltage droop (SIMPLORER).

pulse degradation; the pulse degradation cannot be attributed to a certain parasitic component. Aside from the resulting overshoot at the beginning of the pulse, the voltage droop Δ is also increased. However, by adjusting the timing of the pulse interval T_p, the additional voltage droop due to the main pulse transformer can be compensated. As mentioned in Section IV, in contrast to the main pulse transformer, the influence of the two-winding inductor's parasitics can be neglected. Due to the more than seven times lower turns ratio compared to the pulse transformer and the thinner isolation needed in between the windings because of the lower secondary voltage, the two-winding inductor can be built more compact and will lead to smaller parasitics. Even if the two-winding inductor would show the same parasitics referred to the primary as the pulse transformer, the influence on the pulse distortion would be more than 49 times smaller due to the turns ratio.

Aside from the analytical optimization method discussed in this paper, more accurate solutions are feasible based on a numerical computation of the component values C_c and L_c. There, a numerical solver determines the component values within the given parameter space. Depending on the respective set of input parameters, the computation can become highly complex and time consuming.

The intuitive nature of the presented analytical method facilitates a deeper understanding of the employed bouncer circuit and enables the fast calculation of C_c and L_c close to the optimum.

VI. Conclusion

In this paper, the design and the analytical optimization of a two-winding inductor bouncer circuit have been presented in order to achieve an output voltage droop of less than 1%. Due to the realized galvanic isolation, a new degree of freedom is obtained, which allows an adaptation of the bouncer circuit's voltage and current ratings to existing semiconductor switches, like IGBT modules.

With an analytically optimized design of the two-winding inductor bouncer circuit for the existing system, the input capacitance is reduced from $C_{\mathrm{in}} = 15$ mF to 13.8 μF, which results in a volume reduction by a factor of 10.5 to 6.57 l. Additionally, the stored energy is decreased by a factor of 24 to 319.4 J, which is only 3.2 times the amount of the pulse energy compared to 50 times of the pulse energy for the system without the bouncer circuit. Furthermore, it is shown that the parasitics caused by the two-winding inductor bouncer circuit result in no degradation of the pulse performance.

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