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Ultra-Low-Inductance Power Module for Fast Switching Semiconductors

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Abstract

An ultra-low-inductance power module using silicon carbide (SiC) devices has been developed by using an advanced packaging technology. The switching cell inductance was reduced significantly due to the absence of bond wires for chip interconnection. This was achieved by using PCB technologies on a DCB substrate to provide more interconnection layers and design freedom. The test result after fabrication showed the superiority of advanced packaging methods relating to switching behaviour. Almost no overshoot voltage and no ringing during turn-off were detected. The measured switching cell inductance went below 1nH which allows high speed switching and/or high efficiency applications by virtue of low switching losses.

1. Introduction

With wide band gap semiconductors like SiC improvements towards an ideal switch for Power Electronics are continuing. The properties of an ideal switch can quickly be derived from the known restrictions of the existing semiconductors: an ideal switch would show infinitely fast switching (for zero switching loss), no conducting losses and no semiconductor capacitance. In this case the package of the power semiconductor will become the only influencing factor on the switching behavior, especially the parasitic capacitances and inductances. Although this level of semiconductor behavior is not nearly reached, an increase in research activity can be observed for the design of the electro-magnetic properties of packages. The parasitic DC-link inductance and its influence on switching is well known and mentioned e.g. in [1]. Design of packages with low DC-link inductance is described in [2] and [3]. The calculation of the parasitic properties of semiconductor packages is treated in [4] and with the special focus on paralleling semiconductors e.g. in [5]. Finally the authors in [6] propose geometrical optimization of power modules the use of flip chip assembly of the semiconductors to reduce interference generation.

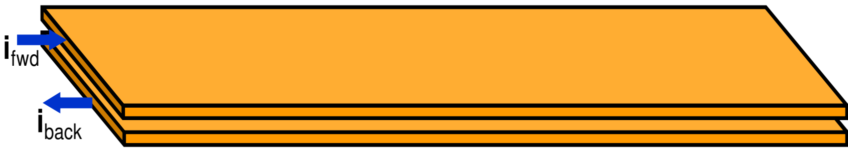
The aim of this paper is to investigate the switching behavior of state of the art SiC semiconductors in a package with ultra low DC-link inductance. By reducing the package influence to a neglectable value future possibilities and requirements for very fast semiconductors will be worked out. Therefore the packaging technology has to be improved to provide more degrees of freedom compared to recent bond wire setups. The design and the package technology are described in Chapter 2, while simulation of the developed setup is shown in the following chapter. Chapter 4 describes briefly the manufacturing process and chapter five the measurement equipment and the measurement results.

2. Design and technical realisation

Conventional semiconductor packages either contain single semiconductors or as modules a higher number of chips. Typically all packages have a single layer, either a DCB substrate or a lead frame and provide additional interconnects by bond wires.

In this technology the wire bonds give a bottom value for inductance and there are no possibilities of compensating magnetic fields. Common strategy for low inductance in DC-links is

the strip line or bus bar geometry. It relies on two phenomena: on the one hand a wide conductor creates a long path for the magnetic flux to close around it. The resulting magnetic resistance is high and the inductance is low. On the other hand the return path of the current is brought close in order to cancel the magnetic fields (Fig. 1).



$$L \approx 0.004 * l * \pi * \frac{d}{B} \quad in\ \mu H$$

l : Length of conductor in cm

d : Distance of conductors

B : Width of conductors

Fig. 1. Principle of bus bar design. Example value: 30mm width, 100mm length and 0.5mm distance will result in an inductance of 2.1nH

Main issue in power electronics is to reduce the inductance of the switching cell. It is formed by the switching semiconductors, e.g. a half bridge, the DC-link capacitor and all interconnects between both. As DC-link and semiconductors are normally separate components, interfaces between both like screw terminals or pins add additional inductance. Therefore in this investigation a module construction was developed comprising the High Side (HS) and Low Side (LS) semiconductors of a half bridge as well as ceramic capacitors as 1st stage or high frequency DC-link. This construction thereby includes the whole switching cell and avoids the need for highly educated engineers to design this critical part.

To apply this idea to a power module a new packaging technology is needed. The solution developed for this investigation uses a PCB (Printed Circuit Board) production process in combination with a Direct Copper Bond (DCB) substrate. Thereby the high number of layers of a PCB process can be utilized to freely design the current path in the module.

A triple-layer setup was found to be sufficient for the design goal. The lower layer is provided by the upper side of the DCB, the middle and top layer are manufactured by the PCB process. The design of the module and a cross section are shown in Fig 2.

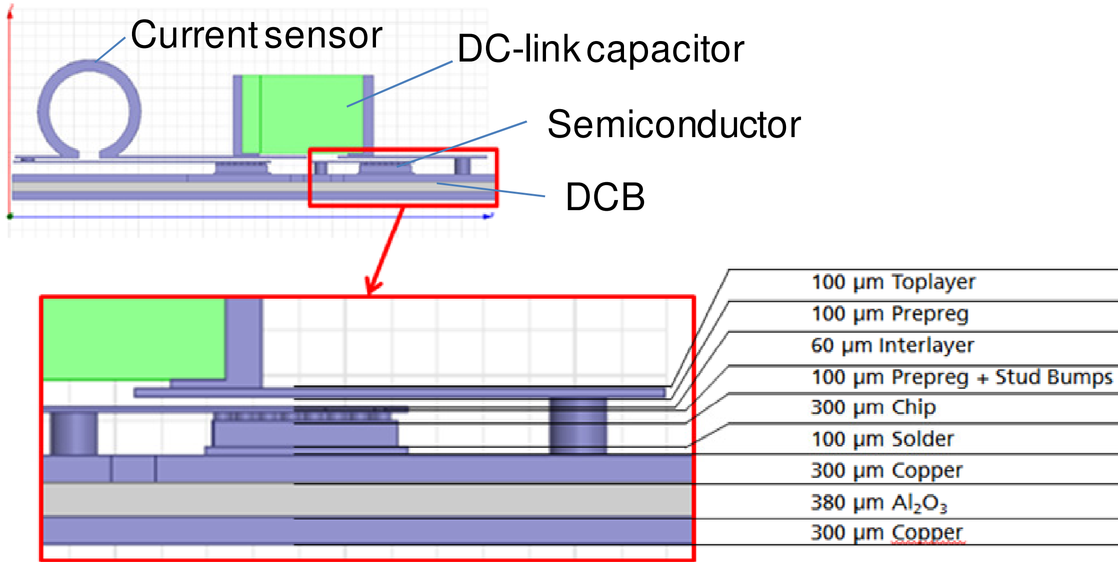


Fig. 2. Cross section of the developed module with current sensor and DC-link capacitors assembled

Normally-on JFETs from Infineon ($R_{DS,On}$ = 100mΩ) were selected as semiconductors. They were assembled as bare dies by sintering them to the DCB. As shown in Fig. 3a, the DCB is structured into two parts. The potential of DC+ is located on the outer segment and the two paralleled HS transistors are placed on it. The LS transistors are located on the inner segment of the DCB which forms the OUT potential of the half bridge. All transistors are positioned symmetrically on the DCB to equalize stray inductance and the current density distribution of the individual transistors. A trace goes from the inner segment to the outer right,

which will later serve as a load output. The width of the conduction track cannot be increased arbitrarily because of the influence of parasitic capacitance increases with increasing surface. At this point, a compromise between resistive power losses and parasitic capacitance has to be made. The width of the conduction track is predetermined in this design by the calculation of the specified maximum ohmic resistance for the power module.

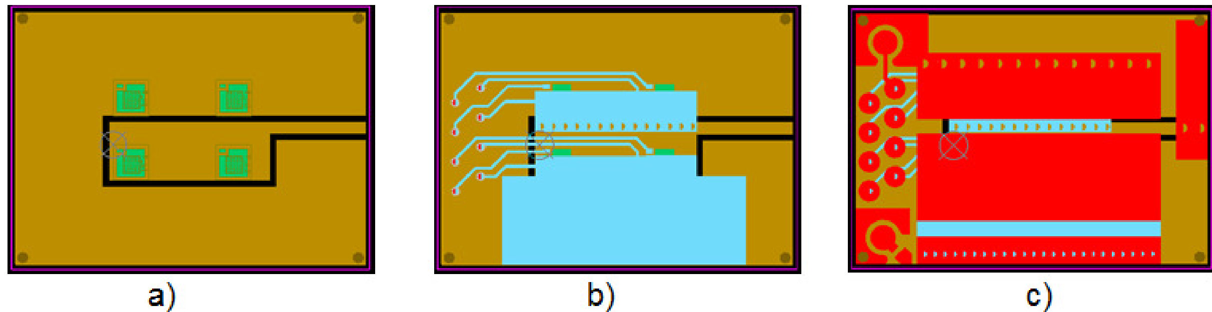


Fig. 3. Design of the different layers of the module

The light blue center position in Fig. 3b connects the chip top sides. The gate and auxiliary emitter terminals of the relevant transistors were conducted close to one another to the left outside with the reduction of self-inductance as a background. The gate and auxiliary emitter conductors were rotated 90° relative to the load current direction to minimize the inductive coupling between the load and control circuit. The blind vias connects the sources terminals of the HS-transistors with the drain terminals of LS transistors. Thereby the largest possible number of vias is selected for this connection in order to avoid parasitic inductance and resistance. The track connected to the source terminals of the LS transistors lie on DC- potential, therefore they can be shaped to a large area. It leads from the chip terminals to the bottom edge in 3b.

The upper layer is a direct interface of the power module to power supply and control unit, it is shown in red in Fig. 3c. The upper track area is located on the DC+ potential and is connected to the DCB layer by vias. The middle and lower track area in Fig. 3c will be bridged later by the current sensor. The vias connect the lower track area to the middle layer. The measuring points for the HS-drain-source voltage are on the left side as well as measuring points for the current sensor voltage. These measuring points were prepared as plugs for an oscilloscope probe shielding the probe tip by a tube that provides the ground connection for the probe. Contact points for the gate or auxiliary emitter terminals are also situated on the left hand side and are connected by vias to the middle layer. The gap between the upper and middle area of the isolation path for later soldered ceramic capacitors on the top-layer. The right red area will be reserved for the load output; this connection path with the output load in the DCB-top is also done through vias. Fig. 4 gives an overview of the connections of the power module on the top layer. Measurement-, control- and power-connections will be introduced later by spring contacts from above in the center of the circles. The DC-link capacitors can be mounted directly on the top layer, from which the connections were created between DC+ with the drain pin of HS and between DC- with the source pin of LS transistors through vias.

The application of this packaging method decreased the interconnecting distance between the power switches on a plane surface; this allowed the conductive paths from and to DC-link voltage keeping very tight to each other for increasing magnetic coupling among them by reason of additional reducing of the stray inductance.

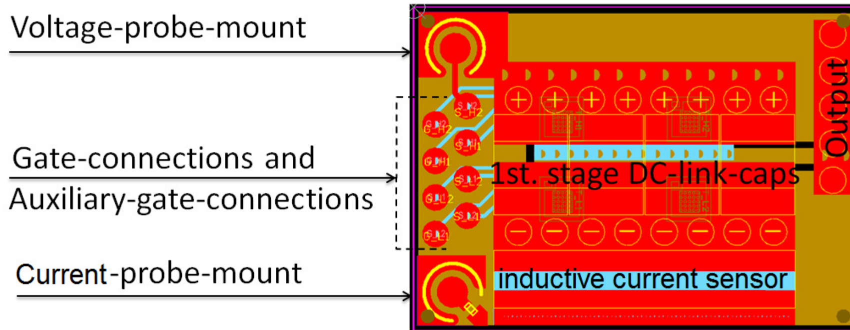


Fig. 4. Connections of the power module

3. Simulation

The design was evaluated by simulation with the software GeckoEMC as the primary guidance for the module development in this work. The program used the so-called Partial Element Equivalent Circuit Method (PEEC), a method for the calculation of electromagnetic fields. Thereby structures will be discretized in sub-structures with smaller volumes, which would be modeled by an electrical equivalent circuit and then solved using methods of network analysis [7].

A 3D simulation model is created starting from construction data of the previous section. As shown in Fig. 5 the commutation circuit with turned on transistors is considered as a current loop. The plotted virtual current serves as an excitation for the calculation of the conducting structure. In this way, one obtains a value of 1.1nH for the total commutation inductance and 0.43nH for the current sensor at 10MHz.

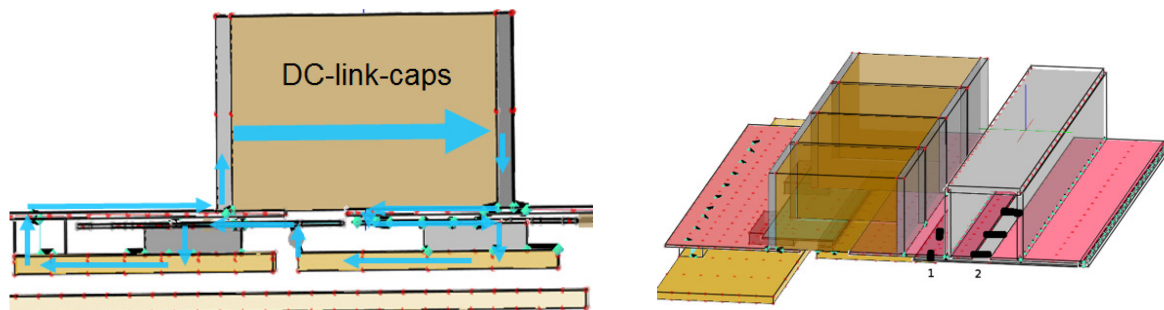


Fig. 5. Current path and simulation model of the power module

4. Manufacturing process

The manufacturing technology is based on previous work on embedding semiconductors in a PCB [8].The die attach of JFETs on the DCB was done by silver sintering, then the gold stud bumps were bonded on the gate and source contact surfaces of the transistors to make the aluminum surface of the chip accessible to the following processes. The Al_2O_3 substrate of power module to be produced has a small size of 20x30mm, the mounting of this substrate on a larger sub-structure is necessary to ensure the further manufacturing steps with this dimension for the production facility. After that, the interlayer was applied; this layer consists of a copper foil for the electrical connection between the construction elements and a fiberglass/epoxy resin composite material (FR4) in copper-free areas as insulation. In the next step, the milling head cut through the insulating layer mechanically and separated the contact surfaces of semiconductors, while blind vias were created by drilling. Electroplating

brought a copper layer with a thickness of 60µm on the FR4 with the free areas. The connections of the semiconductors were created this with this copper layer. The depressions caused by the milling left after the electroplating bathtub-shaped ditch, which were filled by an electrical conductive paste to avoid under-etching in these places by later processing. Then the etching revealed the structure of the interlayer, the traces of the gate and auxiliary emitter cables and the connection between the source ports were separated from each other during this process. After the middle layer with FR4 is isolated, the application of the last layer (top layer) follows with a layer thickness of 100µm. The structure of this layer is carried out again by etching. Then the finished module was separated from substrate by cutting. Fig. 6 shows the manufactured module.

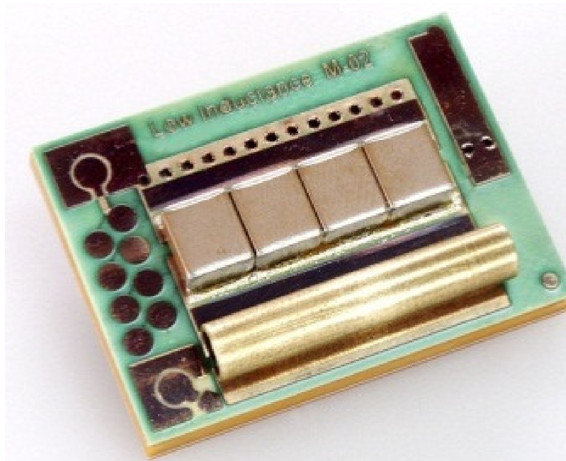


Fig. 6. Manufactured module with DC-link capacitors and current measurement

5. Measurement

The investigation of the power module's switching behaviour necessitates very high speed voltage and current measurement. For this purpose two 1GHz voltage probes used with an oscilloscope of Tektronix were applied in a double pulse test circuit. The first one measured the drain-source voltage V_{DS} directly, the second one gripped the voltage of the current Sensor V_{coil} caused by the change of the drain current I_D during turn-on and turn-off. The current sensor is a specially designed Rogowski coil placed in an Ω-shaped brass tube. The reconstruction of the module's current can be made by integrating the coil voltage.

5.1. Current sensor

The current comprises a primary and a secondary winding (Fig. 7). The primary winding consists of a brass tube having an outer diameter of 4mm. It has one winding and is meanwhile the protective sheath that protects the shunt against mechanical as well as electromagnetic influence. The use of brass tube with this diameter causes an additional inductance of 350pH. This value appears to not unsubstantial regarding to the intention of producing a commutation cell with less than 2nH. A tube with a smaller diameter would result in less additional inductance; however it also would cause difficulty for later mechanical connection by soldering and for the accommodation of the secondary coil.

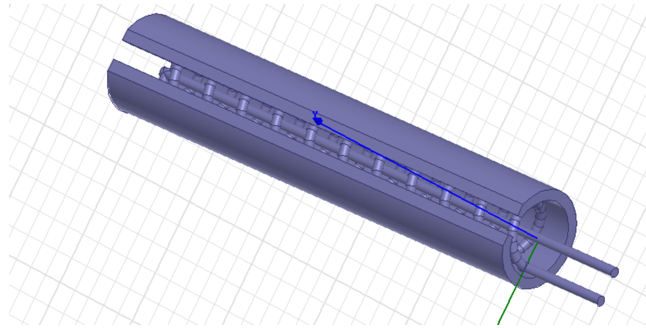


Fig. 7. Construction of the current sensor

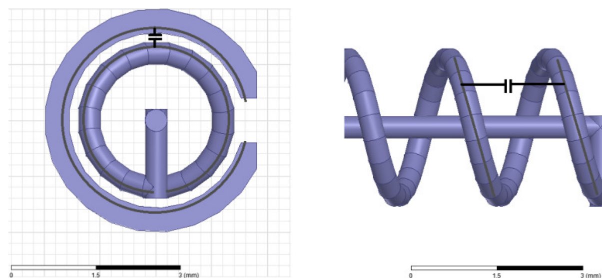


Fig. 8. Construction related parasitic capacitances

The coil was made of a 200um thick wire with 10 turns. The enamelled wire was wound around a roll of paper with an outer diameter of 2.4mm. Paper is selected due to its low ε_r, the availability and flexibility.

To achieve a high measurement bandwidth the winding capacitance has to be kept as low as possible. Fig. 8 shows the relevant factors influencing its value, the capacitance to the brass tube and the capacitance between the turns. In both cases more distance reduces capacitance. Nevertheless the capacitance of the oscilloscope probe and the coil capacitance will create a resonance at high frequency, which was damped in this investigation by a resistor between both. In Fig. 9 the transfer function from current to voltage at the oscilloscope is shown. The voltage signal has to be integrated.

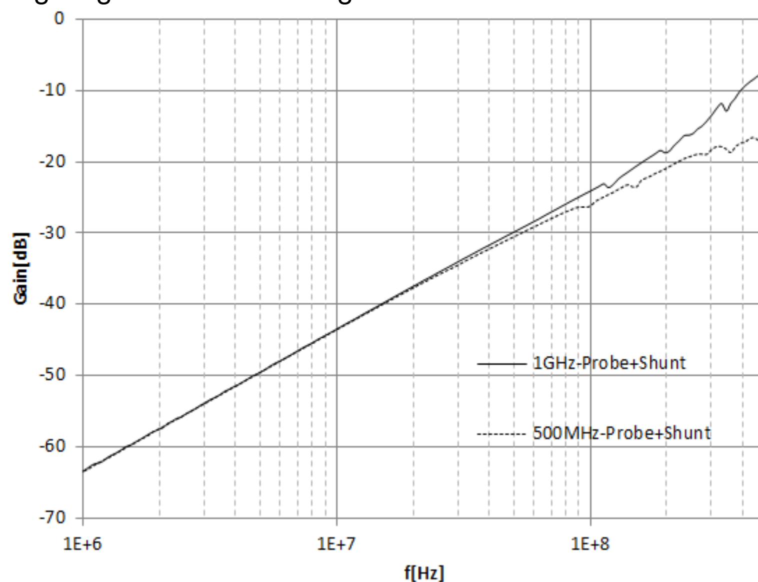


Fig. 9. Transfer function of the current sensor and different voltage probes and a damping resistor

The measurement of the modules with low additional inductance of 350pH could be realized by the chosen structure of the shunt. With the decoupling of measurement and load circuit inductive shunt exhibits distinct advantage in terms of measuring security. It is immune to electromagnetic interference. The study also shows the importance of the probe choice and its adaptation for later measurement. By measurement of slow switches where the di/dt is small, the use of larger number of turns can be considered to increase the self-inductance of the coil. In this case, the length of the coil must be adapted accordingly and one has to expect a former resonance phenomenon of measuring equipment. The current waveform can be represented by a simple integration of a potent oscilloscope.

5.2. Principle of the measurement and results

Based on the parasitic ringing during turn-off, in which the output capacitance of the turned-off transistor and the commutation inductance are involved, the inductance value can be determined. Therefore a precise determination of the output capacitance C_{oss} of the HS-transistor at a given voltage is required. The value of the output capacitance can be read directly by the manufacturer's specifications in many cases, but the integration of semiconductors in such a power module inevitably causes an increase of the Miller capacitances and thus the manufacturer's specification is only partly usable. It is more appropriate at this point to secure the accuracy of the output capacitance value of a measurement at a certain voltage. Then, the resonance frequency f_{res} of the parasitic oscillation is determined at the same blocking voltage after switching off. Because the available impedance analyzer only provides a maximum bias voltage of 40V, the output capacitance and the parasitic oscillation can be measured at 40V. Fig. 9 illustrates the results of the measurement of the power module, a deviation from 80pF by the comparison between the measured and specified output capacitance is found, which confirms the previous statement.

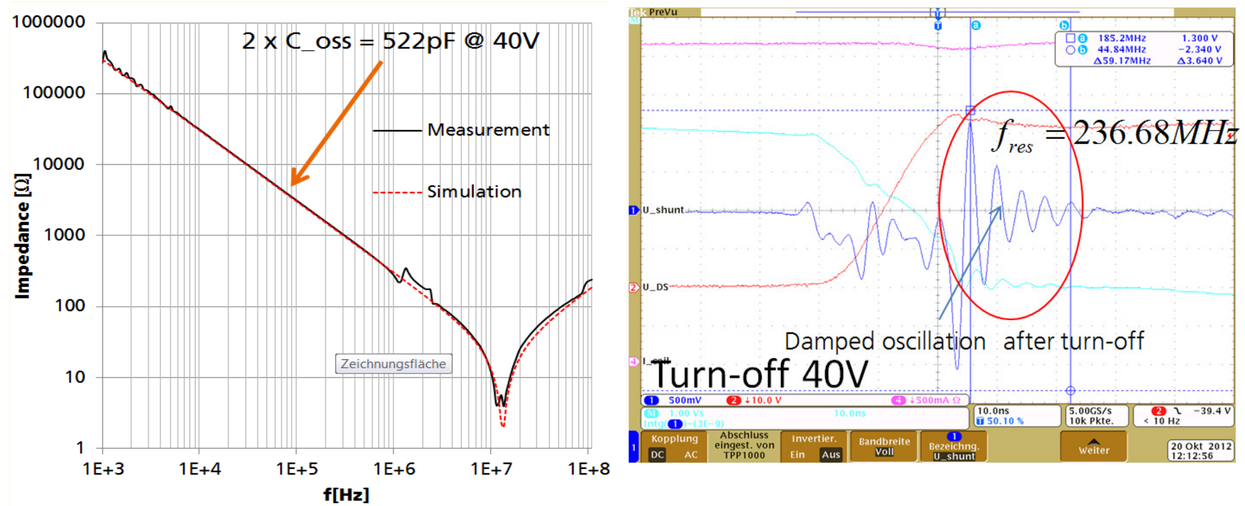


Fig. 10. Determination of the commutation inductance

With 522 pF as measured value for C_{oss} and 236.7 MHz for f_{res} at 40V DC-link voltage (Fig. 10), according to the formula $f_{res} = \frac{1}{2\pi\sqrt{C_{oss} \cdot L_{comm}}}$

the switching cell inductance L_{comm} has to be 0.86 nH.

The turn-off behavior of the power modules in Fig. 11 also confirmed the size of the determined commutation inductance, the almost absence of the overvoltage is to record during the entire turn-off.

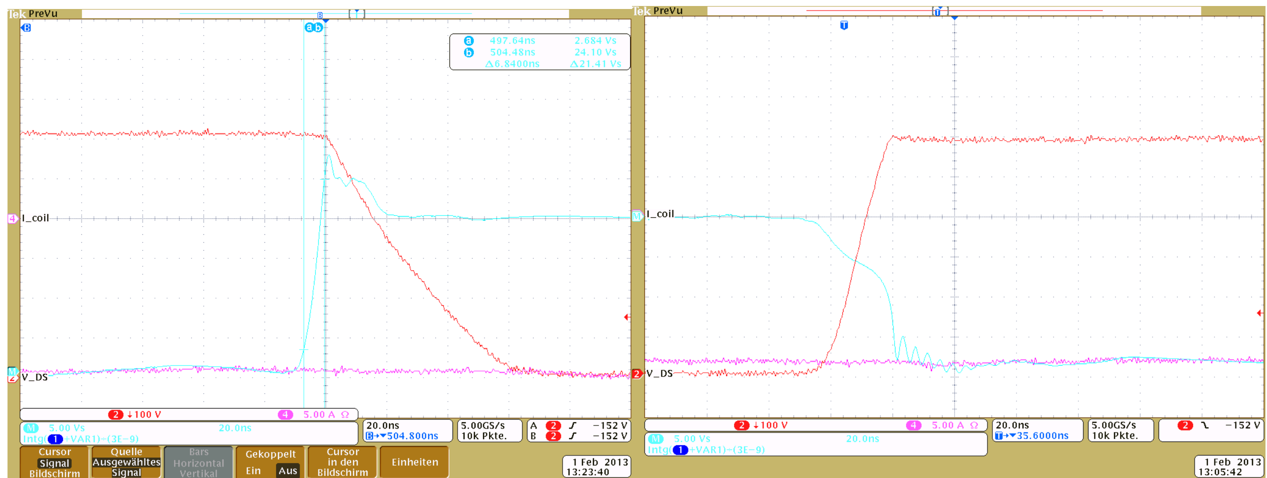


Fig. 11. Turn-on and turn-off at 600V/20A, voltage in red, current in light blue

6. Conclusion

The demonstration on this paper shows that remarkable improvements can be achieved for modern power modules by using advanced packaging technology in consideration of dynamic as well as static behaviour of the switching devices. The integration of the whole switching cell into the semiconductor package is one part to make high speed switching applicable to device designers. The proposed packaging technology leads the way to a package for the ideal switch.

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7. References

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