Pareto-Optimal Design and Performance Mapping of Telecom Rectifier Concepts

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***Abstract*—In the course of the design of single-phase PFC rectifiers, the demand for a high efficiency η and a high power density ρ must be met at the same time. Depending on the weight on these two design criteria different topologies could be advantageous. However, a comprehensive comparison of the topologies is difficult, since a large number of parameters must be determined and constraints in different physical domains, as e.g. magnetic or thermal properties, and EMI issues must be considered. Therefore, in this paper an approach based on relatively simple analytical equations is presented for calculating the limiting curves of conventional, bridgeless and TCM resonant-transition single-phase PFC rectifiers in the ρ-η-plane. These Pareto-Limits represent the Topology Performance Map of the considered topologies and allow a direct comparison of the achievable performance and the limitations with respect to power density and/or efficiency.**

I. Introduction

Over the last decades, the development of power electronics systems was mainly targeting higher power densities ρ and a reduction of the realisation costs [1]–[4]. A power loss reduction and/or increase of the conversion efficiency η was only indirectly required, as the surface area available for power loss dissipation decreases with decreasing converter volume. However, due to environmental concerns, high efficiency is more and more important, so that today at least two design requirements, i.e. high power density and high efficiency, have to be met. This results in a multi-objective design optimisation, where a best possible compromise must be found between the two conflicting criteria, since a higher efficiency usually leads to a higher system volume, i.e. a lower power density.

In the design process, a large number of parameters must be determined and constraints in different physical domains, as e.g. magnetic or thermal properties, and EMI issues must be considered. This is complicated by the fact that many of the design parameters take influence not only on a single design aspect but on different converter properties as given e.g. the switching frequency, which influences the losses in the semiconductors, the cooling system, the design of the magnetics, etc. Accordingly, the set of parameter values which results in an optimal design is difficult to identify.

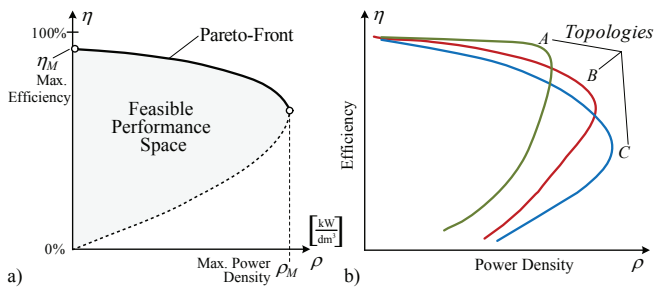

Fig. 1: a) Power density – efficiency plane (ρ-η-plane), where the maximal efficiency η_M and the maximal power density ρ_M as well as the ρ-η-Pareto-Front are shown. The Pareto-Front defines the maximal achievable performance for a compromise between power density and efficiency. b) System Performance Map, which shows the ρ-η-Pareto-Fronts of different converter topologies.

Based on multi-domain converter models [3], [5]–[7], an optimal mapping of the design parameters into the system Performance Space could be performed as described in [8]. There, different design criteria or quality indices could be considered and/or the best compromise of the required system level performances could be determined. Such an optimisation has been performed for telecom power supplies in [3], [4] or for single-phase bridgeless PFC rectifiers in [8], [9]. There, however only a single design criteria (either power density or efficiency) has been maximised, i.e. a 1- dimensional (1D) optimisation has been performed.

With an 1D optimisation, the maximal achievable efficiency and the maximal achievable power density can be identified for a given set of technologies, i.e. for unipolar/bipolar semiconductor switches, core materials, foil/electrolytic capacitors, etc. By simultaneously optimising the efficiency and the power density with different weights a performance limit and/or Pareto-Front could be determined in the ρ-η-plane (cf. Fig. 1a) [8]. The Pareto-Front directly indicates e.g. the maximal achievable efficiency for a required power density or shows how much the efficiency would be sacrificed in case the power density would have to be increased.

In case the Pareto-Limits of e.g. single-phase rectifier topologies would be known the performance of different concepts could be directly compared. This would allow to immediately identify the concept best suited for satisfying a given power density and efficiency requirement (cf. Fig. 1b).

In alternative to optimising the systems with different weights, the Pareto-Front also could be approximated directly by relatively simple analytical models as will be shown in this paper for single-phase PFC rectifiers in the

power range of a few kilowatts. There, the standard PFC boost rectifier, a bridgeless converter and a resonant-transition (i.e. zero voltage switching), triangular current mode (TCM) PFC rectifier are considered and a Topology Performance Map is derived.

First, the considered topologies are shortly discussed with respect to efficiency and power density in **section II**. Thereafter, the equations for calculating approximations of the Pareto-Limit are presented in **section III**. The Pareto-Limits of the different rectifier concepts are calculated in **section IV**. There, also experimental systems for validating the calculations and measurement results are presented.

II. Single-Phase PFC Rectifier Topologies

With the specifications of a converter system given, one of the first steps in the design process is the selection of the converter topology. For single-phase PFC rectifiers numerous topologies are described in literature. The most common concepts are shown in Fig. 2, where the simplest topology is the conventional PFC boost rectifier. However, this converter requires the largest silicon area for achieving a high efficiency as shown in Fig. 3. There, the required chip area for the MOSFET and the number of diodes is shown for the case that all converters have the same conduction losses. All diodes, which are only commutated with mains frequency (D_1-D_4 in Fig. 2a and D_2 &D_4 in Fig. 2c), are replaced by MOSFETs used as synchronous rectifiers in order to reduce the conduction losses.

With the bridgeless PFC rectifier the smallest amount of silicon area, which is proportional to costs, is required for achieving a high efficiency. Consequently, this topology has been used in [9] to optimise a single-phase PFC rectifier for maximal efficiency. There, an efficiency of 99.3% has been achieved at a relatively low switching frequency of 18kHz, which is necessary to limit the switching losses. Due to the low switching frequency, the volume of the boost inductor is large resulting in a relatively low power density of 1.35kW/dm^2.

The hard switching operation of the bridgeless PFC rectifier as well as of the conventional concept and the AC-switch PFC rectifier is a fundamental limitation, since the parasitic capacitances of the MOSFETs and the boost diode are causing losses at the MOSFET turn on. Besides the higher switching losses, this also prevents replacing the fast commutated freewheeling diodes with synchronous rectifiers, since the MOSFETs employed instead of the diodes exhibit a relatively large nonlinear capacitance, which would cause large turn-on current peaks resulting in even higher switching and total losses. Consequently, it is not possible to achieve a high power density and a high efficiency at the same time as will be demonstrated later with the help of Pareto Fronts, which clearly show the limits of the hard switching concepts in the ρ-η-plane.

In order to avoid the capacitive losses occurring for hard switching, a Triangular Current Mode (TCM) resonant-transition single-phase PFC rectifier with a switching scheme according to Fig. 4 has been proposed [10], [12]–[14]. At the top of this figure an equivalent circuit of the converter given in Fig. 2d) with only a single

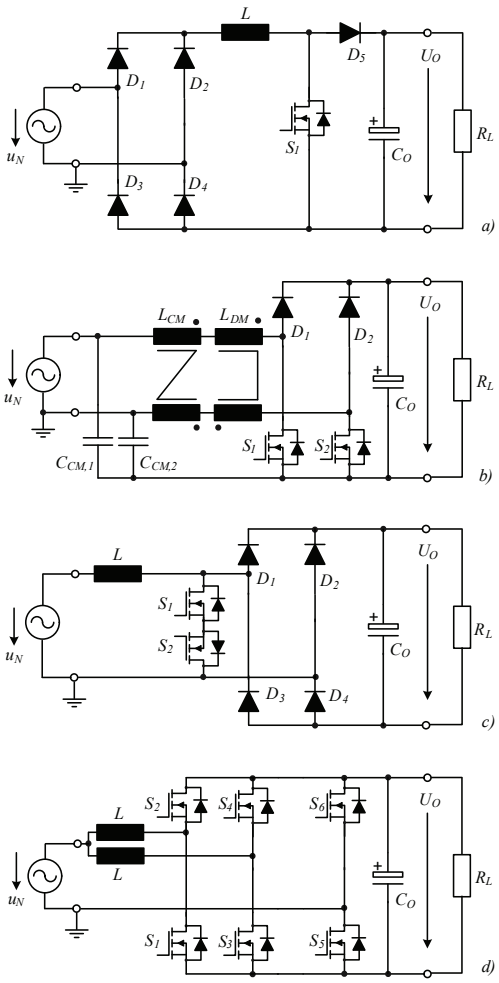

Fig. 2: Schematics of the conventional (a), the bridgeless with integrated CM-filter [8] (b), the AC-switch (c) and the triangular current mode (TCM) resonant-transition PFC rectifier with synchronous rectification [10] (d) are shown. The bridgeless PFC rectifier also could be realised with clamping diodes instead of capacitors C_{CM1} and C_{CM2} [11].

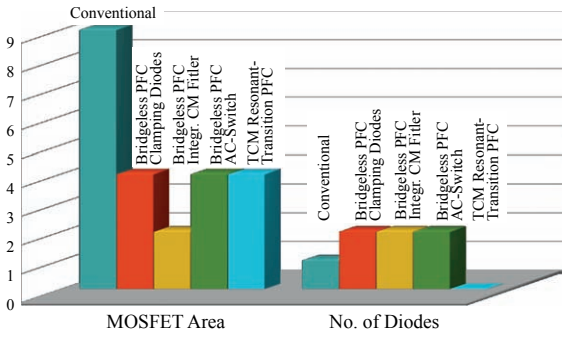

Fig. 3: Total MOSFET chip area for equal conduction losses of the topologies given in Fig. 2. Additionally, the quantity of required fast recovery diodes (SiC) is shown. There, D_1-D_4 in Fig. 2a) and D_2 & D_4 in Fig. 2c) are replaced by MOSFETs (synchronous rectifiers).

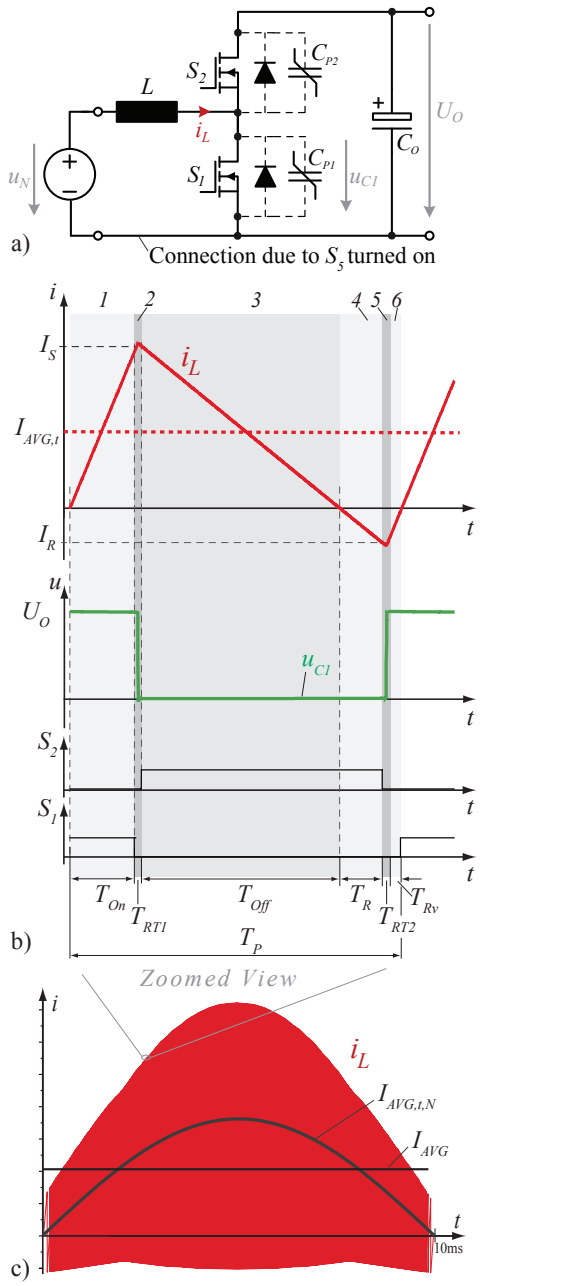

Fig. 4: a) One leg of the TCM resonant-transition PFC rectifier with nonlinear parasitic capacitors $C_{P\nu}$ and b) waveforms of the inductor current i_n and of the voltage u_{C1} across the lower MOSFET.

half bridge leg (e.g. MOSFETs S_1 and S_2 in Fig. 2d) for shaping the input current is shown. This equivalent circuit is valid for the positive mains cycle, where switch S_5 is constantly turned on and not shown in Fig. 4.

In Fig. 4b) the control signals, the voltage across MOSFET S_1, and the inductor current i_L are shown for one switching period T_P. The turn-off current I_S of switch S_1 is always chosen such, that the energy stored in inductor L is large enough to increase voltage u_{C1} up to U_O in order to enable ZVS turn on of switch S_2 after the resonant transition time T_{RT1}. With S_2 turned on, the energy stored in L is transferred to the output capacitor and S_2 acts as synchronous rectifier.

Due to capacitors C_{P1} and especially C_{P2}, which shows a large capacitance for $u_{C1} \approx U_O$, current i_L in L reverses after the time interval T_{off}, so that again energy is stored in L for a resonant-transition of u_{C1} down to zero. Assuming, that the mains voltage u_N is smaller than $U_O/2$ and neglecting losses, switch S_2 can be turned off at the zero crossing of i_L (i.e. at T_R=0 in Fig. 4b) and due to the resonance of L and $C_{P1}||C_{P2}$ voltage u_{C1} reaches zero. Shortly thereafter switch S_1 is turned on at zero voltage and the new cycle starts.

In case $u_N > U_O/2$, the resonance of L and $C_{P1}||C_{P2}$ is not enough to bring u_{C1} down to zero. Therefore, switch S_2 is kept turned on for time T_R after T_{off} and i_L reverses, so that finally the negative amplitude of i_L is increased as shown in Fig. 4. Time T_R is chosen such, that enough energy is stored in L for decreasing u_{C1} down to zero. As soon as i_L is equal to I_R or after time T_R, switch S_2 is turned off and u_{C1} resonates down to zero and S_1 is turn on at ZVS condition.

With this control scheme, the boost diodes can be replaced with synchronous rectifier MOSFETs without causing additional capacitive switching losses. This allows a significant reduction of the conduction losses in the semiconductors. However, the RMS currents in the boost inductor and in switches S_1/S_2 are larger than for the conventional PFC rectifier, as for $u_N > U_O/2$ an additional negative current I_R for achieving ZVS must be generated. With an increased I_R also I_S must be increased in order not to change $I_{AVG,t}$, which is the average current during a switching period. This $I_{AVG,t}$ should show a sinusoidal time behaviour equal to $I_{AVG,t,N}$ as shown in Fig. 4c) and/or its average over half a mains cycle should be equal to the average mains current I_{AVG} required for the desired output power.

The larger RMS current could be compensated concerning the losses by increasing the chip area of S_1/S_2 and/or by reducing the R_{DSon} and consequently the conduction losses. However, for a larger chip area again the RMS current values must be increased as the parasitic capacitances C_{P1} and C_{P2} have a larger value. Furthermore, the gate drive losses increase as the gate charge increases with the chip area. Thus, there is an optimal value for the chip area resulting in minimal overall losses as will be shown below.

The MOSFETs S_1-S_4 connected to an inductor in Fig. 2d) are operating at a high switching frequency and due to the resonant-transition with ZVS conditions. With these MOSFETs the input current is shaped. The return path for the inductor currents is provided by MOSFETs S_5 and S_6, which change their switching state at each zero crossing of the mains voltage, i.e. at very low frequency. This common return path used for all fast switching legs simplifies the control and reduces the circuit complexity.

Due the return path operating at low frequency, the output of the rectifier is always connected to the mains. Consequently, the potential of the output voltage with respect to ground varies only twice during one mains

cycle, so that the generated CM current is relatively small. By interleaving several stages also the DM input ripple could be decreased significantly, so that only a small EMI filter is necessary. Further details about the synchronisation of interleaved bridge legs can be found in [15].

Details about the EMI behaviour of the bridgeless PFC rectifier can be found in [8]. There, a setup with clamping diodes and one with integrated CM-filter has been investigated and measurement results for the bridgeless PFC rectifier are presented.

The MOSFET area for the TCM resonant-transition PFC rectifier shown in Fig. 3 depends on the forward voltage drop of the boost diode, the input current (modulation index) and the specific on-resistance of the MOSFET. In order to obtain the same conduction losses for a 3kW PFC rectifier operating at 230V mains voltage and a specific on resistance of 25mΩcm^2, for the TCM rectifier in total 1.2 times the MOSFET chip area of the bridgeless PFC rectifier with integrated CM-filter would be required. In Fig. 3 for the TCM rectifier it is assumed that the MOSFETs have the same chip area as the bridgeless PFC rectifier with integrated CM-filter, i.e a factor of 2 between the areas is shown. This results in the same conduction losses at low line voltage, but higher efficiency of the TCM rectifier at u_N=230V.

III. Calculation of the ρ-η-Pareto-Limits of Different PFC Rectifier Concepts

For determining the limiting curves in the ρ-η-plane and/or the *Feasible Performance Space* [8], [16], in the following mathematical expressions for the losses and the volumes of the components of the single-phase PFC rectifier topologies discussed in section 2 are derived. These expressions are relatively simple approximations but nevertheless allow an identification of the limits and also of the relative performance of the different topologies.

In contrast to the equations presented in [8], where a direct relation between the power density and the efficiency for the bridgeless PFC rectifier has been derived, here the losses and the volumes are calculated in dependency on the switching frequency and then a parametric plot of the limiting curve is performed. This simplifies the calculation of the Pareto-Front significantly and allows to easily add additional volume and/or loss contributors.

A. Power Semiconductors

First, the losses in the power MOSFETs and the diodes are calculated in dependency of the operating frequency based on general equations for the conventional PFC rectifier. Based on this, the loss equations for the different topologies are derived.

For the loss equations, the RMS and the average currents in the devices are required. These can be calculated with

$$I_{RMS,N} = \frac{P_{IN}}{U_N} \qquad I_{RMS,S} = \sqrt{\frac{1}{2} - \frac{4}{3\pi M}}\hat{I}_N$$
$$I_{AVG,S} = \frac{2}{\pi} - \frac{1}{2M}\hat{I}_N \quad I_{RMS,BD} = \sqrt{\frac{4}{3\pi M}}\hat{I}_N$$
$$I_{AVG,BD} = \frac{1}{2M}\hat{I}_N \qquad I_{RMS,RD} = \frac{1}{2}I_{RMS,N}$$
$$I_{AVG,RD} = \frac{1}{\pi}\hat{I}_N$$

with the modulation index $M = U_O/\hat{U}_N$.

Currents $I_{RMS,S}/I_{AVG,S}$ are the RMS and the average current in the switch, $I_{RMS,BD}/I_{AVG,BD}$ the RMS and the average current in the boost diode and $I_{RMS,RD}/I_{AVG,RD}$ are the characteristic current values of the rectifier diodes.

These equations are all for the conventional boost PFC rectifier and used in the following to determine the losses for the different topologies. There, first the conventional PFC is considered and based on the results the losses for the other topologies are determined.

The conduction losses in the boost diode are

$$P_{V,BD} = U_{F,BD}I_{AVG,BD} + R_{D,BD}I^2_{RMS,BD} \qquad (1)$$

with $R_{D,BD} \sim 1/A_{Chip,BD}$. There, U_{F_BD} is the forward voltage drop and $R_{D,BD}$ the differential resistance of the diode. The differential resistance is linearly dependent on the chip area of the diode $A_{Chip,BD}$, which also determines the value of the parasitic boost diode capacitance. This parasitic capacitance must be charged during turn-on of the boost switch and generates switching losses in the boost switch. The larger the diode chip area is, the lower are $R_{D,BD}$ and the conduction losses, but the higher are the switching losses in the MOSFET. Consequently, there is an optimal value for $A_{Chip,BD}$ resulting in minimal losses. The calculation of the optimal area will be shown below.

In order to achieve a high efficiency and a compact design, switching losses should be minimised, so that it is assumed here that SiC Schottky diodes are utilised as boost diode [17]–[19]. The conduction losses of the rectifier diodes $P_{V,RD}$ can be calculated analogously and the switching losses are negligible.

The conduction losses in the MOSFET can simply be calculated with the on-resistance R_{DSon} and the RMS current. The switching losses are mainly determined by the output capacitance of the MOSFET and the capacitance of the boost diode, which are both discharged via the MOSFET during turn-on. The additional switching losses caused during the commutation of the inductive current are relatively small if a high efficiency is desired, since the time for the commutation decreases linearly with an increasing chip area of the MOSFET. As for a high efficiency a large chip area is required, the commutation losses become relatively small in comparison to the losses due to the output capacitance, which increase with

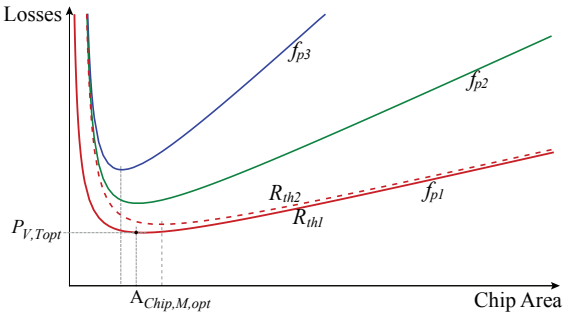

Fig. 5: Dependency of the sum of conduction and capacitive switching losses of a power MOSFET on the chip area $A_{Chip,M}$. The capacitive switching losses are due to the output capacitance C_{oss}. Parameter: Switching frequency f_P and thermal resistance R_{th}. A larger chip area reduces the conduction losses ($R_{DSon} \sim 1/A_{Chip,M}$) but results in increased capacitive losses ($C_P \sim A_{Chip,M}$). Accordingly, depending on f_P minimum total losses are achieved for a chip area $A_{Chip,M,opt}$. For higher thermal resistance $R_{th2} > R_{th1}$ and/or higher junction temperature and on-resistance, the loss minimum is shifted to higher chip areas but despite the larger chip area higher total losses do occur. (Similar relations can be shown for $A_{Chip,BD}$.)

the chip area. Moreover, by decreasing the gate drive resistor, the time for turning on decreases. Therefore, the MOSFET losses are approximately given by

$$P_{V,T} = R_{DSon} I^2_{RMS,S} + f_P \frac{(C_{eq,M} + C_{eq,BD})\, U_O^2}{2} \qquad (2)$$

with $R_{DSon} \sim A^{-1}_{Chip,M}$ and $C_{eq,\nu} \sim A_{Chip,\nu}$. There $C_{eq,M}$ is a constant equivalent capacitance, which results in the same switching losses as the voltage dependent output capacitance C_P of the switching MOSFETs. The voltage dependency of C_P could be approximated by $C_P = C_0 \sqrt{U_O/u_{DS}}$ with $C_0 = C_P$ at U_O. This results in W_{C_P} = 2/3 $C_0\, U_O^2$ for the energy stored in the output capacitance at a blocking voltage U_O. Consequently, the equivalent capacitance is

$$C_{eq,M} = \frac{4}{3} C_0. \qquad (3)$$

Analog considerations can be performed for the capacitance $C_{eq,BD}$ of the boost diode, which also results in the same switching losses as the voltage dependent diode capacitance.

Due to the strongly nonlinear behaviour of C_P of Super-Junction MOSFETs, the turn-off losses are relatively small (ZVS condition) and are neglected in the following.

In (2) it could be seen that the conduction losses decrease and the switching losses increase with increasing MOSFET and/or diode chip area. Therefore, there is an optimal value of the chip areas, which minimises the MOSFET and the boost diode losses. This could be seen in Fig. 5, where the MOSFET losses are plotted as function of the chip area with the switching frequency as parameter.

For determining the optimal chip area the minimum of

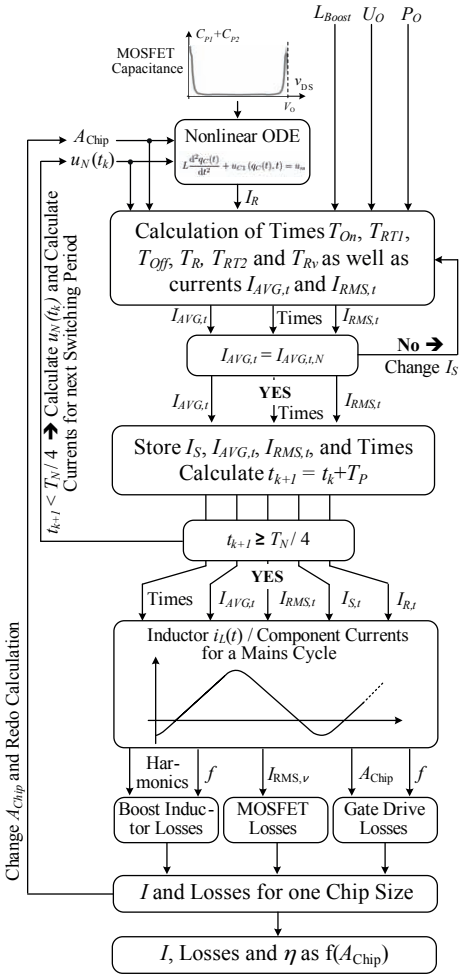

Fig. 6: Flow chart of the procedure for calculating the losses and the RMS currents of the TCM resonant-transition PFC rectifier as function of the chip area for optimising the chip area of the MOSFETs.

the losses

$$\frac{\mathrm{d}\left(P_{V,BD} + f_P \frac{C_{eq,BD} U_O^2}{2}\right)}{\mathrm{d}A_{Chip,BD}} = 0 \;\Rightarrow\; A_{Chip,BD,opt} \qquad (4)$$

$$\frac{\mathrm{d}P_{V,T}}{\mathrm{d}A_{Chip,M}} = 0 \;\Rightarrow\; A_{Chip,M,opt} \qquad (5)$$

must be calculated. In the equation for the optimal diode chip area $A_{Chip,BD,opt}$, also the capacitive switching losses in the MOSFET caused by the parasitic diode capacitance must be considered as these depend also on $A_{Chip,Bd}$.

The temperature dependency of the on-resistance and the differential resistance of the diode is calculated by

$$R_{D,BD} = \frac{1}{G^*_{D,25°C} A_{Chip,BD}} (1 + \alpha_{BD} P_{V,BD} R_{th,j-a,BD})$$
$$R_{DSon} = \frac{1}{G^*_{T,25°C} A_{Chip,M}} (1 + \alpha_T P_{V,T} R_{th,j-a,T}). \qquad (6)$$

There, $R_{th,j-a,\nu}$ is the thermal resistance between the junction of the diode/MOSFET and the ambient and it is

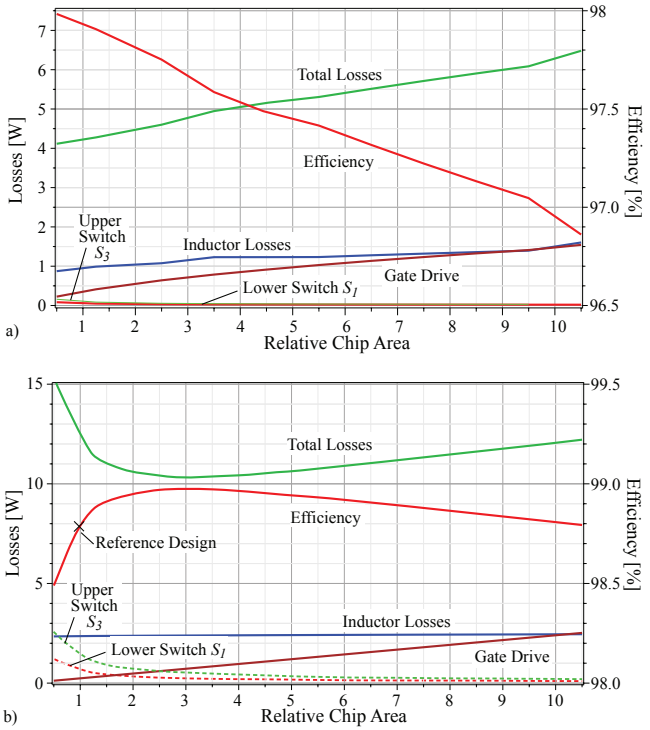

Fig. 7: Variable Losses in a 1kW TCM resonant-transition PFC rectifier with the specifications given in Table I as function of the chip area including losses in the EMI-filter, the output capacitor and the control, which are not shown separately. In a) the loss distribution at 20% output power and in b) for 100% output power are shown.

assumed that no thermal coupling between the semiconductors exists. Including a thermal coupling is basically possible but requires a numerical solution for the optimal chip areas. This is also true if the dependency of the thermal resistance on the semiconductor chip area should be considered $R_{th,j-a,\nu} \sim R_{th,j-a,0,\nu}/A_{Chip,\nu} + R_{th,j-a,HS,\nu}$, where $R_{th,j-a,HS,\nu}$ describes the part of the thermal resistance, which is independent of the chip area (e.g. heat sink). With $G^*_{\nu,25°C}$ the specific conductivity at 25°C and with α_ν the temperature coefficient of the diode/MOSFET on-resistances is denominated.

The losses in the rectifier diodes $P_{V,RD}$ can simply be determined with the forward voltage drop and the average current. In case the rectifier diodes are replaced by synchronous rectifiers (MOSFETs) with an on-resistance $R_{DSon,S}$, the losses are $R_{DSon,S} I^2_{RMS,RD}$.

The total semiconductor losses of the conventional boost rectifier are

$$P_{V,Conv} = P_{V,T} + P_{V,BD} + 2P_{V,RD}. \tag{7}$$

Based on these losses the volume of the heat sink could be calculated as described in the following section. For the bridgeless converter the semiconductor losses could be calculated by

$$P_{V,BL} = P_{V,T} + P_{V,BD} + 2P_{V,RD}. \tag{8}$$

TCM resonant-transition PFC rectifier: For the hard switching PFC topologies, the increase of the optimal chip area of the boost diodes and MOSFETs (i.e. reduction of the conduction losses) is limited by the corresponding increase of the switching losses due to the parasitic capacitances. In the TCM resonant-transition PFC rectifier, the switching losses are eliminated as described in section II and in detail in [10]. However, the RMS currents in the boost inductor and in the switches as well as the required gate drive power still increase with the chip area and an optimal chip area can be calculated. Therefore, the losses in the boost inductor, the switches and the gate drives must be determined in dependency of the semiconductor area following the procedure depicted in Fig. 6.

In this procedure, the currents $I_{AVG,t}$, $I_{RMS,t}$ and the times T_{On}, T_{RT1}, T_{Off}, T_R, T_{RT2}, and T_{Rv} (cf. Fig. 4) are calculated for each switching period separately for a fixed chip area and output power level as described in detail in [10]. There, the time for the resonant transition is determined by solving a differential equation including the nonlinear parasitic capacitances C_{P1} and C_{P2} and the turn off current I_S is determined iteratively until the average current for the considered switching period $I_{AVG,t}$ is equal to required one $I_{AVG,t,N}$. This is repeated until a quarter of a mains cycle is reached.

With the times and the current values for the different switching periods, the boost inductor and the component currents are described by a piecewise linear function for a mains period and the harmonics of the currents are calculated for determining the HF losses in the winding. Furthermore, the RMS and average currents are determined. Thereafter, the chip area is modified and the whole procedure is repeated for the new area. Finally, the currents, the losses and also the efficiency are given as function of the chip area. Further details about the calculation procedure can be found in [10].

In Fig. 7 the resulting losses for the TCM resonant-transition PFC rectifier with the specifications shown in Table I are given as function of the chip area for full output power and for 20% of the nominal load. There, also the gate drive losses are considered, since these also depend on the chip area and finally have a significant influence on the optimal chip area in the TCM PFC rectifier. For the inductor losses a magnetic core E42 made of ferrite material N87 and a litz wire with 420 strands each with a diameter of 0.071mm has been considered. The core losses are calculated with the approach presented in [20] and for the winding losses also the skin and the proximity effect losses are included. Additionally, the constant losses for the controller/auxiliary supply, the ohmic losses for the EMI filter and the losses in the output capacitor due to the high ripple current are considered.

As could be seen, with decreasing output power the optimal chip area decreases rapidly and in order to achieve a high efficiency for a wide operating range for the prototype system shown in Fig. 15 a relative chip area of 1, i.e. a realisation of a switch with a single MOSFET STW77N65M5, has been chosen.

B. Cooling System

The cooling system is a major limitation for the achievable power density, especially in case the efficiency is low, so that a large amount of heat has to be dissipated and a large share of the system volume is occupied by the cooling system. The cooling system volume, i.e. heat sink + fan/pump, is dependent on the applied cooling technique (natural convection, forced air or water cooling), the performance of the fan/pump and the material of the heat sink (e.g. aluminium, copper, graphite). For air cooled systems this dependency could be described with the cooling system performance index (CSPI) defined in [21], where the R_{th} is directly related to the volume of the heat sink by

$$CSPI\left[\tfrac{W}{K dm^3}\right] = \frac{1}{R_{th}\left[\tfrac{K}{W}\right] V_H\,[dm^3]} = \frac{G_{th}\left[\tfrac{W}{K}\right]}{V_H\,[dm^3]}. \quad (9)$$

The thermal resistance could be calculated with the maximal allowed junction temperature $T_{j,max}$ and the semiconductor losses (cf. section III-A), i.e. $R_{th} = P_V/(T_{j,max} - T_A)$, what finally results in the heat sink volume. For forced air cooled systems the CSPI is approximately between 5 for commercial cooling systems and 30 for optimised systems.

C. Input Inductor

Besides the semiconductors, the magnetic components are the main cause for losses in the PFC system. In order to minimise the losses, the design of the inductor, i.e. the geometry and the number of turns must be optimised for minimal losses. As the losses decrease with increasing volume due to the decreasing current and flux density even in case the HF losses are considered as has been shown in [8], the volume must be limited during the design of the inductor. Otherwise, the volume would go to infinity during the optimisation for minimal losses and there are minimal losses for a given inductor volume. In the following the losses are calculated as function of the inductor volume and the optimal number of turns is determined.

These considerations are performed with basic equations neglecting the HF losses, since these depend also on the geometric design of the magnetic component. As has been shown with numerical optimisations for the bridgeless PFC rectifier in [8], the results for the system level Pareto-Limits, which are determined with the basic equations, show the same basic tendency as the curves calculated with the numeric models, but allow a much faster calculation.

The core losses are expressed as function of the geometry and the Steinmetz parameters, which can be obtained from the data sheets of the core material. The flux density is calculated with the winding voltage and the mean turn length l_{MNT} is expressed as function of the cross sectional area of the core A_{Co} and the shape factor k_{SC}. Furthermore, it is assumed that the pulse duration T is proportional to $1/f$.

$$\begin{aligned} P_{Co} &= C B^{\beta} f^{\alpha} V_{Co} = C \left(\frac{UT}{N A_{Co}}\right)^{\beta} f^{\alpha} A_{Co} l_{Co} \\ &= C \left(\frac{U}{N}\right)^{\beta} f^{\alpha-\beta} \frac{1}{\sqrt{k_{CW}}} k_{SC} A_{Co}^{\frac{3}{2}-\beta} \end{aligned} \quad (10)$$

with

$$k_{CW} = \frac{A_{Co}}{A_W} \quad \text{and} \quad k_{SC} = \frac{l_{MNT}}{\sqrt{A_{Co}}}.$$

The winding losses neglecting HF-effects are calculated as function of the geometry, where the cross sectional area of one turn is calculated with the copper fill factor k_{CU} times the window area A_W divided by the number of turns N.

$$\begin{aligned} P_{Wdg} &= R_W I_{RMS}^2 = \frac{N^2 l_W}{\sigma A_W k_{CU}} I_{RMS}^2 \\ &= \frac{N^2 k_{CW} k_{SW}}{\sigma \sqrt{A_{Co}} k_{CU}} I_{RMS}^2 \end{aligned} \quad (11)$$

with $k_{SW} = l_{MNT}/\sqrt{A_W}$.

Since the winding losses increase with the number of turns N and the core losses decrease with N, there is an optimal number of turns N_{Opt} resulting in minimal losses. This N_{Opt} is calculated in the third step and then used to eliminate N in the winding and core loss equations.

By minimising $P_{Co} + P_W$ as function of N with respect to the losses one obtains

$$\begin{aligned} N_{Opt} &= U_I\, D\, 2^{-\frac{1}{2+\beta}} \\ &\cdot \left(\frac{A_{Co}^{2\beta-4} k_{CW}^3 U_I^4 D^4 k_{SW}^2 I_{I,RMS}^4 f^{-2\alpha+2\beta}}{C^2\, \beta^2\, k_{SC}^2\, \sigma^2}\right)^{\frac{-1}{4+2\beta}} \end{aligned} \quad (12)$$

for the optimal number of turns.

For relating the losses and the inductor volume, the core and the winding volume are expressed by

$$V_{Co} = A_{Co} k_{SC} \sqrt{A_W} = A_W^{\frac{3}{2}} k_{CW} k_{SC} \quad (13)$$

$$V_W = A_W k_{SW} \sqrt{A_{Co}} = A_W^{\frac{3}{2}} k_{SW} \sqrt{k_{CW}}. \quad (14)$$

Solving this for the core area and setting $V_L = V_{Co} + V_W$ results in

$$A_{Co} = k_{CW} \left(\frac{V_L}{k_{CW} k_{SC} + k_{SW}\sqrt{k_{CW}}}\right)^{\frac{2}{3}}. \quad (15)$$

Inserting the optimal number of turns and the expression for the core losses in the sum of (10) and (11) and summarising the constants in $k_{\sum} = f(\beta)$ results in the total losses

$$P_L = k_{\sum} V_L^{\frac{4(2-\beta)}{3(2+\beta)} - \frac{1}{3}} f^{\frac{2\alpha-2\beta}{2+\beta}} I_{RMS}^{\frac{2\beta}{2+\beta}} U^{\frac{2\beta}{2+\beta}}. \quad (16)$$

Assuming for example $\beta = 2$ and $\alpha = 1$ results in

$$P_L \sim \frac{U I_{RMS}}{\sqrt{f} V_L^{\frac{1}{3}}} \quad (17)$$

which shows that the losses decrease with an increasing inductor volume. Furthermore, the losses monotonically decrease with higher operating frequencies what is true only if the HF losses are neglected. In reality, the losses increase again at high operating frequencies.

For determining the losses P_L and also for calculating the power density of the system, the volume of the inductor is required. This is related to the switching frequency by the current ripple. Assuming an equivalent DC-DC boost converter with a duty cycle D, the ripple of the inductor current is given by

$$\Delta i_L = \frac{V_I}{L} D T_P \rightarrow \frac{\Delta i_L}{I_L} = \alpha_{\Delta i_L} = \frac{V_I}{I_L L} D \frac{1}{f_P}$$
$$\rightarrow L = \frac{V_I D}{\alpha_{\Delta i_L} I_L} \frac{1}{f_P} \tag{18}$$

with the relative ripple current $\alpha_{\Delta i_L}$.

Furthermore, the inductor volume is approximately proportional to the stored energy, i.e.

$$V_L = \alpha_{V_L} \frac{1}{2} L I_L^2, \tag{19}$$

where α_{V_L} is a technology factor of the inductor, which relates the volume to the stored energy. At higher operating frequencies and higher relative ripple currents, factor α_{V_L} decreases due to thermal limitations. This is neglected in the following, since this would require a thermal model, that depends very much on the geometrical design of the converter.

With the inductance value calculated in (18) and the approximation $I_L \approx I_{L,RMS} \approx I_I$, the inductor volume is

$$V_L \approx \alpha_{V_L} \frac{1}{2} \frac{V_I D}{\alpha_{\Delta i_L} I_I} \frac{1}{f_P} I_I^2 = \frac{D \alpha_{V_L}}{2 \alpha_{\Delta i_L}} \frac{P_I}{f_P} \approx \frac{D \alpha_{V_L}}{2 \alpha_{\Delta i_L}} \frac{P_O}{f_P} \tag{20}$$

assuming a high efficiency, i.e. $P_O \approx P_I$.

With (16) and (20) the losses and the volume of the magnetic device are given as function of the frequency and can be utilised to calculate the Pareto curve. There, the parameters are adapted, so that these fit to the different considered topologies.

D. Output Capacitor

For the output capacitor either electrolytic, film or ceramic capacitors could be used. Electrolytic capacitors offer the highest amount of stored energy per volume. However, the losses in the electrolytic capacitors due to the ESR and the leakage current are the highest. Ceramic capacitors offer a high ripple current capability and a good stored energy per volume, but for realising a high output capacitance a large number of capacitors must be connected in parallel. Furthermore, the capacitors are more sensitive to mechanical forces, what could influence the system reliability, so that in the following the ceramic capacitors are not considered any more. Film capacitors also have a high ripple current capability and low ESR/leakage current, but offer the lowest energy density.

The losses in electrolytic capacitors are given by

$$P_{CE} = R_{ESR,LF} I_{CE,LF}^2 + R_{ESR,HF} I_{CE,HF}^2 + \\ + I_{Leak} U_O \tag{21}$$

where it is assumed that the equivalent series resistance $R_{ESR,HF}$ is constant for all the HF harmonics $I_{C_O,HF}$ and for calculating the losses due to the low frequency ripple current $I_{C_O,LF}$ a separate ESR $R_{ESR,LF}$ is applied. Additionally, the losses due to the leakage current are considered, which are, however, usually quite small.

The energy density of electrolytic capacitors scales approximately linearly with the output voltage [2]. Assuming a constant output voltage, the energy density is fixed and the volume linearly depends on the capacitance value. In the following it is assumed, that the capacitance value of the output capacitor is mainly determined by the ripple current and not by hold up time requirements. Thus, the volume of the electrolytic output capacitor is proportional to the ripple current

$$V_{CE} = \gamma_{V_{CE}}^{-1} I_{C,RMS}, \tag{22}$$

where $\gamma_{V_{CE}}^{-1}$ (energy per volume) is the proportionality factor between the energy and the volume. The ripple current could be directly related to the output power

$$I_{C,RMS}^2 = \frac{1}{M} \left(\frac{4}{3\pi} - \frac{1}{4M} \right) \widehat{I}_N^2 \approx \frac{2M}{U_O^2} \left(\frac{4}{3\pi} - \frac{1}{4M} \right) P_O^2, \tag{23}$$

where M is the modulation index. With this relation the capacitor volume is approximately given by

$$V_{CE} = \gamma_{V_{CE}}^{-1} \frac{P_O}{U_O} \sqrt{\frac{8M}{3\pi} - \frac{1}{2}}. \tag{24}$$

The resulting capacitance value is usually large enough to meet also the voltage ripple requirement.

In contrast to the electrolytic capacitors, the volume of film capacitors scales linearly with the stored energy [2] since the thickness of the capacitor is mainly determined by the thickness of the dielectric layers. Therefore, the volume could be calculated by

$$V_{CF} = \gamma_{V_{CF}}^{-1} \frac{1}{2} C_F U_O^2. \tag{25}$$

In case the output voltage U_O is fixed, the volume just scales with the required capacitance value C_F, which is determined by the allowed ripple voltage. Approximating the capacitor current by a sinusoidal current with an amplitude equal to the average output current, the relative peak output voltage ripple is given by

$$\alpha_{\Delta u_{CF}} = \frac{\widehat{u}_{CF}}{U_O} = \frac{P_O}{4\omega_N} \frac{1}{\frac{1}{2} C_F U_O^2} = \frac{P_O}{4\omega_N} \frac{1}{\gamma_{V_{CF}} V_{CF}}. \tag{26}$$

This could be directly converted to

$$V_{CF} = \frac{P_O}{4\omega_N \alpha_{\Delta u_{CF}} \gamma_{V_{CF}}}, \tag{27}$$

for the volume of the output capacitors based on film technology.

The losses can be evaluated with the same relations as used for the electrolytic capacitors, but the ESR and the leakage current are much smaller, so that the losses often can be neglected.

E. Auxiliary, Control & Gate-Drive

The volume V_{Con} and the power consumption P_{Con} of the control is relatively independent of the applied topology, but slightly depends on the chosen switching frequency. This influence is neglected in the following and just a constant volume and power consumption for the control circuit are assumed.

The volume and power consumption of the auxiliary supply scales with the switching frequency (e.g. gate drive losses), the consumption of the control and with the cooling, i.e. power consumed by a fan/pump. Additionally, a constant power and volume is required e.g. for the control IC of the auxiliary supply or power for a pre-charge relays. Consequently, the volume/power is given by

$$P_{Aux} = P_{Aux,0} + k_{P,Aux} P_{Aux,1} f \tag{28}$$
$$V_{Aux} = V_{Aux,0} + k_{V,Aux} V_{Aux,1} f. \tag{29}$$

With increasing chip area the losses in the gate drive increase as the gate charge increases. Furthermore, the losses increase with switching frequency. Consequently, the gate drive losses for an unipolar gate voltage U_{Gate} are

$$P_{Gate} = Q_{Gate,0} \frac{A_{Chip}}{A_{Chip,0}} U_{Gate} f_P, \tag{30}$$

where $Q_{Chip,0}$ is the reference charge at the reference chip area $A_{Chip,0}$. For the volume of the gate drive only a fixed value is assumed.

F. Overall Systems

In the previous sections, mathematical expressions for the losses in the semiconductors, the boost inductor, gate drives, auxiliary power supply and output capacitor as well as for the volumes of the different components have been derived in dependency of the switching frequency. In order to calculate now the ρ-η-Pareto-Limits of the considered topologies, the total system losses, i.e. the sum of the losses of the individual components, and the system volume are calculated for different frequencies. In case of the bridgeless PFC rectifier with electrolytic capacitors this could be e.g. performed by

$$P_{tot}(f) = P_{V,BL} + P_L + P_{CE} + P_{Con} + P_{Aux} + P_{Gate} \tag{31}$$
$$V_{tot}(f) = V_H + V_L + V_{CE} + V_{Con} + V_{Aux} + V_{Gate}. \tag{32}$$

The resulting values for the losses and for the volume are plotted as parametric plot in the ρ-η-plane. The results are discussed in section IV. In these equations easily further component losses/volumes can be added.

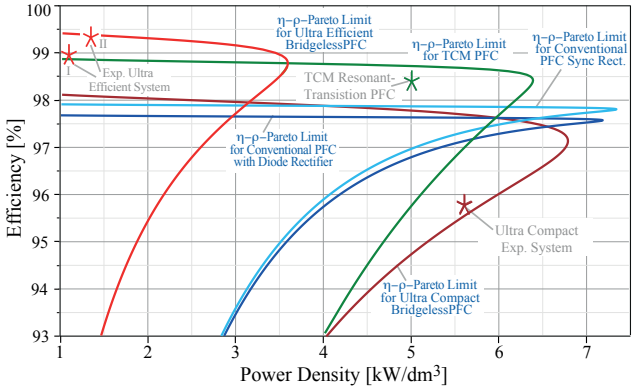

Fig. 8: ρ-η-Pareto-Limits for the conventional, the bridgeless and the TCM resonant-transition PFC rectifier. For the bridgeless PFC concept two technology sets – one facilitating high power density and one facilitating high efficiency – are shown. The dark blue curve shows the limits for the conventional PFC rectifier with diode bridge and the light blue curve for a system with synchronous rectifiers. The the curves are calculated for systems with parameters optimised for operation only at nominal voltage u_N=230V.

TABLE I: Specifications of the single-phase PFC rectifiers. The nominal output power of the TCM resonant-transition PFC rectifier is 3kW.

Output power P_O	3.2kW
Line voltage U_N	230V±10%
Output voltage U_O	365V
Ambient Temperature	45°C

IV. Topology Performance Map and Sensitivity Analysis

Based on the algorithms and models presented in section III, the ρ-η-Pareto-Limits are calculated for the topologies presented in section II and the specifications given in Table I. The results for systems optimised for u_N = 230V are shown in Fig. 8, where the limits for the conventional PFC rectifier, for the bridgeless PFC system and for the TCM resonant-transition PFC rectifier as well as the performance of prototypes of the systems (cf. next section) are depicted. For the bridgeless PFC rectifier two different technology sets, one optimised for efficiency (natural convection, large inductor volume, low loss EMI-filter, etc.) and one optimised for power density (forced air cooling, small inductor volume, compact auxiliary power supply, etc.) are considered.

This ρ-η-Performance-Map clearly reveals the performances achievable with the different topologies and technologies. For example, for achieving an ultra-high efficiency the bridgeless topology with integrated EMI-filter (cf. Fig. 2b) is a very promising candidate if it is combined with technologies as e.g. control circuit, auxiliary supply, cooling, EMI filter which are optimised for minimal losses. As already mentioned, the required silicon area for the bridgeless converter is relatively small compared to the other topologies. Similar efficiency values can be achieved with the TCM resonant-transition PFC rectifier. However, a slightly larger silicon area is required for the switches.

The ultra-high efficiency values are all achieved at

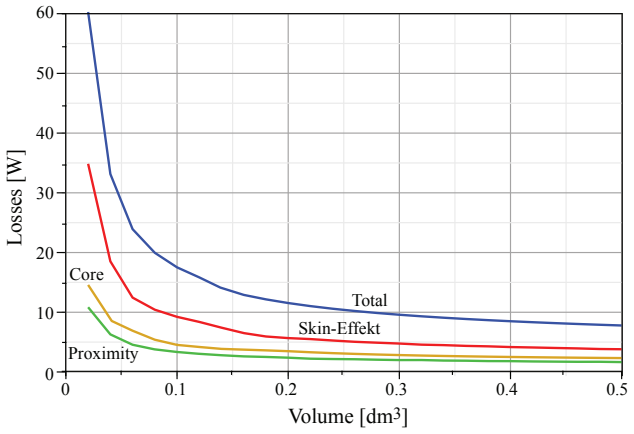

Fig. 9: Winding losses, i.e. resistive losses considering skin and proximity effect and core losses of an inductor in dependency of the inductor volume. The core geometry is optimised for minimum total losses; winding losses due to the fringing field of the air gap are not considered. An increase of the overall inductor volume results in a reduction of the total losses.

low switching frequencies, which limit the HF losses in the magnetic components and keep the switching losses low in case of the hard switched topologies. During the optimisation for minimal losses the volume of the magnetic components must be limited, since the losses monotonically decrease with increasing volume as could be seen for example in Fig. 9. There, the winding and the core losses including HF-effects of an inductor are shown as function of the inductor volume.

At the low switching frequencies, the switching losses are low and the chip area could be increased in order to reduce the conduction losses (cf. Fig. 5). This reduces the size of the heat sink for the semiconductors. However, the volume of the inductor must be increased in order to limit the current ripple at the low switching frequency and in order to reduce the losses. Consequently, the ultra-high efficiency comes with a relatively low power density. This is also validated by two ultra-efficient prototype systems which are discussed in detail in [8] and [9]. The prototype system showing the highest efficiency is also shortly presented in section IV-B.

By increasing the switching frequency the inductor value decreases and therewith also the volume. However, the switching/gate drive losses increase, so that with the increasing power density, efficiency drops. This could be also seen in Fig. 8, where all the Pareto-Limits in the ρ-η-plane start at the left hand side with low switching frequency. The parameter with which one moves along the Pareto-Limits is the operating frequencies, which reaches values in the range of approximately 500kHz in the area of the sharp bend. At this point the power density as well as the efficiency drops resulting in non-optimal designs.

In Fig. 8 it could be seen that the efficiency of the bridgeless PFC rectifier drops slightly faster with increasing power density than the efficiency of the conventional system since with the bridgeless PFC rectifier, the chip area of both MOSFETs (S_1 and S_2 in Fig. 2b) must be decreased with increasing switching frequency in order to limit the switching losses. However, in the bridgeless PFC rectifier one of the MOSFETs is constantly turned on and provides the return path for the current, which becomes more and more lossy with increasing switching frequency due to the reduced chip area. In case of e.g. the conventional PFC rectifier, the return path (either diode or synchronous rectifier) is unaffected by the increasing switching frequency. In the graphs shown in this paper a fixed chip area is assumed for the return MOSFETs of the TCM resonant-transition PFC rectifier as well as for the synchronous rectifier MOSFETs.

This is also true for the TCM resonant-transition PFC rectifier, which has a separate return path, that operates at low frequency. With this rectifier topology also the best compromise between power density and efficiency could be achieved. Power density values up to 5kW/dm^3 at efficiencies higher than 98% are possible.

It is important to note, that in all the ρ-η-Performance-Maps shown in this paper always the net volume, i.e. only the component volume without additionally required volume for interconnection and mounting, is used for calculating the power density. Thus, the power density values shown in the graphs typically must be reduced by 20%-25% for real systems, what also could be seen for the depicted performances of the prototype systems, which are lower than the calculated maximal power density values but still show outstanding power density values.

So far in the ρ-η-plane given in Fig. 8 only one operating point, i.e. in the depicted case the nominal operating point (u_N), has been considered. In case of a wide operating range, a design compromise is required due to the strongly varying mains currents for u_N=100V and for u_N=230V. This affects also the achieveable power density and efficiency values as could be seen in Fig. 10a), where the Pareto-Limits in the ρ-η-plane are given for an input voltage of u_N = 100V in a). Due to the high mains current the achievable efficiency values significantly drop. In case of the bridgeless PFC rectifier approximately by 0.5%-0.75% and for the conventional and the TCM resonant-transition system by significantly more. There, it is important to note, that the chip area of the return MOSFETs of the TCM resonant-transition PFC rectifier as well as for the synchronous rectifier MOSFETs is the same as in case of the design optimised for u_N = 230V. Increasing these chip areas results approximately in an efficiency drop of 1% for the conventional and the TCM resonant-transition PFC rectifier compared to the case where the systems where optimised only for operation at u_N = 230V and also increased chip area.

In case of a wide input voltage range operation, also the efficiency values at u_N = 230V drop as could be seen in Fig. 10b) where the limiting curves for operation at u_N = 230V are shown. There, the system parameters are chosen so, that the system could operate also at low line (u_N=100V), i.e. at high input current, what for example

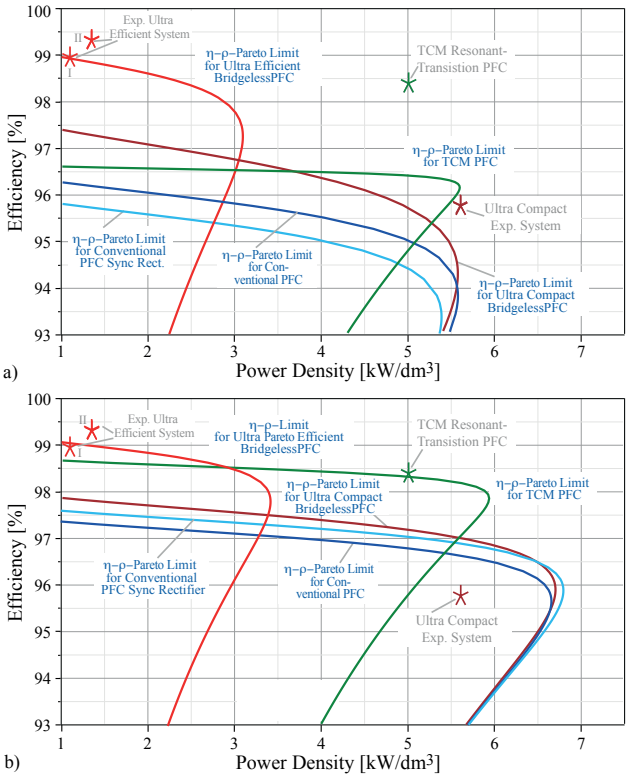

Fig. 10: The same limiting curves in the ρ-η-plane as shown in Fig. 8 but in a) for low line operation, i.e. with an input voltage of 100V. In b) the limiting curves of the systems with parameters optimised for low line operation, i.e. the chip area and the inductor are designed for the high input current at u_N = 100V, are shown for nominal input voltage (u_N = 230V). There, it could be seen that due to the wide input voltage range, the Feasible Performance Space is reduced since the designs need to be a compromise between optimal operation for high and for low line operation.

results in a larger chip area that causes higher switching losses at u_N=230V. Compared to the systems where only the nominal operating point (u_N=230V) is considered for determining the parameters, the maximal efficiency drops by approximately 0.5% for all systems.

The shown Pareto-Limits in the ρ-η-plane are typical for heterogeneous systems which consist of semiconductors, magnetics and other passive components. In these systems often the volume distribution between the passives and the cooling is relatively balanced in case of optimised system parameters. For systems which only consist of a cooling system and passive components (e.g. DC link capacitor) that are relatively independent of the operating frequency as for example given in inverter drives, the limiting curves are very different, since such system do not have components, which could be made more compact at the expense of the efficiency. Consequently, the Pareto-Limits shows an increasing efficiency with increasing power density, since the cooling system becomes smaller for higher efficiency values. An example for such a line is given in Fig. 11, where all the losses/volumes of the ultra-efficient bridgeless PFC rectifier are included except for the inductor losses/volume. The achievable maximal power density depends in this

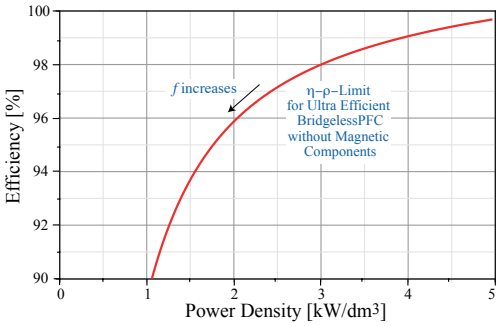

Fig. 11: Limiting curves in the ρ-η-plane for the bridgeless PFC rectifier, when the volume and the losses of the magnetic components are neglected. The maximal achievable power density is determined by the constant volume contributions as e.g. the output capacitor or the control and is reached at very low switchting frequencies, where the semiconductor losses become negligible, i.e. the volume of the heat sink becomes zero.

case on the volume of the heat sink and the volumes of the components which are independent of the operating frequency (e.g. output capacitor, control, gate drive). The maximal power density and efficiency is reached for the smallest operating frequency and the power density and efficiency drops with increasing switching frequency due to the switching/gate drive losses.

In the heterogeneous systems for each system a compromise between the power and the efficiency has to be made as the efficiency decreases with increasing power density. In order to compare different systems a performance indicator as

$$\tan \alpha_D = \frac{1-\eta_D}{\rho_D} \tag{33}$$

could be used [22], where α_D is the angle between a horizontal line and a line starting at ρ=0, η=1 and ending at ρ_D, η_D of the considered system. Further details can be found in [22].

Note: Strictly speaking, the Pareto optimal solutions are only the upper part of the Pareto-Limits in the ρ-η-plane starting at the left hand side at small frequencies and ending at the point where the highest power density is achieved. The part below the maximal power density represents non-optimal solutions, since for the considered power density a higher efficiency is possible (at a lower operating frequency).

A. DC-DC Converter

Based on the approach presented in section III also the limiting curves for other systems as e.g. DC-DC converters can be calculated. In Fig. 12 the resulting curves are shown for a current doubler rectifier, for which in [4] a highly compact prototype system was presented. In [4] also some basic analytic models are presented for calculating the losses and the volumes. Details are omitted here for the sake of brevity and will be published in a future paper. A comparison between different DC-DC converter topologies with respect to power density could

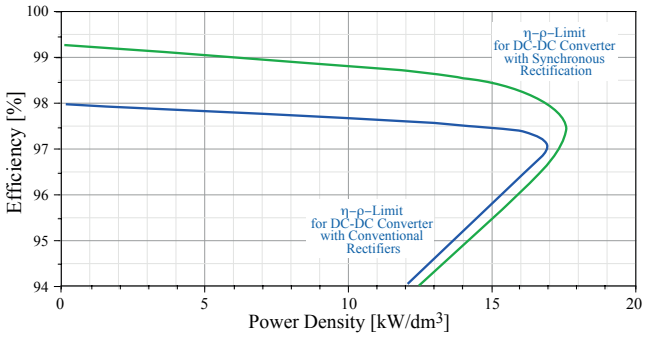

Fig. 12: Limiting curves in the ρ-η-plane for a current doubler DC-DC converter with the specifications given in Table II.

TABLE II: Specifications of the considered current doubler DC-DC converter.

Output power P_O	5kW
Input voltage U_{IN}	400V
Output voltage U_{Out}	48V
Ambient Temperature	45°C

be found in [23]. The efficiency limit of a phase-shift DC-DC converter with voltage output has been evaluated in [24], [25], where a maximal efficiency of 99% has been achieved.

B. Experimental Results

In order to validate the presented models and calculations, different prototype systems have been realised and tested. In Fig. 13 a 3.2kW ultra high efficiency PFC rectifier based on the bridgeless topology (cf. Fig. 2b) with the specifications given in Table I is shown. This converter has an efficiency of 99.3% [9], and a power density of 1.35kW/dm^3. With the focus on power density the bridgeless PFC system shown in Fig. 14 has been designed, where a power density of 5.6kW/dm^3 at an efficiency of 95.6% has been achieved. The 3kW prototype system of the TCM resonant-transition PFC as given in Fig. 15 has been built. It consists of three interleaved 1kW units resulting in a much smaller input current ripple and has a power density of 5kW/dm^3 at an efficiency of 98.3%. In Fig. 16 measurement results for nominal output power are shown, where it could be seen, that the mains current is sinusoidal and the system operates as predicted.

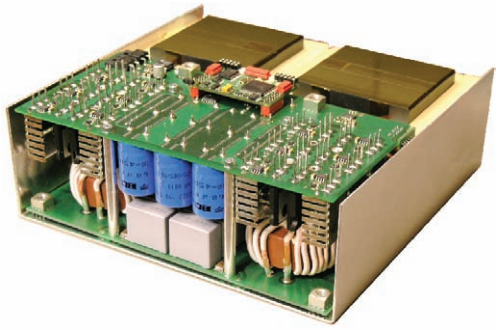

Fig. 13: Laboratory prototype of the ultra-efficient 3.2kW bridgeless PFC rectifier composed of two interleaved 1.6kW units with f_P=16kHz; overall dimensions: 190mm×188mm×65mm; output power density: 1.35 kW/dm^3, efficiency: 99.3%. (V_{in}=230V, V_{out}=365V).

Fig. 14: Prototype of the ultra-compact 3.2kW bridgeless PFC rectifier composed of two interleaved 1.6kW units; overall dimensions: 175mmx80mmx42mm; output power density: 5.6kW/dm^3.

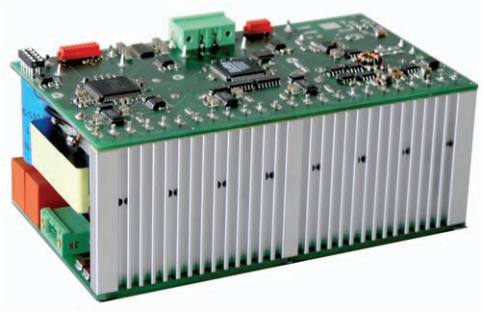

Fig. 15: Laboratory prototype of the ultra-efficient and ultra-compact 3kW TCM resonant-transition PFC rectifier with the specifications and components given in Table I. Dimensions: 137×56×78mm^3, power density: 5kW/dm^3, efficiency ≈ 98.3%.

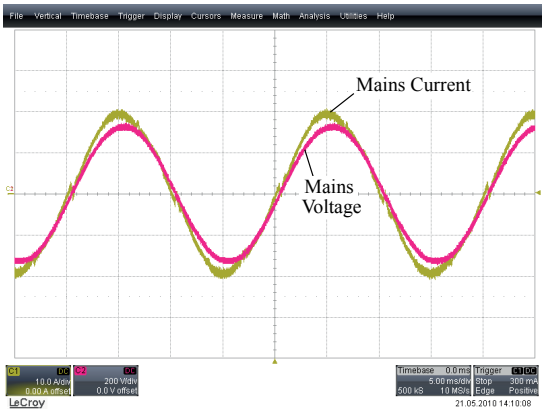

Fig. 16: Measured mains voltage and current for the TCM resonant-transition prototype system shown in Fig. 15 for P_{Out} = 3kW.

V. Conclusion

In this paper the mapping functions, defining the relation of the material parameters and/or components performance and the system performance (efficiency/power density) are analysed for single-phase PFC rectifier systems. There, the conventional, the bridgeless and a TCM (Triangular Current Mode) resonant-transition PFC rectifier are considered and a relatively simple approach is presented to determine the limiting Pareto curves of the different systems in the ρ-η-plane.

These limiting curves define the boundary of the Performance Space in the ρ-η-plane for the different topologies, i.e. the performance of the different topologies with repsect to power density and/or efficiency could be directly identified. Consequently, this topology performance map significantly simplifies the topology selection based on the desired system performance requirements. It has been for example demonstrated that with the TCM resonant-transition PFC rectifier the best compromise between power density and efficiency could be achieved, which could not be reached with the other considered topologies.

For validating the considerations different prototype systems are presented, which nicely confirm the presented limiting curves.

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REFERENCES

[1] H. Ohashi, "Research activities of the power electronics research center with special focus on wide band gap materials," *Proc. of the 4th Conf. on Integrated Power Systems, Napels, Italy*, pp. 153–156, 2006.

[2] J. W. Kolar, U. Drofenik, J. Biela, M. L. Heldwein, H. Ertl, T. Friedli, and S. D. Round, "PWM converter power density barriers," in *Proc. of the Power Conversion Conf. (PCC), Nagoya*, 2-5 April 2007, pp. 9–29.

[3] J. Biela, U. Badstuebner, and J. W. Kolar, "Design of a 5-kW, 1-U, 10-kW/dm^3 resonant DC-DC converter for telecom applications," *IEEE Transactions on Power Electronics*, vol. 24, no. 7, pp. 1701–1710, 2009.

[4] U. Badstübner, J. Biela, B. Fässler, D. Hösli, and J. W. Kolar, "An optimized 5kW, 147W/in^3 telecom phase-shift DC-DC converter with magnetically integrated current doubler," in *Proc. of the 24$^{\mathrm{th}}$ IEEE Applied Power Electronics Conference (APEC)*, 2009, pp. 21–27.

[5] C. J. Wu, F. Lee, S. Balachandran, and H. L. Goin, "Design optimization for a half bridge DC-DC converter," in *IEEE Transactions on Aerospace and Electronic Systems*, vol. AES-18, no. 4, 1982, pp. 497–508.

[6] S. Busquets-Monge, J.-C. Crebier, S. Ragon, E. Hertz, D. Boroyevich, Z. Gurdal, M. Arpilliere, and D. K. Lindner, "Design of a boost power factor correction converter using optimization techniques," *IEEE Transactions on Power Electronics*, vol. 19, no. 6, pp. 1388–1396, 2004.

[7] S. Busquets-Monge, G. Soremekun, E. Hefiz, C. Crebier, S. Ragon, D. Boroyevich, Z. Gurdal, M. Arpilliere, and D. K. Lindner, "Power converter design optimization," *IEEE Industry Applications Magazine*, vol. 10, no. 1, pp. 32–38, 2004.

[8] J. W. Kolar, J. Biela, and J. Miniboeck, "Exploring the Pareto front of multi-objective single-phase PFC rectifier design optimization - 99.2% efficiency vs. 7kW/dm^3 power density," in *Proc. of the 6$^{\mathrm{th}}$ IEEE Power Electronics and Motion Control Conf. (IPEMC)*, 2009.

[9] J. Biela and J. Kolar, "Optimal design of a compact, 99.3 % efficient single-phase PFC rectifier," in *Proc. of the 25$^{\mathrm{th}}$ IEEE Applied Power Electronics Conference (APEC)*, February 2010.

[10] J. Biela, D. Hassler, J. Miniboeck, and J. Kolar, "Optimal design of a 5kW/dm^3 / 98.3% efficient TCM resonant transition single-phase PFC rectifier," in *Proc. of the IEEE/IEEJ International Power Electronics Conference (ECCE Asia/IPEC)*, June 2010.

[11] Y. Jang and M. M. Jovanovic, "A bridgeless PFC boost rectifier with optimized magnetic utilization," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 85–93, 2009.

[12] J. W. Kolar, J. Miniböck, J. Biela, and C. Marxgut, "Bidirektionaler, verlustarm schaltender Konverter (Modulation and topology for a bidirectional, soft switching PFC converter)." Patent Application, 2009.

[13] J. W. Kolar, J. Biela, and D. Hassler, "Bidirektionaler, verlustarm schaltender Konverter (Control concept and topology for a bidirectional, soft switching PFC converter)." Patent Application, 2010.

[14] C. Marxgut, J. Biela, and J. W. Kolar, "Design of a multi-cell, DCM PFC rectifier for a 1mm thick, 200W off-line power supply – The Power Sheet," in *Proc. of the 6$^{\mathrm{th}}$ International Conference on Integrated Power Electronic Systems (CIPS), Nuremberg, Germany*, 2010.

[15] ——, "Novel interleaved bridgeless PFC rectifier topology for high efficiency, high power density systems," in *Proc. of the IEEE/IEEJ International Power Electronics Conference (IPEC/ECCE Asia), Sapporo, Japan*, 2010.

[16] D. Mueller, G. Stehr, H. Graeb, and U. Schlichtmann, "Deterministic approaches to analog performance space exploration (PSE)," in *Proc. of the 42$^{\mathrm{nd}}$ Design Automation Conference*, June 13-17 2005, pp. 869–874.

[17] M. Janicki, D. Makowski, P. Kedziora, L. Starzak, G. Jablonski, and S. Bek, "Improvement of PFC boost converter energy performance using silicon carbide diode," in *Proc. International Conference Mixed Design of Integrated Circuits and System (MIXDES)*, 2006, pp. 615–618.

[18] G. Spiazzi, S. Buso, M. Citron, M. Corradin, and R. Pierobon, "Performance evaluation of a Schottky SiC power diode in a boost PFC applications," *IEEE Transactions on Power Electronics*, vol. 18, no. 6, pp. 1249–1253, 2003.

[19] A. R. J. Hefner, R. Singh, J.-S. Lai, D. W. Berning, S. Bouche, and C. Chapuy, "SiC power diodes provide breakthrough performance for a wide range of applications," *IEEE Transactions on Power Electronics*, vol. 16, no. 2, pp. 273–280, 2001.

[20] K. Venkatachalam, C. R. Sullivan, T. Abdallah, and H. Tacca, "Accurate prediction of ferrite core loss with nonsinusoidal waveforms using only Steinmetz parameters," in *Proc. of the IEEE Workshop on Computers in Power Electronics (COMPEL)*, 2002, pp. 36–41.

[21] U. Drofenik, G. Laimer, and J. W. Kolar, "Theoretical converter power density limits for forced convection cooling," in *Proc. of the Power Conversion and Intelligent Motion (PCIM)*, June 2005, pp. 608–619.

[22] J. W. Kolar, J. Biela, S. Waffler, T. Friedli, and U. Badstuebner, "Performance trends and limitations of power electronic systems," in *Proc. of the 6$^{\mathrm{th}}$ International Conference on Integrated Power Electronic Systems (CIPS), Nuremberg, Germany*, 2010.

[23] J. Biela, U. Badstuebner, and J. W. Kolar, "Impact of power density maximization on efficiency of dc-dc converter systems," *IEEE Transactions on Power Electronics*, vol. 24, no. 1, pp. 288–300, 2009.

[24] U. Badstuebner, J. Biela, and J. W. Kolar, "Design of an 99%-efficient, 5kW, phase-shift PWM DC-DC converter for telecom applications," in *Proc. of the 25$^{\mathrm{th}}$ IEEE Applied Power Electronics Conf. and Exposition (APEC)*, February 2010, pp. 773–780.

[25] ——, "An optimized, 99% efficient, 5kW, phase-shift PWM DC-DC converter for data centers and telecom applications," in *Proc. of the International Power Electronics Conference (IPEC / ECCE Asia), Sapporo, Japan*, June 2010.