ACTIVE GATE CONTROL FOR CURRENT BALANCING IN PARALLEL CONNECTED IGBT MODULES IN SOLID STATE MODULATORS

D. Bortis, J. Biela and J.W. Kolar
Power Electronics System Laboratory (PES)/ ETH Zurich
Physikstrasse 3, Zurich, Switzerland

Abstract - **In modern pulsed power systems often fast solid state switches like MOSFETs and IGBT modules are used to generate short high power pulses. In order to increase the pulsed power, solid state switches have to be connected in series or in parallel. Depending on the interconnection of the switches, parameter variations in the switches and in the system can lead to an unbalanced voltage or current. Therefore, the switches are generally derated, which results in an increased number of required devices and volume. With an active gate control, derating and preselection of the switching devices can be avoided.**
In this paper an active gate control of paralleled IGBT modules, which has been developed for converters with inductive load, is explained in detail and adapted to a solid state modulator. There, the paper focuses on the low inductance IGBT current measurement, the control unit implementation with a FPGA and DSP, as well as the balancing of the pulse currents.

I. INTRODUCTION

Over the last few decades, developments in semiconductor technology have lead to today's high current and voltage rated IGBTs. This enables the substitution of older switch technologies (e.g. thyratrons, ignitrons or spark gaps) in various high power applications, such as solid state modulators with several MW pulse power. However, due to the lower blocking voltage of IGBTs (usually ≤6.5kV) compared to that of thyratrons (tens of kV), higher currents (10-20 kA) have to be switched to achieve the same pulsed power. Another possibility is to connect IGBTs in series.
For large currents, high power IGBT modules have to be connected in parallel, as shown for the solid state modulator in **Figs. 1** and **2.** In **Table 1** the specifications of the solid state modulator are given.

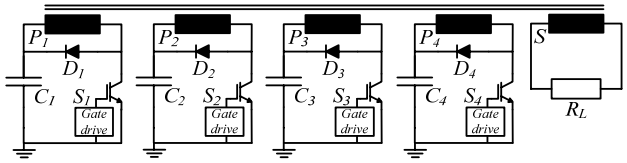


Figure 1: Schematic of the solid state modulator with four paralleled IGBT modules and pulse transformer with four primary windings and one secondary winding.

Due to tolerances in IGBT parameters, the geometry of the modulator and different propagation delays in driver circuits, a symmetric current balancing between the parallel connected IGBTs is not always guaranteed. To ensure a safe operation the IGBTs have to be derated, which results in an oversized design. To achieve a better current balancing the manufacturer commonly preselects the IGBTs depending on the relevant parameters of the IGBT. But also after this costly classification the maximal power ratings of the IGBT must be reduced.

In [1] an active gate control to symmetrize the currents in converters with paralleled IGBTs and inductive load is presented, where no derating or preselection of the IGBTs is required. To balance the current among all IGBT modules, first the current is measured with a broad band current probe [2]. Then, depending on the transient and static currents in each IGBT, the switching times and gate voltage of the individual IGBT are adjusted, which finally results in a balanced current distribution.

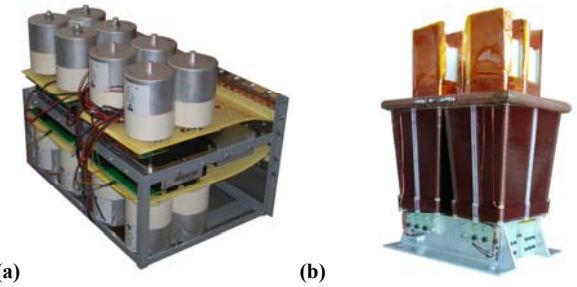


Figure 2: Solid state modulator: (a) Four 3.6kA-IGBT Modules plus capacitors/freewheeling diode connected to corresponding primary windings of the pulse transformer in (b).

Table 1: Specifications of the considered solid state modulator.

Pulse generator voltage V_{pulse}	*1kV*
Pulse generator current I_{pri}	*20kA*
Pulse duration T_{pulse}	*5us*
Pulse repetition frequency f_{rep}	*200Hz*

In this paper the active gate control for paralleled IGBTs based on [1] is adapted to solid state modulators. First, in **Section II** the active gate control, as implemented for the solid state modulator, is explained in detail. Thereafter, the low inductive current measurement in the individual IGBT modules, which is a key component of the active gate control, is described in **Section III.** Due to the short current pulses in the solid state modulator, a PCB-Rogowski coil with additional measurement electronics is applied. The signals from the measurement circuit are fed to a control unit, based on a DSP and FPGA, which is described in **Section IV**. In **Section V** experimental results of the current measurement circuit and the active gate control are presented.

II. ACTIVE GATE CONTROL FOR CURRENT BALANCING

Due to tolerances of the device parameters / modulator geometry a derating of parallel connected IGBTs accounting for a possible unbalanced current distribution is usually required. In order to avoid this derating, two different approaches for achieving an equal current distribution have been proposed.

One possibility is to insert additional components, like series resistances or chokes, in the current path. The series resistances, however, result in additional losses and chokes slow down the rising and falling edges of the pulse. Alternatively, the currents can be balanced with an active gate control, which does not use series elements [1] and which will be examined in the following.

The only drawback of the active gate control is the need of a current measurement circuit for each IGBT, a more complex gate drive circuit and a parameter initialization before normal operation as explained below.

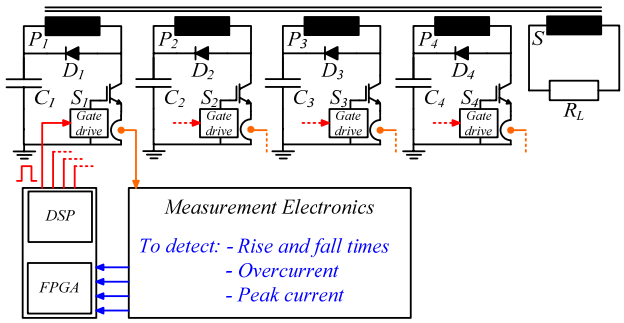


Figure 3: Block diagram of the modulator with active gate control.

In **Fig. 3** the schematic of a solid state modulator with four paralleled branches and the block diagram of the active gate control are shown. Each branch can be divided into a power and a control part. The power part consists of a storage capacitor C_i, an IGBT module S_i, a freewheeling diode D_i and a primary winding P_i, whereas the control loop embodies a gate drive circuit, a current probe and a measurement electronic for detecting the rise and fall times as well as the peak values of the current pulses. The control loop of each branch is closed with one control unit for all four IGBT modules. To achieve simultaneous turn on and off as well as an equal current distribution the active gate control is divided into a *rise and fall time control* and a *peak current control*, which will be explained in the following.

Fig. 4 schematically shows possible unbalanced current waveforms of the four paralleled branches without active gate control, where all gates are triggered at the same time with the same gate voltage. At a predefined trigger level I_{trig} the point of time of each rising and falling edge $t_{r1}\ldots t_{r4}$ / $t_{f1}\ldots t_{f4}$ is detected.

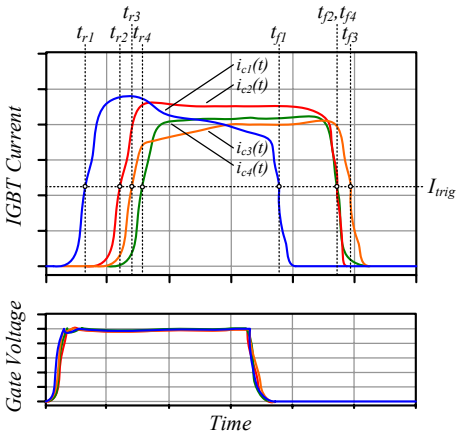


Figure 4: Schematic example for unbalanced current waveforms without *rise and fall time control* showing rise and fall time detection at the trigger level I_{trig}.

Before the next pulse is triggered the *rise and fall time controller* shifts the turn on and off times of the gate signals depending on the time delay compared to a master pulse, whereas any branch can be selected as the master. To achieve the desired pulse duration T_{Pulse} also the turn off point of time t_{fi} of the master has to be adapted.

The example current waveforms, as shown in **Fig. 5,** result with the shifted turn on/off times of the gate signals.

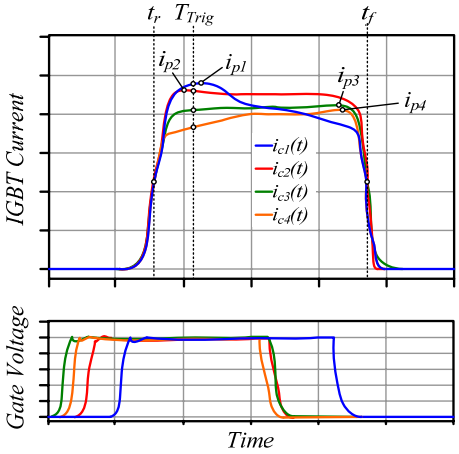


Figure 5: Schematic examples for IGBT current pulses with synchronized rising and falling edges based on shifted gate signals. Furthermore, the detection of the current amplitudes at the time T_{Trig} and the peak currents i_{pi} are shown.

To achieve fast rise and fall times, which are required in many applications, the IGBT modules must be fully turned on/off at the beginning/end of the pulse. Therefore, the IGBTs can not be operated in the linear mode and the static current can not be controlled with the amplitude of the gate voltage as described in [1].

Nevertheless, the derivative/slope of the collector current ic can be controlled with the gate voltage vG [1] based on

$$\frac{di_C}{dt} = \frac{v_G - v_{th}}{\frac{R_g C_{gs}}{g_m} + L_\sigma} \qquad (1)$$

where an operation in the linear mode is avoided since v_g is always significantly larger than the threshold voltage v_{th}. In (1) R_g is the gate resistance, C_{gs} the gate-source-capacitance, g_m the transconductance of the IGBT and L_σ the parasitic inductance of one branch (IGBT, $C_{\square}$ and primary P_i).

Therefore, current balancing at the beginning of the pulse can be achieved by controlling the slope of the current with the gate voltage v_G and synchronizing the rising edge of the pulse as described above. In case IGBTs with positive temperature coefficient of the on-voltage (e.g. Non-Punch-Through IGBTs) are applied also a static current balancing can be achieved by applying this method, since a larger IGBT current leads to an increasing on-voltage what balances the currents automatically.

In order to determine the current slope/gate voltage v_G, the amplitudes of the IGBT currents are required. These are sampled at the time T_{Trig} (cf. **Fig. 5**), which could be defined by the user via the DSP. With the current amplitudes the gate voltages are determined based on (1), so that the slopes of the IGBT currents are equalized before the next pulse.

Additionally, the absolute maximum values i_{p1} to i_{p4} of the IGBT current pulses are detected (cf. **Fig. 5**) and monitored, in order to guarantee balanced IGBT currents.

In **Fig. 6** the resulting IGBT current pulses with *rise and fall time control* and slope synchronization are shown. There, the amplitude as well as the points of time of rising/falling edges of the gate signals have been adjusted.

Remark: Before normal operation of the modulator the presented active gate control requires a few pulses at reduced output power, in order to determine the appropriate shift of gate signals and the amplitude of the gate signal, so that the currents are balanced.

During normal operation the variation of the parameters due to temperature drift is relatively small and slow, so that the correction of a measured current unbalance at the successive pulse is sufficient.

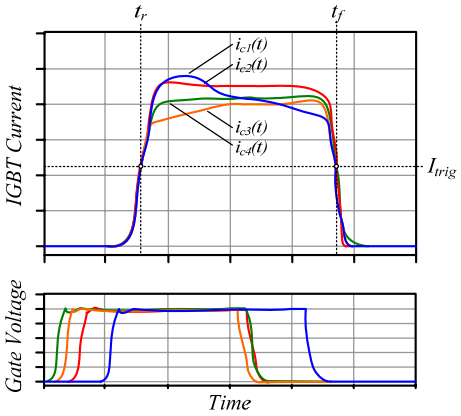


Figure 6: Schematic example for IGBT current pulses with synchronized rising/falling edge and synchronized slope of the rising current edge.

III. PULSE CURRENT MEASUREMENT OF IGBT MODULES

One of the key elements of the active gate control is a reliable, fast and accurate current measurement. Due to the short pulses generated by the solid state modulator only an AC current measurement circuit is required. Furthermore, the parasitic inductance of the modulator (IGBT, capacitors, transformer and load), which must be very low for proper operation, must not be increased by the current probe. Therefore, a measurement circuit based on a Rogowski coil is used.

A. PCB-Rogowski coil

Rogoswki coils basically consist of a coreless coil, which forms a closed loop. This loop encloses the conductor where the current, which should be measured, flows (cf. Fig 7) [3], [4].

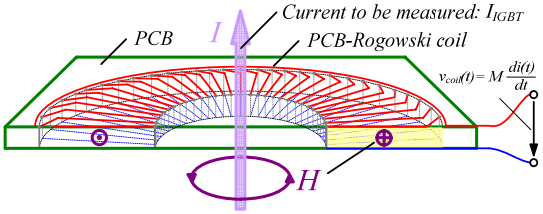


Figure 7: Measuring principle with a PCB-Rogowski coil.

Consequently, a part of the magnetic field H generated by the flowing current I_{IGBT} flows through the turns of the Rogowski coil.
Whenever the current varies also the amplitude of the magnetic field varies and a voltage is induced in the coil (Faraday's law) [2], [5]-[7]. This is similar to a transformer with a single turn primary. The resulting voltage at the ends of the coil is

$$v_{coil}(t) = M\frac{di(t)}{dt}. \qquad (2)$$

There, M is the mutual inductance of the Rogowski coil and the conductor, which depends on the geometry and the number of turns of the coil. The voltage v_{Coil} at the end of the Rogowski coil is proportional to the derivative of the IGBT current.

The Rogowski coil basically can be wound on a flexible or on a rigid bobbin. To realize a flat and reproducible measurement setup for each IGBT module in the solid state modulator a PCB-Rogowski coil is used. This can be designed for the desired specifications and easily be reproduced having always the same signal behavior due to the tight tolerances during the PCB manufacturing process [8]. To reduce the signal distortion and to achieve high signal quality, design rules, like the layout of the return conductor, as described in [2] have to be applied.

In Fig. 8 the PCB-Rogowski coils, which are used in the considered solid state modulator, are depicted. In order to measure the total current of one switch (= one module) the three coils - each enclosing one of the three parallel connected IGBT (Emitter-) terminals - are connected in series. Alternatively, a PCB-design with one coil enclosing all three terminals would be possible, which will be investigated in a later design.

Figure 8: IGBT Module (single switch) with three PCB Rogowski coils, where one coil encloses one (Emitter-) terminal of the IGBT. The coils are connected in series for measuring the total switch current.

B. Signal processing circuit

Due to the operating principle of the Rogowski coil (2), the voltage v_{Coil} must be integrated in order to obtain the IGBT current. For relatively large mutual inductances M the integration can be done passively with a simple RC-low-pass filter. There, the cut-off frequency of the filter defines the lower frequency limit of the current measurement. For achieving a wide measurement bandwidth a low cut-off frequency of the RC-filter is necessary. The low cut-off frequency, however, leads to a high attenuation of the current measurement signal at higher frequencies.

In case of small mutual inductances, i.e. small measurement signal amplitudes, this would lead to a low signal quality. Therefore, the signal has to be integrated actively for smaller mutual inductances. Basically, also a combination of passive and active integration is possible [6], [7].

The integrated voltage, which is proportional to the current, is fed to comparator K_1 (cf. Fig. 9) in order to detect the rising and falling edges of the pulse current. The respective points of time $t_{r1}\ldots t_{r4}$ / $t_{f1}\ldots t_{f4}$ (cf. Fig. 4) are measured in the FPGA with a resolution of 10ns. With comparator K_2 an over current can be detected and the IGBTs can directly be turned off very fast via the FPGA in order to protect the modulator.

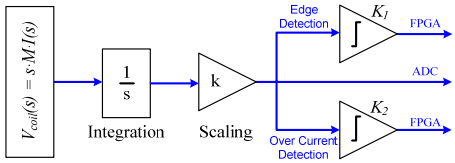
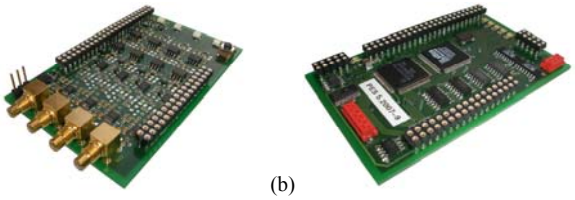


Figure 9: Block schematic of the measurement and signal processing electronic with edge detection K_1, over current shutdown and peak value measurement K_2.

The peak values of the IGBT currents are detected and sampled by the ADC, which is integrated in the DSP. With these values the total load current is determined, which is divided by the number of paralleled IGBTs in order to obtain a reference value for the IGBT current. In **Fig. 10** a photo of the current measurement electronics for four channels is shown. There, the signal processing electronics (cf. Fig. 10(a)) is mounted on top of the DSP board (Fig. 10(b)) in the final assembly.

It is important to note, that in the explained control scheme the propagation delay from the current probes to the DSP is not critical as long as the delays of all channels are the same, since a potential current unbalance is compensated just in the successive pulse.



(a) (b)

Figure 10: (a) Photo of the signal processing electronics and **(b)** of the DSP/FPGA board (credit card size for both boards: 86mm x 54mm).

IV. Implementation

The active gate control is implemented on the DSP/FPGA board (cf. Fig. 10), which is also used for measuring the currents. This board performs the sampling of the signals coming from the measurement electronics in parallel. Due to the clock frequency of 100MHz time steps / shifts of the gate voltage of 10ns are possible.

The active gate control is initiated by the DSP, which triggers the gate drives at the beginning of the control sequence. Simultaneously, a counter is started on the FPGA. As soon as the rising and falling edges are detected, the FPGA stores the times of the corresponding event in the corresponding register (cf. Fig. 11). Additionally, at the predefined time T_{Trig} the DSP samples the actual current values of each IGBT. Then, the DSP calculates the new turn on and off times, adjusts the gate voltage of each gate drive and is ready for the next pulse.

Parallel to the DSP the peak current values are monitored.

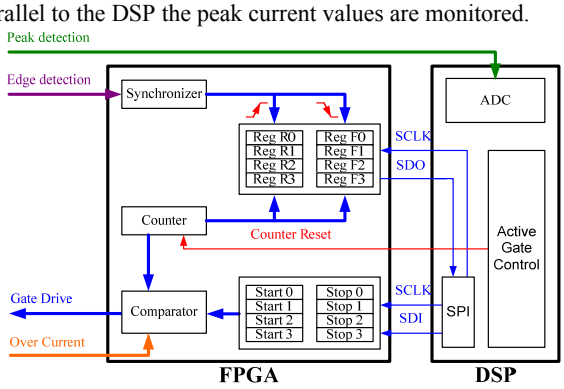


Figure 11: Block schematic of the implemented active gate controller in the DSP/FPGA. There, the detection of the pulse falling and rising edges, the detection of the peak values and the generation of the gate signals is shown.

V. Measurement Results

In **Fig. 12** the resulting signal of the PCB Rogowski coil with signal processing circuit as described in the last section is compared to a commercially available current probe CWT150B from PEM for two different pulse lengths and amplitudes. There, it could be seen that the signals of both current probes are in good correspondence.

The performance of the active current balancing circuit could be seen in **Fig. 13.** There, the current distribution for two directly paralleled branches without transformer is depicted for operation without active gate control in (a) and with active gate control in (b). These results clearly show the ability of the presented balancing circuit to symmetrize the current distribution, while keeping the fast rise and fall times. Measurement results for four parallel connected IGBT modules will be presented in a future paper.

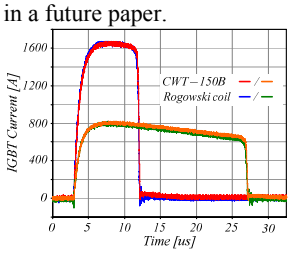


Figure 12: Comparison of the measurement results of the PCB-Rogowski to the results obtained with a commercial CWT-150B from PEM.

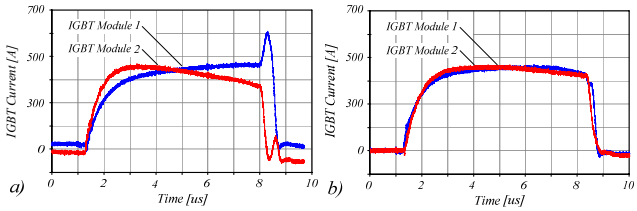


Figure 13: Current distribution in two direct parallel connected IGBT modules (Eupec FZ3600R17KE3) without **(a)** and with active gate control **(b)**.

VI. Summary

In this paper an active gate control for balancing the currents in parallel connected IGBT modules for a solid state modulator is presented. The balancing control shifts the rising and falling edges of the gate signals and adjusts the amplitude of the gate voltage so that the load current is equally shared. For determining the current distribution a fast and accurate current measurement system consisting of a PCB Rogowski coil and a signal processing electronic is described in the paper and experimentally verified.

Furthermore, the implementation of the active gate control in a DSP-/FPGA-board is described. This is also experimentally verified by pulse current measurements and shows excellent performance.

VII. References

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