SiC Power Semiconductors in HEVs: Influence of Junction Temperature on Power Density, Chip Utilization and Efficiency

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***Abstract*—With SiC, junction temperatures of power semiconductors of more than $700\,^\circ\mathrm{C}$ are theoretically possible due to the low intrinsic charge carrier concentration of SiC. Hence, a lot of research on package configurations for power semiconductor operation above $175\,^\circ\mathrm{C}$ is currently carried out, especially within the automotive industry due to the possible high ambient temperatures occurring in hybrid electric vehicles (HEVs). This paper shows, that a higher junction temperature though does not necessarily guarantee a higher utilization of the SiC chips with respect to the current that the device can conduct without overheating. The reason is, that for most power devices the power losses start to increase very rapidly at high junction temperatures while the power that can be dissipated always increases linearly with the junction temperature.**

The junction temperature, where the device current starts to decrease at, is derived for different SiC chips using measured on-state conduction and switching losses in this paper. This paper furthermore analyzes in detail, how the junction temperature on the one hand is influenced by boundary conditions and on the other hand influences itself the core parameters of a converter such as efficiency, the required chip area (i. e. cost) as well as the volumetric power density and thus forms an additional degree of freedom in the design of a power electronic converter. While calculating the optimum junction temperature and analyzing its impact on the system performance, it is demonstrated, how these results can help to find the best suited power semiconductor device for the particular application.

The performance of the calculations is shown on a design applied to a drive inverter for hybrid electric vehicles with normally-off SiC JFETs. Operated close to the optimum junction temperature of the SiC JFETs, it reaches a power density of 51 kW/l for the power modules and the air-cooling system, which is shown to be doubled by increasing chip size and using an advanced power semiconductor package with a lower thermal resistance from junction to ambient than the for this case assumed 1 K/W.

I. Introduction

An increasing trend towards more compact power electronic converters for high ambient temperatures can be observed in the development of hybrid electric vehicles (HEVs). Often, existing car concepts are enhanced by a model with a hybrid power train. There, small converters for hot surroundings (e. g. close to the internal combustion engine or the gearbox) can help to simplify packaging and manufacturing issues of the vehicle [1], [2]. Fig. 1 shows the topology of a typical converter used in HEVs to drive the electrical machine of the vehicle from the a high voltage traction battery.

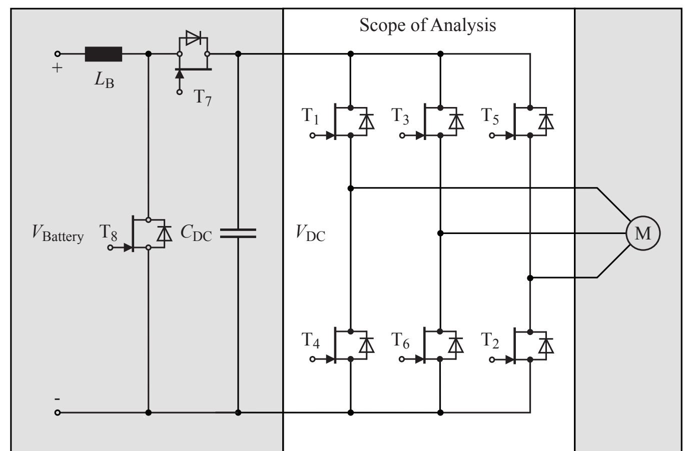

Fig. 1. Topology of a typical drive inverter with DC-DC converter used in HEVs. The impact of the power semiconductor junction temperature is carried out for a six-switch air-cooled inverter system. A power density of 51 kW/l at an ambient temperature of $120\,^\circ\mathrm{C}$ and an efficiency of 97.8% can be reached when operated close to the optimum junction temperature.

To achieve the goals of small size and high temperature capability, the power semiconductors employed in these converters must exhibit a low on-resistance and low switching energies in order to reduce the power losses. With the reduced losses, the amount of heat that needs to be removed by the cooling system is minimized.

To minimize the volume of a particular cooling system, the temperature difference between the ambient temperature and the junction temperature of the power semiconductor chip should be high. Hence, at high ambient temperatures, the semiconductor must be able to operate at higher junction temperatures. The maximum operation temperature of most power semiconductors made of Silicon (Si) is $175\,^\circ\mathrm{C}$.

The group III-V compound semiconductor Silicon Carbide (SiC) features physical properties superior to those of the widespread elemental semiconductor Si when manufacturing power semiconductor devices for high power density convert-

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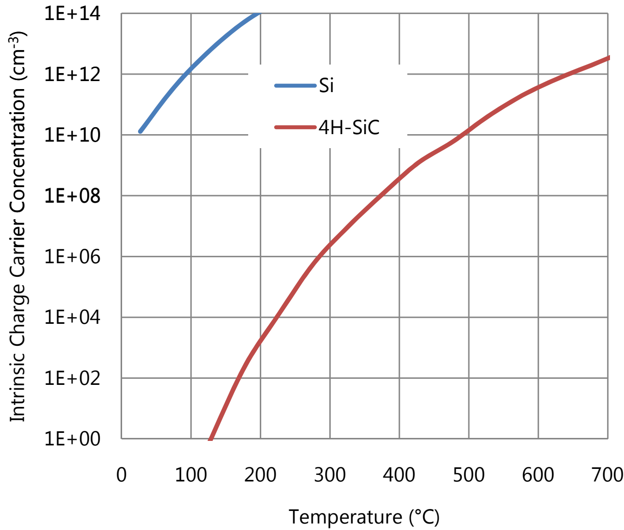

Fig. 2. Intrinsic charge carrier concentration n_i of Si and SiC vs. temperature. The comparably low n_i is the reason for the high temperature capability of SiC power semiconductors.

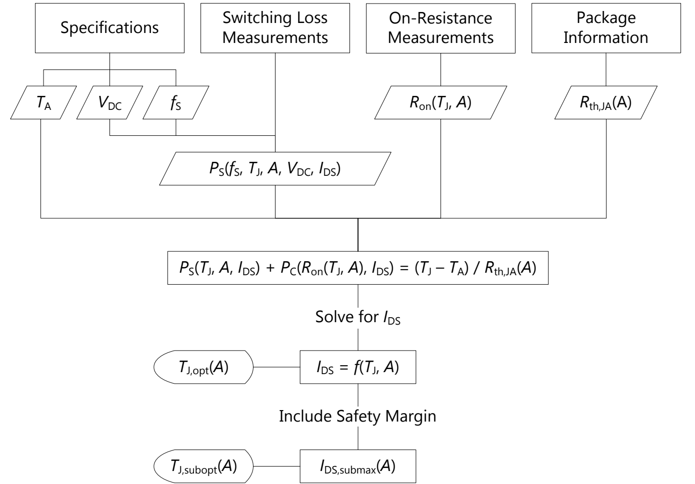

Fig. 3. Flow chart illustrating the way of determining the optimum junction temperature of SiC power semiconductors: Input parameters (specifications and device characteristics) are used to derive an equation for the thermally stable operation of the converter. This equation is solved for the device current in order to calculate the junction temperature that maximizes the device current. For a safe operation of the converter, the maximum current is reduced by a safety margin. This usually provides a huge additional benefit with respect to reliability issues of the package as it is shown in Section II-C that the junction temperature can be decreased by more than 100 °C while still conducting 90% of the maximum possible drain current.

ers in (hybrid) electric vehicles [3]. Therefore, automotive power electronic converters start to feature switches made of SiC [4].

The for the objective of this paper most important favorable physical property of SiC compared to Si is its low intrinsic charge carrier concentration n_i. Fig. 2 shows, that for a large temperature range n_i of 4H-SiC stays below $10^{15}\,\mathrm{cm}^{-3}$, where the intrinsic conduction of the semiconductor starts and it behaves as a bulk resistor [5] — at 700 °C, n_i of 4H-SiC is equal to that of Si at 100 °C. This is the reason, why SiC power semiconductors can be operated at much higher junction temperatures than power semiconductors made of Si.

Further superior properties include a three times higher band-gap leading to an order of magnitude higher breakdown electrical field (328 MV/m for 4H-SiC, the most common SiC crystal structure for SiC power semiconductors, compared to 29 MV/m for Si) while having a comparable electron mobility [6]–[11]. These characteristics allow SiC devices to block higher voltages while having a lower on-resistance. Hence, unipolar devices with low switching losses (due to the absence of carrier injection), are feasible and competitive even for high operating junction temperatures and voltages exceeding 1000 V with SiC [12].

It arises the question, whether it is desirable to operate the SiC device up to its maximum temperature limit. On the one hand, the higher the junction temperature, the more power can be dissipated for the same cooling system. On the other hand, very advanced packaging technologies are needed and reliability issues need to be solved [13] for temperatures considerably above 175 °C. A third aspect concerns the losses: For most SiC power semiconductors, the losses increase more than linearly with device temperature while the power, that can be dissipated by the package, increases linearly with temperature. That is, at a certain temperature, the device current cannot be risen any more even though the junction temperature increases but must be decreased in order to prevent the device from a thermal runaway [14]. This point, where the device current starts to decrease with increasing temperature, is the optimum junction temperature with respect to the utilization of the power semiconductor switch because this is the point, where the device current reaches its maximum for a given cooling system.

In contrast to [14], this paper derives the optimum junction temperature using real measurements of on-resistances and switching energies of different SiC power semiconductors (*cf.* Section II). As the switching losses are now included in the calculations, the dependencies become more complex. The influence of the device characteristics as well as of the operating conditions such as switching frequency f_S, ambient temperature T_A and the thermal resistance $R_\mathrm{th,JA}$ on the optimum junction temperature is exemplarily analyzed in detail for a 1200 V normally-off JFET (*cf.* Section III).

The impact of the junction temperature on the core performance parameters of a power electronic converter such as efficiency η, the volumetric power density p and the required chip area A is shown in Section IV. The performance of the calculations is demonstrated for an inverter in hybrid electric vehicles (*cf.* Fig. 1). This reference design reaches a power density of 51 kW/l for the power modules and the air-cooling system including heat sinks and fans.

II. Optimum Junction Temperatures

The flow chart in Fig. 3 illustrates how the optimum junction temperature $T_\mathrm{J,opt}$ for SiC power semiconductors is derived in this paper. First, the input parameters have to be obtained.

A. *Specifications*

The input parameters consist of predefined specifications:

- The ambient temperature T_A is around $120\,°\mathrm{C}$ for power electronic converters placed under the engine hood of hybrid electric vehicle regardless of the cooling fluid (water-glycol mixture or air).
- The DC link voltage V_DC is usually chosen as high as possible in order to minimize the current for a certain power level so that the I^2R losses in the switches, supply lines and the electrical machine(s) are minimal. The DC link voltage is directly given by the maximum voltage that can be applied to the machine in the power train. Due to partial discharge issues in the machine, V_DC stays usually below 800 V for electrical machines used in hybrid electric vehicles and is assumed to be 700 V in this case.
- The switching frequency f_S is specified depending on EMI filtering requirements and the desired rotational speed of the electrical machine and thus the required frequency of the output current in the case of an inverter. For a DC/DC converter, the size of the passive elements influences the choice of the switching frequency. Here, f_S is chosen to be 50 kHz in order to be able to drive high speed electrical machines that can provide power density benefits [15].
- The thermal resistance $R_\mathrm{th,JA}$ from the power semiconductor junction to the ambient is determined by the particular package configuration. It will not stay constant for different chip sizes as the heat spreading of a larger chip or several small chips is better than that of a single small chip. Hence, a correlation between $R_\mathrm{th,JA}$ and the chip area A is required for precise results. This can be obtained by measuring or simulating the package configuration with different chip sizes. A curve fitting algorithm using the correlation

$$R_\mathrm{th,JA}(A) = \frac{a_{R\mathrm{th}}}{A} + b_{R\mathrm{th}} \qquad (1)$$

usually gives good fitting results because for very small chip sizes, the thermal resistance approaches infinity, and for chip sizes close to the maximum (i. e. the surface where the chips are soldered onto and that is feeding the heat into the cooling system is fully covered with chips) it has got a value close to its minimum $b_{R\mathrm{th}}$. The constants $a_{R\mathrm{th}}$ and $b_{R\mathrm{th}}$ are positive real values. For the exemplary calculations in this paper, a very conservative estimate of $R_\mathrm{th,JA}(0.16\,\mathrm{cm}^2) = 1\,\mathrm{K/W}$ is used.

B. *Device Characteristics*

In addition to these predefined parameters, the device characteristics of the considered power semiconductors need to be identified, as the temperature behavior of the on-resistance and the switching energies determine the optimum junction temperature with respect to a maximum utilization of the semiconductor area.

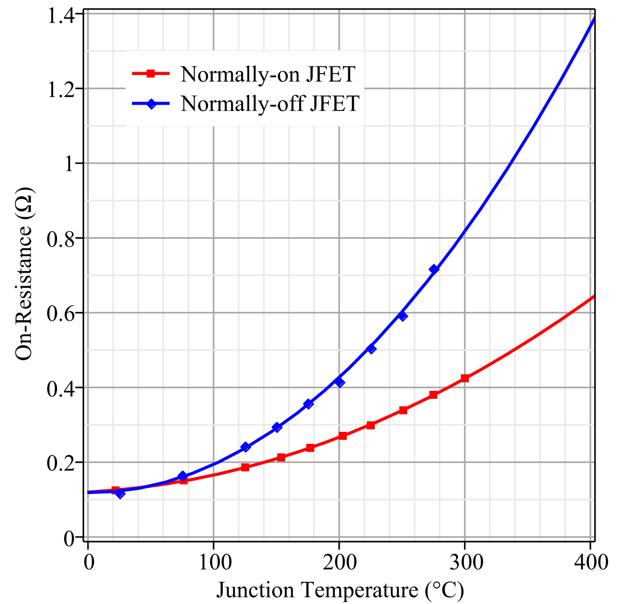

Fig. 4. Measured and curve fitted temperature dependency of the on-state resistance of the latest normally-on and normally-off 1200 V SiC JFETs. The chip area is $17.3\,\mathrm{mm}^2$ for the normally-on JFET and $4\,\mathrm{mm}^2$ for the normally-off JFET.

1) On-Resistance: Most power semiconductors feature a positive temperature coefficient of their on-state resistance, i. e. the on-resistance increases with rising device temperature. This can be advantageous as it ensures an even current distribution among different dies if several chips are connected in parallel. The on-resistances R_on of the latest normally-on and normally-off SiC vertical junction field effect transistors (VJFETs) are shown in Fig. 4.

The change in on-resistance is mainly influenced by the change in charge carrier mobility, which is for unipolar devices the mobility of the majority charge carriers (electrons for n-type semiconductors). The decrease in mobility can be partially compensated though: Depending on the doping density of the semiconductor material, not all dopants are ionized at low temperatures. With rising temperature, the ionization degree increases, i. e. new charge carriers are generated, especially in the channel and substrate region [16]. This effect can clearly be seen for the normally-on JFET, whose slope in on-resistance is lower than that of the normally-off JFET.

For the following calculations, analytic expressions of the on-resistances need to be derived with curve fitting algorithms. Polynomial functions of second order give better fittings than power functions due to the mentioned side effects that superimpose the change in charge carrier mobility.

2) Switching Energies: As for the on-resistance, an analytic expression must be derived for the measured switching energies in order to be able to analytically calculate the optimum junction temperature. When measuring the switching energies, the turn-off and turn-on energies can be summated. The load conditions should be as close as possible to the later application especially with respect to the parasitic capacitance

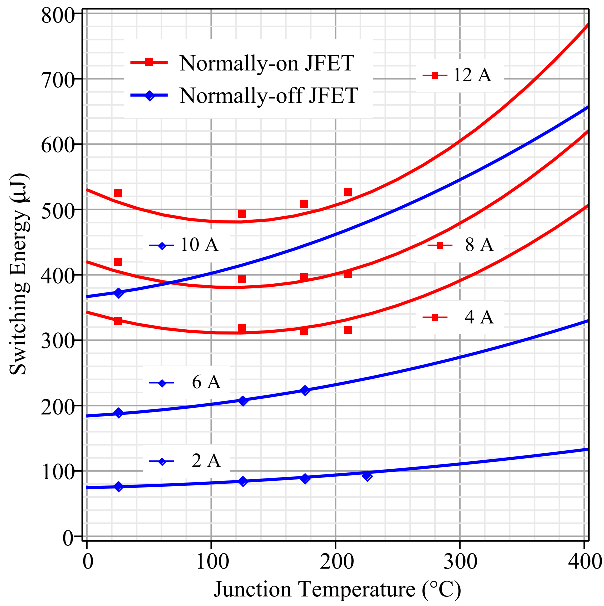

Fig. 5. Measured and curve fitted switching energies (turn-on and turn-off) for different temperatures and drain currents of the latest normally-off 1200 V SiC JFETs with an antiparallel SiC diode (Cree C2D10120) on an inductive load. The normally-on JFET has got a four times larger chip area than the normally-off JFET. The switched voltage is 700 V for both devices.

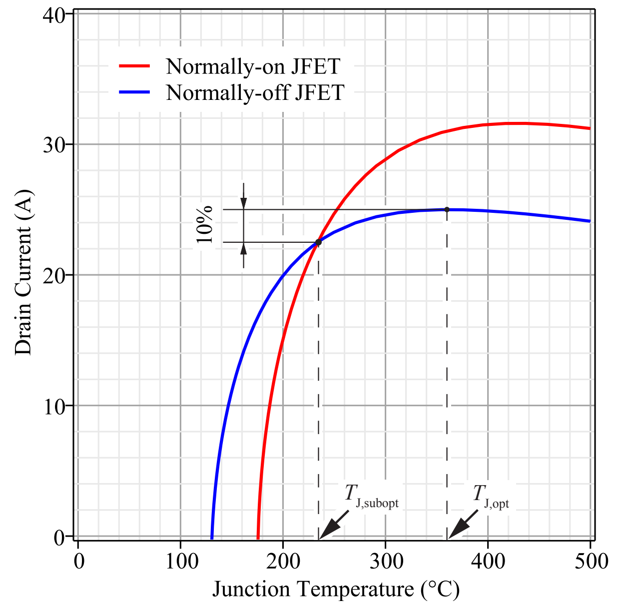

Fig. 6. Drain currents of the normally-on and normally-off JFET (each with four single devices in parallel) as functions of the junction temperature for the values of Section II-A and Section II-B. Optimum and suboptimum junction temperature are shown on the example of the normally-off JFET. The differences in maximum drain current and optimum junction temperature between the two devices are mainly due to the differences in the temperature behavior of the on-resistance. For very small drain currents, the junction temperature does not exactly equal the ambient temperature due to the (at low currents high) portion of switching losses, which are not close to zero for drain currents close to zero, especially for the normally-on JFET with a four times larger chip area compared to the normally-off device.

of the load that needs to be charged during every switching transition.

Fig. 5 shows the measured switching energies and the curve fitting results. At high junction temperatures, the device current has to be decreased in order not to go beyond the current carrying limit of the device. The measurement results of the switching energies show that as a good approximation, the temperature behavior of the switching energies is independent of the drain-source current and correspondingly the dependency of the switching energy on the drain-source current is equal for all measured temperatures. Hence, the impact of drain-source current and the impact of temperature on the switching energy can be calculated independently and the resulting function describing the switching energy is a product of two independent functions.

$$E_{\mathrm{S}}(I_{\mathrm{DS}}, T_{\mathrm{J}}) = k_E \cdot g_E(I_{\mathrm{DS}}) \cdot h_E(T_{\mathrm{J}}) \tag{2}$$

The constant k_E is a proportionality factor. The function $g_E(I_{\mathrm{DS}})$ represents the normalized dependency of the switching energy on the drain current and can be derived using the measured switching energies at a constant temperature, e. g. 25 °C for the normally-off JFET as it is the only temperature where measured values up to 10 A are available. The function $h_E(T_{\mathrm{J}})$ forms the normalized temperature behavior which can be determined using the measured switching energies at constant drain current level. Both functions, h_E and g_E, are second-order-polynomials of the form

$$g_E(I_{\mathrm{DS}}) = a_E + b_E \cdot I_{\mathrm{DS}} + c_E \cdot I_{\mathrm{DS}}^2 \tag{3}$$

and

$$h_E(T_{\mathrm{J}}) = d_E + e_E \cdot T_{\mathrm{J}} + f_E \cdot T_{\mathrm{J}}^2. \tag{4}$$

The switching energies depicted in Fig. 5 are measured with a single JFET, i. e. not multiple devices in parallel. If larger currents than measured are conducted through several chips connected in parallel, an ideal current distribution can be assumed for a symmetrical module structure due to the above mentioned positive temperature coefficient of the on-resistance of the JFETs. That is, for i paralleled switches, the switching losses can be calculated for one switch with one ith of the overall current. These switching losses are then multiplied by i to obtain the switching losses for all chips. For the following calculations, four devices (four normally-on and four normally-off JFETs, respectively) are assumed to be connected in parallel, which gives a factor of $i = 4$.

C. Calculation of the Optimum Junction Temperature

Having derived all input parameters according to Fig. 3, the calculation of the optimum junction temperature can now be started by equalizing the power losses and the power, that can be dissipated by the package. The losses in the off-state due to leakage currents ($< 100\,\mu$A per chip at 700 V and 250 °C for both devices) and the losses arising at the gate (< 1 W per chip) can be neglected. Hence, the power losses consist only

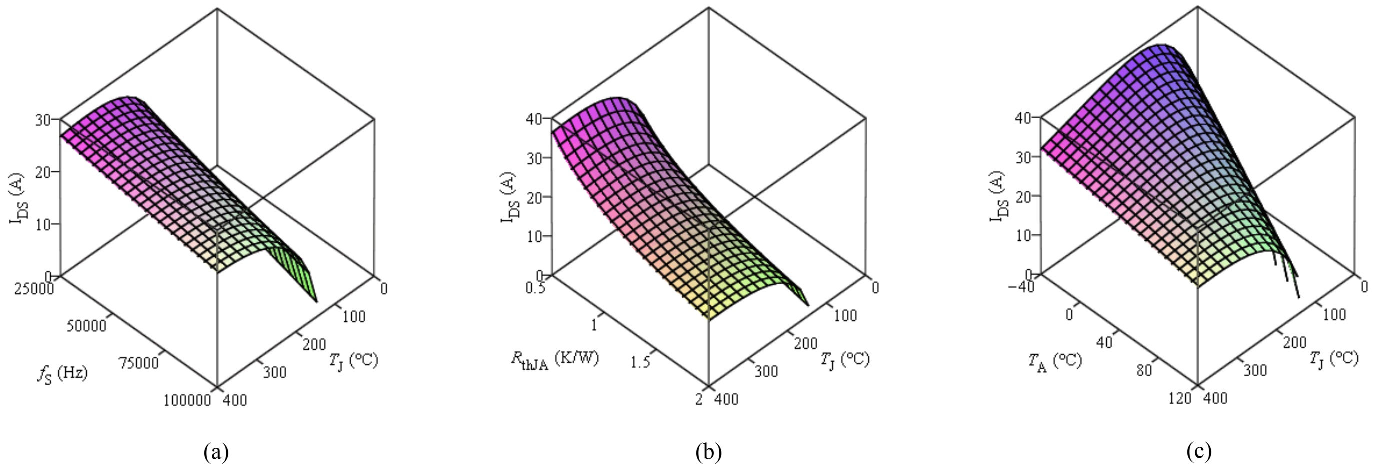

Fig. 7. Drain current as a function of the junction temperature as well as (a) ambient temperature, (b) switching frequency and (c) thermal resistance for four 1200 V normally-off SiC JFET connected in parallel.

of the conduction and switching losses, which leads to

$$I_{\mathrm{DS}}^2 R_{\mathrm{on}} + f_{\mathrm{S}} \cdot E_{\mathrm{S}} = \frac{T_{\mathrm{J}} - T_{\mathrm{A}}}{R_{\mathrm{th,JA}}} \tag{5}$$

for the thermal equilibrium.

Using (2), the junction temperature, where the drain current reaches its maximum, can be calculated by deriving an equation for I_{DS} from (5) first,

$$I_{\mathrm{DS}} = \frac{1}{2(R_{\mathrm{on}}(T_{\mathrm{J}}) - c_E f_S h_E(T_{\mathrm{J}}))} \cdot (-b_E f_S h_E(T_{\mathrm{J}}) + \sqrt{b_E^2 f_S^2 h_E^2 - 4(R_{\mathrm{on}} - c_E f_S h_E)(a_E f_S h_E - \left(\frac{T_{\mathrm{J}} - T_{\mathrm{A}}}{R_{\mathrm{th,JA}}}\right)}), \tag{6}$$

where a_E, b_E, c_E denote the zeroth, first and second order coefficients respectively of the drain current for $g_E(I_{\mathrm{DS}})$ in (2). Fig. 6 shows a plot of (6) for both the normally-on and normally-off JFET.

It can clearly be seen from Fig. 6, that there is a junction temperature $T_{\mathrm{J,opt}}$ which maximizes the drain current for each device. This maximum $I_{\mathrm{DS,max}}$ can be calculated by differentiating (6) with respect to T_{J} and setting the derivative to zero. For the conditions of Section II-A and Section II-B, the optimum junction temperature for the normally-off JFET is

$$T_{\mathrm{J,opt,n\text{-}off}} = 361\,^{\circ}\mathrm{C}, \tag{7}$$

assuming that the extrapolation of the on-resistance is valid in this temperature range.

If the junction temperature stays below this value, the JFET is not fully utilized. This is disadvantageous with respect to the material cost of the converter as more chip area was used than it was needed but is advantageous in terms of the reliability of the power module and the achievable efficiency as at a higher temperature the conduction and switching losses will be higher. If the junction temperature rises above its optimum, the semiconductor switch is operated with far lower efficiency and lower utilization due to lower current that can be conducted. If the current is not decreased quickly enough at temperatures above $T_{\mathrm{J,opt}}$, it can start a positive feedback mechanism leading to a thermal runaway which results finally in a thermal destruction of the device.

In order to prevent the chip from heating up higher than $T_{\mathrm{J,opt}}$, a safety margin for the drain-source current can be chosen so that I_{DS} is not allowed to rise to more than 90% of its maximum value, which in this case leads to a current of 22.5 A. Then, the suboptimum junction temperature is in this case

$$T_{\mathrm{J,subopt,n\text{-}off}} = 234\,^{\circ}\mathrm{C}, \tag{8}$$

which is significantly below the optimum junction temperature because the slope in I_{DS} is very small around its maximum. This small slope becomes particularly interesting when the trade-off between current utilization of the chip and reliability is considered. By reducing the junction temperature by $127\,^{\circ}\mathrm{C}$ the reliability rises by orders of magnitude while the maximum current is decreased by 10% only.

For the normally-on JFET, the effect of the slower increase in on-resistance with junction temperature can be seen: The optimum junction temperature

$$T_{\mathrm{J,opt,n\text{-}on}} = 428\,^{\circ}\mathrm{C}, \tag{9}$$

is reached significantly later, and thus the drain current at the suboptimum junction temperature

$$T_{\mathrm{J,subopt,n\text{-}on}} = 293\,^{\circ}\mathrm{C}, \tag{10}$$

can be larger with 28.4 A.

Due to the larger chip area of the normally-on JFET, its switching losses are higher compared to the normally-off JFET (*cf.* Fig. 5). Considering the fact, that the switching energies are not negligible for negligible drain current currents, Fig. 6 shows, that the switching losses account for a high portion of the overall losses at small drain currents, leading to a temperature difference between the ambient and junction temperature for zero drain current.

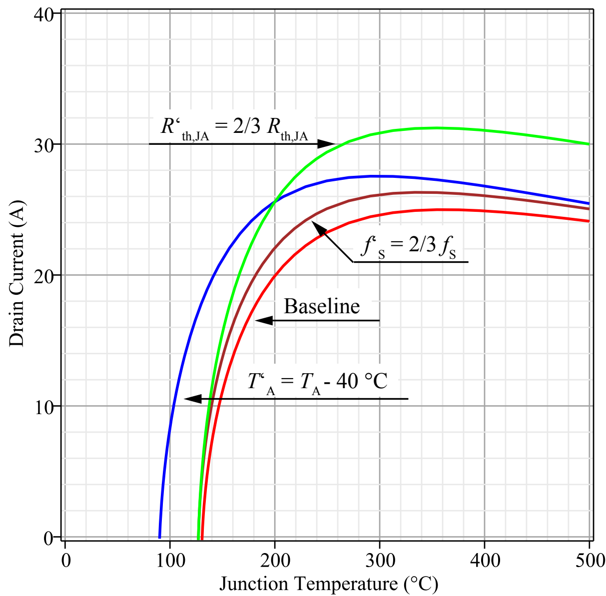

Fig. 8. Drain-source current as a function of junction temperature with variations in the ambient temperature, the switching frequency and the thermal resistance for the normally-off 1200 V SiC JFET with a chip area of $0.16\,\mathrm{mm}^2$.

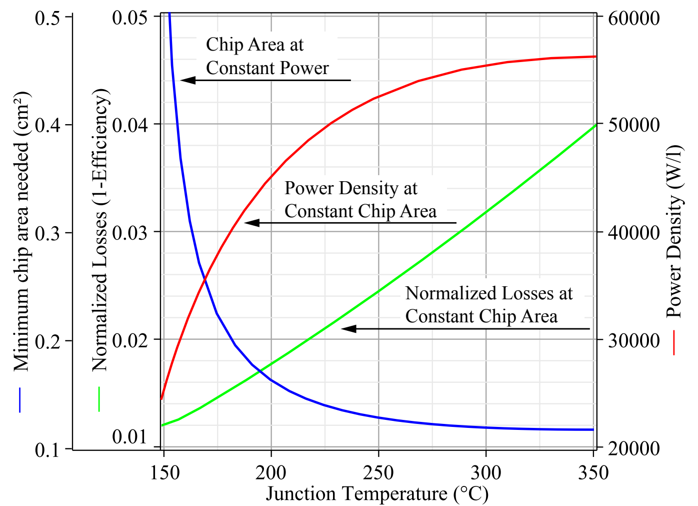

Fig. 9. Impact of the junction temperature on the system performance parameters chip area, power density and losses for a SiC normally-off JFET employed as a switch in an inverter for hybrid electric vehicles at an ambient temperature of 120 °C and a switching frequency of 50 kHz.

III. Sensitivity of the Optimum Junction Temperature

Equation (6) shows, that I_{DS} and thus the optimum junction temperature depend on

- the on-resistance and the switching energies of the power semiconductor, i. e. the respective absolute value and the respective temperature behavior
- the DC link voltage
- the chip size
- the switching frequency
- the ambient temperature
- the thermal resistance from the junction to the ambient.

Most of these parameters become fixed at a certain point in the design process of a power electronic converter. The resulting value is the consequence of a trade-off consideration between different impacts on the converter properties of a particular parameter. This section presents the impact of three parameters on the optimum junction temperature and the maximum device current for the example of the normally-off JFET.

Fig. 7 shows, that the switching frequency f_{S} exhibits the lowest impact on $T_{\mathrm{J,opt}}$ and $I_{\mathrm{DS,max}}$. A change in f_{S} changes the portion of switching and conduction losses in the overall losses. As the switching losses increase slightly less with temperature compared to the conduction losses (*cf.* Fig. 4 and Fig. 5), $T_{\mathrm{J,opt}}$ increases slightly with an increasing portion of switching losses. Due to the overall higher losses at higher f_{S}, $I_{\mathrm{DS,max}}$ decreases with rising f_{S}.

With the switching losses considered in (5), the thermal resistance $R_{\mathrm{th,JA}}$ from the semiconductor junction to the ambient does not cancel out, if (6) is differentiated and set to zero. Therefore, an increased $R_{\mathrm{th,JA}}$ shifts $T_{\mathrm{J,opt}}$ slightly towards higher values and drastically decreases the maximum device current.

The ambient temperature T_{A} has by far the biggest influence on the optimum junction temperature $T_{\mathrm{J,opt}}$. The lower T_{A}, the lower $T_{\mathrm{J,opt}}$ and the higher $I_{\mathrm{DS,max}}$ because at lower junction temperatures, the on-resistance and switching losses are lower. Hence, more current can be conducted at constant losses. The correlation between T_{A} and $T_{\mathrm{J,opt}}$ is linear with a slope of approximately 1, i. e. every degree reduction in T_{A} reduces $T_{\mathrm{J,opt}}$ likewise.

Precise values of the change in device current and optimum junction temperature due to the change in parameters can be read of Fig. 8 by comparing the respective curves with the baseline curve.

IV. Impact on System Performance of a Drive Inverter for HEVs

In Section II, the impact of the power semiconductor junction temperature on the device current is investigated and thus the optimum junction temperature with respect to a maximum current is determined.

The junction temperature influences also other system parameters: The chip area that is needed to conduct a certain amount of current at different junction temperatures can be calculated by solving (6) for the chip area A. In Fig. 9, the current is the suboptimum current of 22.5 A for a switch with a chip size of $0.16\,\mathrm{cm}^2$ out of Section II-C. For junction temperatures close to the ambient temperature, the required chip area approaches infinity because the low temperature difference between the junction and the ambient means according to (5), that only very few losses can be dissipated. Hence, the chip area must be large to adequately minimize the on-resistance of the switch.

The power density and the normalized losses also depicted in Fig. 9 apply to a six-switch three-phase inverter that can

be used to drive the electrical machine of a (hybrid) electric vehicle. For deriving both parameters, the correlation between the rms value of the drain current of a single switch, I_{DS}, and the input power of the complete inverter is required.

The input power can be calculated using the the DC link voltage V_{DC} and the DC current I_{DC} drawn from the DC link capacitor or a high voltage battery,

$$P_{\mathrm{in}} = V_{\mathrm{DC}} \cdot I_{\mathrm{DC}} = 3 \cdot V_{\mathrm{DC}} \cdot \bar{i}_{\mathrm{DS}}. \tag{11}$$

I_{DC} is the sum of the three average currents $\bar{i}_{\mathrm{DS}}$ flowing through each inverter leg and thus through each switch.

With unipolar devices, the channel can be turned on during the conduction period of the freewheeling diode. That is, each switch conducts the equivalent of a sine half wave. Then, the ratio of I_{DS} upon $\bar{i}_{\mathrm{DS}}$ is $\pi/2$ yielding with (11)

$$P_{\mathrm{in}} = \frac{6}{\pi} \cdot V_{\mathrm{DC}} \cdot I_{\mathrm{DS}}. \tag{12}$$

It is assumed, that the losses during the freewheeling states of the inverter (i. e. either all high-side or all low-side switches are turned on) are negligible, that the switching frequency is with 50 kHz much higher than the electrical output frequency of the inverter and that the converter is PWM controlled, which provides an upper estimation of the losses as they will decrease with space vector control compared to PWM control.

Together with the volume of the package for the power semiconductors and cooling system including heat sinks and fans, $V_{\mathrm{C}} = 0.5934\,\mathrm{l}$, the power density p can be plotted (*cf.* Fig. 9) with

$$p = \frac{P_{\mathrm{out}}}{V_{\mathrm{C}}} = \frac{P_{\mathrm{in}} - P_{\mathrm{D}}}{V_{\mathrm{C}}}. \tag{13}$$

For operation at the suboptimum junction temperature of $234\,^{\circ}\mathrm{C}$, the drain-source current $I_{\mathrm{DS}} = 22.5\,\mathrm{A}$ of Section II-C leads to a power density of

$$p_{\mathrm{subopt}} = 50.7\,\mathrm{kW/l} \tag{14}$$

at a power level of

$$P_{\mathrm{subopt}} = 30.1\,\mathrm{kW}. \tag{15}$$

Both the power and the power density can be significantly increased by simply increasing the die area by a certain amount as this will reduce the conduction losses by the same amount. Reduced losses lead to increased power that can be transferred at a constant efficiency as the amount of losses that can be dissipated by the cooling system remains constant. Increased chip area also leads to a lower thermal resistance from junction to ambient; this can be further enhanced by advanced packaging methods as double-sided cooling. If the calculations of Section II-C are conducted with eight instead of four chips leading to a chip area of $32\,\mathrm{mm}^2$ for each of the six switches and the thermal resistance is cut in half, which is a realistic assumption for double sided cooling as thermal simulations show, the power density can be doubled to more than 100 kW/l.

The efficiency decreases with temperature according to Fig. 9 due to the increasing losses, which can be calculated with the suboptimum junction temperature (*cf.* (8)) and the suboptimum drain current of 22.5 A (*cf.* Fig. 6) using (5). At the suboptimum junction temperature, the efficiency is

$$\eta_{\mathrm{subopt}} = 97.8\% \tag{16}$$

for the inverter depicted in Fig. 1.

V. Conclusion

The latest SiC JFETs can make a significant contribution to the development of ultra compact and efficient power electronic converters for hot surroundings in HEVs. In this paper, the influence of the junction temperature of SiC power semiconductor devices on the device current is calculated. This calculation is based on theoretical considerations and measurements of the temperature behavior of on-resistance and switching energies for real SiC switches. It is shown, that a 1200 V normally-off JFET with a chip area of $0.16\,\mathrm{cm}^2$ and realistic boundary conditions for automotive use, is utilized to 90% with respect to the maximum device current at a junction temperature of $234\,^{\circ}\mathrm{C}$.

The sensitivity of the optimum junction temperature is also investigated: A lower optimum junction temperature can be achieved by decreasing the ambient temperature. $1\,^{\circ}\mathrm{C}$ lower ambient temperature means $1\,^{\circ}\mathrm{C}$ lower optimum junction temperature as a good approximation. The most effective way to increase the device current, is to reduce the thermal resistance of the package and cooling system. Cutting the thermal resistance in half corresponds to a 50% higher device current.

The calculations are applied to an inverter for hybrid electric vehicles which is operated close to the optimum junction temperature at an ambient temperature of $120\,^{\circ}\mathrm{C}$. Then, the employed power semiconductor chips are utilized with $141\,\mathrm{A/cm}^2$ and the inverter reaches a power density of 51 kW/l at a power level of 30 kW and an efficiency of 97.8%, assuming a high thermal resistance of $R_{\mathrm{th,JA}} = 1\,\mathrm{K/W}$, which is shown to be doubled by increasing chip size and using an advanced power semiconductor package with a lower thermal resistance from junction to ambient than the for this case assumed 1 K/W.

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